A Dual-Switch Discontinuous Current-Source Gate Driver for a Narrow On-Time Buck Converter

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***Abstract*—This paper presents a new discontinuous current-source driver (CSD) with two control switches. The introduced CSD is appropriate for narrow on-time applications such as buck voltage regulator module. This driver has some important features such as considerable gate drive loss reduction due to gate energy recovery, significant reduction of switching losses, low circulating losses, and high *Cdv/dt* immunity. Compared to other discontinuous CSDs, the proposed circuit has following advantages: 1) reduced number of switches; 2) capability of operating at higher frequency for a specific duty cycle or ability to achieve smaller minimum duty cycle for a certain switching frequency. The proposed gate drive is analyzed and a 1-MHz prototype is implemented to validate the features of the proposed circuit.**

***Index Terms*—Buck voltage regulator module (VRM), conduction losses, discontinuous current-source driver (CSD), resonant gate driver (RGD), switching losses.**

I. Introduction

THE switching frequency of voltage regulator modules (VRMs), which supply power to CPUs, has increased to MHz range in recent years [1]–[3]. The main purposes of increasing the switching frequency in VRMs are increasing power density, reducing size of passive elements, and achieving fast transient response [1]–[5].

Due to advantages such as simplicity, low component count, and low cost, VRMs supplied by 12 V input voltage are almost universally based on the multiphase buck converter topology [1], [4]. However, buck converters using conventional voltage source driver (VSD) suffer from two serious issues as the switching frequency increases: 1) high gate drive losses, and 2) high switching losses [4]. It should be noted that due to parasitic inductances, switching losses increase even higher [6]. In conventional VSDs, all the gate driving energy is dissipated at each switching cycle, which results in lower efficiency at high switching frequencies [7]–[9].

Resonant gate driver (RGD) circuits are proposed to reduce gate drive losses [10]–[15]. Although RGDs can effectively recover high gate drive losses, they cannot reduce the switching losses [8]. Therefore, RGD circuits are not suitable for applications, where switching losses are considerable [8], [16]. But RGDs are suitable for synchronous rectifier (SR) of buck VRMs, since the switching losses of the SR are negligible [16].

In comparison to RGDs, current-source gate drivers (CSDs) not only recover the gate drive losses but also reduce the switching losses effectively [16]–[18]. CSD circuits reduce the switching loss by charging and discharging the power MOSFET gate capacitance with a relatively large constant current [16]. CSDs enhance the efficiency without changing the multiphase buck architecture of today's VRMs, which results in low cost and simple control [18], [19]. The CSDs operate either under continuous current mode (CCM) [19]–[23] or discontinuous current mode (DCM) [24]–[29]. Comparison between CCM CSDs and DCM CSDs applied to high-side switch of buck VRM is presented in [30] and summarized as following:

1) Discontinuous CSDs achieve lower gate drive losses compared to continuous CSDs [30].
2) The inductor in discontinuous CSDs is much smaller than continuous CSDs. This yields to space saving on the motherboards, and DCM CSDs are easier to integrate as an IC [16], [30].
3) Unlike continuous CSDs, peak driver current of discontinuous CSDs is independent of duty cycle or switching frequency [30]. In commercial pulse width modulation (PWM) controller ICs for buck VRM [31], the frequency is reduced proportionally according to load current to enhance light-load efficiency. But in continuous CSDs, decreasing the switching frequency would increase the peak current value, which causes higher conduction losses of gate drive circuit [30]. Also, multiphase constant on-time current-mode control (with variable switching frequency) based on pulse distribution structure is widely used in voltage regulator application for microprocessors [32], [33]. Thus, discontinuous CSD is suitable for aforementioned applications.
4) Discontinuous CSDs have better performance when a step change of duty cycle occurs [30].

Due to the advantages of discontinuous CSD circuits, they are highly suitable for driving high-side switch of buck VRMs [30], [34]. Nevertheless, It should be noted that discontinuous CSDs proposed in the previous research [5], [8], [18], [24]–[27] have several drawbacks when they are adopted in order to drive high-side switch of buck VRMs, which are as following:

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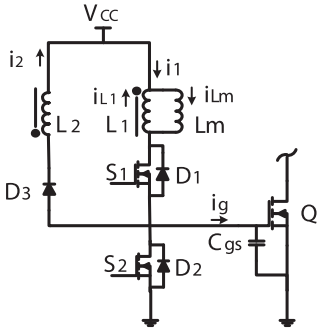

Fig. 1. Proposed discontinuous CSD.

1) Existing discontinuous CSDs [5], [8], [18], [24]–[26] have high number of control switches (four switches) which require large amount of logics and predrivers.
2) As shown in Section III and in [26], there are constraints on the minimum power MOSFET on-time $t_{on(\min)}$ for existing CSDs [5], [8], [24]–[27]. Power MOSFET on-time t_{on} is equal to D/f_{sw}, where *D* is the power MOSFET duty cycle, and f_{sw} is the switching frequency. Constraints on $t_{on(\min)}$ limit the maximum achievable switching frequency of discontinuous CSDs (switching frequency should meet $f_{sw} \leq f_{sw(\max)}$) for a required minimum duty cycle value $D_{\min-req}$. Or it limits the minimum duty cycle $D_{\min}$ for a certain switching frequency value.

The main purpose of this paper is to present a dual-switch discontinuous CSD, which is suitable for driving the high-side switch of buck VRM with narrow on-time. In comparison to other discontinuous CSDs, the proposed dual-switch discontinuous CSD has following advantages: 1) employs fewer switches, and 2) is capable of operating at higher switching frequency for the required minimum duty cycle or is able to achieve smaller minimum duty cycle for a certain switching frequency. In the proposed CSD, the current direction through the magnetizing inductance does not change before discharging the gate capacitance. However, in other CSDs, the direction of current through inductor should change before discharging gate capacitor, which limits the minimum achievable switch on time. Similar to other CSDs, the dual-switch discontinuous CSD is able to reduce both gate drive and switching losses. It also has high *Cdv/dt* immunity to prevent the power MOSFET gate of undesired triggering. It should be noted that the proposed dual-switch discontinuous CSD is effective for narrow on-time applications such as high frequency buck VRMs and is not suitable for applications where, the power MOSFET on-time is wide.

The principle of operation is presented in Section II, and is followed by discussions on loss analysis and design procedure in Section III. The advantages of the proposed CSD are described in Section IV. Section V of the paper presents the experimental results, and the drawn conclusions are provided in Section VI.

II. Operating Principles

Fig. 1 shows the proposed CSD circuit, which consists of two control switches S_1, S_2 (n-channel), one Schottky diode D_3, and a pair of coupled inductors L_1, L_2 ($L_1 = L_2$). In Fig. 2, the

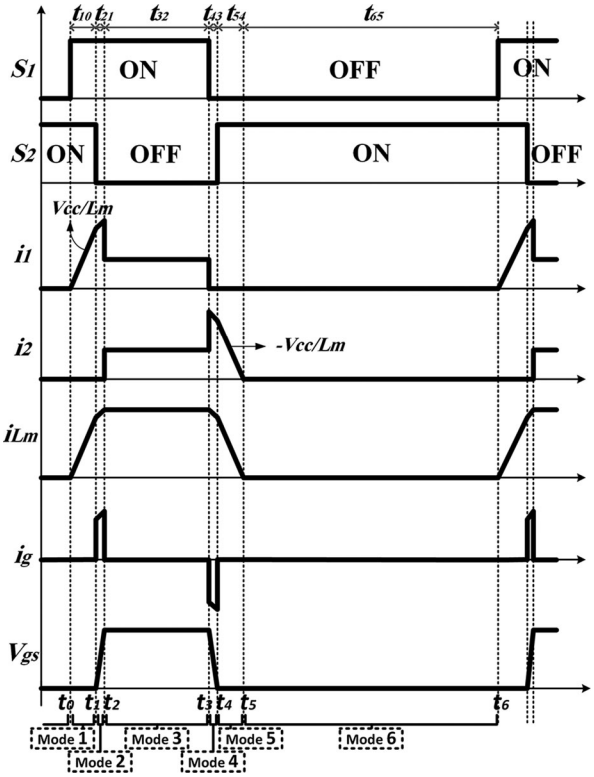

Fig. 2. Key waveforms of the proposed CSD.

drive signals for the control switches S_1 and S_2 are shown. Also, i_1, i_2, and i_g are the current waveforms through S_1, D_3, and the power MOSFET gate, respectively. i_{Lm} is the magnetizing inductance current, and V_{gs} is the gate-to-source voltage of the power MOSFET. The circuit operation at each stage is shown in Fig. 3.

It is assumed that control switch S_1 is OFF and S_2 is ON before t_0. Thus, the gate voltage of power MOSFET *Q* is clamped to zero and consequently *Q* is in OFF state.

1) Stage 1 [t_0, t_1) (magnetizing inductor current precharge interval)

At the beginning of this interval, S_1 is turned ON at zero current switching (ZCS) that allows the magnetizing inductance current i_{Lm} to increase linearly and the gate of power MOSFET *Q* is clamped to zero. The time interval of this stage is predetermined, based on the required charging current for the gate capacitance.

2) Stage 2 [t_1, t_2) (power MOSFET gate charge interval)

At t_1, switch S_2 is turned OFF under zero-voltage switching (ZVS) due to the large power MOSFET shunt capacitance C_g. During this interval, i_{Lm} is considered as a current-source. This stage ends when the gate–source voltage (V_{gs}) reaches the drive supply voltage $V_{CC} + V_F/2$. Since the forward voltage of diode is divided between L_1 and L_2 and thus the voltage across L_1 is $V_F/2$ and gate voltage increases to $V_{CC} + V_F/2$.

3) Stage 3 [t_2, t_3) (freewheeling interval)

At t_2, V_{gs} is clamped to $V_{CC} + V_F/2$ and the Schottky diode D_3 starts to conduct. During this interval, half of i_{Lm} flows through L_1 and the other half flows through L_2 and D_3. In other

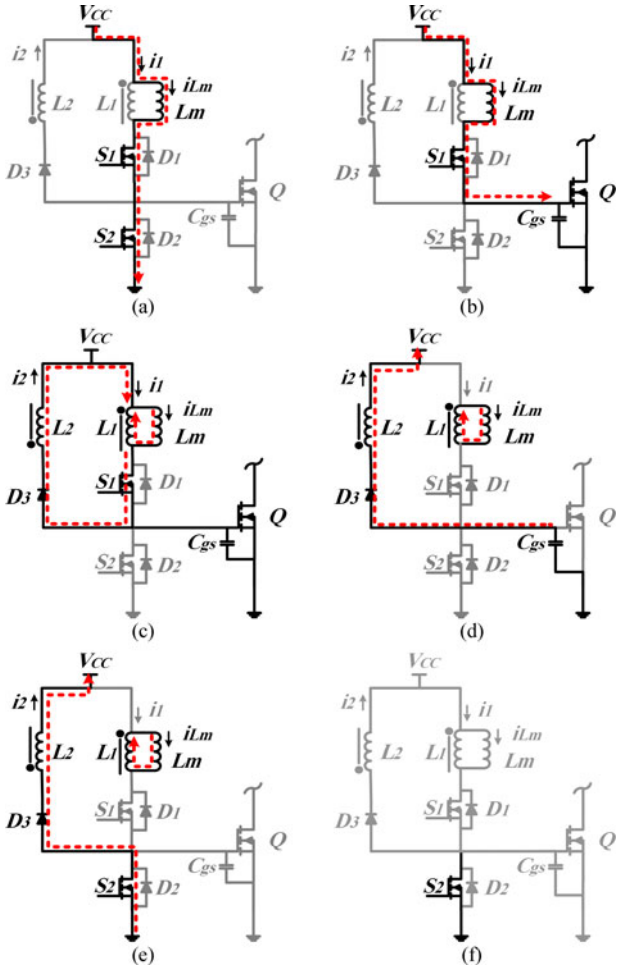

Fig. 3. Current path for each operating modes of the proposed circuit. (a) Mode 1. (b) Mode 2. (c) Mode 3. (d) Mode 4. (e) Mode 5. (f) Mode 6.

words, i_{Lm} is freewheeling during this stage. i_{Lm} equation is as follows:

$$i_{Lm} = i_{L1} + i_2. \tag{1}$$

Due to narrow duty cycle of buck VRMs, this interval is short especially at high switching frequencies.

4) Stage 4 $[t_3, t_4)$ (power MOSFET gate discharge interval)

At t_3, switch S_1 is turned OFF (under ZVS, due to C_g), which allows i_{Lm} to discharge the power MOSFET gate capacitance. During this interval, i_{Lm} is considered as current-source. This stage ends when V_{gs} reaches zero.

5) Stage 5 $[t_4, t_5)$ (energy recovery interval)

At t_4, D_2 begins to conduct and S_2 can be turned ON under ZVS. In this stage, the magnetizing inductance energy is recovered to power supply. This interval ends when i_{Lm} reaches zero.

6) Stage 6 $[t_5, t_6)$ (noise immunity interval)

During this interval, switch S_2 is ON and the gate–source voltage of Q remains clamped to zero. In other words, S_2 supports a low impedance path from the gate of power MOSFET to the ground, which protects the power MOSFET from undesired triggering.

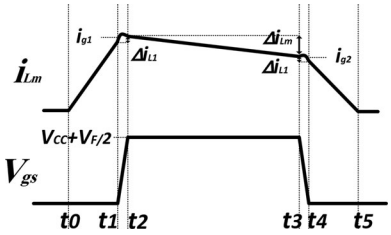

Fig. 4. Detailed waveforms of magnetizing inductance current i_{Lm} and power MOSFET gate-to-source voltage V_{gs} during the turn ON interval.

III. Loss Analysis and Design Procedure

Fig. 4 illustrates i_{Lm} and V_{gs} waveforms in details. Considering V_F and neglecting the ON state voltage drop of S_1 and S_2, V_{gs} reaches $V_{CC} + V_F/2$ at time t_2. As shown in Fig. 4, i_{g1} and i_{g2} are the average current flowing through the gate terminal of the power MOSFET during $[t_1 - t_2]$ (t_{21}) and $[t_3 - t_4]$ (t_{43}), respectively. i_{g1} and i_{g2} can be expressed as

$$i_{g1} = \frac{C_g \cdot (V_{CC} + V_F/2)}{t_{21}} \tag{2}$$

$$i_{g2} = \frac{C_g \cdot (V_{CC} + V_F/2)}{t_{43}}. \tag{3}$$

It is assumed that the power MOSFET gate is driven by constant currents of i_{g1} and i_{g2} during t_{21} and t_{43}; therefore, V_{gs} increases and decreases linearly. According to Fig. 3(a), the precharge current i_{Lm} attained at t_1 to turn ON the power MOSFET is

$$i_{Lm-ON} = \frac{V_{CC}}{L_m} \cdot t_{10} \tag{4}$$

where t_{10} is the time from t_0 to t_1 (the precharge time) and L_m is the magnetizing inductance. During intervals t_{21} and t_{43}, the average voltage of L_m is $\frac{V_{CC}+V_F/2}{2}$. Using the approximation used in [5], the current ripple Δi_{L1} (see Fig. 4) can be obtained as

$$\Delta i_{L1} = \frac{(V_{CC} - V_F/2) \cdot t_{21}}{2L_m}. \tag{5}$$

According to (4) and (5), the approximate equation relating the precharge current i_{Lm-ON} and i_{g1} is as follows:

$$i_{Lm-ON} = i_{g1} - \Delta i_{L1}/2. \tag{6}$$

As shown in [26, Fig. 12], Δi_{L1} is small when CSD circuit is applied to the high-side switch of buck VRMs ($\Delta i_{L1} \ll$ i$_{g1}$). The equation between i_{g1} and i_{g2} is

$$i_{g1} = i_{g2} + \Delta i_{Lm} \tag{7}$$

where Δi_{Lm} is the magnetizing inductance current drop from t_2 to t_3 (see Fig. 4).

Δi_{Lm} can be expressed as

$$\Delta i_{Lm} = \frac{V_F \cdot D}{2L_m \cdot f_{sw}} \tag{8}$$

where D is the duty cycle of power MOSFET and f_{sw} is the switching frequency.

Due to high frequency and narrow duty cycle of buck VRMs, the value of Δi_{Lm} is small ($\Delta i_{Lm} \ll i_{g1}$). For instance, in a 12-V buck VRM with CSD, for $f_{sw} = 1\,\text{MHz}$, $D = 0.1$, $V_{out} = 1.2\,\text{V}$, $V_F = 0.36\,\text{V}$, $L_m = 64\,\text{nH}$ and $t_{21} = 3.9\,\text{ns}$ [according to (2) and by considering the values of $i_{g1} = 2.5\,\text{A}$ and $C_g = 1.8\,\text{nF}$], Δi_{Lm} and Δi_{L1} values would be 0.28 A and 0.15 A, respectively. Δi_{Lm} and Δi_{L1} can be neglected in (6) and (7), since $|\Delta i_{Lm}| \ll i_{g1}$ and $|\Delta i_{L1}| \ll i_{g1}$. With these simplifications, it is assumed that $i_{g1} = i_{g2} = i_{Lm-ON} = i_g$.

A. Loss Analysis

Total loss in the proposed discontinuous dual-switch CSD circuit includes conduction losses, coupled inductors losses, gate resistance of power MOSFET losses, gate losses in control switches, and the output capacitance C_{OSS} losses. Since switch S_2 operates under ZVS, no additional switching losses are considered for S_2.

1) Conduction Losses: The rms currents flowing through S_1 and S_2 are obtained as follows:

$$i_{S1-RMS} = i_g \sqrt{f_{sw}\left(\frac{t_{10}}{3} + t_{21} + \frac{t_{32}}{4}\right)} \tag{9}$$

$$i_{S2-RMS} = i_g \sqrt{\frac{f_{sw}}{3}(t_{10} + t_{54})} \tag{10}$$

where t_{21} is the time duration from t_1 to t_2, t_{32} is the time duration from t_2 to t_3, and t_{54} is the time duration from t_4 to t_5. The conduction losses of the control switches S_1 and S_2 are

$$P_{cond-switch} = R_{ds(on),S1} \cdot I^2_{S1-RMS} + R_{ds(on),S2} \cdot I^2_{S2-RMS} \tag{11}$$

And the conduction losses of D_3 are equal to

$$P_{cond-D3} = V_F \cdot i_g \cdot f_{sw} \cdot \left(\frac{t_{32}}{2} + t_{43} + \frac{t_{54}}{2}\right) \tag{12}$$

where t_{43} is the time from t_3 to t_4. Due to high switching frequency and narrow duty cycle of buck VRMs, t_{32} $(= D/f_{sw})$ is small and the conduction losses of D_3 are insignificant. Therefore, the proposed CSD is not suitable for wide duty cycle applications. Consequently, the total losses can be expressed as

$$P_{cond-total} = P_{cond-switch} + P_{cond-D3} \tag{13}$$

2) Coupled Inductor Losses:

a) Copper losses: The rms current of i_{Lm} is

$$i_{Lm-RMS} = i_g \sqrt{f_{sw}\left(\frac{t_{10} + t_{54}}{3} + t_{41}\right)} \tag{14}$$

where t_{41} is the time duration from t_1 to t_4. The copper losses of inductor winding are as follows:

$$P_{copper} = ACR \cdot i^2_{Lm-RMS} \tag{15}$$

where *ACR* is the ac resistance of the coupled inductors windings [35].

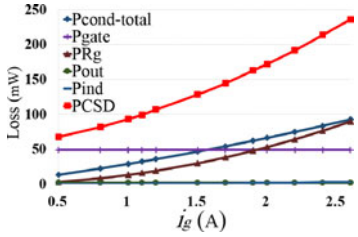

Fig. 5. Loss analysis of the proposed CSD.

b) Core losses: A general form of the ferrite core losses formula is

$$P_{core} = K_1 \cdot f^x_{sw} \cdot B^y \cdot V_e \tag{16}$$

where K_1 is a constant parameter which depends on core material, *B* is the maximum flux density in Gauss, *x* is the frequency exponent, *y* is the flux density exponent, and V_e is the effective core volume in cm^3 [35]. Thus, the total coupled inductor losses P_{ind} are

$$P_{ind} = P_{copper} + P_{core}. \tag{17}$$

3) Gate Losses of Control Switches: The gate losses equation for S_1 and S_2 is

$$P_{gate} = (Q_{gs(S1)} \cdot V_{gs1} + Q_{gs(S2)} \cdot V_{gs2}) \cdot f_{sw} \tag{18}$$

where $Q_{gs(S1)}, Q_{gs(S2)}$ are the total gate charge of switches S_1, S_2, respectively, and V_{gs1}, V_{gs2} are the drive voltages for these switches.

4) Gate Resistance Losses: The losses of power MOSFET gate resistance (R_g) can be calculated as

$$P_{Rg} = R_g \cdot i_g^2 (t_{21} + t_{43}) \cdot f_{sw}. \tag{19}$$

5) Output Capacitance Losses: Due to the ZCS operation of switch S_1 at turn ON instant, switching loss is only caused by the output capacitance (C_{OSS}) which can be expressed as

$$P_{out} = \frac{1}{2} C_{OSS(S1)} \cdot {V_{CC}}^2 \cdot f_{sw}. \tag{20}$$

Therefore, the total loss of the proposed CSD is

$$P_{CSD} = P_{cond-total} + P_{ind} + P_{gate} + P_{Rg} + P_{out}. \tag{21}$$

Fig. 5 illustrates the plot of $P_{cond-total}$, P_{ind}, P_{gate}, P_{Rg}, P_{out}, and P_{CSD} versus the gate current i_g.

B. Optimal Design

It is assumed that the gate of power MOSFET is driven by a constant current (the gate current i_g) during t_{21} and t_{43}. The first step of design optimization is to choose the optimal gate current. Design optimization involves a trade-off between switching losses and gate drive losses reduction [19], [26].

As illustrated in [19], higher gate drive current results in shorter switching transition time, which leads to lower switching losses. On the other hand, this increases the inductor rms current, which results in greater conduction losses of the CSD [19], [26]. In order to achieve the optimal design, the proposed CSD is applied to a buck converter as shown in Fig. 6. The specifications of buck VRM driven by the proposed CSD are:

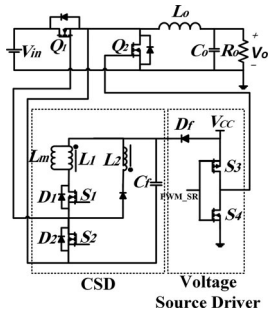

Fig. 6. Buck VRM with the proposed CSD.

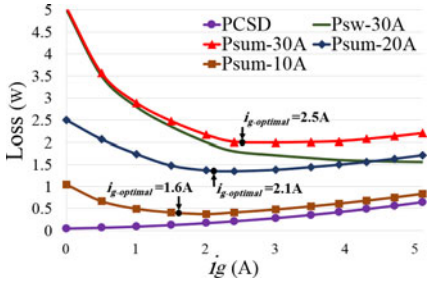

Fig. 7. Optimal design curves.

$V_{in} = 12\,\text{V}$; $V_o = 1.3\,\text{V}$; $V_{CC} = 5\,\text{V}$; $I_o = 30\,\text{A}$; $f_{sw} = 1\,\text{MHz}$; $L_o = 360\,\text{nH}$; high-side MOSFET Q_1: IRF7811AV ($R_g = 1.7\,\Omega$; total gate charge $Q_g = 17\,\text{nC}$ @ $V_{gs} = 5\,\text{V}$); low-side MOSFET Q_2: IRF6691; control switches S_1, S_2: FDN335N ($R_{ds(ON)} = 70\,\text{m}\Omega$; $Q_g = 3.5\,\text{nC}$ @ $V_{gs} = 5\,\text{V}$); diode D_3: MBR0520 (forward voltage $V_F = 0.36\,\text{V}$).

In order to achieve the optimal design, the analytical loss model in [19] is used. The total loss of the proposed CSD (P_{CSD}) and the switching loss P_{sw} along with their summation $P_{sum} = P_{CSD} + P_{sw}$ for various loads as a function of gate current i_g are illustrated in Fig. 7. The optimal value of the gate current $i_{g-optimal}$ is where P_{sum} reaches the minimum value. As can be observed, the optimal gate current value $i_{g-optimal}$ at 30 A load is around 2.5 A.

The second step of design optimization is to find the value of L_m. The optimal value of L_m is chosen based on the optimal design curve for $I_o = 30\,\text{A}$. According to (4), the optimal L_m can be expressed as

$$L_m = \frac{V_{CC}}{i_{g-optimal}} \cdot t_{10}. \tag{22}$$

It should be noted that t_{10}, the precharge time, can be selected. For $V_{CC} = 5\,\text{V}$, $i_{g-optimal} = 2.5\,\text{A}$ and by considering $t_{10} = 32\,\text{ns}$, the magnetizing inductor value is equal to 64 nH.

The third step of design optimization is to find the precharge time t_{10} for other load currents. According to optimal design curves (see Fig. 7), at load currents of 20 and 10 A, the optimal drive current $i_{g-optimal}$ is 2.1 and 1.6 A, respectively. According to (4), at load currents of 20 and 10 A, the precharge time t_{10} is chosen 27 and 20 ns, respectively.

For load currents less than 5 A, commercial IC PWM controllers of buck VRM [31] reduce the switching frequency

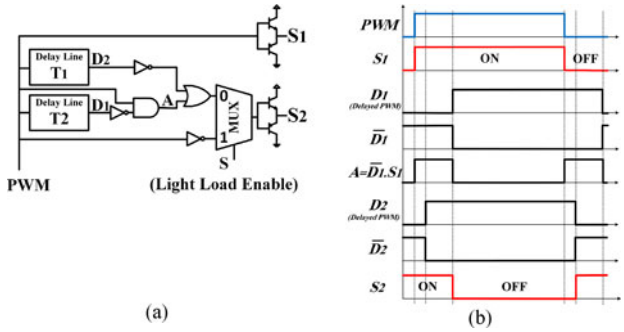

Fig. 8. Logic circuit and logic waveforms used to create the control switch gating signals of S_1 and S_2.

proportional to the load in order to reduce the switching and gate drive losses. During the light load condition ($I_o < 5\,\text{A}$), the gate drive losses are critical. The VRM spends 20% of the time at full load and the other 80% of time at light load [16]. Thus, in order to achieve further gate loss reduction, the proposed circuit operates as an RGD for $I_o < 5\,\text{A}$. In this case, first S_1 turns ON and gate capacitor is charged in a resonance with L_m. Then, gate voltage reaches to $V_{CC} + V_F/2$ and current of L_m freewheels in D_3. Then, S_2 is turned ON and gate capacitor is discharged in S_2, and also, magnetizing inductance energy is recovered. Under this condition, only charging energy of gate capacitor is recovered and it is discharged in S_2. Also, gate drive losses are minor since L_m is not precharged.

The logic circuit presented in Fig. 8(a) can be employed to create the two signals for S_1 and S_2. High-speed gates should be used for the logic elements. Delay line such as Maxim DS1100 can be used to give the proper delay time. A two input multiplexer can be used to change the operating condition between light load and normal load. Also, the logic waveforms at normal load condition (when multiplexer selector *S* is zero) are shown in Fig. 8(b). Delay line T_2 delays the PWM signal as much as the time period from t_0 to t_1. Delay line T_1 delays the PWM signal as much as the time period from t_3 to t_4.

IV. Advantages of the Proposed CSD

Compared to continuous CSDs, discontinuous CSDs can achieve lower drive losses, thus they are more suitable for buck VRMs as illustrated in this paper and in [30]. The proposed CSD has many advantages over previous discontinuous CSDs [5], [8], [18], [24]–[27]:

1) *Fewer control switches*: Previous discontinuous CSDs [5], [8], [18], [24]–[26] employ four control switches but the proposed discontinuous CSD requires only two switches.
2) *High stability and Cdv/dt immunity*: In the proposed CSD, the power MOSFET gate is either clamped to zero or to $V_{CC} + V_F/2$, similar to other CSDs, which prevents the power MOSFET from undesired triggering.
3) *Capability of operating at higher switching frequencies based on the minimum duty cycle required (or ability to achieve smaller minimum duty cycle for a certain switching frequency).*

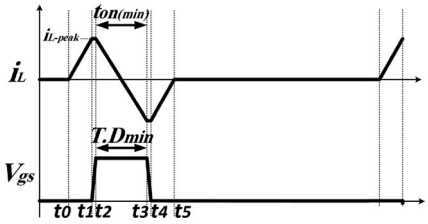

Fig. 9. Key waveforms of the previous CSDs with minimum duty cycle.

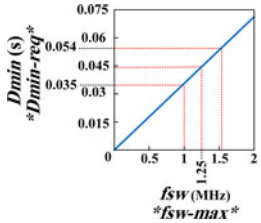

Fig. 10. Maximum switching frequency versus minimum required duty cycle for the introduced CDS in [26].

Fig. 9 illustrates the inductor current i_L along with the power MOSFET gate-to-source voltage V_{gs} for existing discontinuous CDSs [5], [8], [24]–[27] which are operating at their highest achievable switching frequency $f_{sw(\max)}$ for the required minimum duty cycle $D_{\min-req}$ (or operate with minimum achievable duty cycle $D_{\min}$ for a certain f_{sw}). As shown in Fig. 9, a minimum period of time $t_{on(\min)}$ is required for inductor current to change from the positive peak i_{L-peak} to the negative peak value, in order to discharge the power MOSFET gate capacitance in the gate drive circuit of [5], [8], and [24]–[27]. In other words, in all existing current-source gate drive circuits, due to the structure, the inductor current direction should be reversed for discharging the gate capacitor, which is time consuming. Since this occurs at switch ON time, therefore the minimum duty cycle is limited. The required $t_{on(\min)}$ limits the maximum achievable switching frequency $f_{sw(\max)}$ for the required minimum duty cycle $D_{\min-req}$ (or limits the minimum duty cycle $D_{\min}$ for a certain value of f_{sw}).

$f_{sw(\max)}$ as the function of $D_{\min-req}$, or f_{sw} as a function of $D_{\min}$, for the introduced CDS in [26] is presented in Fig. 10 and [26, Fig. 6], where the peak inductor current is 2.3 A, inductor value is 22 nH, and the precharge time is 15 ns. According to Fig. 10 and [26, Fig. 6], at $f_{sw} = 1$ MHz, the minimum duty cycle is limited to 3.5%.

The duty cycle of buck VRM in CCM mode is

$$D = \frac{V_{out} + I_o(r_{DS2} + R_L)}{V_{in} - I_o(r_{DS1} - r_{DS2})} \tag{23}$$

where r_{DS1} and r_{DS2} are on-resistance of high-side and low-side switches of buck VRM, respectively, and R_L is the output-inductor series resistance. The sixth generation of Intel processors requires a voltage between 0.55 and 1.52 V [36]. When the CPU current is low, VR output voltage should be high and when the CPU current is high, VR output voltage should be low [37]. The VR controller achieves this and the process is called adaptive voltage positioning control (AVP)

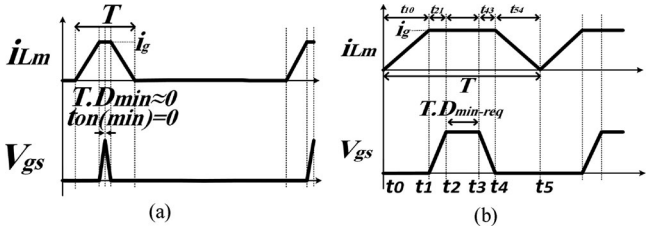

Fig. 11. Key waveforms of the proposed CSD. (a) At minimum duty cycle. (b) At maximum achievable switching frequency.

[37]. AVP causes less power consumption in the CPU [37]. So, the minimum output voltage (or minimum duty cycle required in CCM mode) occurs at maximum load. For $V_{in} = 12$ V $\pm$ 5%, $I_o = 30$ A per-phase, $V_{out} = 0.55$ V, $r_{DS1} = 12\,\text{m}\Omega$ (IRF7811AV) and $r_{DS2} = 2.5\,\text{m}\Omega$ (IRF6691), $D_{\min-req}$ in CCM mode is equal to 5.4% and then according to Fig. 10 and [26, eq. (11)], maximum switching frequency $f_{sw(\max)}$ of introduced CSD in [26] is limited to 1.54 MHz. Laptop voltage regulators are required to operate with a wide range of input voltage values from 8.7 to 19 V [37], [38]. The adaptor has a voltage of 19 V $\pm$ 5% [38]. Intel core i7-900 mobile processors require voltage between 0.75 and 1.4 V [39]. Thus, $D_{\min-req}$ is equal to 4.4% and according to Fig. 10, maximum switching frequency of introduced CSD in [26] $f_{sw(\max)}$ is limited to 1.25 MHz.

Fig. 11(a) illustrates i_{Lm} and V_{gs} waveforms of the proposed CSD at the minimum duty cycle. Unlike existing discontinuous CSDs, the proposed CSD does not require the inductor current to change from the positive to the negative peak value, in order to discharge the power MOSFET gate capacitance. As can be observed, the proposed CSD can achieve ultranarrow minimum duty cycle $D_{\min}$ ($D_{\min} \approx 0$).

Fig. 11(b) shows i_{Lm} and V_{gs} waveforms of the proposed CSD at the maximum achievable switching frequency for the minimum required duty cycle requirement $D_{\min-req}$. Since the proposed CSD does not require $t_{on(\min)}$, to change the inductor current from the positive peak i_{L-peak} to the negative peak value, the sum of t_{10}, t_{21}, t_{43}, and t_{54} limits the switching frequency.

According to Fig. 11(b), $f_{sw(\max)}$ can be expressed as

$$t_{10} + t_{21} + DT_{\min} + t_{43} + t_{54} = T_{\min} \rightarrow f_{sw(\max)} = \frac{1 - D_{\min-req}}{t_{10} + t_{21} + t_{54} + t_{54}} \tag{24}$$

where $T_{\min}$ is the minimum switching period.

For $t_{10} = 32$ ns, $i_g = 2.5$ A (according to optimal design curve), $L_m = 64$ nH, power MOSFET: IRF7811A, $t_{21} = t_{43} = 3.9$ ns [according to (2) and (3)] and $D_{\min-req} = 5.4\%$, the maximum achievable switching frequency $f_{sw(\max)}$ is 13.9 MHz. In comparison to existing discontinuous CSDs [5], [8], [24]–[27], the proposed CSD can operate at higher switching frequency.

A comparison between the features of the proposed CSD and circuits presented in [5], [20], [25], [26], and [29] is provided in Table I.

TABLE I
COMPARISON BETWEEN THE PROPOSED CSD AND OTHER INTRODUCED CIRCUITS

Driver circuit	DCM operation capability	Number of control switches	Capability of operating at very small duty cycle	Capability of operating at very high frequency
Proposed CSD	√	2	√	√
Presented in [5]	√	4	×	×
Presented in [20]	×	2	×	×
Presented in [25]	√	4	×	×
Presented in [26]	√	4	×	×
Presented in [29]	√	4	×	×

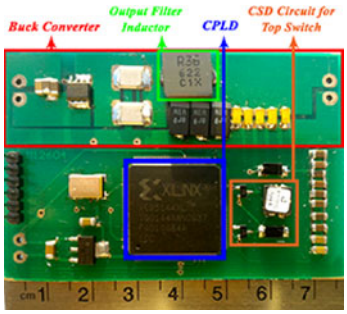

Fig. 12. Photo of buck VRM prototype with the proposed CSD.

TABLE II
DESIGN PARAMETERS

Input voltage V_{in}	12 V
Output voltage V_{out}	1.3 V
Output current I_o	30 A
Switching frequency f_{sw}	1 MHz
Gate driver voltage V_{CC}	5 V
Top switch Q_1	IRF7811AV
Bottom switch Q_2	IRF6691 (two parallel)
Output filter inductance L_o	360 nH
Driver switches S_1, S_2	FDN335N
Magnetizing inductance L_m	64 nH-(SLC7530D,Coilcraft)
Schottky diode D_3	MBR0520

V. EXPERIMENTAL RESULTS

A. Buck VRM With the Proposed CSD

In order to verify the theoretical analysis, a prototype of the buck VRM with the proposed CSD is implemented and shown in Fig. 12. As illustrated in Fig. 6, high-side switch of the buck converter is driven by the proposed CSD, while the synchronous MOSFET is driven with a conventional voltage-source-driver. The design parameters of the implemented prototype are presented in Table II. A Xilinx XC95144XL CPLD is used to generate the control signals. The nonground referenced control switches S_1, S_2 are driven with the level-shift circuit (ISL6207).

Fig. 13(a) shows the control signal of switches S_1 and S_2, along with the power MOSFET gate voltage. The two top waveforms in Fig. 13(a) are the gating signals for S_1 and S_2, and the bottom waveform is the gate–source voltage of the high-side FET. Fig. 13(b) illustrates the currents of diode D_3, i_2, and the

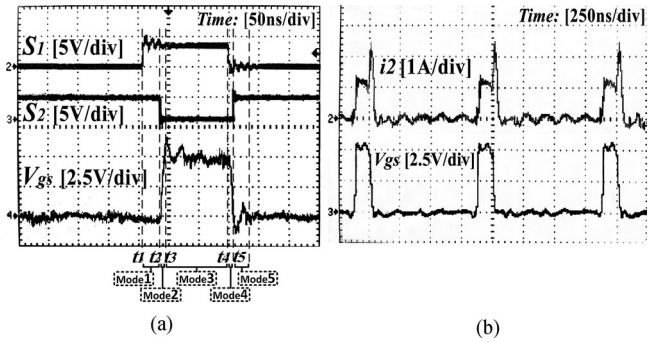

Fig. 13. Experimental waveforms. (a) CPLD gate waveforms for S_1 and S_2 with V_{gs}. (b) i_2 and V_{gs}.

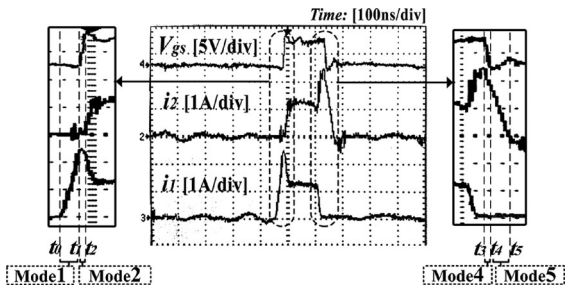

Fig. 14. Experimental waveforms of V_{gs} with i_1 and i_2.

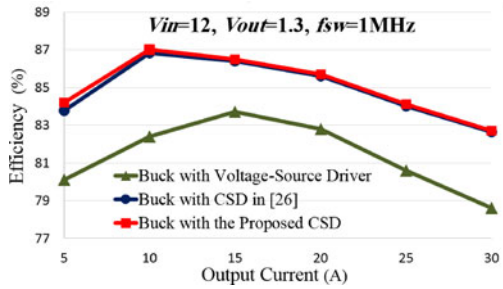

Fig. 15. Efficiency comparison.

power MOSFET IRF7811AV gate voltage V_{gs}. The peak value of i_{Lm} is 2.5 A, which is the optimized CSD current value. Fig. 14 shows the gate-to-source voltage of power MOSFET IRF7811AV V_{gs} along with the current of diode D_3, i_2, and the current of switch S_1, i_1. It is observed that the gate of power MOSFET is charged and discharged with nearly constant current. So quick turn-ON and turn-OFF transition times can be observed, which means that fast switching speed is achieved and switching losses are reduced.

Fig. 15 shows the efficiency comparison between a buck VRM driven by the proposed CSD and a similar buck VRM driven by the CSD proposed in [26] (with gate driver peak current and precharge time equal to 2.5 A and 32 ns, respectively), along with a buck VRM driven by conventional VSDs. It should be noted that the efficiency is improved from 78.6% to 82.7% at 30 A output current by using the proposed CSD compared to conventional voltage-source drivers. The voltage source gate driver was implemented with FDN342P and FDN335N switches.

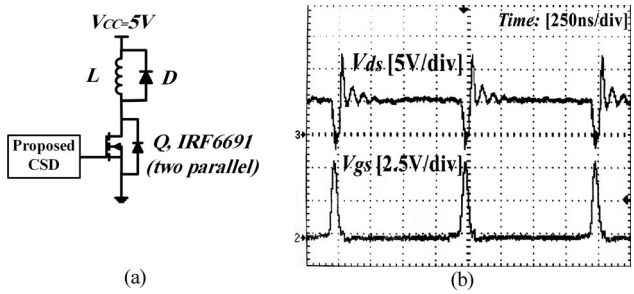

Fig. 16. (a) Gate driver testing circuit. (b) Experimental waveforms of drain–source voltage and gate–source voltage at narrow duty cycle.

B. Narrow Duty Cycle Operation

The introduced CSD can achieve ultranarrow duty cycles, and in order to verify this feature, the proposed CSD is applied to two parallel MOSFET IRF6691, as shown in Fig. 16(a). IRF6691 drain-to-source and gate-to-source voltage at narrow duty cycle is shown in Fig. 16(b).

VI. Conclusion

In this paper, a dual-switch discontinuous CSD is proposed for a buck converter with narrow switch on time which is proper for VRM. This paper provides optimal design considering the trade-offs between the switching losses reduction and drive loss reduction at different loads. In comparison to other CSDs, the presented CSD has fewer switches and can operate at higher switching frequencies. The significant reduction of switching losses, gate energy recovery, noise immunity, and soft switching for the drive switches are other features of the proposed CSD. In order to verify the analysis, a 12 V buck VRM with the introduced CSD at 1 MHz is implemented. The efficiency of the buck converter using the proposed CSD has improved as compared to the conventional voltage-source drivers.

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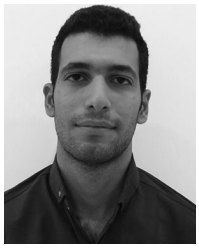

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