Soft-Switching Solid-State Transformer (S4T)

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***Abstract*—This paper presents a new topology for a fully bidirectional soft-switching solid-state transformer (S4T). The minimal topology, featuring 12 main devices and a high-frequency transformer, does not use an intermediate dc voltage link, and provides sinusoidal input and output voltages. The S4T can be configured to interface with two- or multiterminal dc, single- or multiphase ac systems. An auxiliary resonant circuit creates zero-voltage-switching conditions for main devices from no-load to full-load, and helps manage interactions with circuit parasitic elements. The modularized structure allows series and/or parallel stacking of converter cells for high-voltage and high-power applications.**

***Index Terms*—Bi-directional power control, dc, high-frequency isolation, multiterminal, single-phase ac, soft switching, solid-state transformer (SST), three-phase ac, zero-voltage-switching (ZVS).**

I. Introduction

THE idea of a solid-state transformer (SST) has attracted tremendous interest for almost five decades, ever since the principles of power conversion were first understood. The promise of replacing numerous existing 60 Hz transformers, with a power electronics based device that was smaller, controllable, and more flexible, has an undeniable appeal. However, the reality has been much more challenging. It has proven difficult to match the low cost ($25/kVA), high efficiency (>97%), and long life (40 years) of the 60 Hz grid-connected transformer. Furthermore, the practical challenges posed by fault current coordination (>10 kA) with downstream switchgear, and, for transformers connected directly to the 13 kV grid (or higher), the need for 120 kV (or higher) basic insulation level, seem well beyond the capability of cost-effective state of the art power conversion technology.

In more specific applications, the potential for SST's is real. Unidirectional ac/dc converters with high-frequency isolation are really switched mode power supplies, and should not be included in the family of SSTs. An SST should convert ac (or dc) voltage to another ac (or dc) voltage with galvanic isolation between the input and output, possibly at a different voltage level and/or frequency, and should inherently be able to provide bidirectional control of real and/or reactive power flows. Applications include locomotives, light rail, electric vehicle (EV) fast chargers, photovaltaic (PV) inverters, and battery energy storage systems—many of them emerging fields. It could also include specialized bidirectional drives where 60 Hz isolation transformers are often used to manage noise and transient injection into long cables or motors, along with converters to condition the voltage applied to the motor.

Significant work on SSTs has been documented in the literature [1]–[14]. These can be classified as single stage with ac switches on input and output, connected with a high-frequency transformer [1]–[4], two-stage with an ac/dc converter followed by an inverter [5], [6], and three-stage based on ac/dc–dc/dc (including isolation)–dc/ac converters in cascade [7]–[9]. Several papers have concluded that the three-stage converter, including a dual-active-bridge (DAB) soft-switched dc/dc converter, offers perhaps the best performance and controllability [10], [11]. Scaling the SST for higher power and higher voltages required for traction and direct grid connected applications is also seen to be challenging, and has been addressed in many papers [12]–[14].

One of the major restrictions of direct ac/ac types of conversion comes from the leakage inductance of the transformer. At higher frequencies, this becomes the limiting element in the ability to transfer power across the isolation barrier [15], [16]. Factors such as diode reverse recovery can result in energy trapped in the leakage inductance, which in turn causes excessive stress on the components and limits operating range and efficiency [16]. The DAB converter is considered attractive because it handles all real device and transformer parasitic elements, and still allows zero-voltage-switching (ZVS), albeit over a narrow range of voltage transfer ratios [17]. Even for the three-stage SST, assuming that the DAB converter always operates under ZVS conditions, the rectifier and inverter have to operate in hard switching mode and incur high switching losses [18].

Several authors have attempted to address these issues, for instance with resonant switching to reduce losses, or simpler minimal topologies to reduce complexity, but the efforts have always fallen short of addressing the myriad of issues that can limit SST performance [3], [4], [19]. Recent papers on the Dyna-C showed a minimal SST topology with 12 devices that realized a three-phase ac/three-phase ac (or dc) conversion, with trapped leakage energy management [20]–[23]. However, efficiencies were poor primarily due to high device conduction and switching losses, as well as diode reverse recovery related losses [16]. The Dyna-C circuit did exhibit desirable properties in terms of

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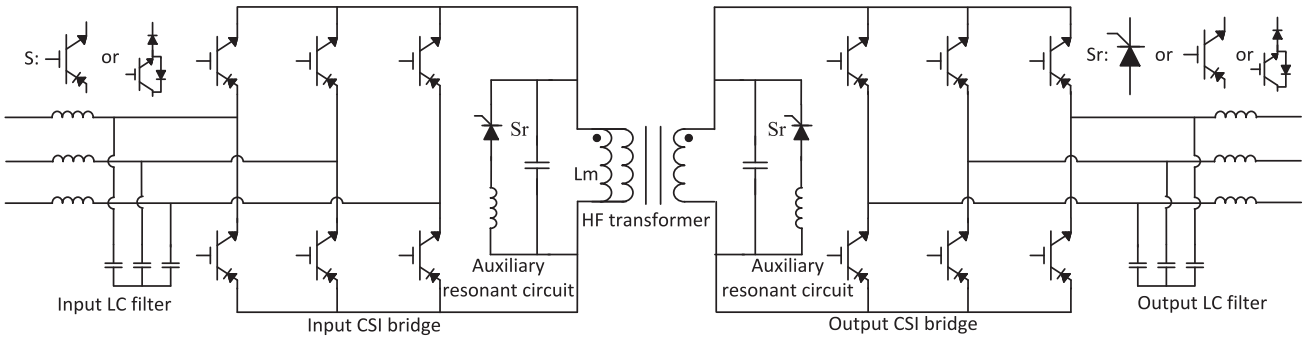

Fig. 1. Topology for the three-phase soft-switching solid-state transformer (S4T).

scaling the voltage, and realizing multiport structures for renewable energy applications.

This paper presents a new patent pending topology for a soft-switching solid-state transformer (S4T), which has a simple and symmetrical architecture, minimal device and component count in the power flow path (similar to [19] and [20]), with small rated auxiliary components that enable the soft switching property [26]. Unlike the DAB converter, the S4T realizes ZVS for all its main devices over the entire load range, and features controlled *dv/dt* and *di/dt* rates. Furthermore, it can realize dc, single- or multiphase on the input/output at arbitrary frequencies and power factors with sinusoidal voltages and low electromagnetic interference (EMI). It shows simple control and benign shut down under fault and failure modes, and is relatively insensitive to key parameters such as transformer leakage inductance. By eliminating components such as electrolytic capacitors, it can also realize higher power density and longer life. Finally, it holds the promise of achieving high efficiency, particularly as it scales up in voltage and power. It provides the simplicity of single-stage SSTs, with the control attributes of the three-stage SSTs, with higher efficiency, lower *dv/dt* rate, and an ability to scale that seems unique.

II. S4T Topology

Fig. 1 shows the topology for the three-phase S4T, which comprises four elements:

1) an air-gapped high-frequency transformer to provide galvanic isolation and a limited amount of energy storage;
2) current source inverter (CSI) bridges to interface with sources and loads;
3) terminal *LC* filters for suppressing harmonics; and
4) auxiliary resonant circuits to provide ZVS switching conditions for all the main devices.

The CSI bridges are configured with switches that conduct current in one direction but block voltage in both directions, and can be implemented with either an insulated gate bipolar transistor (IGBT) in series with a diode, or a reverse blocking IGBT (RB-IGBT), with the latter providing lower losses and more compact converter design. The auxiliary resonant circuit comprises an active device, an inductor, and a capacitor. The auxiliary active device can be implemented with an IGBT in series with a diode, an RB-IGBT, or a thyristor (at least in principal), with the device operated under zero-current-switching (ZCS). In the case of a nonisolated topology in which the transformer is replaced by an inductor, a single auxiliary resonant circuit could be used to provide ZVS conditions for both bridges. For real transformers, the finite transformer leakage inductance would interfere with the resonant transitions. As a result, the use of two auxiliary resonant circuits is proposed, one for each bridge.

Even though the circuit only requires 12 main active devices and two low-rated auxiliary devices, the S4T can provide all functionalities of the more complex three-stage SSTs, which include:

1) bidirectional power flow control;
2) independent input and output VAr injection;
3) voltage step-up and step-down; and
4) arbitrary power factor and frequency (including dc) for the input and the output.

The S4T topology possesses several key advantages that conventional SST solutions do not have:

1) no bulky dc energy storage capacitors;
2) no inrush current under start-up and fault conditions;
3) fast dynamic performance due to direct current control;
4) modular structure to scale to high-voltage and high-power levels; and
5) ZVS soft-switching conditions for all the main devices over the full load range.

It should be noted that the S4T could implement a variety of conversion functions. These include dc/dc, single-phase ac to dc, single-phase ac to three-phase ac, and multiport structures. The device topology and configuration remain the same for both dc and ac sources/loads, and the power transfer with ZVS is purely achieved through control. As an example, a triport topology shown in Fig. 2 is exactly the same as that of Fig. 1, but it can interface with PV, battery, and three-phase grid as shown in the figure. Fig. 3(a) shows the dc to single-phase ac topology, for which both the input and output converter bridges have two device poles. This topology also has a modular feature, allowing it to be stacked for medium voltage and high power. Fig. 3(b) shows the stacked low-voltage dc to medium-voltage three-phase ac converter by using this dc to single-phase ac converter module. On the low-voltage/high-current side (dc side), the converter modules are connected in parallel to share current. On the high-voltage/low-current side (three-phase ac side), the converters are connected in series for each phase to configure a high-voltage single-phase ac, and three of these stacks compose

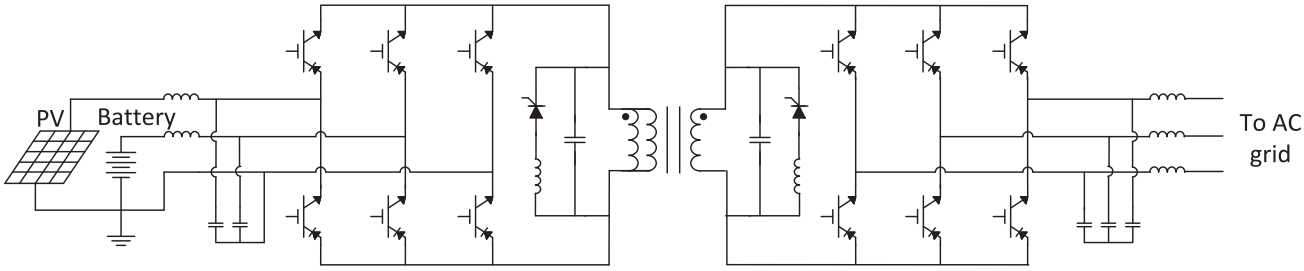

Fig. 2. Triport topology to interface with PV, battery, and three-phase grid.

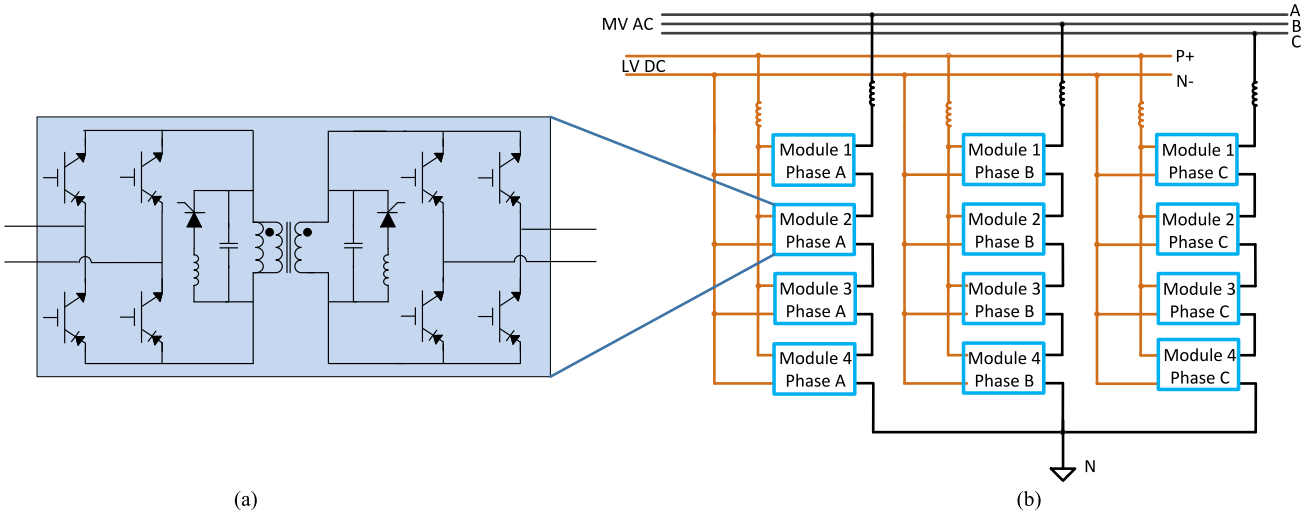

Fig. 3. DC to single-phase ac converter module and its stacking: (a) single module; and (b) stacking the modules for medium-voltage high-power.

the three-phase medium-voltage ac. All the series-connected modules on the medium-voltage side are properly controlled to equally share voltage.

III. Principle of Operation

In the steady state, the S4T maintains a constant dc current through the transformer magnetizing inductance. Its operation is similar to the dc/dc flyback converter in that the input bridge charges the transformer magnetizing inductance and the output bridge discharges it (although the concept of input and output in bidirectional converters in purely notional). Over one switching cycle, the S4T has the following types of states:

1) five active states in which the transformer magnetizing current flows in a loop between the input or output bridge and the transformer magnetizing inductance,
2) one ZVS transition state between any two adjacent active states in which the magnetizing current flows through the resonant capacitors to provide ZVS conditions for turning-off and turning-on devices, and
3) one resonant state in which a capacitor voltage is reset so as to be ready for the next switching cycle operation.

For the five active states, the duty cycle of each state is determined by the actual charge delivered to the specific terminal over each switching cycle. The device duty cycle dT_S is governed by

$$\int_0^{dT_S} I_m\,dt = Q \tag{1}$$

$$I_g^* = Q^* * T_S \tag{2}$$

where I_m is the dc current flowing through the transformer magnetizing inductance L_m, I_g^* is the referenced line current, and T_S is the switching period.

The operating states over one switching cycle are shown as follows. The corresponding circuit states and conceptualized waveforms are shown in Figs. 4 and 5. An overall cycle can be summarized as follows. The "charging" cycle where the current in the transformer magnetizing inductance is built up consists of two active states. The incoming line–line voltage with the highest voltage level (a_i and b_i in this example) is connected to the transformer [see Fig. 4(a)]. After a time determined by (1) and (2), $S_{\rm ibn}$ is turned off and $S_{\rm icn}$ is turned on. The magnetizing current flowing through the resonant capacitors $C_{\rm ri}$ and $C_{\rm ro}$ causes the voltage across the transformer to vary with a controlled *dv/dt* rate until switch $S_{\rm icn}$ begins to conduct [ZVS transition state in Fig. 4(f)]. This allows zero turn-off loss for $S_{\rm ibn}$ and zero turn-on loss for $S_{\rm icn}$. When the controller determines that $S_{\rm icn}$ should be turned off, the same process is repeated, with the input converter entering a free-wheeling mode [see Fig. 4(c)]. The output bridge now continues the process,

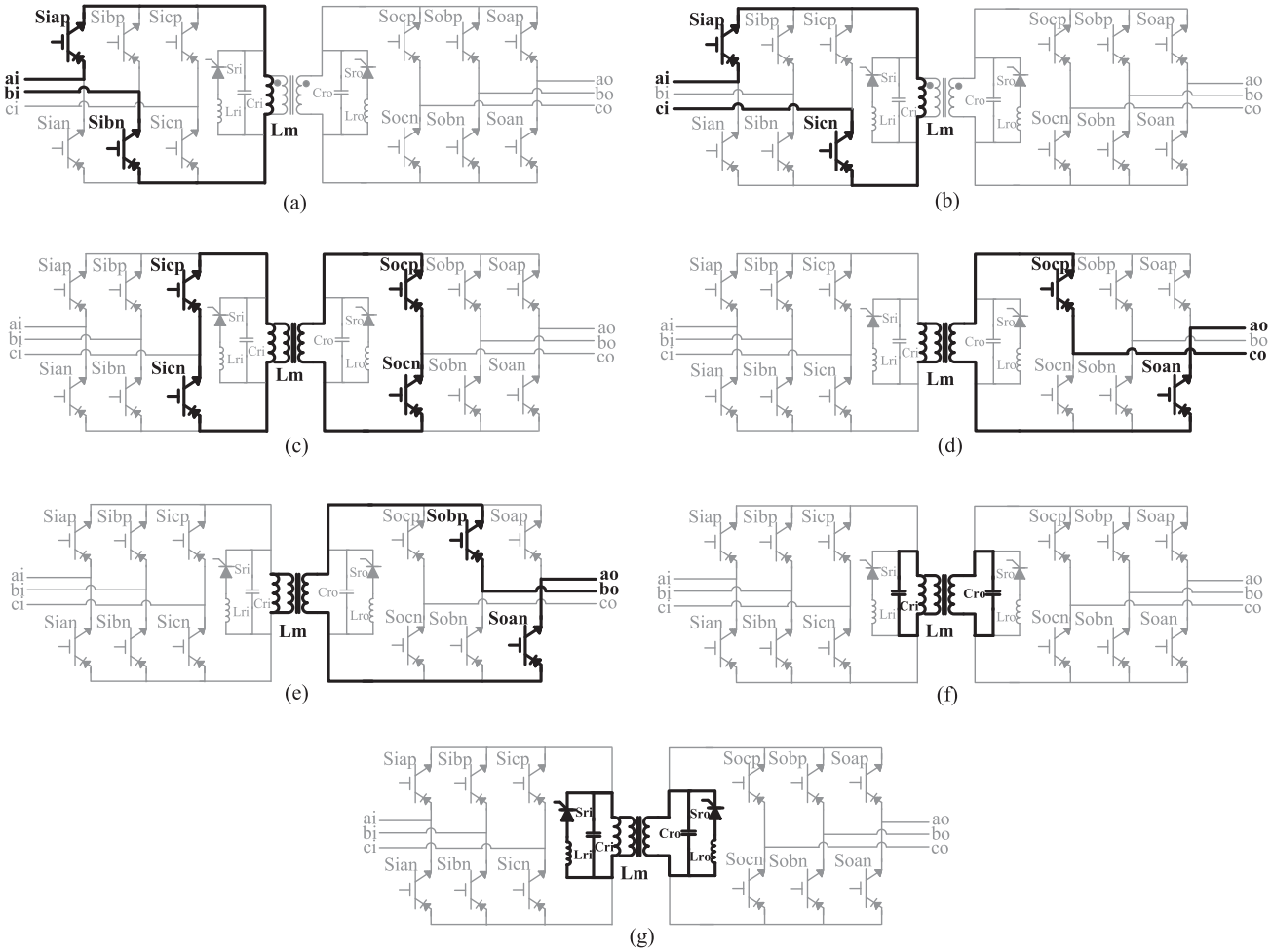

Fig. 4. Operating states over one switching cycle: (a) state 1—charging the magnetizing inductance with the first line-to-line input voltage; (b) state 2—charging the magnetizing inductance with the second line-to-line input voltage; (c) state 3—freewheeling; (d) state 4—discharging the magnetizing inductance with the first line-to-line output voltage; (e) state 5—discharging the magnetizing inductance with the second line-to-line output voltage [(a)–(e) are the five active states]; (f) state 0—ZVS transition state; and (g) state 6—resonant state.

discharging the transformer magnetizing current, while continuing the process of moving from state to state, using ZVS transitions to achieve the desired soft switching. The discharge cycle ends when the line–line voltage with the highest magnitude on the output side is connected across the transformer. At this point, a resonant transition is enabled by the auxiliary resonant circuit, which resets the voltage across the resonant capacitors, and sets up the conditions for the next switching cycle. The process is described in greater detail as follows.

A. State 1: Charging the magnetizing inductance with the first line-to-line input voltage [see Fig. 4(a)]

The transformer is connected to phases a_a and b_i by turning on S_{iap} and S_{bin}. The voltage across the resonant capacitors, which is V_{cr}, equals to the first line-to-line input voltage V_{abi}. The transformer magnetizing inductance L_m is being charged by V_{abi}, and thus the current i_m increases linearly. This state ends when the average current delivered to phase b_i over one switching cycle equals to its reference current, as governed by (2).

B. State 0: ZVS transition state [see Fig. 4(f)]

S_{ibn} is turned OFF, causing the magnetizing current to flow through the resonant capacitor, providing significantly reduced *dv/dt* rate. S_{ibn} can be turned off with zero switching loss. Capacitors are charged by i_m, and its voltage starts dropping from V_{abi}. Within this state, the incoming device S_{icn} can be gated-on. However, there is no current flowing through the devices since V_{cr} is larger than V_{aci} and the devices are reverse blocked. This state ends when V_{cr} drops to a value equal to V_{aci}, then S_{iap} and S_{icn} conduct. S_{icn} is actually turned on with zero switching loss.

C. State 2: Charging the magnetizing inductance with the second line-to-line input voltage [see Fig. 4(b)]

S_{iap} and S_{icn} conduct, and L_m is charged by V_{aci}. i_m linearly increases again and V_{cr} equals to V_{aci}. This state again continues

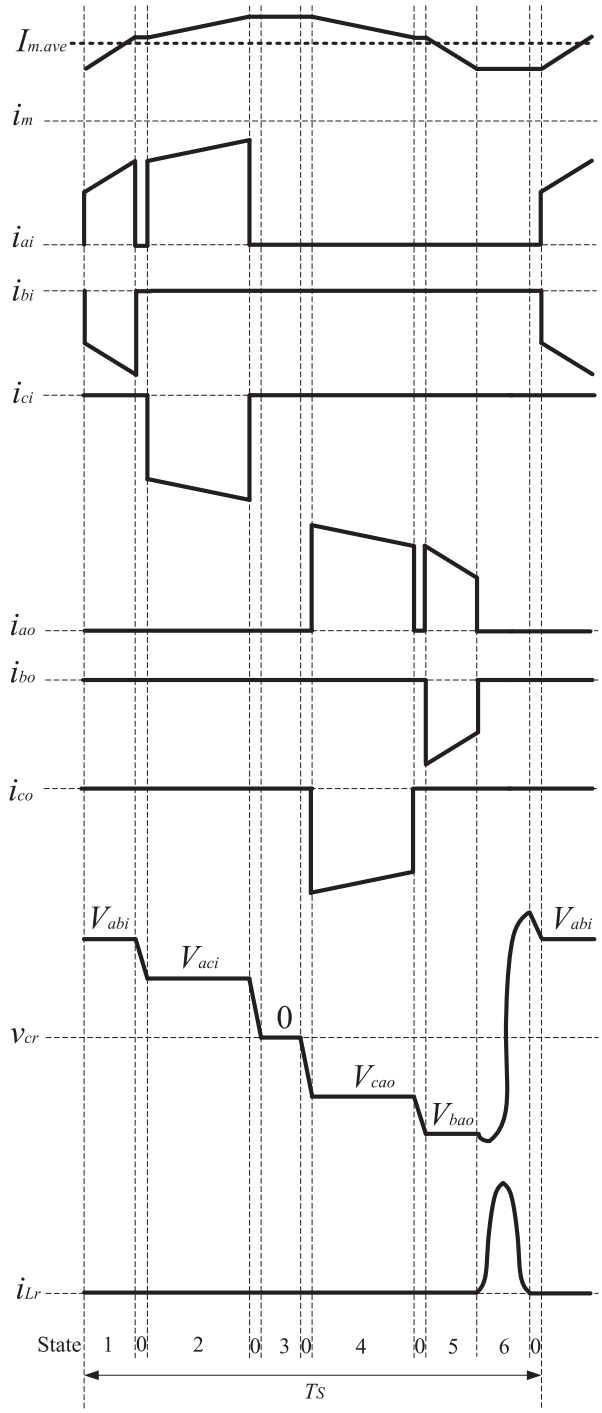

Fig. 5. Conceptualized waveforms [states 1–5 correspond to Fig. 4(a)–(e); state 0 corresponds to Fig. 4(f); and state 6 corresponds to Fig. 4(g)].

until the average current delivered to phase $c_{\rm i}$ over one switching cycle equals its reference.

D. State 0: ZVS transition state [see Fig. 4(f)]

$S_{\rm iap}$ and $S_{\rm icn}$ are turned off under ZVS conditions. The resonant capacitors are charged by i_m again until its voltage drops to zero.

E. State 3: Freewheeling [see Fig. 4(c)]

The converter enters the freewheeling state by turning on $S_{\rm icp}$ and $S_{\rm icn}$ of the input bridge as well as $S_{\rm ocp}$ and $S_{\rm ocn}$ of the output bridge under ZVS conditions. i_m flows through these two legs rather than flowing to the input/output terminals. $V_{\rm cr}$ equals to zero in this state.

F. State 0: ZVS transition state [see Fig. 4(f)]

$S_{\rm icp}$, $S_{\rm icn}$, and $S_{\rm ocn}$ are turned off under ZVS conditions. Resonant capacitors are charged by i_m again, and its voltage starts dropping to a negative value.

G. State 4: Discharging the magnetizing inductance with the first line-to-line output voltage [see Fig. 4(d)]

$S_{\rm ocp}$ and $S_{\rm oan}$ conduct under ZVS conditions, and L_m is discharged by $V_{\rm cao}$. $V_{\rm cr}$ equals to $V_{\rm cao}$. This state ends when the average current delivered to phase c_o over one switching cycle equals to its reference.

H. State 0: ZVS transition state [see Fig. 4(f)]

$S_{\rm ocn}$ is turned off under ZVS condition. Resonant capacitors are charged by i_m again until its voltage equals to $V_{\rm bao}$.

I State 5: Discharging the magnetizing inductance with the second line-to-line output voltage [see Fig. 4(e)]

$S_{\rm obp}$ and $S_{\rm oan}$ conduct under ZVS conditions, and L_m is discharged by $V_{\rm bao}$. $V_{\rm cr}$ equals to $V_{\rm bao}$. This state ends when the average current delivered to phase b_o over one switching cycle equals to its reference.

J. State 6: Resonant [see Fig. 4(g)]

$S_{\rm obp}$ and $S_{\rm oan}$ are turned off under ZVS conditions. Auxiliary switch S_r is turned on under ZCS condition to initiate the resonant operation between L_r and C_r. This state ends when the current through L_r drops to zero, and S_r is turned off under ZCS condition. As a result, the voltage polarity of C_r is reversed. Since the current through the auxiliary switch self-commutates to zero, devices such as SCRs can be used for S_r. The two auxiliary resonant circuits can be simultaneously activated to start the resonant operation rather than being controlled individually.

K State 0: ZVS transition state [see Fig. 4(f)]

After the resonant operation, the capacitor voltage reaches a value larger than the highest line-to-line voltage $V_{\rm abi}$ again. To ensure this, a state 0 can be flexibly inserted between state 5 and state 6 to deliver more energy to the capacitor if needed such that the capacitor voltage can always resonate to a voltage level higher than $V_{\rm abi}$. Then the incoming devices $S_{\rm iap}$ and $S_{\rm ibn}$ can be turned-on under ZVS condition. Resonant capacitors are charged by i_m till its voltage drops to a value equal to $V_{\rm abi}$, which starts the operating of next switching cycle.

During the entire switching cycle, the resonant capacitors provide ZVS transition for turning off the outgoing devices and turning on the incoming devices. ZVS transitions occur in a

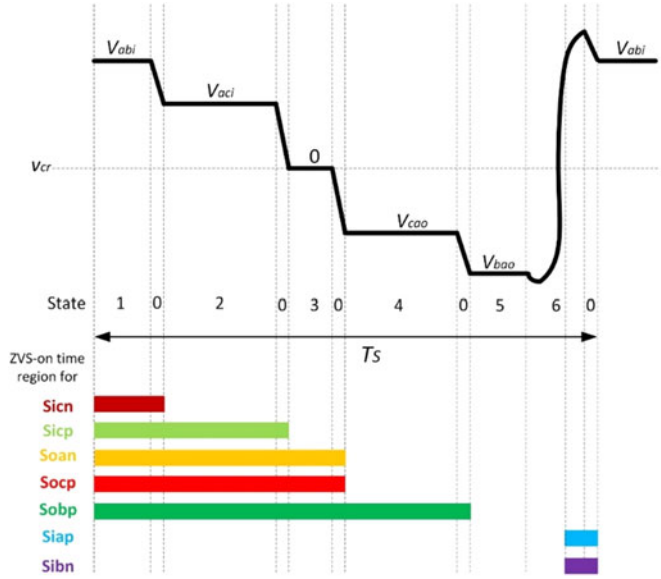

Fig. 6. Allowed ZVS turning-on time region for each device corresponding to the example switching cycle of Fig. 5.

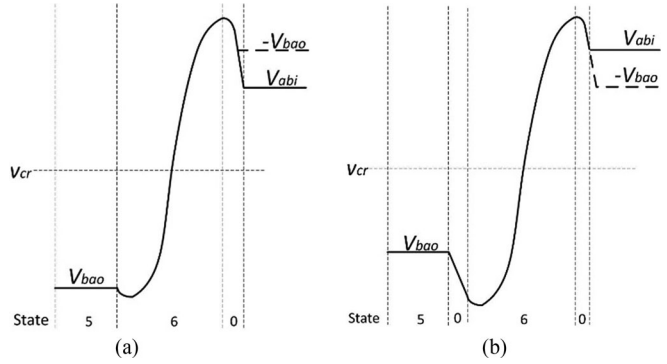

Fig. 7. Conceptualized $V_{\rm cr}$ waveforms with optional state "0" after state "5" under: (a) voltage-boost operation; and (b) voltage-buck operation.

passive manner in which the transformer magnetizing current automatically transfers between the active devices and the resonant capacitors. As a result, the converter does not require any intentionally added dead-time or overlap-time for device transitions. The auxiliary device is only operated once at the end of each switching cycle to reset the resonant capacitor voltage. Unlike other resonant converters which involve great complexity, the passive ZVS transitions simplify S4T control.

IV. Full Range of Soft Switching

Unlike the DAB converter which has a limited soft-switching range, the S4T realizes ZVS over the full load range. From the above-stated operating principles, it can be seen that device turn-off always occurs under ZVS conditions. To ensure ZVS turn-on, the resonant capacitor voltage should be higher than the incoming line–line voltage when the device is turned on, which means that the incoming device should be always reverse biased when its gate is turned on.

Over one switching cycle, before the end of state 5, ZVS turn-on can be always guaranteed as long as the device gate is turned on before the end of state 0. However, the ZVS turn-on region is not restricted within state 0. Instead, the incoming device allows to be turned on even before state 0 starts. For example, the gate of $S_{\rm icn}$ can be turned-on within state 1. In this case, since $V_{\rm abi}$ is larger than $V_{\rm aci}$, $S_{\rm icn}$ is reverse blocked, and it does not conduct. The ZVS transition from $S_{\rm ibn}$ to $S_{\rm icn}$ automatically occurs within state 0, and it does not need any intentional control. Fig. 6 shows the allowed ZVS turn-on region of each device that corresponds to the example switching cycle of Fig. 5. The devices can be turned on at any time within their specific regions, and the ZVS turn-on transitions are always guaranteed. This figure shows that the devices of the S4T realize ZVS switching over a wide four-quadrant range, including for voltage buck and boost modes of operation. This is a great advantage compared with other soft-switching converters, for which the devices have a very short time period over which they must be turned on. Additionally, for the proposed converter, even if the device misses the allowed time region and it is turned-on after the end of state 0 because of faulty operation, the only issue is that the device is turned on with losses, while the converter is still able to operate normally after the transition.

After state 5, the resonant capacitor voltage $V_{\rm cr}$ reaches the most negative value. To ensure ZVS operation of the subsequent switching cycle, after the resonant operation of state 6, $V_{\rm cr}$ should reach a value higher than that of the incoming highest positive voltage, $V_{\rm abi}$ in this example. This is achieved by flexibly adding state 0 between state 5 and state 6.

Under voltage-boost operation in which the amplitude of the output is higher than the input, state 6 can occur immediately after state 5, since $V_{\rm cr}$ can always reach a value higher than the highest input voltage after the resonant operation of state 6. The conceptualized waveform of $V_{\rm cr}$ for this case is shown in Fig. 7(a). The amplitude of the output voltage $V_{\rm bao}$ is higher than that of the input voltage $V_{\rm abi}$, indicating a voltage-boost operation. Under voltage-buck operation, however, the amplitude of $V_{\rm bao}$ is lower than $V_{\rm abi}$. Therefore, state 0 is needed after state 5. $V_{\rm cr}$ will be then charged to a greater negative value to ensure that it can be resonated to a value higher than $V_{\rm abi}$ after state 6. The conceptualized waveform of $V_{\rm cr}$ under voltage-buck operation is shown in Fig. 7(b).

V. S4T Analysis

A. Analysis of the Magnetizing Current

The control of the magnetizing current in the high-frequency transformer is crucial in S4T operation. A stable and robust magnetizing current regulation must be guaranteed to maintain the converter's normal operation. On a cycle to cycle basis, the input side charges the magnetizing inductance and the output side discharges it. Duty cycle of the converter bridges is controlled such that the magnetizing inductance delivers desired charge to each phase and thus sinusoidal voltages/currents can be maintained on the input and output sides. The magnetizing current regulation has the following attributes:

1) Loss in the converter and the high-frequency transformer should be compensated such that the magnetizing current is regulated at a specific dc level;
2) The magnetizing inductance should have a relative small value to achieve a compact transformer design. This will lead to large current ripples on the magnetizing current due to the charge and discharge operation;
3) Since the magnetizing inductance and its energy storage capability is relative low, single-phase ac to single-phase ac conversion with different power factors on the input and output sides may not be viable. Magnetizing current regulation from single-phase ac source is not feasible since the instantaneous power on that side is fluctuating;
4) If one side of the S4T is connected to dc or three-phase ac sources, loss compensation can be fulfilled on that side since it can always provide energy to regulate the magnetizing current; and
5) Small magnetizing inductance also allows rapid change of the magnetizing current according to the load levels within a few switching cycles, which achieves very fast dynamic response for the converter.

1) Optimal Transformer Magnetizing Current Level: The S4T enters the freewheeling state (state 3 of Fig. 4) after delivering the referenced charge from the input to the output terminals, in which the current flows through a closed phase leg, representing conduction loss. Thus, it is essential to shrink the freewheeling state duration. A higher magnetizing current leads to shorter time duration for the active states (states 1, 2, 4, and 5 of Fig. 4), while a longer time for the freewheeling state. Therefore, the magnetizing current should be dynamically regulated at a level such that reference charges are just able to be delivered from the input to the output terminals within one switching cycle T_s, without much time remaining for freewheeling. The following analysis excludes the effect of the ZVS transition period (state 0 of Fig. 4) and the resonant period (state 6 of Fig. 4), which are small compared to the entire switching cycle. Assuming that the high-frequency transformer has a 1:1 turns ratio and that the input and output voltages are in phase and both have unity power factor, the average magnetizing current should satisfy

$$I_{\mathrm{m.ave}} * t_i = I_{\mathrm{ip}} * T_S \tag{3}$$

$$I_{\mathrm{m.ave}} * t_o = I_{\mathrm{op}} * T_S \tag{4}$$

in which I_{ip}, I_{op} are peak values of the sinusoidal current on input and output sides, and t_i, t_o are the operation time durations of the input and output bridges, respectively. Neglecting the time spent on the ZVS transition and resonant operation

$$t_i + t_o = T_S \tag{5}$$

should be satisfied to minimize or eliminate the free-wheeling duration when the input and output instantaneous currents are at their peaks, which in turn leads to the minimal average magnetizing current in

$$I_{\mathrm{m.ave}} = I_{\mathrm{ip}} + I_{\mathrm{op}}. \tag{6}$$

The value shown in (6) is also the optimum average magnetizing current that the high-frequency transformer should be designed for.

2) Switching Ripple of the Magnetizing Current: The voltages applied across the transformer during states 1 and 2 are governed by

$$V_{i1} = V_{\mathrm{ip}} \left|\cos \omega t\right| \tag{7}$$

$$V_{i2} = V_{\mathrm{ip}} \left|\cos\left(\omega t + \frac{2\pi}{3}\right)\right| \tag{8}$$

in which V_{ip} is the peak line-to-line voltage of the input. These voltages rotate among three phases every $\pi/6$ radians based on three-phase voltage amplitudes. The average voltages in states 1 and 2 over $\pi/6$ cycle are calculated as

$$V_{i1.\mathrm{ave}} = \frac{6}{\pi}\int_0^{\pi/6} V_{\mathrm{ip}} \left|\cos \omega t\right| d\left(\omega t\right) = \frac{3}{\pi} V_{\mathrm{ip}} \tag{9}$$

$$\begin{aligned} V_{i2.\mathrm{ave}} &= \frac{6}{\pi}\int_0^{\pi/6} V_{\mathrm{ip}} \left|\cos\left(\omega t + \frac{2\pi}{3}\right)\right| d\left(\omega t\right) \\ &= \frac{3}{\pi}\left(\sqrt{3} - 1\right) V_{\mathrm{ip}}. \end{aligned} \tag{10}$$

For unity power factor, the following equation is valid, in which $t_{1.\mathrm{ave}}$ and $t_{2.\mathrm{ave}}$ are the operation times for states 1 and 2, and $I_{i1.\mathrm{ave}}$ and $I_{i2.\mathrm{ave}}$ are the average line currents that are delivered to the line in states 1 and 2:

$$\frac{V_{i1.\mathrm{ave}}}{V_{i2.\mathrm{ave}}} = \frac{I_{i1.\mathrm{ave}}}{I_{i2.\mathrm{ave}}} = \frac{t_{1.\mathrm{ave}}}{t_{2.\mathrm{ave}}}. \tag{11}$$

The average voltage applied across the transformer for the input bridge is then given by

$$\begin{aligned} V_{i.\mathrm{ave}} &= \frac{V_{i1.\mathrm{ave}} t_{i1.\mathrm{ave}} + V_{i2.\mathrm{ave}} t_{i2.\mathrm{ave}}}{t_{i1.\mathrm{ave}} + t_{i2.\mathrm{ave}}} \\ &= \frac{V_{i1.\mathrm{ave}} t_i \frac{V_{i1.\mathrm{ave}}}{V_{i1.\mathrm{ave}} + V_{i2.\mathrm{ave}}} + V_{i2.\mathrm{ave}} t_i \frac{V_{i2.\mathrm{ave}}}{V_{i1.\mathrm{ave}} + V_{i2.\mathrm{ave}}}}{t_i} \\ &= \frac{45 - 18\sqrt{3}}{3\sqrt{3}\pi} V_{\mathrm{ip}}. \end{aligned} \tag{12}$$

The average magnetizing current ripple over $\pi/6$ cycle, in which f_s is the converter switching frequency and V_{op} is the peak line-to-line voltage of the output, is shown as

$$\Delta I_{m.\mathrm{ave}} = \frac{V_{i.\mathrm{ave}} t_i}{L_m} = \frac{\left(45 - 18\sqrt{3}\right) V_{\mathrm{ip}} V_{\mathrm{op}}}{3\sqrt{3}\pi f_S L_m \left(V_{\mathrm{ip}} + V_{\mathrm{op}}\right)}. \tag{13}$$

It can be seen from (13) that a larger L_m leads to a smaller current ripple, thus smaller transformer core loss, but it will result in a large core volume and thus higher copper loss. Therefore, the transformer design should make a compromise between the current ripple, the core loss, and the core volume.

3) Boundary Conditions for Continuous Conduction Mode Operation: The discontinuous conduction mode operation should be avoided for the S4T, i.e., the magnetizing current should never drop to zero for any duration. The maximum magnetizing current ripple over $\pi/6$ radians occurs at $\omega t = \pi/6$, during which time both of the voltages across the transformer

in states 1 and 2 are equal to $2/\sqrt{3}V_{\rm ip}$ $2/\sqrt{3}V_{\rm ip}$; thus, the maximum magnetizing current ripple is as shown in

$$\Delta I_{m.\max} = \frac{2V_{\rm ip}V_{\rm op}}{\sqrt{3}f_S L_m\left(V_{\rm ip}+V_{\rm op}\right)}. \tag{14}$$

To ensure continuous conduction mode operation, the average magnetizing current should be larger than half of its ripple; thus, the following equation should be satisfied:

$$f_S L_m < \frac{V_{\rm ip}V_{\rm op}}{\sqrt{3}\left(V_{\rm ip}+V_{\rm op}\right)\left(I_{\rm ip}+I_{\rm op}\right)}. \tag{15}$$

B. Analysis of the Filter

The S4T has a capacitive filter, for which the capacitance has to be selected properly to maintain desired switching voltage ripples. For the input filter capacitor, when one leg conducts, the filter capacitor connected to that leg will be discharged by the current that equals the magnetizing current minus the grid current. When the leg is switched off, the filter capacitor will be charged by the grid current. As a result, the input filter capacitor voltage ripple can be derived as

$$\Delta V_{\rm cap.in} = \frac{\left(I_{m.\rm ave}-I_{\rm ip}\right)I_{\rm ip}}{C_{\rm cap.in}f_{\rm sw}I_{m.\rm ave}}. \tag{16}$$

The output filter capacitor voltage ripple can be derived similarly by replacing $I_{\rm ip}$ with $I_{\rm op}$. It should be noted that the capacitive filter also ensures very low *dv/dt* and low EMI.

Once the filter capacitance is designed based on (16), the filter inductor can be selected to achieve enough attenuation to meet the desired line current harmonics. For inductive loads such as motors, the filter inductor is not needed.

C. Analysis of the Transformer Leakage Effect

For a real transformer, the energy trapped in the leakage becomes an issue during device commutations, which, if not managed properly, could develop voltage spikes and thus damage devices. The Dyna-C SST [20]–[23] and the isolated matrix converter based SST [15] actively manage the leakage energy by introducing additional switching states. These switching states will lead to additional switching loss for the converter. In addition, the diode reverse recovery causes voltage spikes when the diode snaps off.

For the proposed S4T topology, however, the auxiliary resonant capacitor can inherently sink the transformer leakage energy in a passive manner. This avoids using an additional leakage management strategy and thus eliminates all the associated issues. During the transition from one bridge to another as shown in Fig. 4(f), the two resonant capacitors located on both the primary and secondary sides of the transformer will be simultaneously charged by the magnetizing current. However, it should be noted that during the transition, the leakage inductance will tend to resonate with these two capacitors. When transitioning from one side of the bridge to the other, the energy trapped within the leakage is actually automatically transferred through this resonance, without the need of additional switching state as the Dyna-C and the isolated matrix converter. In the following, the leakage energy transferring from one side to the other will be analyzed.

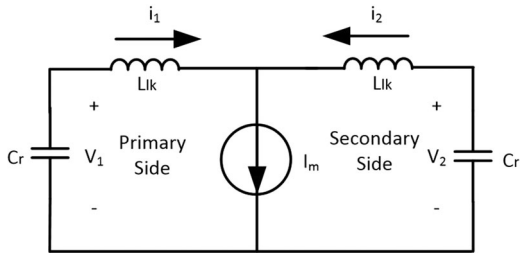

Fig. 8. Equivalent circuit at the ZVS transition.

Take the transitioning instant from state 1 to state 0 as shown in Fig. 4 for an example. Fig. 8 shows the equivalent circuit once the S4T enters state 0, in which the high-frequency transformer is replaced by a constant current I_m, and $L_{\rm lk}$ represents the transformer leakage inductance on the primary and secondary sides. The currents flowing through the primary and the secondary windings are i_1 and i_2. Before this transition, the two resonant capacitors have the same initial voltage of V_0, and all the magnetizing current flows through the primary side winding, i.e., i_1 equals I_m, and i_2 equals 0.

The converter state once entering state 0 is described as follows:

$$\begin{cases} i_1+i_2=I_m \\ L_{\rm lk}\dfrac{di_1}{dt}-L_{\rm lk}\dfrac{di_2}{dt}=v_1-v_2 \\ C_r\dfrac{dv_1}{dt}=-i_1 \\ C_r\frac{dv_2}{dt}=-i_1 \end{cases} \tag{17}$$

with the initial conditions of

$$\begin{cases} i_1(t=0)=I_m \\ i_2(t=0)=0 \\ v_1(t=0)=V_0 \\ v_2(t=0)=V_0 \end{cases}$$

The solution to this equation is given as

$$\begin{cases} i_1=\dfrac{I_m}{2}\left(1+\cos\left(\sqrt{\dfrac{1}{L_{\rm lk}C_r}}t\right)\right) \\ i_2=\dfrac{I_m}{2}\left(1-\cos\left(\sqrt{\dfrac{1}{L_{\rm lk}C_r}}t\right)\right) \\ v_1=-\dfrac{I_m}{2}\sqrt{\dfrac{L_{\rm lk}}{C_r}}\sin\left(\sqrt{\dfrac{1}{L_{\rm lk}C_r}}t\right)-\dfrac{I_m}{2C}t+V_0 \\ v_2=\dfrac{I_m}{2}\sqrt{\dfrac{L_{\rm lk}}{C_r}}\sin\left(\sqrt{\dfrac{1}{L_{\rm lk}C_r}}t\right)-\dfrac{I_m}{2C}t+V_0 \end{cases}. \tag{18}$$

The required time to have the transformer magnetizing current equally distributed to the primary and secondary windings is given as

$$t_{\rm lk}=\frac{\pi}{2}\sqrt{L_{\rm lk}C_r}. \tag{19}$$

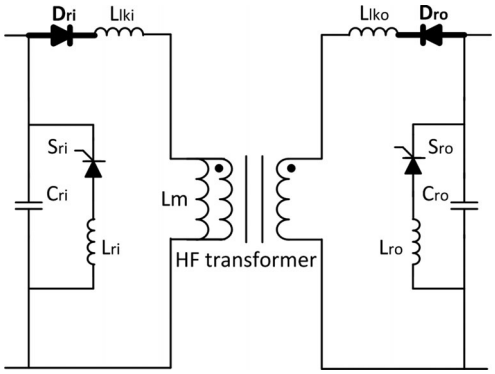

Fig. 9. Two diodes to manage the resonance if leakage inductance is large.

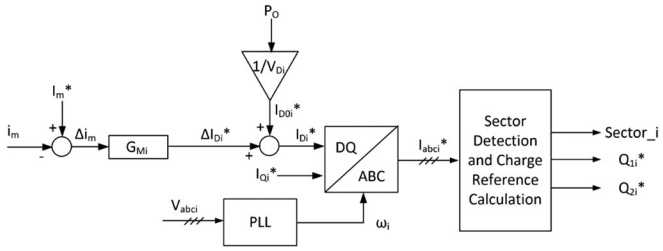

Fig. 10. Outer loop control architecture for the input bridge.

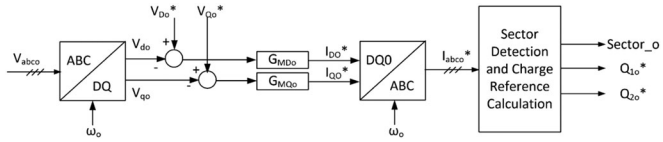

Fig. 11. Outer loop control architecture for the output bridge.

It shows that the time spending on the leakage energy transfer from one winding to another depends on the leakage inductance and the resonant capacitance.

The leakage energy transfer can also be explained in a more intuitive manner. Once the converter enters state 0, (18) shows that the voltages of the two resonant capacitors will be different, due to the resonance between the leakage inductance and the two resonant capacitors. This voltage difference tends to drive the outgoing bridge current down and simultaneously build up the incoming bridge current, achieving a leakage management for bridge-to-bridge transitions.

However, (18) shows that the resonance will continue even after the transformer magnetizing current is equally distributed to the primary and secondary windings at the time specified in (19). The winding resistance of the transformer can help damp the resonance and stabilize the two winding currents. However, if the leakage inductance is too large, a huge resonance that lasts for a very long time may result in operational failure of the converter. In this case, to overcome this issue, two additional diodes $D_{\rm ri}$ and $D_{\rm ro}$ can be connected in series with the transformer to prevent the resonance, which are shown in Fig. 9. The drawback of this solution is that it introduces additional conduction loss for the converter since they are always in the magnetizing current path. It is thus desired to select diodes that have a low voltage drop. It was calculated that these series diodes introduce 2% additional loss for the 10 kVA unit while only 0.3% additional loss for the 50 kVA unit. SiC diodes are preferred here which has negligible reverse recovery. Actually, these diodes are in series with the transformer leakage. During the bridge-to-bridge transition, the leakage inductance significantly reduces the *di/dt* rate, which also effectively mitigates the reverse recovery.

VI. S4T Control

A charge-control based modulator, which was initially proposed to control a rectifier [25], is selected for controlling the S4T, in which the duty cycle of each state is determined by the actual charge delivered to the specific terminal over each switching cycle. The entire controller of the S4T consists of two loops, which are outer loops for input and output bridges to determine the reference phase current and required charge for each switching cycle and an inner loop to regulate the converter running from one switching state to another. The outer loop control architecture of the input bridge is shown in Fig. 10. When synchronized with the input line voltage, the *D* component of the input current is used to regulate the dc magnetizing current. For maintaining a unity power factor, the *Q* current reference is typically set to 0. Load feed-forward is provided on the branch generating $I^*_{\rm D0i}$ to ramp up/down the input current in response to changes in the load, in which P_o is the three-phase output instantaneous active power. The feedback loop generates $\Delta I^*_{\rm Di}$ from magnetizing current error Δi_m and compensator $G_{\rm Mi}$ is used to compensate the converter loss such that i_m is regulated at its reference I^*_m, in which $G_{\rm Mi}$ can be a simple PI regulator. The *DQ* current references are used as inputs to the "sector detection and charge reference calculation" block. This block outputs a signal "*sector_i*," which contains the information of the operating sequence for the device poles corresponding to each phase, based on the three-phase voltage and current amplitudes of the input, and it calculates the required charges $Q^*_{\rm 1i}$ and $Q^*_{\rm 2i}$ that need to be delivered in states 1 and 2 of Fig. 4.

The outer loop control block diagram of the output bridge is shown in Fig. 11. The load voltage regulator forms the outer loop. The compensators, $G_{\rm MDo}$ and $G_{\rm MQo}$, can be PI regulators. If the converter output is connected to active power sources and it is operated in the current control mode, the voltage control loop is not required and current references $I^*_{\rm Do}$, $I^*_{\rm Qo}$ are directly specified. In this case, the outer control loops for the input and output bridges are fully symmetrical. The *DQ* output current references serve as inputs to the "sector detection and charge reference calculation," which outputs a signal "*sector_o*" and the required charges $Q^*_{\rm 1o}$ and $Q^*_{\rm 2o}$ to determine the operating sequence for the output bridge.

Using the sector information and charge references of the input and output generated from the "sector detection and charge reference calculation" block as well as the filter capacitor voltages of the input and the output, the inner control loop shown in Fig. 12 is constructed as a state machine, which runs the converter from one state to another, following the sequence

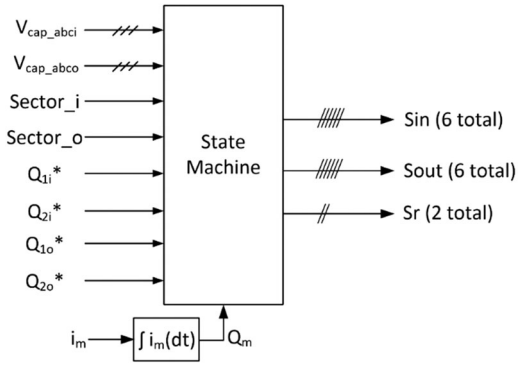

Fig. 12. Inner control loop.

TABLE I
PARAMETERS OF THE S4T

Power rating	Input/output voltage/current	Switching frequency	Magnetizing inductance
10 kVA	208 V / 28 A	15 kHz	200 μH
Filter capacitor	Filter inductor	Resonant capacitor	Resonant inductor
60 μF	150 μH	0.4 μF	8 μH

described in Fig. 4. To determine the duty cycle of each state, the actual charge, which is calculated as the integration of the transformer magnetizing current as shown in (1), is continuously compared with the reference charge. Once the actual charge is equal to the reference, the current state operation is concluded and next state operation starts.

VII. Simulation and Experimental Results

The operation of the proposed converter is validated through simulation, using parameters listed in Table I. Fig. 13 shows the simulated waveforms of the three-phase voltage and current on the input and output, high-frequency transformer magnetizing current, resonant capacitor voltage, and resonant inductor current. Fig. 14 shows the simulation results under unbalanced condition in which phase A voltage on the input side drops to 0.8 p.u. Due to the unbalance, the magnetizing current shows low frequency ripple. However, the load current can still maintain balance. Under heavily unbalanced condition, the four-leg configuration has to be used for neutral current flow, in which the fourth leg provides a virtual neutral point. The configuration, control, and results of the four-leg structure have been covered in paper [28]. Fig. 15 shows the simulation results under input voltage sag condition, in which the input voltage drops to 0.8 p.u. from 0.06 to 0.11 s. The load current is free of disturbance under sag conditions. Fig. 16 shows the simulation results for reactive power injection, in which the output current lags the voltage to provide reactive power for inductive loads.

Fig. 17 shows a fabricated prototype rated at 208 V/10 kVA. The converter is designed with high-current rated multilayer printed circuit board (PCB) boards. Silicon IGBTs are connected in series with silicon-carbide diodes to implement the CSI bridges. A customized DSP/field-programmable gate array (FPGA)-based controller board is used to control the converter. The high-frequency transformer is designed to have

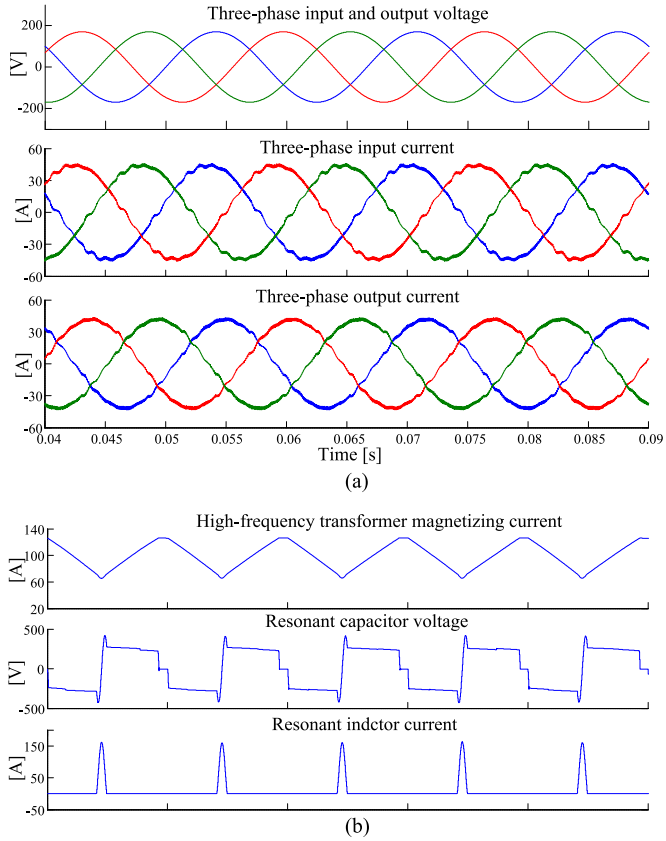

Fig. 13. Simulation waveforms of: (a) three-phase voltage and current of the input and output; and (b) high-frequency transformer magnetizing current, resonant capacitor voltage, and resonant inductor current.

a magnetizing inductance of 180 μH with a current carrying capability of 160 A. Nanocrystalline core and wide copper windings are used for the transformer design to provide low core loss and low winding loss. The selected nanocrystalline core is SC2068M1 from MK Magnetics, which has the area product of 1178.1 cm^4 and gives enough margin to avoid saturation. The transformer is designed to have interleaved primary and secondary windings, achieving a low leakage inductance of 740 nH. Kapton tape provides multi-kV isolation between layers. Detailed transformer design has been discussed in [27]. For this experiment, both input and output ports are connected to the same three-phase, 208 V supply so as to circulate 10 kVA power without having to dissipate it. Fig. 18 shows the experimental waveforms of transformer magnetizing current, line current, and resonant capacitor voltage. Fig. 19 shows the voltage across the active devices and the voltage of the resonant capacitor. It can be seen that the device stress is limited within envelope of the capacitor voltage. The resonant capacitor acts as a voltage clamp for all the devices, which eliminates high-voltage spikes caused by parasitic elements. The zoomed-in cycle-to-cycle waveforms for magnetizing current, resonant capacitor voltage, and resonant inductor current are shown in Fig. 20, which closely matches the conceptual waveforms and simulation waveforms.

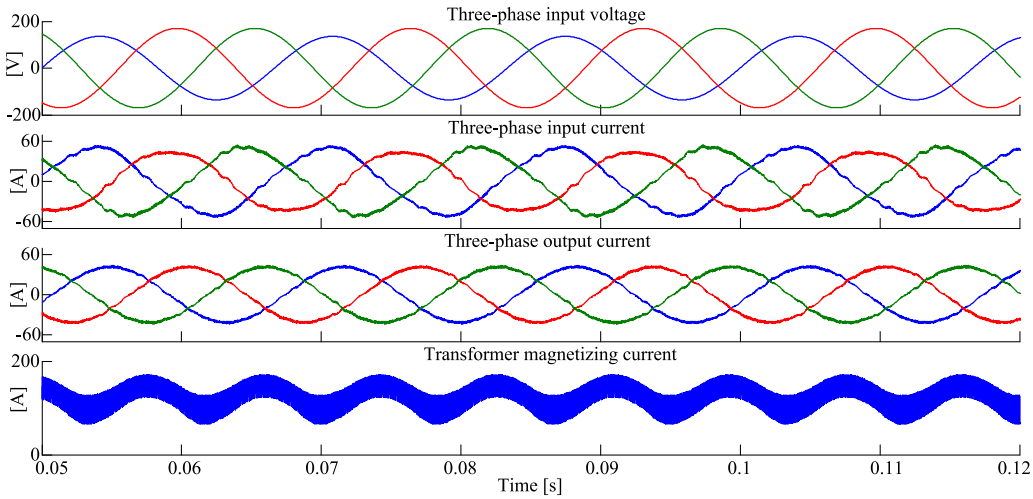

Fig. 14. Simulation results of the S4T under unbalanced condition in which phase A voltage on the input side drops to 0.8 p.u.

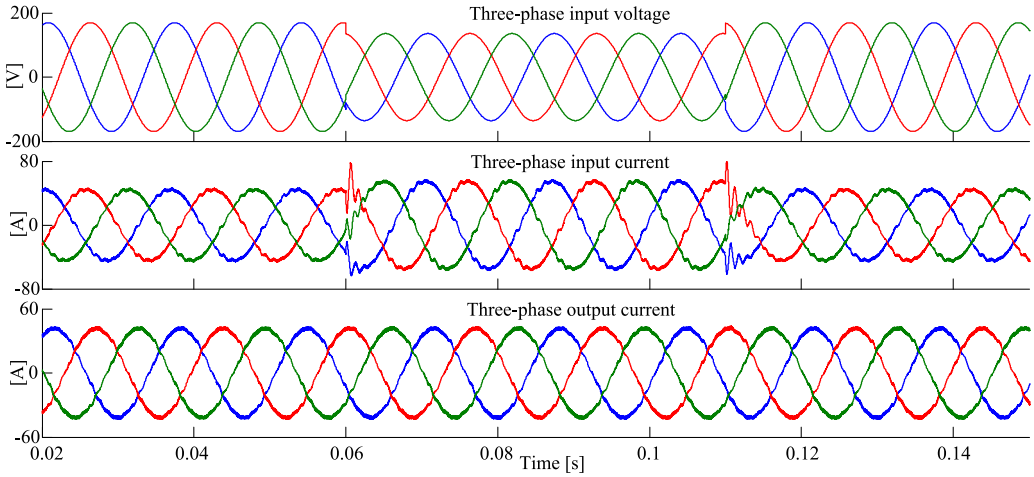

Fig. 15. Simulation results of the S4T under sag condition in which input voltage drops to 0.8 p.u. from 0.06 to 0.11 s.

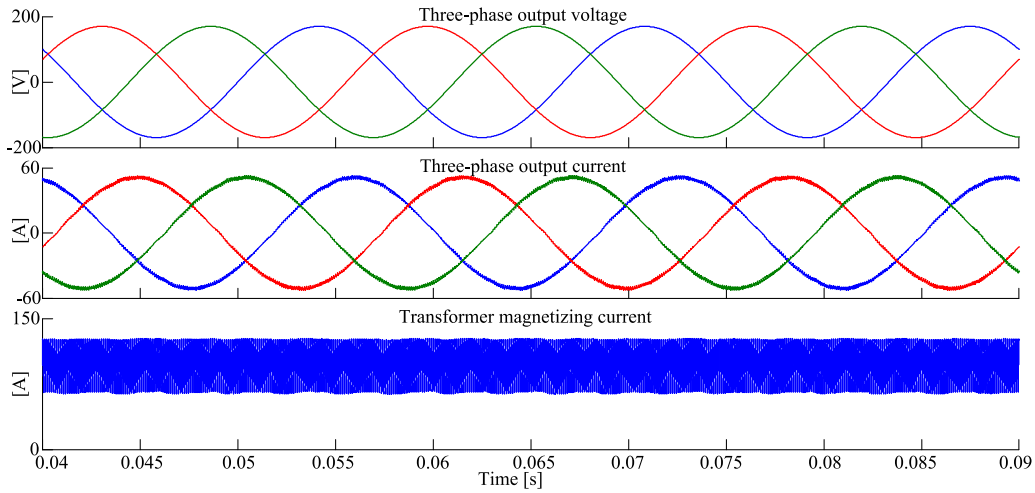

Fig. 16. Simulation results of the S4T for reactive power compensation.

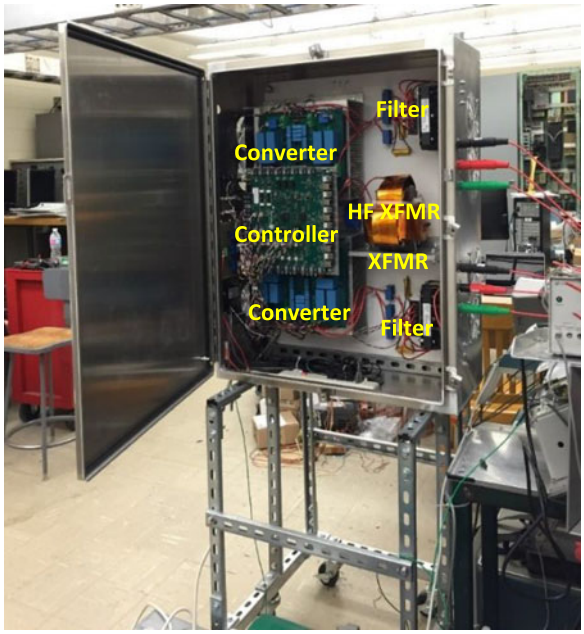

Fig. 17. Photograph of the 208 V/10 kVA S4T prototype.

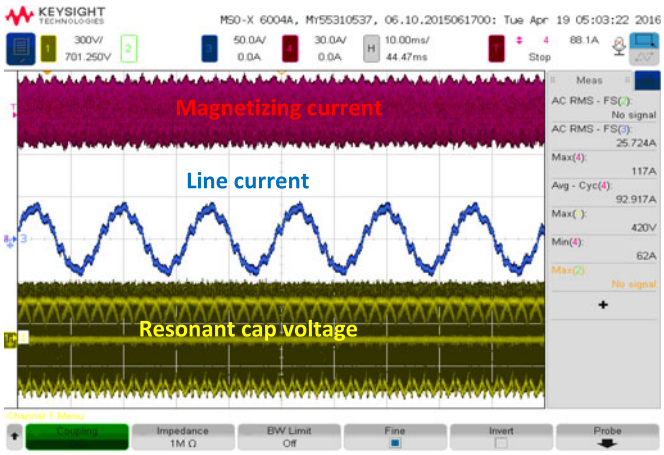

Fig. 18. Experimental results of transformer magnetizing current, line current, and resonant capacitor voltage.

Fig. 21 shows a ZVS transition of devices. It can be seen from the figure that before the device turning-on, the voltage across it already drops to zero, indicating ZVS turn-on. When it is turned off, the device voltage increases with a significantly reduced *dv/dt* rate, indicating ZVS turn-off. At the turning-off transition, the device voltage takes 1.5 μs to rise from 0 to 280 V, corresponding to a *dv/dt* value of $\sim$190 V/μs. This is much smaller than that of the device operated under hard-switching condition, which is 2500 V/μs according to the datasheet [29]. The device voltage shown in the figure does not have any voltage spike at turning-off, while hard-switching will cause a voltage spike due to the parasitic inductance.

Fig. 22 shows the loss measurement results at different dc currents and line voltages using a Yokogawa power analyzer.

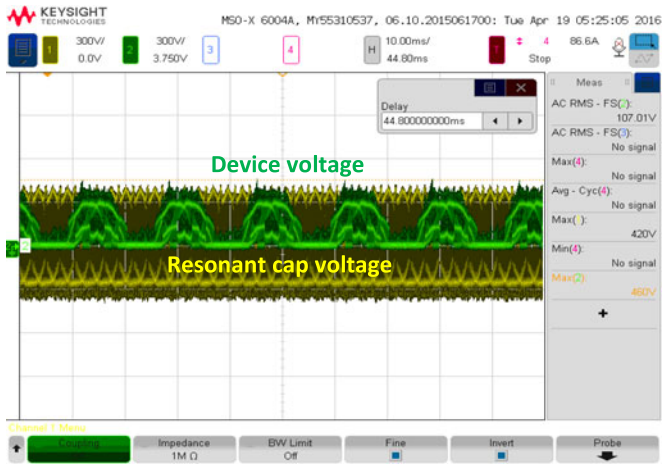

Fig. 19. Experimental results of resonant capacitor voltage and device voltage.

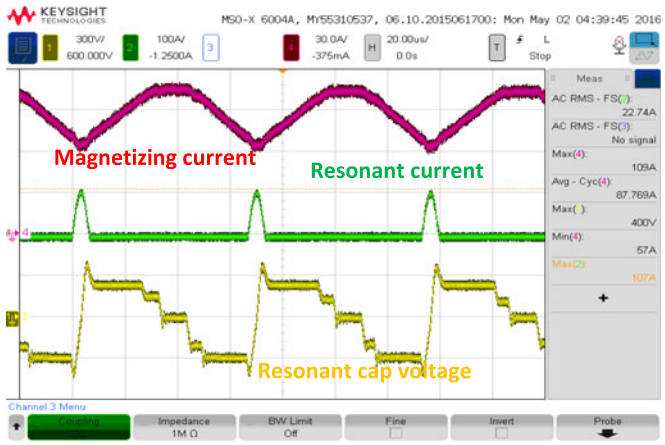

Fig. 20. Zoomed-in cycle-to-cycle waveforms for magnetizing current, resonant capacitor voltage, and resonant inductor current.

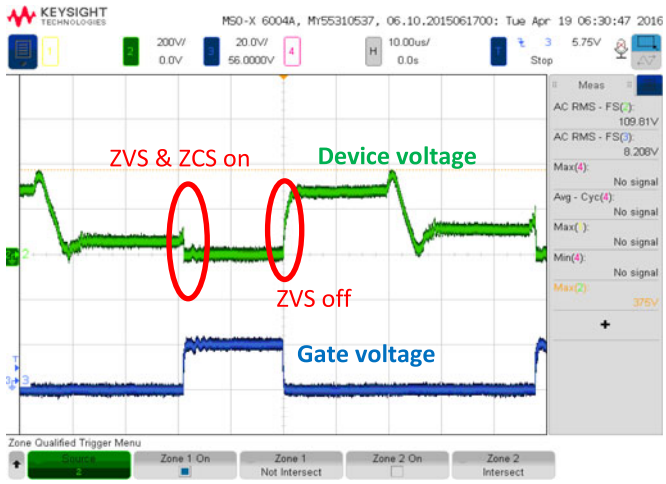

Fig. 21. Device switching waveforms of a ZVS transition.

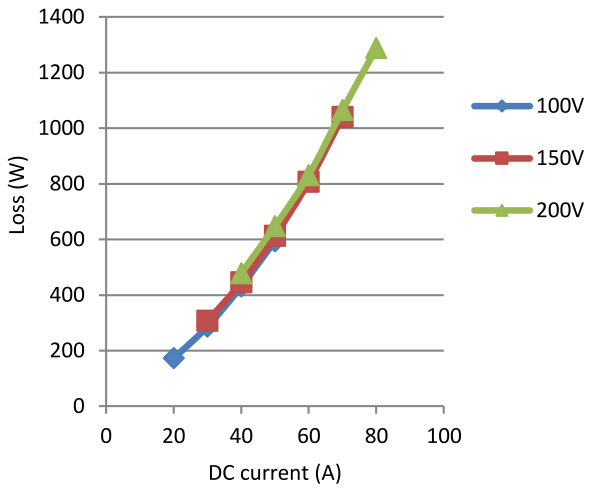

Fig. 22. Measured converter loss with different dc currents and line voltages.

The loss of the converter primarily consists of the transformer loss and the semiconductor loss. The transformer loss is estimated to be 74 W at full power and the remaining is mainly the conduction loss of the semiconductors. Lower dc current corresponds to lower load. From this curve, the S4T unit shows an efficiency of ~89% for 40% load at 200 V. It can be seen from Fig. 22 that the converter loss increases with current as expected, but is almost independent of voltage levels. This clearly shows that ZVS condition is met for all devices and proves the soft-switching feature of the S4T. It is predicted that the converter can achieve significantly higher efficiency at higher voltage and higher power levels, as will be shown later.

VIII. Unique Attributes and Key Comparison

A. Ease of Control

The S4T ZVS soft-switching range is independent of load current, a significant advantage when compared with DAB based three-stage SSTs. Furthermore, a wide range of turn-on and turn-off times provides ease of control at the individual device level. ZVS operation is not sensitive to resonant circuit parameters, and full pulse width modulation fixed-frequency capability is retained. The fundamental frequency control for the S4T is also simple, and uses the instantaneous actual magnetizing current to estimate the duty cycle of each switch. This results in very clean harmonic-free voltage waveforms at the input and output, even as the magnetizing current amplitude varies significantly.

B. Robustness

For the DAB based three-stage SST, bulky dc capacitors are needed to support the dc buses on both sides. This impacts the robustness and reliability of such SSTs. Inrush currents have to be managed at start-up, shutdown, and under grid fault conditions. Under short-circuit and fault conditions, desaturation protection and soft turn-off are required to avoid inductive voltage spikes. This can be particularly challenging for silicon-carbide devices, which may be needed to get to higher voltage levels. By way of contrast, the S4T has inherent current limiting, and eliminates inrush current under both start-up and fault conditions. Desaturation protection is not required for the devices making the gate driver design simpler.

The S4T is also highly differentiated from conventional CSIs. Interrupting current flow in a CSI, for instance due to a loss in control power, can quickly result in a voltage spike across the devices. The high *dv/dt* under open-circuit failure for CSIs requires a very fast acting overvoltage protection scheme. However, for the S4T, since the resonant capacitors significantly reduce the *dv/dt* rate, the devices can be easily protected by only connecting metal-oxide varistor (MOVs) in parallel with the resonant capacitors, and by independent turn-on of the resonant circuit devices if needed.

In addition, the S4T offers several very important features that conventional VSIs and CSIs do not offer:

1) the converter does not require any intentionally added dead time or overlap time for device transitions;
2) there is no severe inrush current when devices on the same leg are turned-on simultaneously by fault;
3) devices do not suffer from catastrophic voltage stress when interrupting the inductive current flowing path; and
4) reduced *dv/dt* rate significantly mitigates all the hard-switching issues such as resonance, spikes, noise, and EMI [24].

C. Fast Dynamic Response

The S4T is operated under charge control, which delivers the required charge to input and output terminals on a cycle-by-cycle basis. This indicates that the source and load current can be controlled with very fast dynamic response. It does not need an external current control loop to regulate the line current as in the conventional VSI, and a fast step response of several switching cycles is easily achieved.

To optimize S4T efficiency, the transformer magnetizing current level can be varied according to the load current. This will decrease the time period of the freewheeling state and will reduce conduction losses. However, for conventional CSIs, dynamically changing the dc current according to load levels can slow down response because of the large inductor. For the S4T, the transformer magnetizing inductance can be made relatively small, which reduces the system inertia. As a result, the transformer magnetizing current can be built up and driven down to a new reference value within several switching cycles.

In addition, the transformer can have a compact design and lower conduction losses due to the smaller magnetizing inductance that is acceptable.

D. Modular Design

The minimal topology lends itself to very efficient packaging. If RB-IGBTs are used, the packaging becomes even simpler. The absence of bulky dc capacitors and the ability to achieve higher switching frequencies reduce the transformer size, while ZVS allows smaller heat-sinks.

The S4T also allows scaling to higher voltage and power levels. Using available silicon devices above 1700 V entails

TABLE II
COMPARISON OF S4T, CONVENTIONAL DAB-BASED MULTISTAGE SST, AND LOW-FREQUENCY TRANSFORMER WITH A RECTIFIER AND AN INVERTER WHEN IMPLEMENTING A THREE-PHASE 480 V/50 KVA SOLID-STATE TRANSFORMER WITH A SWITCHING FREQUENCY OF 15 KHZ

Topology	Active Device Count	Soft-Switching	DC Caps	XFMR Frequency	Device V/I Rating	Total Device I_{RMS} Rating	Fault Current	Efficiency
Soft-switching solid state transformer (S4T)	12 (main) +2 (auxiliary)	Full range	–	15 kHz	1 p.u. / 2 p.u.	12 p.u.	2 p.u.	97.4%
DAB based multi-stage SST	20	DC/DC only with a limited range	2	15 kHz	1 p.u. / 1 p.u.	20 p.u.	> 10 p.u.	93%
Low-frequency transformer with rectifier and inverter	12	No	1	60 Hz	1 p.u. / 1 p.u.	12 p.u.	> 10 p.u.	91.5%

severe compromises in switching speed and losses. Even with emerging high-voltage silicon-carbide devices, the ability to realize grid-connected converters will require series connection of devices or modules. The S4T offers unique advantages in scaling for higher voltage/power. For instance, a traction drive could be realized with an S4T module that has single-phase on the high-voltage side, and a three-phase converter on the low-voltage side. The single-phase converters could be stacked in series, while the three-phase converters could be paralleled to drive the traction motor. This topology could realize fully bidirectional power flow, simple converter design, and high efficiency. Issues of dynamic balancing are important and will be covered in a future paper.

E. Key Comparisons

Table II summarizes the calculated comparison of various topologies when implementing a three-phase 480 V/50 kVA SST with a switching frequency of 15 kHz. The comparison includes the S4T, the conventional DAB based multistage SST, and the low-frequency transformer with a rectifier and an inverter using the same 1200 V IGBT from Infineon. Compared with the other two solutions, even though the device current rating for the S4T is 2 p.u., it does not have severe fault inrush current due to its inherent current limiting capability. It should be also noted that the duty cycle of the 2 p.u. current is less than 0.5. Semiconductors can typically withstand much higher current when the duty cycle is small as the device current withstanding capability is mainly limited by the junction temperature. Besides, since the S4T significantly removes switching losses, the thermal burden becomes even less and thus allows more current being pushed out of the device. Also, using RB-IGBT can give a much more compact design and lower conduction loss. It was reported in [30] that the overall voltage drop can be 25% less for the RB-IGBT compared to the discrete IGBT-diode solution. For the S4T transformer, using the hybrid transformer design methodology that was covered in [27], the required core size for the S4T is around 50% larger than the DAB-based SST, primarily because the S4T transformer needs to temporarily store energy. Although the S4T requires additional capacitors for the filter, the capacitive filter structure and soft-switching feature offer very low *dv/dt*, making the EMI filter much smaller than the DAB-based SST. The S4T really stands out with its features of lower device count, full-range of soft-switching, and high efficiency.

IX. CONCLUSION

This paper has presented a new patent pending topology for an S4T, which has a simple and symmetrical architecture, minimal device and component count in the power flow path, with small-rated auxiliary components that enable the soft switching property. Unlike the DAB converter, the S4T realizes ZVS for all its main devices over the entire load range, and features controlled *dv/dt* and *di/dt* rates. Furthermore, it can realize dc, single- or multiphase on the input/output at arbitrary frequencies and power factors with sinusoidal voltages and low EMI. It shows simple control and benign shut down under fault and failure modes, and is relatively insensitive to key parameters such as transformer leakage inductance. By eliminating components such as electrolytic capacitors, it can also realize higher power density and longer life.

The operation of the proposed converter, the design considerations, and key attributes were discussed in detail. Analysis and simulation verified the operating mechanisms, and experimental validation was obtained with a proof of concept prototype rated at 208 V/ 10 kVA with a switching frequency of 15 kHz. Finally, a detailed comparison was made between the new S4T design and conventional multistage SST as well as the low-frequency transformer implementations.

The S4T holds the promise of achieving high efficiency, particularly as it scales up in voltage and power. It provides the simplicity of single-stage SSTs, with the control attributes of the three-stage SSTs, with higher efficiency, lower *dv/dt* rate, and an ability to scale that seems unique. The topology can flexibly implement varied requirements, and can be scaled through series stacking and paralleling.

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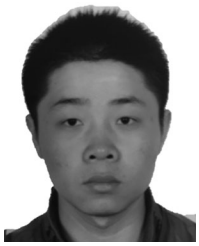

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