Primary Source Inductive Energy Analysis Based Real-Time Multiple Open-Circuit Fault Diagnosis in Two-Level Three-Phase PWM Boost Rectifier

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***Abstract*—Two-level three-phase boost rectifiers are widely used in industrial applications due to their superior performance. According to the survey reports, the transistors often suffer from open-circuit failures due to the lifting of bonding wires caused by thermic cycling, resulting in output fluctuation and current harmonics. This paper proposes a real-time, robust fault diagnosis method for single and multiple transistors open-circuit faults based on the primary inductances energy analysis. Three-phase primary voltages are divided into six states during a period; under healthy condition, the primary source inductances energy storage and release are normal in every state. When transistor open-circuit occurs, they will be abnormal in some states because the primary source electrical circuit will be nonconductive due to connected diode reserve truncation. Line-to-line currents are used to monitor the energy storage condition of primary inductances. Fast detection and isolation are achieved and little tuning effort is needed in the proposed method. Experiments are carried out and the results show high effectiveness, robustness, and merits of the fault diagnosis method.**

***Index Terms*—Fault diagnosis, open circuit, primary source inductive energy analysis, pulse-width modulating (PWM) boost rectifier.**

I. Introduction

THREE-PHASE ac–dc pulse-width modulating (PWM) rectifiers are widely used in motor drives and power quality applications for a sinusoidal input current with a unity power factor, stabilization, and regulation of dc-link voltage (current), low harmonic distortion of line current and bidirectional power flow from the primary source to load and back from load to source [1]. Generally, two basic rectifier topologies are widely accepted, boost rectifier with voltage output and buck rectifier with current output. The former has found the widest application for the main function of a rectifier is to maintain the output voltage on a predefined dc value. The controlled boost rectifiers consisted of transistors are widely applied in medium and large power drive system in recent years, however, the transistors are crashed frequently for their long-time online operation and suffering the voltage surge during transients such as predefined dc value or load changes. It is estimated that about 38% of the faults in power conversion system are due to failures in power devices such as insulated-gate bipolar transistors. Although recent survey shows they reduce to 31% as the most fragile components, followed by capacitors and gate drives [2]–[4], the demand for safety and reliability of power device still makes the development of fault detection and isolation/location methods a hotspot [5]–[9].

Generally, semiconductor power device faults in power converters are subdivided into short-circuit, open-circuit, and gate-misfiring faults. Short circuit will cause an overcurrent, which is very harmful and will shut down the system immediately. Nowadays, short-circuit detection and protection are integrated into the hardware [10]. Gate-misfiring faults are random and ephemeral, the fault features are similar to open-circuit fault. Open-circuit fault does not shut down the system immediately, however, they will lead to overstresses on the healthy switches and in turn cause secondary failures in other components, as well as lead to a torque ripple in the drives fed by inverter and output dc fluctuation in the rectifiers. The power conversion system will be destroyed by the subsequent faults and higher maintenance cost is required.

Various open-circuit fault diagnosis in three-phase dc–ac inverter fed motor drives have been developed during the last decade [11]–[15]. Literature [5] had summarized the existing methods before 2009 for fault diagnosis with special focus on three-phase inverter. Three methods were mainly used for fault detection and isolation in power converters: model-based techniques, data-based techniques, and artificial intelligence. Specially, model-based techniques and data-based techniques are more popular in recent years. However, few researches pay attention to rectifier open-circuit fault diagnosis. Compared with open-circuit fault diagnosis in inverter, fault diagnosis in rectifier has its unique characteristics.

1) The equipped diode will continually work as a rectifier component when one or more transistors open circuit occur, the system does not crash immediately, however, the performance will degrade such as output voltages fluctuation and current harmonics.

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2) The rectifier with faulty transistors works in controlled and not controlled modes alternatively, decided by the number and position of the faulty transistors, which makes it more complex for failure analysis.

Both current and voltage characteristics of faulty rectifiers are different from that of faulty inverter for the reasons mentioned above, most inverter open-circuit fault diagnosis methods cannot be directly grafted to rectifier, such as kinds of Parks vector methods based on current phase angle [10], [16]–[18], load current analysis [19], model-based [15], and various other current-based methods [7], [9], [13], [20]–[22], as well as kinds of voltage-based methods [12], [14]. It is strongly necessary to analyze the fault mechanism of rectifier and find new solutions for fault diagnosis. In [23], the instant converter voltage error is used for failure analysis in three-level neutral-point-clamped boost rectifier, it is able to reliably detect and identify faults when the line current in the affected phase is reduced to zero. In [24], mixed logical dynamic model and generated residual are used for open-circuit fault diagnosis in single-phase rectifier. In [25], an open-circuit fault diagnosis for a three-level T-type rectifier with unity power factor is proposed by using input currents and the angle calculated by grid voltages, the detection time is within a period of current.

On two-level boost rectifier, in [26], an open-switch fault diagnosis method by considering the switching patterns of space vector PWM and the directions of faulty phase current is proposed, combined with fault-tolerant control scheme, robustness of load changes, and variable speed is not mentioned. In [27], differences between open circuit in inverter and rectifier are analyzed, modifying Parks vector method and normalized dc current method are used for fault diagnosis. In [28], a combination of the absolute normalized dc current method and a false alarm suppression algorithm is proposed and reaches fast and robust open-circuit fault diagnosis. In [29] and [30], a novel and fair-robust diagnosis method for back-to-back converter is proposed (including inverters and rectifier). It should be noted that the study of two-level boost rectifier fault diagnosis is very little, what is more, most of the existing methods [26]–[28] only relate to single open-circuit fault diagnosis.

Primary source inductances are core components of boost rectifiers. They play important roles in primary energy storage and release to reach boosting. This paper proposed a diagnostic method for both transistor single and multiple open-circuit faults in two-level three-phase boost PWM rectifiers. In healthy condition, energy storage and release of primary inductances are normal. When open-circuit fault occurs, it will be abnormal because the primary source electrical circuit is nonconductive due to connected diode reserve truncation. Three-phase primary voltages are divided into six states by zero-crossing points, six line-to-line currents are one-to-one match to six voltage states. Two envelopings made up by mean values of crossing points of two neighboring line-to-line currents are used to monitoring the primary inductance energy condition. Insufficient energy storage in primary inductances will lead to line-to-line currents inside the envelopings in relative states. Fault can be detected if there is line-to-line currents inside the enveloping lines. Different faults will cause the primary inductance energy storage abnormal in different states, which leads to peaks or valleys of different line-to-line currents inside the envelopings, the faults can be located according to this phenomenon. The proposed fault diagnosis method is fair robust to transients of load changes, and predefined dc value changes. The structure of this paper is as following, Section II introduces the boost PWM rectifier with fault diagnosis unit. Section III is open-circuit failure analysis. Section VI introduces the proposed fault detection and isolation method, including tuning efforts. Section V is the experimental results. A conclusion is summarized in Section VI.

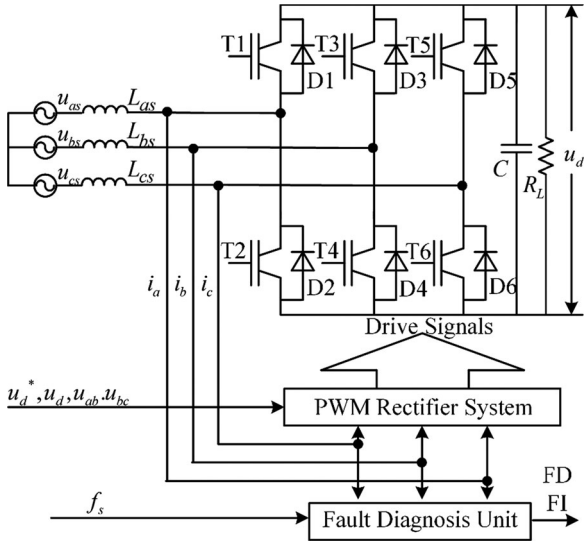

Fig. 1. Structure of three-phase PWM boost rectifier with diagnosis unit.

II. System Description

The structure of three-phase PWM boost rectifier combined with fault diagnosis unit is depicted in Fig. 1. It consists of three-phase primary voltage sources (u_{as}, u_{bs}, u_{cs}), their frequency is f_s, three-phase primary inductances (L_{as}, L_{bs}, L_{cs}), six transistors (T1, T2, T3, T4, T5, T6) equipped with six diodes (D1, D2, D3, D4, D5, D6), rectifier control system, fault diagnosis unit, capacitor filter (C) with resistance load (R_L). Three-phase currents (i_a, i_b, i_c), their direction flows from primary to load are defined positive, line-to-line voltage (u_{ab}, u_{bc}), predefined dc value ($u_d{}^*$), and measured dc value (u_d) of the rectifier are applied to control system for generating drive signals to control the transistors with on and off, alternately. Here, the control strategy of the system is vertual flux oriented-direct power control with no reative power [1], the rectifier three-phase currents, and the frequency of primary source are used for the fault diagnosis unit, two diagnostic signals FD and FI, which represents fault detection and fault location, respectively, are obtained according to the proposed diagnostic method. They can be effective references to monitor the healthy condition of the rectifiers. Because the fault diagnosis unit is independent to control system, it can be easy to insert into the control algorithm as a subroutine without major modification.

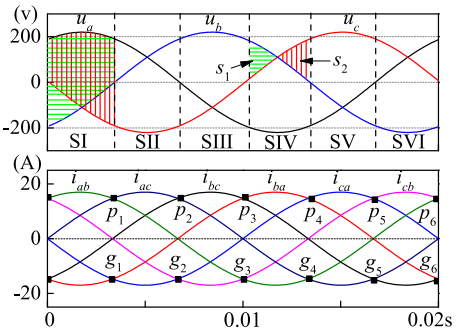

Fig. 2. Primary source voltages distribution and line-to-line currents.

TABLE I
VOLTAGE DISTRIBUTION AND SPACE VECTORS UNDER SVPWM

Voltage	State	Current Direction	Space Vector			
			$Stg1$	$Stg2$	$Stg3$	$Stg4$
u_{ab}, u_{ac}	SI	$i_a > 0, i_b < 0, i_c < 0$	000	100	110	111
u_{ac}, u_{bc}	SII	$i_a > 0, i_b > 0, i_c < 0$	000	010	110	111
u_{bc}, u_{ba}	SIII	$i_b > 0, i_a < 0, i_c < 0$	000	010	011	111
u_{ba}, u_{ca}	SIV	$i_b > 0, i_c > 0, i_a < 0$	000	001	011	111
u_{ca}, u_{cb}	SV	$i_c > 0, i_a < 0, i_b < 0$	000	001	101	111
u_{cb}, u_{ab}	SVI	$i_a > 0, i_c > 0, i_b < 0$	000	100	101	111

III. PRIMARY INDUCTIVE ENERGY ANALYSIS UNDER HEALTHY AND FAULTY CONDITIONS

Three-phase primary voltage sources are sinusoid with $\frac{2}{3}\pi$ phase difference, showed in the bottom plot of Fig. 2. They can be divided into six states according to the crossing points $p_v, g_v (v = 1, 2, 3, 4, 5, 6)$ of the neighboring line-to-line currents, showed in the top plot of Fig. 2, named SI–SVI. During every state, the rectifier operates under two effective line-to-line voltages, such as u_{ab}, u_{ac} in state SI, u_{ac}, u_{bc} in state SII. Six line-to-line currents are affected by their corresponding line-to-line voltages in different states.

During every state, the rectifier operates under four different space vectors when the control scheme is space vector pulse-width module (SVPWM), four space vectors changes their duty cycles during every switching instant. Note that every state is with zero-vector start and zero-vector end. Every state can be divided into four processes, every process is corresponding to a space vector, named $Stg1--Stg4$, showed as Table I, where "0" mean the lower transistor is conducting, "1" means the upper transistor is conduction. Analysis of the conductive primary electrical circuits under healthy condition and faulty condition is given as following, assuming that the currents direction is positive.

A. Healthy Condition

The primary inductances store energy from the grid during zero-vector processes, and then release during the middle space vector process. Taking SI for example, it contains four space vectors, $Stg1(000)$, $Stg2(100)$, $Stg3(110)$, $Stg4(111)$. The rectifier operating mechanism in healthy condition is given as the following.

$Stg1(000)$: During this process, the primary electrical circuit is short-circuit for all the lower transistors conduct. Currents in the rectifier start from phase-a, flow through T2, then back to phase-b and -c through T4 and T6, respectively, ($u_{as} \rightarrow L_{as} \rightarrow$ T2 $\rightarrow$ T4 $\rightarrow$ $\mathrm{L_{bs}} \rightarrow \mathrm{u_{bs}}$, $u_{as} \rightarrow L_{as} \rightarrow$ T2 $\rightarrow$ T6 $\rightarrow$ $\mathrm{L_{cs}} \rightarrow \mathrm{u_{cs}}$). The primary inductances store energy, meanwhile, the filter capacitor discharges to output resistance ($C \rightarrow R_L$), showed as Fig. 3(a).

$Stg2(100)$: During this process, T1, T4, T6 conduct. Currents in the rectifier start from phase-a, flow through T1, then through the filter capacitor and load resistance, back to phase-b and -c through T4 and T6, respectively, ($u_{as} \rightarrow L_{as} \rightarrow$ T1 $\rightarrow R_L/C \rightarrow$ T4 $\rightarrow L_{bs} \rightarrow u_{bs}$, $u_{as} \rightarrow L_{as} \rightarrow$ T1 $\rightarrow R_L/C \rightarrow$ T6 $\rightarrow L_{cs} \rightarrow u_{cs}$). The primary inductances release energy, meanwhile, the filter capacitor charges, showed as Fig. 3(b).

$Stg3(110)$: During this process, T1, T3, T6 conduct. Currents in the rectifier start from phase-a, flow through T1, then subdivide into two circuits, one is directly back to phase-b through T3 ($u_{as} \rightarrow L_{as} \rightarrow$ T1 $\rightarrow$ T3 $\rightarrow L_{bs} \rightarrow u_{bs}$), another flows through capacitor and resistance, then back to phase-c via T6 ($u_{as} \rightarrow L_{as} \rightarrow$ T1 $\rightarrow R_L/C \rightarrow$ T6 $\rightarrow L_{cs} \rightarrow u_{cs}$). The primary inductances (L_{as}, L_{bs}) store energy in the first subcircuit, and (L_{as}, L_{cs}) release energy in the second subcircuit, showed in Fig. 3(c). The filter capacitor discharges. Summarily, the primary inductances release energy to the load.

$Stg4(111)$: During this process, the primary electrical circuit is short-circuit for all the upper transistors conduct. Currents in the rectifier start from phase-a, flow through T1, then back to phase-b and -c through T3 and T5, respectively ($u_{as} \rightarrow L_{as} \rightarrow$ T1 $\rightarrow$ T3 $\rightarrow L_{bs} \rightarrow u_{bs}$, $u_{as} \rightarrow L_{as} \rightarrow$ T1 $\rightarrow$ T5 $\rightarrow L_{cs} \rightarrow u_{cs}$). The primary inductances store energy, meanwhile, the filter capacitor discharges to load resistance, ($C \rightarrow R_L$), showed as Fig. 3(d).

In SI, during zero-vector process, the primary inductances store energy via two line-to-line voltages (u_{ab}, u_{ac}), showed as the areas filled by horizontal and vertical lines in subplot 1, Fig. 2, respectively. During the middle two space vectors, the primary inductances release energy to the load resistance. The analysis mentioned above is also suit to the other five states.

B. Faulty Condition

The boost rectifier operates based on the primary inductances energy storage and release. When transistor single or multiple circuit open-circuit occurs, the inductances energy storage and release will be abnormal in one or more states. The analysis of primary electrical circuit during the inductance energy release is more complex in both healthy and faulty conditions, compared with that during inductance energy storage. Considering the primary inductances energy storage and release are opposite, energy storage of primariy inductances is the same in six states, with two zero-vector processes (all the upper or the lower transistors conduct). Hence, the failure mechansim analysis of

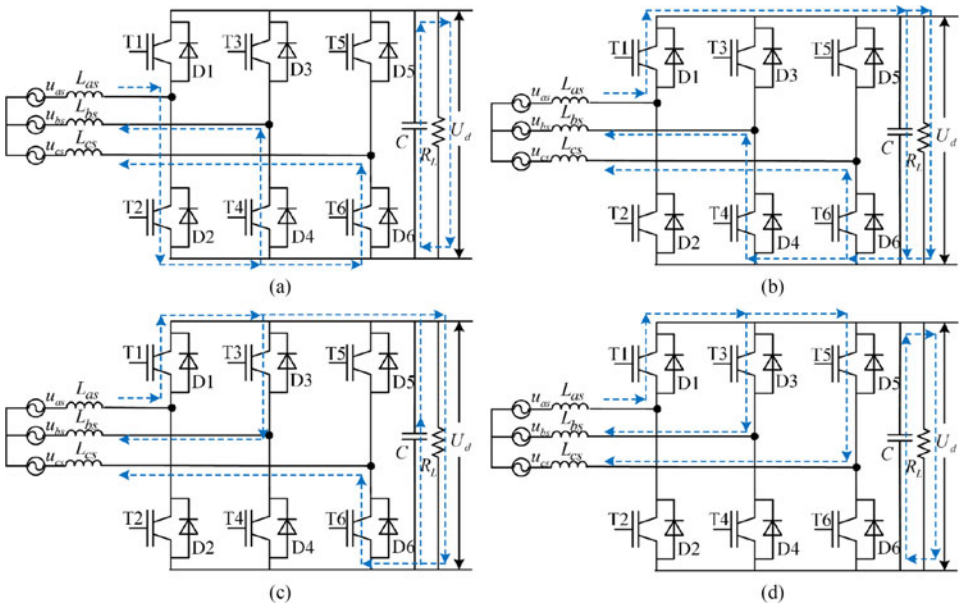

Fig. 3. Three-phase boost rectifier operation mechanism in healthy condition when the rectifier operate in state SI. (a) Currents flow mechanism with zero-vector 000; (b) Currents flow mechanism with vector 100; (c) Currents flow mechanism with vector 110; (d) Currents flow mechanism with zero-vector 111.

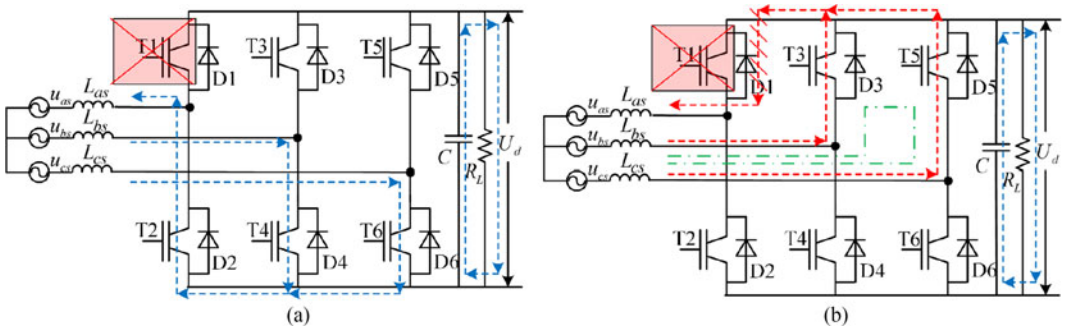

Fig. 4. Three-phase boost rectifier operation mechanism when T1 fails within state SIV. (a) Currents flow mechanism within vector-zero 000; (b) Currents flow mechanism within vector-zero 111.

transistor open-circuit fault in this paper is based on inductance energy storage.

According to the similarities of single and multiple open circuit in PWM boost rectifier. Twenty one types can be divided into four classes, including single fault (FAULT_1), two transistors fault in a same leg (FAULT_2), two transistors fault both on the upper or the lower of legs (FAULT_3), and two transistor fault one is on the upper, the other one is on the lower of different legs (FAULT_4), respectively.

1) Single Failure Analysis: Taking T1 open circuit for example, the inductances energy storage processes are with all the upper or lower transistors conduct. For all the lower transistors are healthy, the corresponding circuit is normal (000), showed in Fig. 4(a). So only the circuit with all the upper transistors (111) is discussed.

SI (u_{ab}, u_{ac}): Currents start from phase-a, flow through equipped diode D1, then back to phase-b and phase-c through T3 and T5. ($u_{as} \rightarrow L_{as} \rightarrow$ D1 $\rightarrow$ T3/T5 $\rightarrow L_{bs}/L_{cs} \rightarrow u_{bs}/u_{cs}$). Energy storage process is normal.

SII (u_{ac}, u_{bc}): Currents start from phase-a and -b, flow through equipped diode D1 and T3, then back to phase-c through T5. ($u_{as}/u_{bs} \rightarrow L_{as}/L_{bs} \rightarrow$ D1/T3 $\rightarrow$ T5 $\rightarrow L_{cs} \rightarrow u_{cs}$). Energy storage process is normal.

SIII (u_{bc}, u_{ba}): Currents start from phase-b, then divide into two subcircuits, one back to phase-c through T5, the other one does not conduct results from diode reverse truncation ($u_{bs} \rightarrow L_{bs} \rightarrow$ T3 $\mapsto$ D1 $\mapsto$ T1 $\rightarrow L_{as} \rightarrow u_{as}$). Even though, the process is still considered normal for one subcircuit successfully store energy.

SIV (u_{ba}, u_{ca}): Both two subcircuits do not conduct for diode reverse truncation, primary electrical circuits are $u_{bs}/u_{cs} \rightarrow L_{bs}/L_{cs} \rightarrow$ T3/T5 $\mapsto$ D1 $\mapsto L_{as} \rightarrow u_{as}$, showed as the red line in Fig. 4(b). In such a situation, a circuit is formed between phase-b and -c, showed as the green line in Fig. 4(b), during the first half process (u_{bc}), currents flow from phase-b through T3, then back to phase-c through T5 ($u_{bs} \rightarrow L_{bs} \rightarrow$ T3 $\rightarrow$ T5 $\rightarrow L_{cs} \rightarrow u_{cs}$). During the second half process (u_{cb}), oppositely, currents flow from phase-c through T5, then back to phase-b

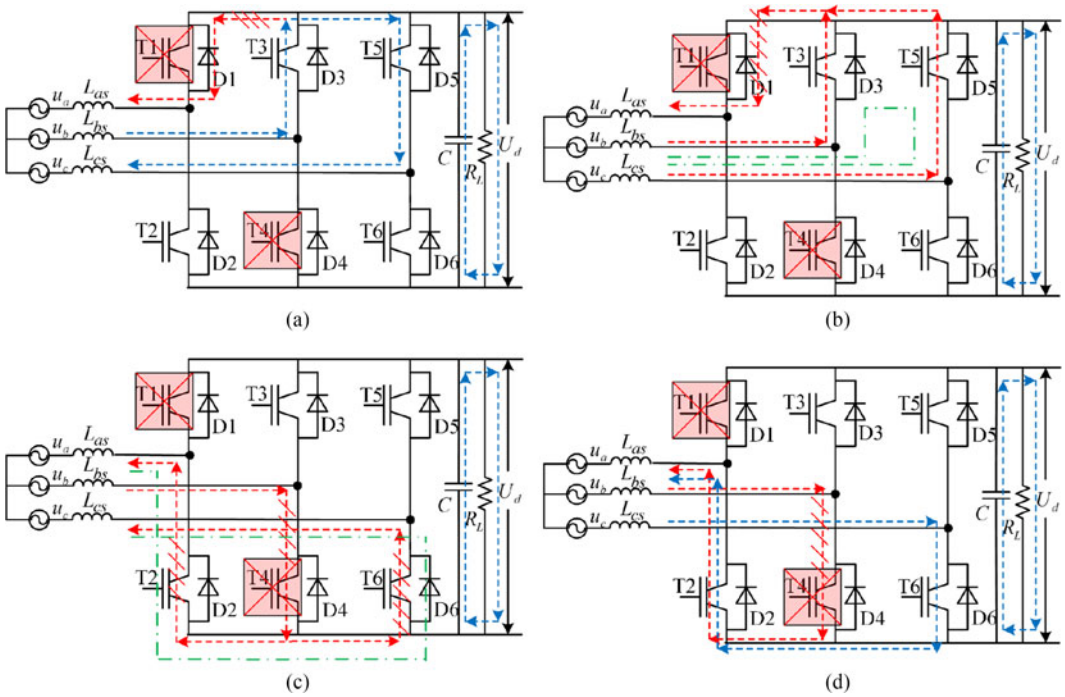

Fig. 5. Three-phase boost rectifier operation mechanism when T1T4 fail within state SIII and SIV. (a) SIII Currents flow mechanism within vector-zero 111; (b) SIV Currents flow mechanism within vector-zero 111; (c) SIII Currents flow mechanism within vector-zero 000; (d) SIV Currents flow mechanism within vector-zero 000.

through T3 ($u_{cs} \rightarrow L_{cs} \rightarrow$ T5 $\rightarrow$ T3 $\rightarrow L_{bs} \rightarrow u_{bs}$). The inductance energy storage can be represented by the areas S_1, S_2 filled by the horizontal and vertical lines, showed in subplot 2, Fig. 2. Because the two half process are opposite, $S_1 = -S_2$, as a result, no energy is stored.

SV (u_{ca}, u_{cb}): Currents start from phase-c, then divide into two subcircuits, one back to phase-b through T3, the other one does not conduct result from diode reverse truncation. The energy storage is normal as SIII.

SVI (u_{cb}, u_{ab}): Currents flow from phase-c and -a through T5 and equipped diode D1, then both of them back to phase-b through T3. Even though, the process is still considered normal for one subcircuit successfully store energy.

2) Multiple Failure Analysis: Taking T1T4 open-circuit as example, the multiple failure analysis is discussed by the primary inductance energy storage.

SI (u_{ab}, u_{ac}): (case 111, all the upper transistors conduct), currents start from phase-a, flow through D1, then back to phase-b and phase-c through T3 and T5, respectively, ($u_{as} \rightarrow L_{as} \rightarrow$ D1 $\rightarrow$ T3/T5 $\rightarrow L_{bs}/L_{cs} \rightarrow u_{bs}/u_{cs}$). (case 000, all the lower transistor conduct), currents start from phase-a, flow through T2, then back to phase-b and phase-c through D4 and T6, respectively. ($u_{as} \rightarrow L_{as} \rightarrow$ T2 $\rightarrow$ D4/T6 $\rightarrow L_{bs}/L_{cs} \rightarrow u_{bs}/u_{cs}$). In a summary, primary inductance energy is normal in this state because all the subcirsuit successfully store energy.

SII (u_{ac}, u_{bc}): (case 111, all the upper transistors conduct), currents start from phase-a and phase-b, flow throught D1 and T3, then back to phase-c through T5 ($u_{as}/u_{bs} \rightarrow L_{as}/L_{bs} \rightarrow$ D1/T3 $\rightarrow$ T5 $\rightarrow L_{cs} \rightarrow u_{cs}$). (case 000, all the lower transistors conduct), there are two subcircuits, one starts from phase-a, flows through T2, then back to phase-c through T6 ($u_{as} \rightarrow L_{as} \rightarrow$ T2 $\rightarrow$ T6 $\rightarrow L_{cs} \rightarrow u_{cs}$). The other one does not conduct results from diode reverse truncation ($u_{bs} \rightarrow L_{bs} \mapsto$ D4 $\mapsto$ T6 $\rightarrow L_{cs} \rightarrow u_{cs}$). In a summary, primary inductance energy is normal in this state because three-fourths the subcirsuit successfully store energy.

SIII (u_{bc}, u_{ba}): (case 111, all the upper transistors conduct), there are two subcircuits, one starts from phase-b, flows through T3, then back to phase-c through T5 ($u_{bs} \rightarrow L_{bs} \rightarrow$ T3 $\rightarrow$ T5 $\rightarrow L_{cs} \rightarrow u_{cs}$), showed as the blue dashed line in Fig. 5(a). The other one doest not conduct due to diode reverse truncation ($u_{bs} \rightarrow L_{bs} \rightarrow$ T3 $\mapsto$ $D_1 \mapsto L_{as} \rightarrow u_{as}$), showed as red dashed line in Fig. 5(a). (case 000, all the lower transistor conduct), both two subcircuits do not conduct due to diode reverse truncation ($u_{bs} \rightarrow L_{bs} \mapsto D_4 \mapsto T_2$/D6 $\rightarrow L_{as}/L_{cs} \rightarrow u_{as}/u_{bs}$), showed as the red dashed line in Fig. 5(c). In this situation, a new circuit is formed between phase-a and phase-c ($u_{as} \leftrightarrow L_{as} \leftrightarrow$ T2 $\leftrightarrow$ T6 $\leftrightarrow L_{cs} \leftrightarrow u_{cs}$), showed as the green dashed line in Fig. 5(c), in the first half process, $u_{as} > u_{cs}$, current flows from phase-a to phase-c, in the second half process, $u_{as} < u_{cs}$, current flows from phase-c to phase-a. These two half processes are opposite, energy storage fails in case 000. In a summary, inductance energy storage is abnormal because only one-fourths subcircuit successfully store energy.

SIV (u_{ba}, u_{ca}): (case 111, all the upper transistors conduct), both two subcircuits do not conduct due to diode reverse truncation ($u_{bs}/u_{cs} \rightarrow L_{bs}/L_{cs} \rightarrow$ T3/T5 $\mapsto$ D1 $\mapsto L_{as} \rightarrow u_{as}$), showed as the red dashed line in Fig. 5(b). A new circuit is formed between phase-b and phase-c, ($u_{bs} \leftrightarrow L_{bs} \leftrightarrow$ T3 $\leftrightarrow$

T5 $\leftrightarrow L_{cs} \leftrightarrow u_{cs}$), showed as the green dashed line in Fig. 5(b). In the first half process, $u_{as} > u_{cs}$, the energy storage can be represented as S_1 in Fig. 2, in the second half process, $u_{as} < u_{cs}$, the energy storage can be represented as S_2 in Fig. 2. These two half processes are opposite, hence, $S_1 = -S_2$, no energy is stored. (case 000, all the lower transistors conduct), there are two subcircuits, one starts from phase-c, flows through T6, then back to phase-a through T2 ($u_{cs} \rightarrow L_{cs} \rightarrow$ T6 $\rightarrow$ T2 $\rightarrow L_{as} \rightarrow u_{as}$), showed as the blue dashed line in Fig. 5(d). The other one does not conduct due to diode reverse truncation ($u_{bs} \rightarrow L_{bs} \mapsto$ D$_4 \mapsto$ T2 $\rightarrow L_{as} \rightarrow u_{as}$), showed as the red dashed line in Fig. 5(d). In a summary, inductance energy storage is abnormal because only one-fourths subcircuit successfully store energy.

SV (u_{ca}, u_{cb}): (case 111, all the upper transistors conduct), there are two subcircuits, one starts from phase-c, flows through T5, then back to phase-b through T3 ($u_{cs} \rightarrow L_{cs} \rightarrow$ T5 $\rightarrow$ T3 $\rightarrow L_{bs} \rightarrow u_{bs}$). The other one does not conduct due to diode reverse truncation ($u_{cs} \rightarrow L_{cs} \rightarrow$ T5 $\mapsto$ D1 $\mapsto L_{as} \rightarrow u_{as}$). (case 000, all the lower transistors conduct), currents start from phase-c, flow through T6, then back to phase-b and phase-c through D4 and T2 ($u_{cs} \rightarrow L_{cs} \rightarrow$ T6 $\rightarrow$ D4/T2 $\rightarrow L_{bs}/L_{as} \rightarrow u_{bs}/u_{as}$). In a summary, primary inductance energy is normal in this state because three-fourths subcircuits successfully store energy.

SVI (u_{cb}, u_{ab}): (case 111, all the upper transistors conduct), currents start from phase-a and phase-c, flow through D1 and T5, then back to phase-b through T3 ($u_{as}/u_{cs} \rightarrow L_{as}/L_{cs} \rightarrow$ D1/T5 $\rightarrow$ T3 $\rightarrow L_{bs} \rightarrow u_{bs}$). (case 000, all the lower transistors conduct), currents start from phase-a and phase-c, flow through T2 and T6, then back to phase-b through D4. ($u_{as}/u_{cs} \rightarrow L_{as}/L_{cs} \rightarrow$ T2/T6 $\rightarrow$ D4 $\rightarrow L_{bs} \rightarrow u_{bs}$). In a summary, primary inductance energy is normal in this state because all the subcirsuit successfully store energy.

The failure analysis mentioned above is also suit to the other faults in FAULT_1, FAULT_2, FAULT_3 (except SV), FAULT_4. When T1T3 fail, during state SV (u_{ca}, u_{cb}), two subcircuits do not conduct for the diode reverse truncation, the inductance energy storage should be abnormal as failure mechanism analyzed above. However, in this situation, the rectifier can be considered as one-phase PWM rectifier (phase-c). The current flows from phase-c, through C and R_L, then back to phase-a and -b through D2 and D4, so the inductance energy storage is still considered normal. Hence, a table of primary inductance energy storage condition can be obtained, showed as Table II. In Table II, T1, T1T2, T1T3, T1T4 represent FAULT_1, FAULT_2, FAULT_3, and FAULT_4, respectively. "N" represents the primary inductance energy is normal, oppositely, "AN" represents the primary inductance energy is abnormal.

TABLE II
PRIMARY INDUCTANCE ENERGY STORAGE CONDITION UNDER DIFFERENT FAULT CLASSES

Fault Class	SI (u_{ab}, u_{ac})	SII (u_{ac}, u_{bc})	SIII (u_{bc}, u_{ba})	SIV (u_{ba}, u_{ca})	SV (u_{ca}, u_{cb})	SVI (u_{cb}, u_{ab})
T1	N	N	N	AN	N	N
T1T2	AN	N	N	AN	N	N
T1T3	N	N	N	AN	N	AN
T1T4	N	N	AN	AN	N	N

IV. PROPOSED FAULT DIAGNOSIS METHOD

A. Fault Detection and Location

Six line-to-line currents are one-to-one mapped to six voltage state ($i_{ab}, i_{ac}, i_{bc}, i_{ba}, i_{ca}, i_{cb} \leftrightarrow$ SI, SII, SIII, SIV, SV, SVI, respectively), showed as Fig. 2. Different open-circuit faults lead to the inductance energy storage abnormal in different states, as analyzed in Section III. Insufficient inductance energy storage will lead to the corresponding peaks or valleys of line-to-line currents distorted, whose amplitudes will be smaller than that in healthy condition. In this paper, two online updated thresholds are proposed as criterion to monitor primary inductances energy storage condition by comparing with peaks and valleys of line-to-line currents. If the absolute value of peaks or valleys of line-to-line currents are larger than the defined thresholds, the inductance energy storage is normal, otherwise, the inductance energy is abnormal.

Considering that six states are divided by crossing points of neighboring line-to-line currents, and the current waveforms above the crossing points are mainly affected by the inductance energy storage and release. Hence, thresholds are defined as the mean values of line-to-line current crossing points $p_1, p_2, p_3, p_4, p_5, p_6$ and $g_1, g_2, g_3, g_4, g_5, g_6$, marked as K_1, K_2, giving as

$$\begin{cases} K_1 = \dfrac{p_1 + p_2 + p_3 + p_4 + p_5 + p_6}{6} \\ K_2 = \dfrac{g_1 + g_2 + g_3 + g_4 + g_5 + g_6}{6} \end{cases}. \tag{1}$$

Thresholds ($K_{\max}$, $K_{\min}$) to describe the inductance energy storage condition is giving as

$$\begin{aligned} K &= \max\big(|K_1|, |K_2|\big) \\ K_{\max} &= K, \quad K_{\min} = -K. \end{aligned} \tag{2}$$

Here, the peak and valley of line-to-line current $i_{mn}(m, n = a, b, c; m \neq n)$ are marked as $i_{mn}\_\max, \mathrm{i_{mn}}\_\min$. Insufficient inductance energy storage during zero-vectors (111, 000) when the current direction is positive will lead to the peak of corresponding line-to-line current not large enough, leading to $i_{mn}\_\max < \mathrm{K_{max}}$, oppositely, sufficient inductance energy storage will lead to $i_{mn}\_\max > \mathrm{K_{max}}$. Insufficient inductance energy storage during zero-vectors (111, 000) when the current direction is negative will lead to the valleys of corresponding line-to-line current not larger enough, leading to $i_{mn}\_\min > \mathrm{K_{min}}$, oppositely, sufficient inductance energy storage will lead to $i_{mn}\_\min < \mathrm{K_{min}}$. Here, the comparison results between $i_{mn}\_\max, \mathrm{i_{mn}}\_\min$ and $K_{\max}, K_{\min}$ are marked as P_{mn}, N_{mn}, in (3) and (4). The inductance normal energy storage will result in $P_{mn} = 1$, abnormal energy storage will result

TABLE III
PROPOSED OPEN-CIRCUIT FAULT DIAGNOSIS TABLE IN TWO-LEVEL THREE-PHASE BOOST RECTIFIER

Fault Class	P_{mn}						N_{mn}						Faulty Transistors	Faulty Type
	P_{ab}	P_{ac}	P_{bc}	P_{ba}	P_{ca}	P_{cb}	N_{ab}	N_{ac}	N_{bc}	N_{ba}	N_{ca}	N_{cb}		
Healthy	1	1	1	1	1	1	1	1	1	1	1	1	NO	0
FAULT_1	1	1	1	0	1	1	0	1	1	1	1	1	T1	1
	0	1	1	1	1	1	1	1	1	0	1	1	T2	2
	1	1	1	1	1	0	1	1	0	1	1	1	T3	3
	1	1	0	1	1	1	1	1	1	1	1	0	T4	4
	1	0	1	1	1	1	1	1	1	1	0	1	T5	5
	1	1	1	1	0	1	1	0	1	1	1	1	T6	6
FAULT_2	0	1	1	0	1	1	0	1	1	0	1	1	T1T2	7
	1	1	0	1	1	0	1	1	0	1	1	0	T3T4	8
	1	0	1	1	0	1	1	0	1	1	0	1	T2T5	9
FAULT_3	1	1	1	0	1	0	0	1	0	1	1	1	T1T3	10
	0	1	0	1	1	1	1	1	1	0	1	0	T2T4	11
	1	0	1	1	1	0	1	1	0	1	0	1	T3T5	12
	1	1	0	1	0	1	1	0	1	1	1	0	T4T6	13
	1	0	1	0	1	1	0	1	1	1	0	1	T1T5	14
	0	1	1	1	0	1	1	0	1	0	1	1	T2T6	15
FAULT_4	1	1	0	0	1	1	0	1	1	1	1	0	T1T4	16
	0	1	1	1	1	0	1	1	0	0	1	1	T2T3	17
	1	1	1	0	0	1	0	0	1	1	1	1	T1T6	18
	0	0	1	1	1	1	1	1	1	0	0	1	T2T5	19
	1	1	1	1	0	0	1	0	0	1	1	1	T3T6	20
	1	0	0	1	1	1	1	1	1	1	0	0	T4T5	21

in $P_{mn} = 0$

$$P_{mn} = \begin{cases} 1, & i_{mn}\_\max \geq K_{\max} \\ 0, & \text{else} \end{cases} \tag{3}$$

$$N_{mn} = \begin{cases} 1, & i_{mn}\_\min \leq \mathrm{K}_{\min} \\ 0, & \text{else} \end{cases} \tag{4}$$

Because $i_{mn} = -i_{nm}$, hence, the peak of i_{mn} is the same with the valley of i_{nm}, there is

$$P_{mn} = N_{nm}. \tag{5}$$

In healthy condition, primary inductances energy storage are all normal in six states, there is $\forall m, n,\ P_{mn} = 1, N_{mn} = 1$. When transistor open-circuit fault occur, primary inductances energy storage are abnormal in one or more states, there is $\exists m, n,\ P_{mn} = 0, N_{mn} = 0$. Therefore, fault can be detected according to the following equation $\forall m, n$:

$$\mathrm{FD} = \begin{cases} 0, & \begin{cases} P_{mn} = 1 \\ N_{mn} = 1 \end{cases} \\ 1, & \text{else} \end{cases}. \tag{6}$$

Different open-circuit faults will lead to inductance energy storage abnormal in different states, as mentioned in Section III, as a result, peaks or vallery of the corresponding line-to-line currents will be not large enough and inside the enveloping lines constituted by $K_{\max}$ and $K_{\min}$. Combining (3), (4), and Table II in Section III, a fault diagnosis table is designed, showed as Table III. All P_{mn} and N_{mn} are listed in the table to correspond the failure analysis in Section III. Taking T1 failure as an example, abnormal energy storage is in SIV during zero-vector (111), $P_{ba} = 0$, abnormal energy storage is in SI during zero-vector (000), $N_{ab} = 0$. Energy storage is normal in other states both during two zero-vectors. As a result, the fault can be located to T1 if only P_{ba} and N_{ab} are equal to zero.

B. Calculation of Peaks, Valleys, and Crossing Point of Line-to-Line Currents

Sliding windows combined with six line-to-line current samples are used to calculate their peaks and valleys, the windows contain current samples during a fundamental period and their lengths are

$$L = \frac{1}{f_s * T_{\mathrm{sp}}} \tag{7}$$

where L is the number of current samples in the sliding windows, T_{sp} is the switching period.

Sliding windows in k instant can be expressed as following:

$$I_{mn}(k) = [i_{mn}(k - L + 1), \ldots, i_{mn}(k - 1), i_{mn}(k)]. \tag{8}$$

Peak of line-to-line current is defined as the maximal current sample in sliding window I_{mn}, valley of line-to-line current is defined as the minimal current sample in sliding window I_{mn}. The sliding window updates in every instant, from $k-1$ to k instant, window ranges from $[i_{mn}(k - L), i_{mn}(k - L + 1), \ldots, i_{mn}(k - 1)]$ to $[i_{mn}(k - L + 1), i_{mn}(k - L + 2), \ldots, i_{mn}(k)]$, by adding the newest sample to window and deleting the ending sample. The flowchart of line-to-line current peak calculation is showed in Fig. 6. Assuming that v_{mn} is the position of maximal current sample in I_{mn} at $k-1$ instant, the maximal current sample will be replaced if it is smaller than the newest samples $i_{mn}(k)$, meanwhile, its position v_{mn} will be updated to L. Otherwise, v_{mn}

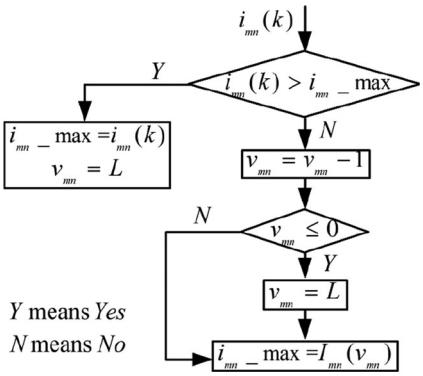

Fig. 6. Flowchart of line-to-line current peak calculation.

will shift left in the updated window. If the maximal current sample is the ending sample in I_{mn} at $k-1$ instant ($v_{mn}=1$), the newest samples are considered as maximal current samples at k instant ($v_{mn}=L$).

p_i and g_i ($i=1,2,3,4,5,6$) are two nearby line-to-line crossing points, showed in Fig. 2. Their mean values form criteria to monitor primary inductance energy storage condition in different states. In this part, the online calculation of p_i and g_i is discussed. First, a mean filter is designed to eliminate the influence of measurement noise and current harmonics, giving as following, where N_1 is a constant for filtering

$$\bar{i}_{mn}(k) = \frac{i_{mn}(k-N_1+1), i_{mn}(k-N_1+2), \ldots, i_{mn}(k)}{N_1}. \tag{9}$$

Second, calculate the position of p_i and g_i by the filtered currents, marked as tp_i, tg_i. Assuming that I_{mn} and I_{kl} are nearby assembly, such as ab and ac, ac and bc. Note that there are characteristics, for the current samples before crossing point (tp_i), $i_{mn}(z) > i_{kl}(z)(z < tp_i)$, for the current samples after crossing point (tp_i), $i_{mn}(z) < i_k l(z)(z > tp_i)$, the analysis result is opposite for crossing point (tg_i). Hence, at k instant, $\forall t \in [k-N_2+1, k-N_2+2, \ldots, k]$, if there is

$$\text{if} \begin{cases} \bar{i}_{mn}(k-N_2) > \bar{i}_{kl}(k-N_2) \\ \bar{i}_{mn}(t) < \bar{i}_{kl}(t) \end{cases} \tag{10}$$

then, the position of the upper crossing point (tp_i) is $k-N_2$, $tp_i = k-N_2$. If there is

$$\text{if} \begin{cases} \bar{i}_{mn}(k-N_2) < \bar{i}_{kl}(k-N_2) \\ \bar{i}_{mn}(t) > \bar{i}_{kl}(t) \end{cases} \tag{11}$$

then, the position of the lower crossing point (tg_i) is $k-N_2$, $tg_i = k-N_2$. Note that $i_m n(k-N_2)$ is inspected at k instant, the delay-time is $N_2 T_{sp}$. N_2 is a constant to eliminate the fluctuation around crossing points.

If $i_m n(k-N_2)$ and all the behind current samples meet (10) or (11), the crossing points update, their values are

$$\begin{aligned} p_i &= \frac{i_{mn}(t) + i_{kl}(t)}{2} \\ g_i &= \frac{i_{mn}(t) + i_{kl}(t)}{2}. \end{aligned} \tag{12}$$

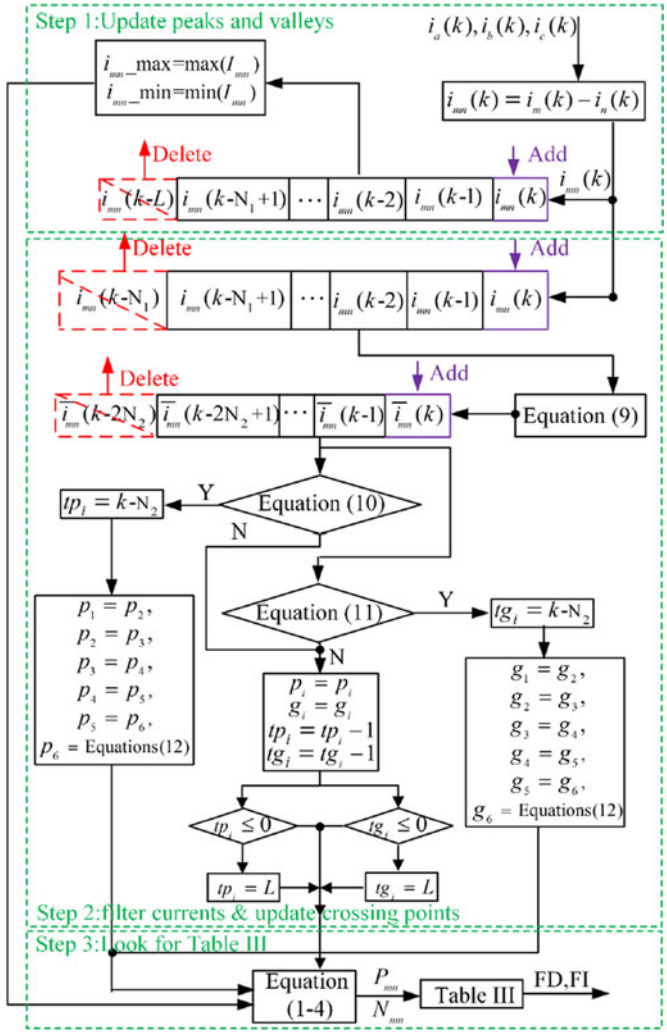

Fig. 7. Flowchart of proposed fault diagnosis algorithm.

Otherwise, the positions of p_i and g_i shift left in the updated windows, their values keep unchanged, showed in the second step in Fig. 7.

C. Tuning efforts

A high-performance and acceptable fault diagnosis method needs to be as few tuning parameters as possible. There are only three parameters in this paper, N_1, N_2, and K ($K_{\max}, K_{\min}$), N_1, N_2 are constants, they are used for accurate calculation of p_i and g_i by eliminating the noise and harmonics in line-to-line currents. K is online calculated by $p_1, p_2, p_3, p_4, p_5, p_6$ and $g_1, g_2, g_3, g_4, g_5, g_6$. In fact, no parameter need tuning by experience in the proposed fault diagnosis method.

D. Algorithm Flowchart

The flowchart of real time proposed fault diagnosis algorithm is showed in Fig. 7, where "Y" represents "yes," "N" represents "no," including three steps: updating the peaks and valleys of line-to-line currents, filtering the currrents, and updating the position of crossing points of the line-to-lint currents, detecting

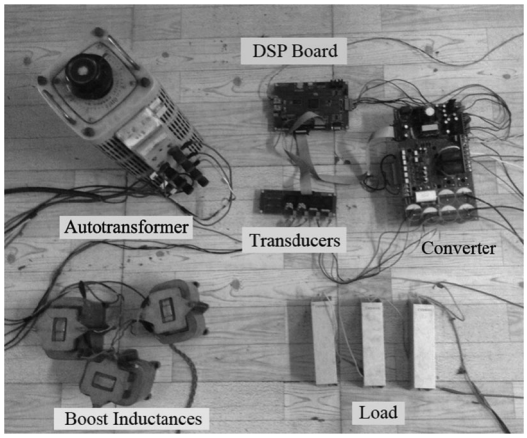

Fig. 8. Experimental setup.

and locating fault by looking for Table III with the calculated diagnostic variables P_{mn}, N_{mn}. Sliding windows are used to add the new samples and delete the latest samples in the algorithm, showed in the blue and red color characters in Fig. 7.

V. Experimental Results

The following analyses are based entirely on the experimental results since they give a better presentation of the algorithm performance in the presence of nonideal properties, such as model uncertainty, measurement noise, inverter dead-time effects, etc., compared with simulation results. SVPWM was applied to the control algorithm in the experiment. Some indices were presented to evaluate the performance of the proposed fault diagnosis method, such as robustness, detection time, effectiveness, etc. Four typical faulty operating conditions were investigated. All kinds of transistor open-circuit faults were performed by inhibiting their respective gate signals while keeping the bypass diode still connected. The experiment results are presented by the signals FD and FI, which represents the results of fault detection and fault location.

The experimental validation of the proposed fault diagnosis method was implemented in a TMS320F28335 board. The experimental setup is showed in Fig. 8, consists of a control board, a power converter with a switching frequency of 10 kHz and the dead time of 3.2 μs, line-to-line primary voltage source of 145 V, primary inductance of 8.6 mH, and resistance load. The thresholds N_1, N_2 for fault diagnosis was set to 4, 3. $K_{\max}, K_{\min}$ were online updated.

A. Disturbance Ability Evaluation

Disturbances of load changes and predefined dc value changes are examined to prove the fair robustness of the proposed diagnostic method, showed in Fig. 9. $u_d{}^*$ ranges from 230 to 280 V and R_L ranges from 120 to 80 Ω, indicated as the olive lines, peaks, and valleys of i_{ab}, i_{ac}, i_{bc} are still outside the enveloping lines consisted of $K_{\max}$ and $K_{\min}$ during the transients, which represents all peaks and valleys of six line-to-line currents are all outside the envelopings according to (5), indicating primary inductance energy storage is normal in all six states. No false alarm occurs.

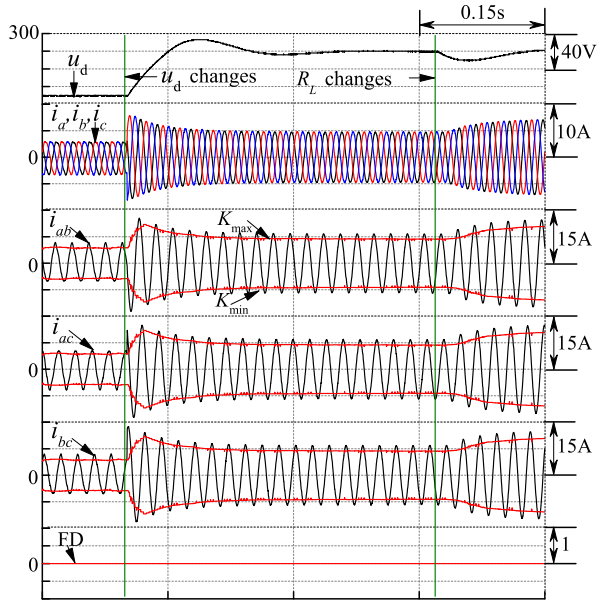

Fig. 9. Experimental results of antidisturbance ability with predefined output voltage ranges $u_d{}^*$ from 230 to 280 V and load R_L ranges from 120 to 80 Ω.

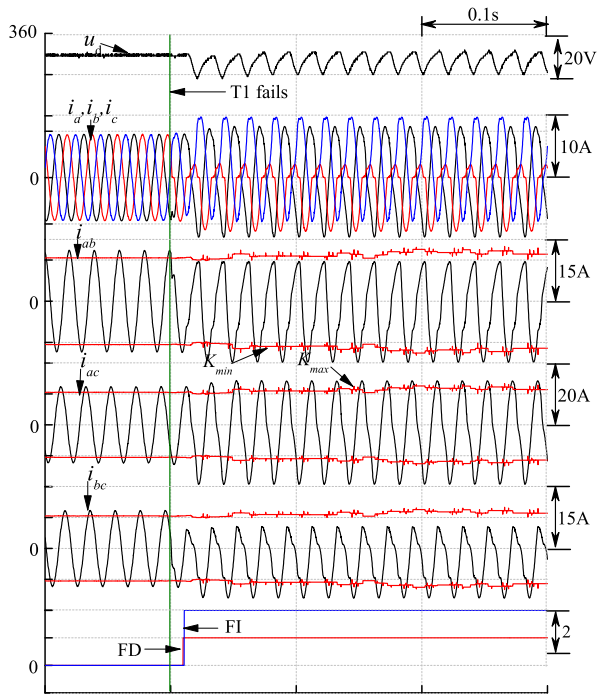

Fig. 10. Experimental results of fault diagnosis process when T2 (represents FAULT_1) fails at 0.1 s with reference voltage $u_d{}^* = 350$ V, from up to down, output voltage, three-phase currents, line-to-line currents, and diagnostic signals.

B. Single Open-Circuit Fault

Fig. 10 shows the diagnosis process when T2 open-circuit occurs, waveforms of output voltage, phase currents i_a, i_b, i_c, line-to-line currents i_{ab}, i_{ac}, i_{bc}, and diagnostic signals. When

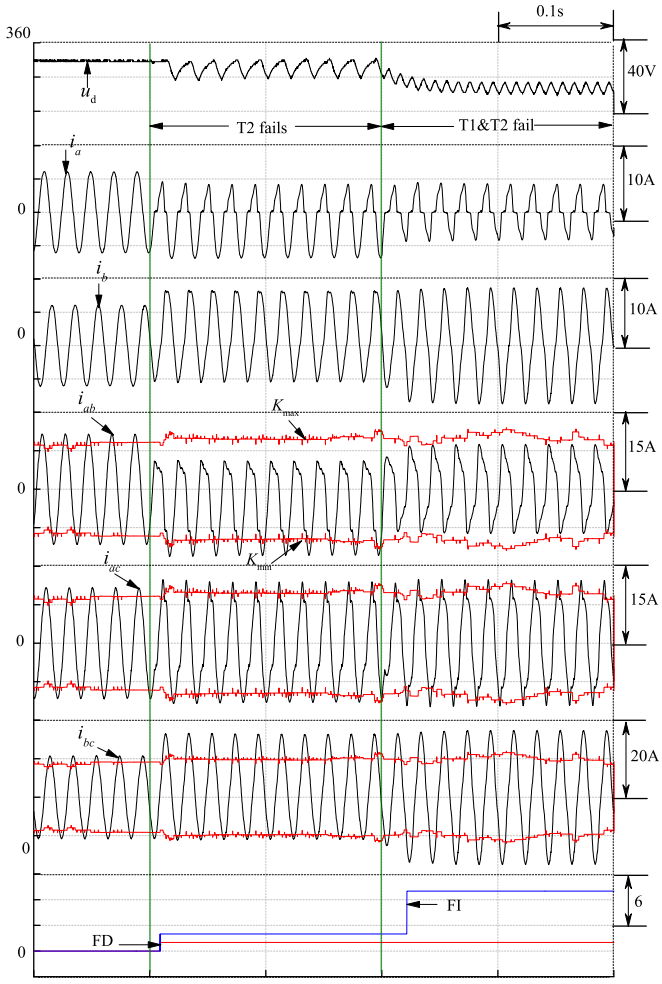

Fig. 11. Fault diagnosis process when T2 fails at 0.1 s and T1 fails at 0.3 s (represent FAULT_2) with reference voltage $u_d{}^* = 350$ V, from up to down, output voltage, three-phase currents, line-to-line currents, and diagnostic signals.

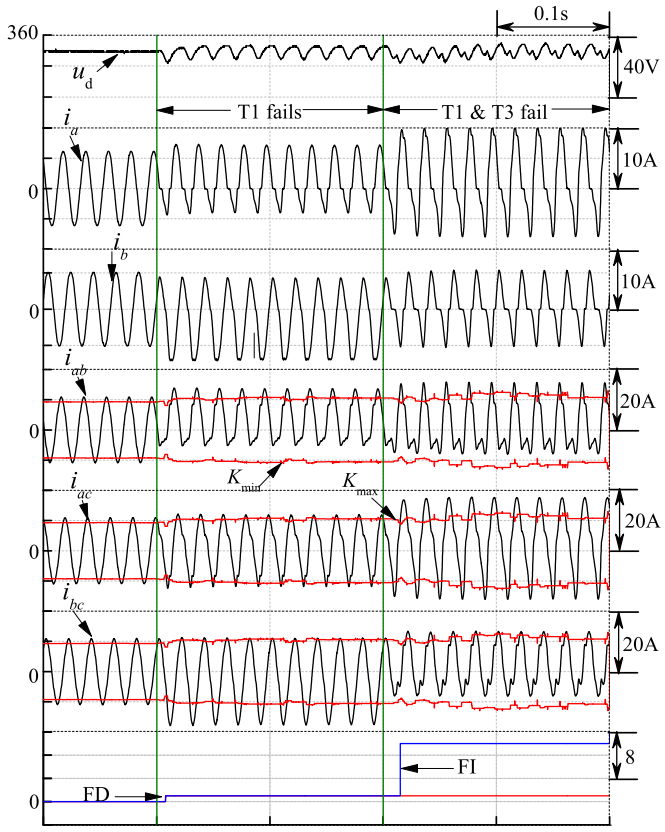

Fig. 12. Fault diagnosis process when T1 fails at 0.1 s and T3 fails at 0.3 s (represent FAULT_3) with reference voltage $u_d{}^* = 350$ V, from up to down, output voltage, three-phase currents, line-to-line currents, and diagnostic signals.

the fault occurs, the peaks or valleys of line-to-line currents are not all outside the envelopes consisted of $K_{\max}$ and $K_{\min}$, indicating the primary inductance energy storage is abnormal, fault is detected. In subfigure 3, 4, 5 of Fig. 10, only the peak of i_{ab} is inside the envelops, which represents only P_{ab} and N_{ba} are equal to zero, indicating the primary inductance energy storage is abnormal in state IV, the results keep unchanged for more than a current fundamental period. Consequently, the fault is confirmed and located to T2 according to Table III. The fault occurs at 0.1 s, and is detected at 0.109 s, located at 0.109 s. The detection and isolation time are within a current period, which proves the proposed method is fast and effective.

C. Multiple Open-Circuit Fault

Fig. 11 shows the experimental results of dc output, phase currents (i_a, i_b, i_c), line-to-line currents (i_{ab}, i_{bc}, i_{ac}) together with envelopes $(K_{\max}, K_{\min})$, and diagnostic results (FD, FI). First, a single open-circuit fault is applied by inhibiting the gate drive signal to T2 at 0.1s, then T1 is inhibited at 0.3 s as secondary fault. The primary line-to-line voltages are 145 V, the predefined dc output is 350 V. It can be seen that after the fault occurrence, the peaks or valleys of line-to-line currents are not all outside the envelopes consisted of $K_{\max}$ and $K_{\min}$, indicating the primary inductance energy storage is abnormal, fault is detected.

During the process of T2 failure (0.1 s $\rightarrow$ 0.3 s), in subfigure 3, 4, 5 of Fig. 11, only the peak of i_{ab} is inside the envelops, which represents only $P_{ab} = 0$ and $N_{ba} = 0$, indicating the primary inductance energy processes are abnormal in state I, consequently, the fault is located to T2 according to Table III. During the process of T1 and T2 failure (0.3 s $\rightarrow$ 0.5 s), in subfigure 3, 4, 5 of Fig. 11, peak and valley of i_{ab} are inside the envelops, which represents $P_{ab}, P_{ba}, N_{ab}, N_{ba}$ are equal to zero, indicating the primary inductance energy processes are abnormal in state I, IV, consequently, the fault is located to T1T2 according to Table III.

Fig. 12 shows the experimental results of dc output, phase currents (i_a, i_b, i_c), line-to-line currents (i_{ab}, i_{bc}, i_{ac}) together with envelopes $(K_{\max}, K_{\min})$, and diagnostic results (FD, FI). First, a single open-circuit fault is applied by inhibiting the gate drive signal to T1 at 0.1 s, then T3 is inhibited at 0.3 s as secondary fault. The primary line-to-line voltages are 145 V, the predefined dc output is 350 V. It can be seen that after the fault occurrence, the peaks or valleys of line-to-line currents are not all outside the envelopes consisted of $K_{\max}$ and $K_{\min}$,

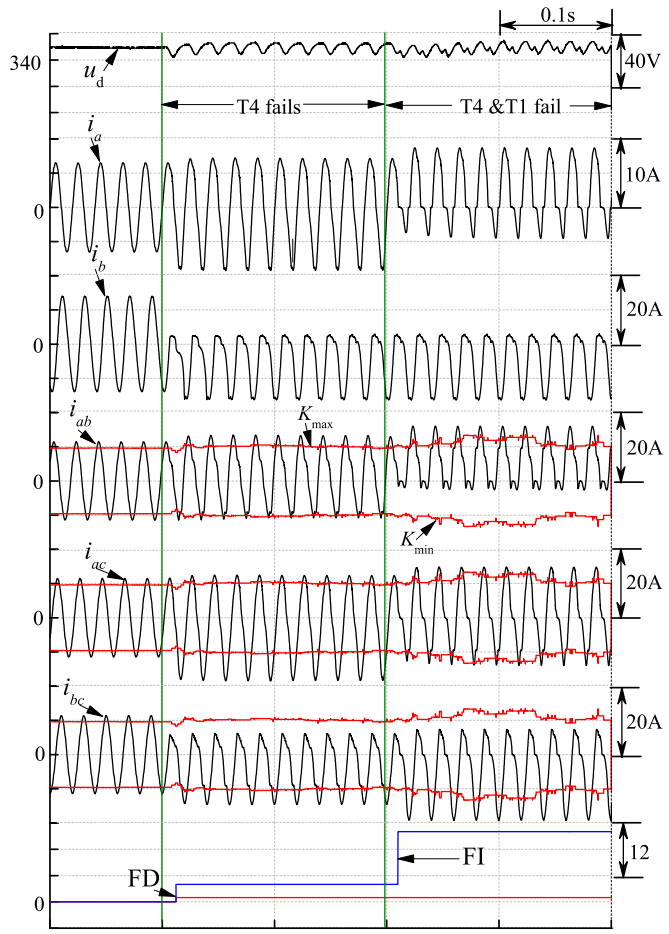

Fig. 13. Fault diagnosis process when T4 (represent FAULT_4) fails at 0.1 s and T1 fails at 0.3 s with reference voltage $u_d{}^* = 350$ V, from up to down, output voltage, three-phase currents, line-to-line currents, and diagnostic signals.

indicating the primary inductance energy storage is abnormal, fault is detected.

During the process of T1 failure (0.1 s $\rightarrow$ 0.3 s), in subfigure 3, 4, 5 of Fig. 12, only the valley of i_{ab} is inside the envelops, which represents only $N_{ab} = 0$ and $P_{ba} = 0$, indicating the primary inductance energy processes are abnormal in state IV, consequently, the fault is located to T1 according to Table III. During the process of T1 and T3 failure (0.3 s $\rightarrow$ 0.5 s), in subfigure 3, 4, 5 of Fig. 12, valleys of i_{ab} and i_{bc} are inside the envelops, which represents $N_{ab}, N_{bc}, P_{ba}, P_{cb}$ are equal to zero, indicating the primary inductance energy processes are abnormal in state IV, VI, consequently, the fault is located to T1T3 according to Table III.

Fig. 13 shows the experimental results of dc output, phase currents (i_a, i_b, i_c), line-to-line currents (i_{ab}, i_{bc}, i_{ac}) together with envelopes $(K_{\max}, K_{\min})$, and diagnostic results (FD, FI). First, a single open-circuit fault is applied by inhibiting the gate drive signal to T4 at 0.1 s, then T1 is inhibited at 0.3 s as secondary fault. The primary line-to-line voltages are 145 V, the predefined dc output is 350 V. It can be seen that after the fault occurrence, the peaks or valleys of line-to-line currents are not all outside the envelopes consisted of $K_{\max}$ and $K_{\min}$, indicating the primary inductance energy storage is abnormal, fault is detected.

During the process of T4 failure (0.1 s $\rightarrow$ 0.3 s), in subfigure 3, 4, 5 of Fig. 13, only the peak of i_{bc} is inside the envelops, which represents only $P_{bc} = 0$ and $N_{cb} = 0$, indicating the primary inductance energy processes are abnormal in state III during, consequently, the fault is located to T4 according to Table III. During the process of T1 and T4 failure (0.3 s $\rightarrow$ 0.5 s), in subfigure 3, 4, 5 of Fig. 13, valley of i_{ab} and peak of i_{bc} are inside the envelops, which represents $N_{ab}, N_{cb}, P_{ba}, P_{bc}$ are equal to zero, indicating the primary inductance energy processes are abnormal in state III, IV, consequently, the fault is located to T1T4 according to Table III.

D. Comparison With Previous Methods

Performance of the proposed fault diagnosis method is compared with previous methods, such as detection time, robustness, tuning effort, cost, efficiency, implementation. The proposed fault diagnosis method can detect and isolate the fault within a current fundamental period, as well as [26], [29]. The difference is that the proposed method can successfully identify 21 fault types due to the perfect failure analysis based on primary inductances energy storage, furthermore, the proposed method shows lower tuning effort, and easier implementation. The merit of proposed fault diagnosis method also can be proved by performance indice such as fast detection and identification, low-cost, fair robustness. and model-independance.

VI. Conclusion

A real-time and robust single and multiple open-circuit fault diagnosis method in a three-phase boost rectifier is proposed based on the primary inductance energy storage and release. Particularly, inductance energy storage process within zero-vector has been deeply analyzed under healthy and faulty conditions. Different faults lead to inductance energy storage abnormal in different states, which cause the corresponding line-to-line currents distorted with unhealthy peaks or valleys. A diagnostic table is designed based on the relationship between peaks and valleys of line-to-line currents and inductance energy storage processes. Lots of experimental results under unity power factor show the effectiveness of the proposed method. The proposed zero-vectors-based method with primary inductance energy analysis is versatile and can be used to other modulation and control strategies, such as SPWM, it also has potential application in rectifiers with different topologies, no extra sensors are required, fair robustness and high performance are evaluated.

References

[1] B. L. Dokić and B. Blanuša, *Power Electronics Converters and Regulators*, 3rd ed. New York, NY, USA: Cham, Switzerland: Springer, 2015.

[2] S. Nandi, H. Toliyat, and X. Li, "Condition monitoring and fault diagnosis of electrical motors—A review," *IEEE Trans. Energy Convers.*, vol. 20, no. 4, pp. 719–729, Dec. 2005.

[3] S. Yang, D. Xiang, A. Bryant, P. Mawby, L. Ran, and P. Tavner, "Condition monitoring for device reliability in power electronic converters: A review," *IEEE Trans. Power Electron.*, vol. 25, no. 11, pp. 2734–2752, Nov. 2010.

[4] S. Yang, A. Bryant, P. Mawby, D. Xiang, L. Ran, and P. Tavner, "An industry-based survey of reliability in power electronic converters," *IEEE Trans. Ind. Appl.*, vol. 47, no. 3, pp. 1441–1451, May–Jun. 2011.
[5] B. Lu and S. K. Sharma, "A literature review of igbt fault diagnostic and protection methods for power inverters," *IEEE Trans. Ind. Appl.*, vol. 45, no. 5, pp. 1770–1777, Sep./Oct. 2009.
[6] I. Jlassi, J. O. Estima, E. Khil, S. Khojet, N. M. Bellaaj, and A. J. Marques Cardoso, "Multiple open-circuit faults diagnosis in back-to-back converters of PMSG drives for wind turbine systems," *IEEE Trans. Power Electron.*, vol. 30, no. 5, pp. 2689–2702, May 2015.
[7] J. O. Estima and A. J. M. Cardoso, "A new approach for real-time multiple open-circuit fault diagnosis in voltage-source inverters," *IEEE Trans. Ind. Appl.*, vol. 47, no. 6, pp. 2487–2494, Nov./Dec. 2011.
[8] M. A. Rodríguez-Blanco, A. Va zquez Pe rez, L. Herna ndez Gonza lez, V. Golikov, J. s. Aguayo-Alquicira, and M. May-Alarcon, "Fault detection for IGBT using adaptive thresholds during the turn-on transient," *IEEE Trans. Ind. Electron.*, vol. 62, no. 3, pp. 1975–1983, Mar. 2015.
[9] J. O. Estima and A. J. Marques Cardoso, "A new algorithm for real-time multiple open-circuit fault diagnosis in voltage-fed pwm motor drives by the reference current errors," *IEEE Trans. Ind. Electron.*, vol. 60, no. 8, pp. 3496–3505, Aug. 2013.
[10] F. Zidani, D. Diallo, M. E. H. Benbouzid, and R. Naït-Saïd, "A fuzzy-based approach for the diagnosis of fault modes in a voltage-fed pwm inverter induction motor drive," *IEEE Trans. Ind. Electron.*, vol. 55, no. 2, pp. 586–593, Feb. 2008.
[11] D. Espinoza-Trejo, D. Campos-Delgado, E. Ba rcenas, and F. Martı nez López, "Robust fault diagnosis scheme for open-circuit faults in voltage source inverters feeding induction motors by using non-linear proportional-integral observers," *IET Power Electron.*, vol. 5, no. 7, pp. 1204–1216, Aug. 2012.
[12] C. Choi and W. Lee, "Design and evaluation of voltage measurement-based sectoral diagnosis method for inverter open switch faults of permanent magnet synchronous motor drives," *IET Electr. Power Appl.*, vol. 6, no. 8, pp. 526–532, Sep. 2012.
[13] J. Zhang, J. Zhao, D. Zhou, and C. Huang, "High-performance fault diagnosis in PWM voltage-source inverters for vector-controlled induction motor drives," *IEEE Trans. Power Electron.*, vol. 29, no. 11, pp. 6087–6099, Nov. 2014.
[14] N. M. Freire *et al.*, "A voltage-based approach without extra hardware for open-circuit fault diagnosis in closed-loop pwm ac regenerative drives," *IEEE Trans. Ind. Electron.*, vol. 61, no. 9, pp. 4960–4970, Sep. 2014.
[15] S.-M. Jung, J.-S. Park, H.-W. Kim, K.-Y. Cho, and M.-J. Youn, "An MRAS-based diagnosis of open-circuit fault in PWM voltage-source inverters for pm synchronous motor drive systems," *IEEE Trans. Power Electron.*, vol. 28, no. 5, pp. 2514–2526, May 2013.
[16] J. Caseiro *et al.*, "Fault diagnosis on a PWM rectifier ac drive system with fault tolerance using the average current park's vector approach," in *Proc. IEEE Int. Electr. Mach. Drives Conf.*, 2009, pp. 695–701.
[17] J. O. Estima *et al.*, "Recent advances in fault diagnosis by park's vector approach," in *Proc. IEEE Workshop Elect. Mach. Design Control Diagnosis*, 2013, pp. 279–288.
[18] D. Diallo, M. E. H. Benbouzid, D. Hamad, and X. Pierre, "Fault detection and diagnosis in an induction machine drive: A pattern recognition approach based on concordia stator mean current vector," *IEEE Trans. Energy Convers.*, vol. 20, no. 3, pp. 512–519, Sep. 2005.
[19] W. Sleszynski, J. Nieznanski, and A. Cichowski, "Open-transistor fault diagnostics in voltage-source inverters by analyzing the load currents," *IEEE Trans. Ind. Electron.*, vol. 56, no. 11, pp. 4681–4688, Nov. 2009.
[20] F. Wu and J. Zhao, "A real-time multiple open-circuit fault diagnosis method in voltage-source-inverter fed vector controlled drives," *IEEE Trans. Power Electron.*, vol. 31, no. 2, pp. 1425–1437, Feb. 2016.
[21] J. Zhang, H. Luo, J. Zhao, and F. Wu, "A fuzzy-based approach for open-transistor fault diagnosis in voltage-source inverter induction motor drives," *Eur. Phys. J. Appl. Phys.*, vol. 69, 2015, Art. no. 20101.
[22] F. Wu, J. Zhao, and Y. Liu, "Symmetry-analysis-based diagnosis method with correlation coefficients for open-circuit fault in inverter," *Electron. Lett.*, vol. 51, no. 21, pp. 1688–1690, 2015.
[23] L. M. Caseiro *et al.*, "Real-time IGBT open-circuit fault diagnosis in three-level neutral-point-clamped voltage-source rectifiers based on instant voltage error," *IEEE Trans. Ind. Electron.*, vol. 62, no. 3, pp. 1669–1678, Mar. 2015.
[24] B. Gou, X. Ge, S. Wang, X. Feng, J. B. Kuo, and T. G. Habetler, "An open-switch fault diagnosis method for single-phase PWM rectifier using a model-based approach in high-speed railway electrical traction drive system," *IEEE Trans. Power Electron.*, vol. 31, no. 5, pp. 3816–3826, May 2016.
[25] J.-S. Lee and K.-B. Lee, "Tolerance control for the inner open-switch faults of a t-type three-level rectifier," *J. Power Electron.*, vol. 14, no. 6, pp. 1157–1165, 2014.
[26] W.-S. Im, J.-M. Kim, D.-C. Lee, and K.-B. Lee, "Diagnosis and fault-tolerant control of three-phase ac–dc PWM converter systems," *IEEE Trans. Ind. Appl.*, vol. 49, no. 4, pp. 1539–1547, Jul./Aug. 2013.
[27] W.-S. Im, J.-S. Kim, J.-M. Kim, D.-C. Lee, and K.-B. Lee, "Diagnosis methods for IGBT open switch fault applied to 3-phase ac/dc pwm converter," *J. Power Electron.*, vol. 12, no. 1, pp. 120–127, Jan. 2012.
[28] S. Khomfoi, W. Sae-Kok, and I. Ngamroo, "An open circuit fault diagnostic technique in IGBTs for ac to dc converters applied in microgrid applications," *J. Power Electron.*, vol. 11, no. 6, pp. 801–810, Nov. 2011.
[29] N. M. Freire *et al.*, "Open-circuit fault diagnosis in PMSG drives for wind turbine applications," *IEEE Trans. Ind. Electron.*, vol. 60, no. 9, pp. 3957–3967, Sep. 2013.
[30] I. Jlassi, J. O. Estima, S. K. E. Khil, N. M. Bellaaj, and A. J. M. Cardoso, "Multiple open-circuit faults diagnosis in back-to-back converters of PMSG drives for wind turbine systems," *IEEE Trans. Power Electron.*, vol. 30, no. 5, pp. 2689–2702, May 2015.

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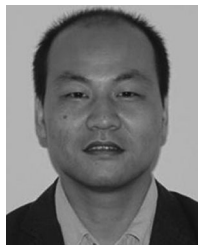

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