Impact of Slim DC Capacitance on Floating Capacitor H-bridge Motor Drive

Siyu Leng, *Member, IEEE*, S. M. Muyeen, *Senior Member, IEEE*, Ahmed Al-Durra, *Senior Member, IEEE*, and Frede Blaabjerg, *Fellow, IEEE*

***Abstract*—This paper discusses the impact of small dc capacitance in a motor drive using a floating capacitor H-bridge topology. The proposed topology is intended for applications where variable frequency control is not required. Special attention is paid on investigating the second-order dc capacitor voltage ripples, whose influence on the induction motor as well as on the motor drive itself is of importance. This issue is addressed in this paper through rigorous mathematical formulations. It is found that by inverting the second-order dc ripple voltage using the conventional SVPWM, no harmful harmonics will be generated in the motor line voltage. This demonstrates the possibility of drastically reducing the dc capacitance of the proposed system. Induction motor as well as H-bridge performance with respect to different dc capacitance values is demonstrated by experiments, which lays the foundation for cost reduction and reliability enhancement of the proposed system.**

***Index Terms*—DC voltage ripple, floating capacitor, H-bridge, induction motor, serial voltage injection.**

I. INTRODUCTION

DIRECT-ON-LINE start of an induction motor usually results in a high inrush current and a large starting torque, which has a negative impact on the motor itself as well as on the electrical power system feeding the motor. Internally, large inrush current induces large magnetic forces in the stator windings to force them to move and distort [1]; the power dissipation associated with high levels of inrush current can produce a rapid temperature rise and may damage the winding insulation [1]. Externally, the inrush current may cause the local grid voltage to dip and circuit breakers to trip [2]. On the other hand, induction motors also require reactive power to establish a magnetic field; therefore, its input power factor is in the lagging area. In fact, induction motors are the prime contributor to the total reactive power demand of any given power system [3]. In order to reduce the start-up impact of induction motors, a number of techniques have been developed, which can be grouped as: a) electromechanical [4], b) solid-state [5], [6], c) variable frequency drive (VFD) [7], [8], and as recently introduced d) serial voltage injection topology [9]–[11].

For a serial voltage injection topology [9]–[11], a power electronics device called "Magnetic Energy Recover Switch" (MERS) was proposed, in which the magnetic energy stored in the inductive load can be restored. The topology of MERS consists of four forced commutated switches and a small dc capacitor [12]. The configuration of MERS is similar to that of a single-phase full bridge, but MERS is connected in series between grid and load. Hence, different control techniques are applied. For the MERS, the capacitor is not connected to a dc power supply, which means the capacitor voltage is allowed to change dynamically and even to become zero. Therefore, the size of the capacitor is several times smaller [13]. By injecting a voltage in series with the grid voltage, induction motor voltage can be controlled in order to achieve soft start and a leading power factor operation for induction motor becomes possible.

The inherent characteristic of MERS is the use of low switching frequency where the semiconductor switches turn ON and OFF only once in a cycle at 50/60 Hz supply frequency. However, due to its low switching frequency, the ac voltage supplied to the motor contains low-order harmonics. The self-excited ac harmonic current introduced by the MERS generates torque that has different synchronous speed and, therefore, may work as a braking torque [14]–[17]. This torque can cause oscillations or even prevent the motor speed from increasing to the rated value. The closed-loop control was found to be useful to damp out such oscillations, but it cannot be completely avoided [9], [10].

In order to provide a more stable soft-start solution, a floating capacitor H-bridge that can also provide soft start and VAR compensation is presented in [18]–[21], as shown in Fig. 1.

It should be noted that the physical installation point of the proposed motor drive shown in Fig. 1 should be as close to the motor as possible so that reflected wave phenomenon from motor cable influence can be minimized.

The main difference between the MERS and the floating capacitor H-bridge shown in Fig. 1 is that the latter uses the SVPWM, which means the switching frequency is much higher than that of the MERS. As a result, only the fundamental ac voltage component plus high-order ac harmonics around the switching frequency is injected between the grid and motor. The later ones can easily be filtered out by the induction

---

Manuscript received February 7, 2017; revised April 19, 2017; accepted May 22, 2017. Date of publication June 1, 2017; date of current version January 3, 2018. This work was supported by the Abu Dhabi National Oil Company. Recommended for publication by Associate Editor S. K. Panda. *(Corresponding author: Ahmed Al-Durra.)*

S. Leng and A. Al-Durra are with the Department of Electrical and Computer Engineering, Khalifa University of Science and Technology, Petroleum Institute, Abu Dhabi 2533, United Arab Emirates (e-mail: sleng@pi.ac.ae; aaldurra@pi.ac.ae).

S. M. Muyeen is with the Department of Electrical and Computer Engineering, Curtin University, Perth, WA 6102, Australia (e-mail: Sm.Muyeen@curtin.edu.au).

F. Blaabjerg is with the Department of Energy Technology, Faculty of Engineering and Science, Aalborg University, Aalborg 9220, Denmark (e-mail: fbl@et.aau.dk).

Color versions of one or more of the figures in this paper are available online at http://ieeexplore.ieee.org.

Digital Object Identifier 10.1109/TPEL.2017.2710882

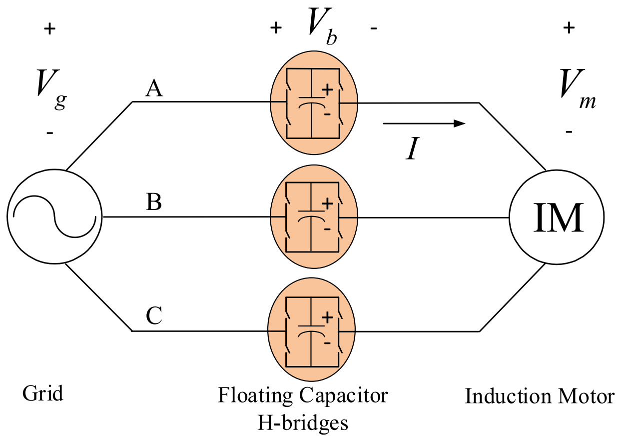


Fig. 1. Floating capacitor H-bridge induction motor drive.

motor. Therefore, self-excited low-order ac harmonic current in the motor can be avoided, which greatly improves the system stability. Note that the proposed floating capacitor H-bridge motor drive cannot change the frequency of the voltage supplied to machine. This approach is only intended for applications where frequency control is not required, such as fans, pumps, and compressors. It should be noted that for the proposed topology in Fig. 1, each phase is subject to power pulsations at twice the grid fundamental frequency. To buffer the energy variations, energy storage elements such as dc capacitors are used. For a 5 HP (3.725 kW) induction motor, the reported dc capacitors used in dc-link were electrolyte capacitors with a capacitance of 8 mF per phase [18]–[21]. This capacitance value is much larger than that of a typical dc capacitor used in a conventional VFD. The large electrolytic capacitor bank poses a lot of issues.

1) High cost of large dc capacitors.
2) Electrolytic capacitor has relatively high equivalent series resistance (ESR), low ripple current ratings, and wear out issue due to the evaporation of electrolyte [22]–[24]. In fact, it has been pointed out in [25] that the nominal lifetime of electrolytic capacitors is not long enough for most applications.
3) High cost on cell protection due to large energy that is dissipated in the event of dc-link shoot-through.
4) Significant weight and volume of the converter, which can make it difficult to build a high power density power electronics system [26].

Therefore, it is desirable that the capacitance of the dc capacitors for the proposed floating capacitor H-bridge system be reduced. In this paper, the impact of such dc capacitance reduction is investigated. It turns out that the second-order dc voltage ripple does not introduce problematic harmonics in the motor current. This is because for capacitive mode of operation, the ripple waveform has the same phase-angle as the absolute value of H-bridge output voltage. Although for the inductive mode, such a phenomenon is not true, but this condition does not occur in the floating capacitor H-bridge motor drive because the proposed system always operates with a leading power factor [20], [21].

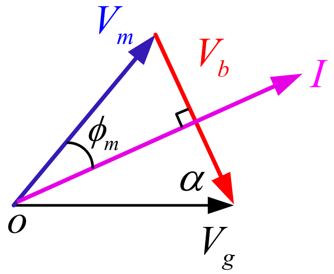


Fig. 2. Voltage vector diagram for an induction motor.

In fact, a similar method has been utilized before for use in cascaded H-bridge (CHB) multilevel inverters where low dc capacitance values can be used [27]–[29]. While the conclusions are similar, the application is totally different. For the CHB systems [27]–[29], the dc capacitor voltages are regulated. However, for the proposed system shown in Fig. 1, the dc capacitor voltages are free-floating. Since no control is needed for floating the dc capacitor voltage, there is no necessity for an analytic filtering scheme [27]. In addition, for the proposed system shown in Fig. 1, the system is assumed to be balanced. Therefore, the second-order dc capacitor ripples can be easily filtered out by averaging the three capacitor voltages. Thus, no dc-link variation feed-forward compensation [28], [29] is needed. All of these features make the proposed control algorithm very easy to be implemented.

Allowing larger dc capacitor voltage variations also implies the use of significantly lower dc capacitance values. Thus, the electrolytic capacitors can be easily replaced with a metalized polypropylene film (MPPF) capacitor, which has a much longer lifetime [30]–[33]. In addition, this paper discovers that when the second-order dc ripple fluctuates, the equivalent modulation index for the H-bridge is boosted. Such a phenomenon will be taken into account in the control algorithm so that a more accurate motor voltage control can be achieved. It should be noted that for an unbalanced grid condition (e.g., in an isolated microgrid), the modulation strategy proposed in this paper will no longer be valid, mainly because a) the presence of negative sequence component will degrade the performance of phase locked loop (PLL) used in this paper; and b) the second-order dc ripple may not cancel each other under unbalanced condition. The method to overcome this issue is out of the scope of this paper.

This paper is organized as follows. In Section II, the basic information on motor terminal voltage control is presented. In Section III, the second-order dc voltage ripple is modeled, which serves as the foundation for the mathematical analysis in Section IV. Section V gives details of the laboratory setup. Then, hardware experimental results are given in Section VI. Finally, conclusions are drawn in Section VII.

II. MOTOR TERMINAL VOLTAGE CONTROL

The motor terminal voltage control strategy of the proposed system can be illustrated using a voltage vector diagram representing one phase of the motor, as shown in Fig. 2.

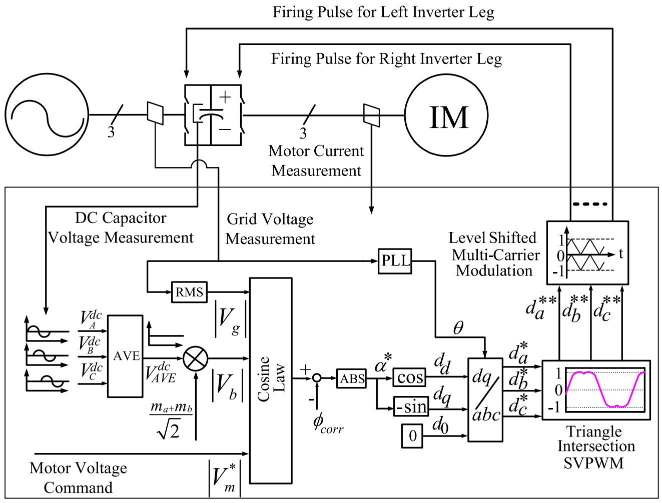


Fig. 3. Block diagram for alpha angle control.

Fig. 2 is based on a rotating frame using d-q transformation. V_g represents the grid voltage vector, which is tracked by a PLL and aligned with the d-axis. V_b represents a serial ac voltage injected by the H-bridge and V_m represents the motor terminal ac voltage. It can be seen that by manipulating angle alpha (the angle between the grid voltage vector V_g and the H-bridge voltage vector V_b), the magnitude of motor terminal voltage V_m can be changed accordingly [19]–[21].

A. Alpha Angle Control

The block diagram for alpha angle control is shown in Fig. 3. Compared with the previously proposed control method in [19]–[21], the main difference in this paper is that drastic dc capacitance reduction will result in the second-order dc voltage ripple. As a result, instead of a constant modulation index for the H-bridge (m_a represents the constant modulation index in [19]–[21]), the equivalent modulation index of the H-bridge is boosted in this paper ($m_a + m_b$ represents the equivalent modulation index). This phenomenon will be taken into account in the control loop so that a more accurate motor terminal voltage control can be achieved.

Assume that the grid is balanced and the second-order dc voltage ripples are also balanced. In Fig. 3, it can be seen that taking the average of three dc capacitor voltages will eliminate the second-order ripple component, leaving only the dc offset value as

$$V_{\mathrm{AVE}}^{\mathrm{dc}} = \frac{V_A^{\mathrm{dc}} + V_B^{\mathrm{dc}} + V_C^{\mathrm{dc}}}{3}. \tag{1}$$

$|V_b|$ in Fig. 3 is the root-mean-square (RMS) for fundamental ac voltage injected by the H-bridge (m_a represents the constant modulation index of the SVPWM, while m_b represents the modulation index boost caused by the second-order dc voltage ripple, which will be explained later in this paper)

$$|V_b| = \frac{V_{\mathrm{AVE}}^{\mathrm{dc}} \cdot (m_a + m_b)}{\sqrt{2}}. \tag{2}$$

The angle α can be set by the controller, using the vector relationships shown in Fig. 2, to supply the motor at a specific desired operating voltage $|V_m^*|$ such that

$$\cos\alpha^* = \frac{|V_g|^2 + |V_b|^2 - |V_m^*|^2}{2 \cdot |V_g| \cdot |V_b|} \tag{3}$$

where $|V_g|$ represents the measured RMS of the grid phase voltage.

In Fig. 3, the reference signal for α^* is derived from (3). A phase correction signal ϕ_{corr} is used to take into account various signal phase delays, such as SVPWM signal generation delays [20], [21]. A PLL is used to track the grid voltage angle (θ), which is used to perform the inverse Park transformation. The SVPWM modulation method used in this paper uses the zero-sequence signal injection to increase the modulation index [34]–[36]. The theoretical upper limit for m_a using zero-sequence injection is 1.1547. In this paper, m_a is set to be slightly lower ($m_a = 1.1$ in this work for minimum pulse width considerations, as will be explained in the next section). For an equivalent modulation index ($m_a + m_b$), it can be quantified, as shown in Section IV C. In order to generate a perfect five-level pulse width modulation (PWM) line voltage waveform, the level-shifted multicarrier waves [37] are used to generate the firing pulses for the H-bridges.

B. Minimum Pulse Width Consideration

Carrier-based PWM methods employ the “per-carrier cycle volt-second balance” principle. A modulation wave is compared with a triangular carrier wave and the intersections define the switching instants. Using zero-sequence signal injection, the peak of modified modulation wave is dampened, allowing higher fundamental component to be fitted into the envelop of carrier waveform. In this way, the modulation index can be increased from 1.0 to 1.1547. Should $m_a = 1.1547$ be chosen, the peak of modulation wave will have the same magnitude as the peak of carrier wave. This means in the regions where modulation waves are near the tip of carrier waves, the PWM firing pulses will be very short. If the duration of PWM firing pulses is less than dead time and IGBT turn ON/OFF time combined, this will result in missing IGBT output. In other words, IGBT is not switching despite its firing pulse is provided simply because the pulse is too short. For the IGBT modules used in this paper (SEMiX202GB12E4s), the adaptor board (Board 2s SKYPER 32PRO R) has a dead time of 2.2 μs. Also, the turn ON and turn OFF time of IGBT is tuned at 0.4 μs and 0.7 μs, respectively. Therefore, theoretically for IGBT to respond, the duration of its firing pulse should not be less than 3.3 μs. Considering the fact that carrier period is 133 μs (7.5 kHz switching frequency, as can be seen in Section V), this means the peak of modulation wave should be no more than 95% of the carrier envelop ($1 - \frac{3.3}{133/2} = 0.95$) to avoid generating pulses that are too short for IGBT to respond. Therefore, $m_a = 1.1547 \times 0.95 = 1.1$ is chosen for minimum pulse width considerations.

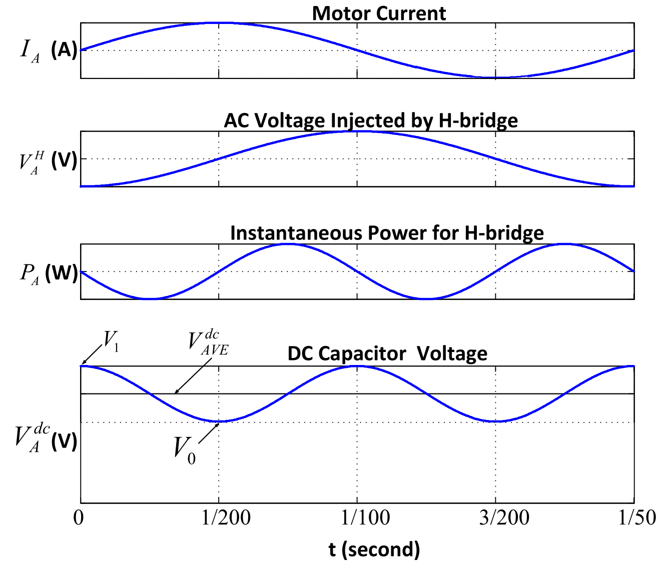


Fig. 4. Waveform of different parameters for the proposed system.

III. DC RIPPLE VOLTAGE MODELING

To quantify the dc voltage ripple, a rigorous energy analysis is carried out in this section. Assuming a balanced system with 50 Hz grid frequency, the instantaneous power flow from/to the H-bridge in phase A can be expressed as

$$P_A = -\left|V_b\right| \cdot I_m \cdot \sin(200 \cdot \pi \cdot t) \tag{4}$$

where $|V_b|$ represents the RMS for ac voltage injected by the H-bridge, I_m represents the RMS for motor current. (4) implies that a) the instantaneous power flow from/to the H-bridge is fluctuating at twice the grid frequency; b) neglecting losses in IGBT and capacitors, the average net power to the H-bridge is zero. For the proposed H-bridge topology, the dc capacitors are not connected to dc power supply and thus free-floating. This means the only element that can absorb/release such fluctuating energy is the dc capacitor. Due to this fluctuating power flow, the dc capacitor is constantly being charged and discharged, causing a second-order dc ripple voltage, as shown in Fig. 4. It should be noted that the purpose of Fig. 4 is to illustrate the phase relationship between different parameters of the proposed system. Therefore, neither absolute value nor p.u. value is provided in Fig. 4.

To quantify the magnitude of dc ripple voltage, the energy removed from the dc capacitor during the discharging period (the first ¼ cycle in Fig. 4) can be calculated as

$$W_{\text{discharge}} = \int_0^{\frac{1}{200}} P_A \cdot dt = -\frac{\left|V_b\right| \cdot I_m}{100 \cdot \pi}. \tag{5}$$

On the other hand, the energy removed from the dc capacitor during the discharging period (the first ¼ cycle in Fig. 4) can also be calculated by the voltage difference between the initial and final state as

$$\begin{aligned} W_{\text{discharge}} &= \frac{1}{2}\left(V_0^2 - V_1^2\right) \cdot C \\ &= -\frac{1}{2} \cdot (V_1 + V_0) \cdot (V_1 - V_0) \cdot C \\ &= -V_{\text{AVE}}^{\text{dc}} \cdot \Delta V \cdot C \end{aligned} \tag{6}$$

where C represents the capacitance of dc capacitor. Combining (2), (5), and (6), the magnitude of the dc ripple (peak to peak) can be obtained as

$$\Delta V = V_1 - V_0 = \frac{I_m \cdot (m_a + m_b)}{100 \cdot \sqrt{2} \cdot \pi \cdot C}. \tag{7}$$

Equation (7) shows that the magnitude of the dc ripple is generally proportional to motor current and inversely proportional to the capacitance of the dc capacitor. Since the motor current is determined by the motor load condition, the only factor that can reduce the dc ripple is to increase the capacitance of the dc capacitor. However, such an approach requires a very large dc capacitance value and it is not practical. In this paper, another approach is taken and it will be shown in the next section.

IV. IMPACT OF DC RIPPLE

This section systematically explores the impact of the dc ripple. First, the ac voltage injected by the H-bridge in each phase is modeled in the time domain (phase A and B, respectively). Then, the line voltage is revealed by calculating the difference between the two phases. Following that, IGBT voltage stress caused by the dc ripple is discussed and ripple current of capacitor is calculated. Finally, a general method to estimate the minimum dc capacitance value for the floating capacitor H-bridge system is proposed.

A. H-bridge Phase Voltage

From Fig. 4, it is obvious that the dc capacitor voltage ripple is lagging the instantaneous power by 90 degree. Therefore, in the time domain, the dc capacitor voltage in phase A of the H-bridge system can be modeled as

$$V_A^{\text{dc}} = V_{\text{AVE}}^{\text{dc}} - \frac{\Delta V}{2} \cdot \sin\left(200 \cdot \pi \cdot t - \frac{\pi}{2}\right). \tag{8}$$

If the H-bridge is injecting ac voltage using the conventional SVPWM (m_a fixed at 1.1, no dc-link variation feedforward compensation used), the RMS of fundamental ac voltage injected by the H-bridge in phase A can be modeled as

$$\begin{aligned} V_A^{\text{RMS}} = \frac{m_a}{\sqrt{2}} \cdot V_{\text{AVE}}^{\text{dc}} - \frac{I_m \cdot m_a \cdot (m_a + m_b)}{400 \cdot \pi \cdot C} \\ \cdot \sin\left(200 \cdot \pi \cdot t - \frac{\pi}{2}\right). \end{aligned} \tag{9}$$

From Fig. 4, it can also be seen that ac voltage injected by the H-bridge is 90 degree lagging the motor current. Therefore, the voltage injected by the H-bridge in the time domain can be expressed as

$$V_A^H = V_A^{\text{RMS}} \cdot \sin\left(100 \cdot \pi \cdot t - \frac{\pi}{2}\right). \tag{10}$$

Combining (9) with (10), after simplification, the ac voltage injected by the H-bridge in the time domain can be expressed as

$$V_A^H = -\left(\frac{m_a}{\sqrt{2}} \cdot V_{\mathrm{AVE}}^{\mathrm{dc}} + \frac{I_m \cdot m_a \cdot (m_a + m_b)}{800 \cdot \pi \cdot C}\right) \cdot \cos(100 \cdot \pi \cdot t) - \frac{I_m \cdot m_a \cdot (m_a + m_b)}{800 \cdot \pi \cdot C} \cdot \cos(300 \cdot \pi \cdot t). \tag{11}$$

From (11), it can be seen that the dc ripple in capacitor voltage actually introduces a third harmonic component to the voltage injected by the H-bridge. This phenomenon is because multiplications of the harmonic components in the time domain are the convolutions in the frequency domain. For example, when the first harmonic component is multiplied by the second harmonic component in the time domain, both first and third harmonic components will be generated.

Taking into account the fact that in this paper, zero-sequence signal injection is used to increase the modulation index [34]–[36]. As a result, one-sixth of the third harmonics will also be added to the output of the H-bridge [38]. This means besides the third harmonic component caused by the dc voltage ripple [see (11)], there should be an additional third harmonic component caused by the SVPWM. Interestingly, it is found that the two-third harmonic components have an opposite phase angle, which means the third harmonic created by dc ripple voltage will cancel out part of the third harmonic component generated by the SVPWM.

Therefore, the ac voltage injected by the H-bridge in the time domain, which takes into account the dc ripple effect as well as the third harmonic injection effect from the SVPWM should be expressed as

$$V_A^H = -\left(\frac{m_a}{\sqrt{2}} \cdot V_{\mathrm{AVE}}^{\mathrm{dc}} + \frac{I_m \cdot m_a \cdot (m_a + m_b)}{800 \cdot \pi \cdot C}\right) \cdot \cos(100 \cdot \pi \cdot t) + \left(\frac{1}{6} \cdot \frac{m_a}{\sqrt{2}} \cdot V_{\mathrm{AVE}}^{\mathrm{dc}} - \frac{I_m \cdot m_a \cdot (m_a + m_b)}{800 \cdot \pi \cdot C}\right) \cdot \cos(300 \cdot \pi \cdot t). \tag{12}$$

B. H-bridge Line Voltage

Assuming a balanced system, the voltage in phase B of the system is lagging phase A by 120 degree. Using a similar analysis for phase A, the ac voltage injected by the H-bridge in phase B is

$$V_B^H = -\left(\frac{m_a}{\sqrt{2}} \cdot V_{\mathrm{AVE}}^{\mathrm{dc}} + \frac{I_m \cdot m_a \cdot (m_a + m_b)}{800 \cdot \pi \cdot C}\right) \cdot \cos\left(100 \cdot \pi \cdot t - \frac{2\pi}{3}\right) + \left(\frac{1}{6} \cdot \frac{m_a}{\sqrt{2}} \cdot V_{\mathrm{AVE}}^{\mathrm{dc}} - \frac{I_m \cdot m_a \cdot (m_a + m_b)}{800 \cdot \pi \cdot C}\right) \cdot \cos(300 \cdot \pi \cdot t). \tag{13}$$

Using (12) and (13), the line voltage produced by the H-bridges can be modeled as

$$V_{AB}^H = V_A^H - V_B^H = \sqrt{3} \cdot \left(\frac{m_a \cdot V_{\mathrm{AVE}}^{\mathrm{dc}}}{\sqrt{2}} + \frac{I_m \cdot m_a \cdot (m_a + m_b)}{800 \cdot \pi \cdot C}\right) \cdot \sin\left(100 \cdot \pi \cdot t - \frac{\pi}{3}\right). \tag{14}$$

Since the proposed H-bridge motor drive system works on the principle of serial voltage injection, as shown in Figs. 1–2, the actual motor line voltage is the end result between grid line voltage and line voltage produced by H-bridges. Assuming that the grid line voltage is sinusoidal and free of low-order harmonics, (14) shows that if line voltage produced by the H-bridge is also free of low-order harmonics, then the motor line voltage will be free of low-order harmonics as well.

C. Equivalent Modulation Index

By definition, the equivalent modulation index of the H-bridge is the ratio between the injected fundamental ac voltage RMS and the average dc capacitor voltage. Therefore, the following equation holds:

$$m_a + m_b = \frac{\dfrac{m_a \cdot V_{\mathrm{AVE}}^{\mathrm{dc}}}{\sqrt{2}} + \dfrac{I_m \cdot m_a \cdot (m_a + m_b)}{800 \cdot \pi \cdot C}}{\dfrac{V_{\mathrm{AVE}}^{\mathrm{dc}}}{\sqrt{2}}}. = \frac{m_a}{1 - \dfrac{\sqrt{2} \cdot I_m \cdot m_a}{800 \cdot \pi \cdot C \cdot V_{\mathrm{AVE}}^{dc}}} \tag{15}$$

Equation (15) implies that if the dc voltage ripple cannot be neglected, the equivalent modulation index $(m_a + m_b)$ for the H-bridge will be higher than the modulation index of the conventional SVPWM (m_a).

This phenomenon can be explained by the fact that the conventional SVPWM method assumes a constant dc link voltage and manipulates only the width of the pulses over each cycle. For the floating capacitor H-bridge topology with a small dc capacitance value, besides the SVPWM manipulating the width of the pulses, the magnitudes of the pulses are also changed due to the dc ripple (pulse magnitude is reduced at the beginning and the end of each half cycle, pulse magnitude boosted around center region for each half cycle, as can be seen in Fig. 10, Section VI). Thus, the combined factors (width modulation caused by the SVPWM as well as magnitude modulation naturally caused by the dc ripple) sometimes can push the equivalent modulation index $(m_a + m_b)$ above the conventional 1.1547 limit without entering the nonlinear region.

Equation (15) will be used throughout this paper in many ways: It will be combined with (2) to improve the motor voltage control accuracy, as it is shown in Fig. 3. It will be combined with (7) to predict IGBT voltage stress and it will also be combined with (22) to assess the capacitor ripple current magnitude. It should be noted that the equivalent modulation index cannot be amplified infinitely above 1.1547 as there is a theoretical upper limit for it, as will be shown in (21).

D. IGBT Voltage Stress

Since the dc capacitor voltages for the proposed topology are free-floating, the IGBT voltage stress needs to be characterized. Combining (12) with (15) and only considering fundamental component, the following equation can be obtained:

$$\left(V_{\mathrm{AVE}}^{\mathrm{dc}}\right)^2 - \frac{\sqrt{2}\cdot|V_b|}{m_a}\cdot V_{\mathrm{AVE}}^{\mathrm{dc}} + \frac{|V_b|\cdot I_m}{400\cdot\pi\cdot C} = 0. \tag{16}$$

Solving (16) yields

$$V_{\mathrm{AVE}}^{\mathrm{dc}} = \frac{|V_b|}{\sqrt{2}\cdot m_a} + \sqrt{\frac{|V_b|^2}{2\cdot(m_a)^2} - \frac{|V_b|\cdot I_m}{400\cdot\pi\cdot C}}. \tag{17}$$

Meanwhile, from Fig. 2, it can be seen that $|V_b|$ can be expressed as

$$|V_b| = V_m\cdot\sin(\phi_m) + \sqrt{V_g^2 - (V_m\cdot\cos(\phi_m))^2} \tag{18}$$

where ϕ_m represents the motor power factor angle [39]. Suppose that V_g is constant and V_m can be maintained by H-bridges at the rated motor voltage, (17) and (18) show that the average dc capacitor voltage as a function of dc capacitance can be obtained as long as ϕ_m and I_m are known. This is not difficult because ϕ_m and I_m can be deduced from motor nameplate. Upon solving (17), the value of equivalent modulation index of the H-bridge $(m_a + m_b)$ can be deduced (see (15)). Then, the magnitude of the dc capacitor ripple voltage can be obtained [see (7)]. Finally, the peak dc capacitor voltage for the proposed topology will be the average dc capacitor voltage plus one-half of the dc capacitor ripple voltage magnitude as

$$V_{\mathrm{peak}} = V_{\mathrm{AVE}}^{\mathrm{dc}} + \frac{\Delta V}{2}. \tag{19}$$

Equation (19) will be used to predict IGBT voltage stress.

E. Maximum Equivalent Modulation Index

Equation (15) shows the possibility of increasing the equivalent modulation index of the H-bridge over the conventional 1.1547 limit. This section investigates the boundary condition for (15). It can be seen that the boundary condition for (17) is

$$C_{\mathrm{bond}} = \frac{I_m\cdot(m_a)^2}{200\cdot\pi\cdot|V_b|} \quad V_{\mathrm{AVE}}^{\mathrm{dc}} = \frac{|V_b|}{\sqrt{2}\cdot m_a}. \tag{20}$$

Substituting (20) into (15), the boundary condition for $m_a + m_b$ is found to be

$$(m_a + m_b)_{\max} = 2\cdot m_a. \tag{21}$$

Equation (21) is exactly twice of the modulation index if a dc capacitor with infinite capacitance is used [$C = \infty$,$m_a + m_b \approx m_a$ as can be seen from (15)]. This means that although reducing dc capacitance can boost the equivalent modulation index of the H-bridge, in theory, such boost has an upper limit, which is $2.0 \times 1.1547 = 2.3094$. Please note that this value is only a theoretical limit. In practice, due to other constrains, it is not easy to achieve such high value, as will be explained in Section IV G.

F. Capacitor Ripple Current

Due to ESR in the capacitor, the maximum permitted ripple current is set by the manufacturer so that capacitor load life specification will not be compromised. From (7) and (8), the RMS ripple current of the floating capacitor can be derived as

$$\begin{aligned} I_{\mathrm{ripple}} &= \frac{1}{\sqrt{2}}\cdot C\cdot\frac{dV_{\mathrm{A}}^{\mathrm{dc}}}{dt} \\ &= -\frac{I_m\cdot(m_a + m_b)}{2}\cdot\cos\left(200\cdot\pi\cdot t - \frac{\pi}{2}\right). \end{aligned} \tag{22}$$

From (22), it can be seen that capacitor ripple current is oscillating at 100 Hz and it is proportional with the motor current. Taking into account the upper boundary for $m_a + m_b$, as shown in (21), the theoretical maximum ripple current RMS for the capacitor is found to be

$$I_{\mathrm{ripple}}^{\max} = I_m\cdot m_a. \tag{23}$$

Equation (23) is the worst case scenario for capacitor ripple current and in reality, such a value can never be reached. (23) can be used in the design phase to select the dc capacitor with correct current rating.

G. Minimum DC Capacitance in Practice

The previous analysis shows that dc capacitance of the proposed system has a theoretical lower limit [see (20)]. However, in practice, the minimum dc capacitance value will be several times higher than what (20) predicts. This is because in practice, extreme conditions have to be taken into account when selecting the minimum dc capacitance, where I_m reaches its maximum value and magnitude of V_b reaches its minimum value. For I_m to reach its maximum value, this happens during soft-start process, where the motor current is controlled around 3–4 p.u. for the proposed system [20]. For the magnitude of V_b to reach its minimum value, such condition also happens during soft-start process under full load condition [20]. Considering these scenarios, the actual minimum dc capacitance will be k_a times higher than what (20) predicts $(k_a = 3 - 4)$

$$k_a\cdot\frac{I_m^{\mathrm{rated}}\cdot(m_a)^2}{200\cdot\pi\cdot|V_b|^{\mathrm{rated}}} \le C. \tag{24}$$

Substituting (24) into (15), the equivalent modulation index as a function of k_a under full motor load condition is found to be

$$m_a + m_b = \frac{m_a}{1 - \dfrac{1}{2\cdot k_a\cdot\left(1 + \sqrt{1 - \dfrac{1}{k_a}}\right)}}. \tag{25}$$

Equation (25) implies that when $k_a = 1$, $m_{a+}\, m_b = 2m_a$; when $k_a = \infty$, $m_{a+}\, m_b = m_a$. This means the equivalent modulation index of the H-bridge will be in the range of $[m_a, 2m_a]$, depending on the selection of k_a. For example, when $m_a = 1.1$ and $k_a = 3$, $m_{a+}\, m_b = 1.211$; when

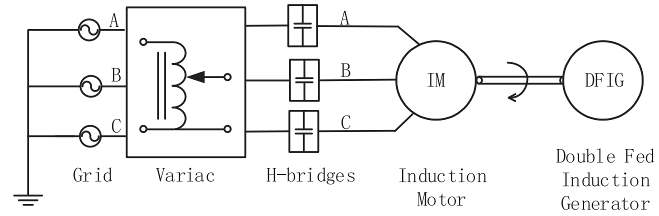


Fig. 5. Test platform schematic.

$m_a = 1.1$ and $k_a = 4$, $m_{a+}\, m_b = 1.179$; when $m_a = 1.1$ and $k_a = 5$, $m_{a+}\, m_b = 1.161$ (see Fig. 12).

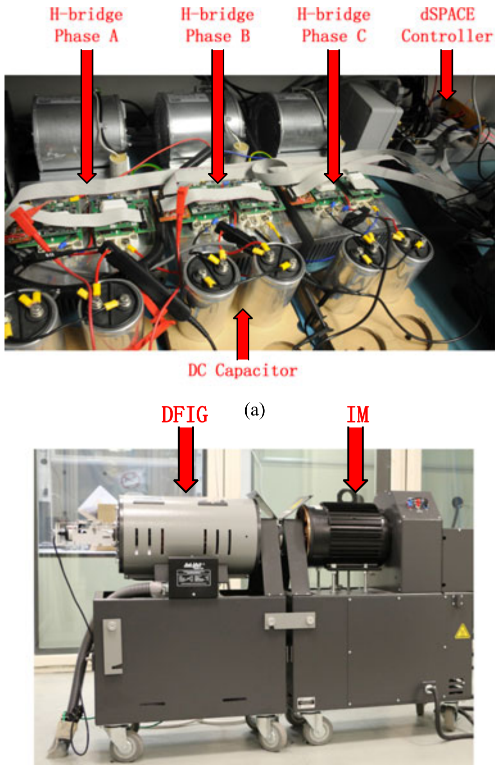
V. EXPERIMENTAL SETUP

A motor–dynamometer set is used as test platform to validate the theory proposed in this paper. The schematic for the test platform is shown in Fig. 5.

From Fig. 5, it can be seen that a variac is used to step down the 415 V 50 Hz grid voltage to 330 V and feed it to the H-bridges. The reason behind such a configuration is to see if under slim dc capacitance condition, the proposed motor drive can still boost motor terminal voltage to its rated value [21] and the answer is positive (see Fig. 18). Three single-phase floating capacitor H-bridges are installed between the variac and the induction motor. A double fed induction generator (DFIG) is mechanically coupled with the induction motor as a dynamometer to achieve a torque load. The actual experimental facility is shown in Fig. 6.

The control algorithm shown in Fig. 3 is implemented in a dSPACE DS1104 platform, with a sampling frequency of 7.5 kHz and a switching frequency of 7.5 kHz. Each H-bridge is made up of two separate inverter legs using Semikron IGBT modules (SEMiX202GB12E4s). In total, six IGBT modules are used (12 IGBT switches). The dc capacitors are metalized polypropylene film capacitors made by EPCOS (B25620-B0407-K881) with a capacitance of 400 μF each and a rated voltage of 880 VDC. In order to investigate the performance of the proposed system under different dc capacitance values, five identical 400 μF capacitors are used in each phase. These capacitors can be connected in series, in parallel or in a mixed configuration (Fig. 6 (a) shows two dc capacitors connected in series, $C = 200\ \mu F$). In this way, the range of equivalent dc capacitance per phase is between 2000 μF to 200 μF, which is equivalent to 33–3.3 p.u. with $V_{\text{base}} = 380\,\text{V}$, $S_{\text{base}} = 2200/0.8 = 2750\,\text{VA}$. The reason for varying dc capacitance from 2000 μF to 200 μF is to see if the proposed topology can operate well under slim dc capacitance condition. If it does, this means instead of expensive, bulky, and unreliable electrolyte capacitor banks, cheaper, small, and reliable MPPF capacitors can be used for the proposed system, which greatly improves its competitiveness over other motor drive topologies.

The motor-dynamometer set shown in Fig. 6 (b) was previously used for wind energy research [40] but modified to accommodate research requirement for this paper. The main change is that the original Mitsubishi VFD is replaced with three H-bridges to drive the induction motor, as is shown in Fig. 5. The induction motor under test is a general purpose 4-pole 3 HP (2.2 kW) 60 Hz motor made by Marathon Electric. The nameplate states that rated voltage for the induction motor is 460 V / 60 Hz with a full load current of 4.2 A. Taking into account the fact that the motor will be operating at a fixed frequency of 50 Hz, the rated motor voltage has been reduced to 380 V to accommodate the V/f characteristics. The DFIG is a 4-pole 2 HP (1.5 kW) machine made by Lab-Volt. Loading of the DFIG is controlled by a dSPACE DS1103 controller so that a constant electromagnetic torque can be provided by the DFIG, independent of the shaft speed.



(a)

(b)

Fig. 6. Experimental facility (a) floating capacitor H-bridges and controller (b) induction motor with dynamometer.

VI. EXPERIMENTAL RESULTS

The performance of the proposed floating capacitor H-bridge motor drive system under the influence of different dc capacitance values will be shown in this section. It should be noted that soft-start results are not provided in this paper mainly because the soft-start control algorithm used in this paper is the same as the one used in [20]. Since [20] had already provided detailed waveforms showing transient state (from no load condition up to full load condition), the commonly known results regarding soft start are not shown in this paper.

A. *H-bridge Output Voltage*

Fig. 7 shows the motor current, the H-bridge output voltage as well as capacitor voltage ripple in phase A under very small dc

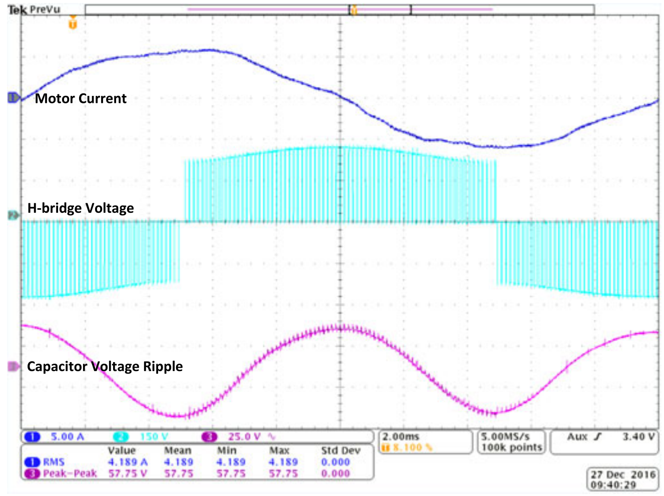


Fig. 7. H-bridge output voltage under very small dc capacitance and full motor load condition.

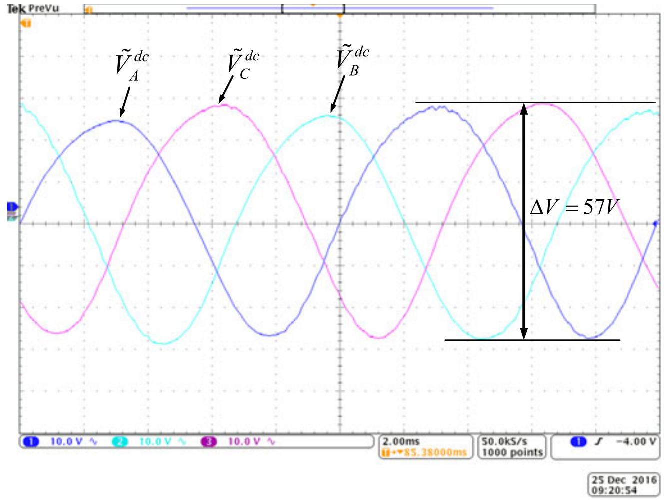


Fig. 8. Capacitor voltage ripples under very small dc capacitance and full motor load condition.

capacitance ($C = 200\ \mu\text{F} = 3.3\,\text{p.u.}$) and full motor load condition ($m_a = 1.1,\ I_m = 4.2\,\text{A} = 1.0\,\text{p.u.}$). It should be noted that in Fig. 7, for the dc capacitor voltage measurement, the dc offset has been filtered out, leaving only the ac component. In this way, the ripple can be more easily seen.

The first observation from Fig. 7 is that there is a hump for each half cycle of the H-bridge output voltage, which is different from what can be obtained from the conventional SVPWM. The dc capacitor voltage ripple is oscillating at 100 Hz, which is twice the grid frequency (50 Hz). It can also be seen that despite a large dc ripple (57.75 V, peak to peak), the motor current remains sinusoidal. In addition, the voltage injected by the H-bridge is about 90 degree lagging the motor current, which means the average energy flowing in/out of the H-bridge per cycle is near zero. This explains why the capacitor voltages for the proposed system only oscillate but they do not collapse or increase to infinity under steady state. Comparing Fig. 7 with Fig. 4, it can be seen that the waveform obtained from the experiment agrees very well with theoretical curves, especially in terms of phase relationship.

B. Capacitor Voltage Ripple

Fig. 8 shows three capacitor voltage ripples under very small dc capacitance ($C = 200\ \mu\text{F} = 3.3\,\text{p.u.}$) and full motor load condition ($m_a = 1.1,\ I_m = 4.2\,\text{A} = 1.0\,\text{p.u.}$).

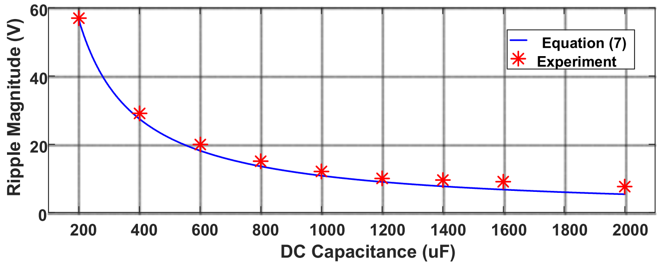


Fig. 9. Ripple magnitude versus dc capacitance under full motor load condition.

According to (7), under the condition shown in Fig. 8 ($C = 200\ \mu\text{F},\ m_a = 1.1,\ I_m = 4.2\,\text{A}$), the magnitude of the voltage ripple (peak to peak) should be 56.9 V. It can be seen from Fig. 8 that actual voltage ripple magnitude is 57 V, which perfectly matches the theory. It is worth noting that despite a large ripple in the individual capacitor voltage (57 V, peak to peak), such second-order ripples are well balanced. This means averaging three dc capacitor voltages can successfully filter out the second-order harmonic component, leaving only dc offset value, which is used in the control block diagram shown in Fig. 3. This explains why the proposed system can remain stable despite large oscillations in the dc link. It can also be observed from Fig. 8 that ripple voltages have a negative sequence. To further prove (7) which describes the ripple magnitude, Fig. 9 is plotted where the magnitude of the dc ripple is recorded under various dc capacitance values. It should be noted that for Fig. 9, the induction motor is always running under full load condition ($m_a = 1.1,\ I_m = 4.2\,\text{A} = 1.0\,\text{p.u.}$).

From Fig. 9, it can be seen that the experimental results match the theory very well. Generally, the smaller the dc capacitance, the larger the ripple magnitude.

C. Third Harmonic Injection

In order to analyze the frequency spectrum, Fig. 10 is plotted where fast Fourier transform (FFT) is performed for the H-bridge output voltage. The actual dc capacitor voltage and H-bridge output voltage are superimposed in Fig. 10. It clearly explains that the hump for each half cycle of the H-bridge output voltage is indeed caused by the oscillating dc capacitor voltage.

Equation (12) shows that due to the dc ripple, besides the fundamental component, only third harmonic component will be introduced to the H-bridge output voltage. This is confirmed in Fig. 10. It shows that besides the fundamental component (175 V), only the third harmonic component is present (22 V). In fact, according to (12), under the conditions shown in

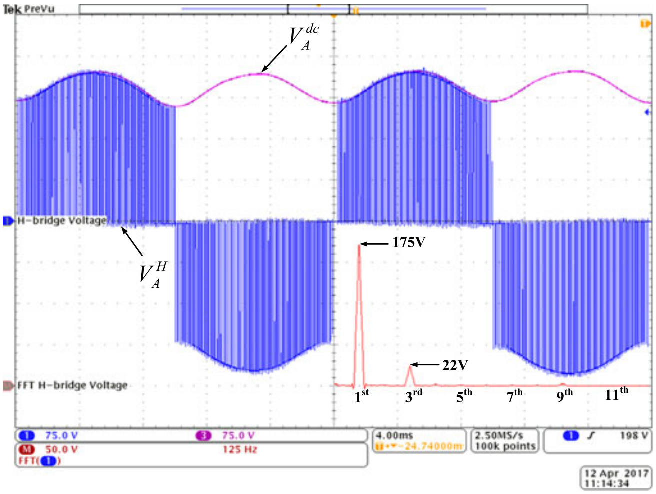


Fig. 10. FFT analysis for H-bridge output voltage under very small dc capacitance and full motor load condition.

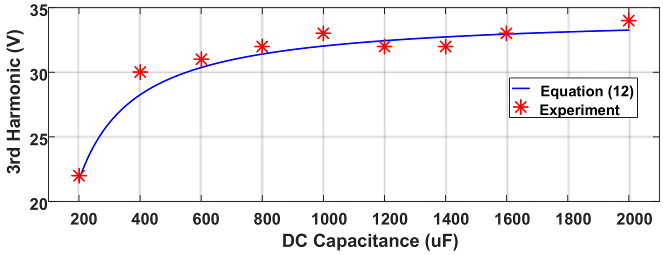


Fig. 11. Third harmonic magnitude versus dc capacitance under full motor load condition.

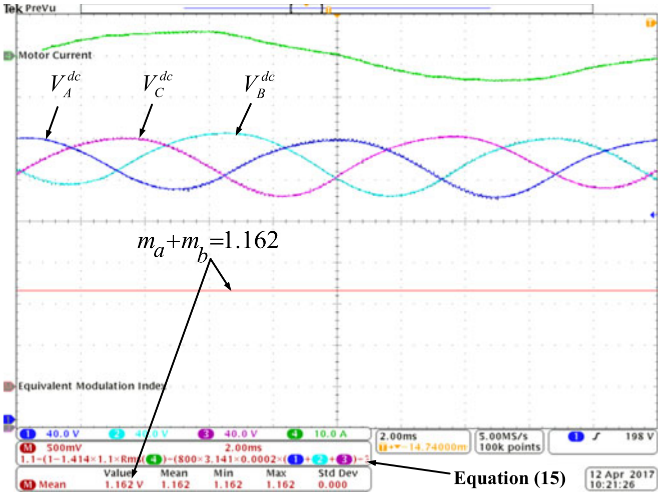


Fig. 12. Equivalent modulation index under very small dc capacitance and full motor load condition.

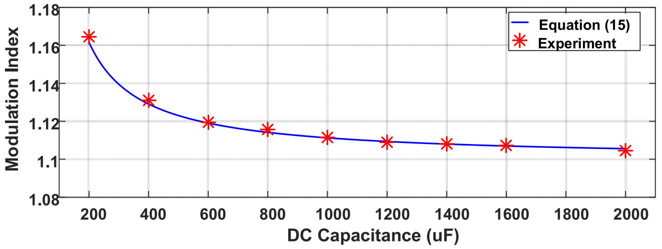


Fig. 13. Equivalent modulation index versus dc capacitance under full motor load condition.

Fig. 10 ($C = 200\ \mu$F, $m_a = 1.1$, $I_m = 4.2$ A), the magnitude of the third harmonic should be around 22 V, which perfectly matches the experimental result. To further prove (12) describing the third harmonic injection, Fig. 11 shows the magnitude of the third harmonic component under various dc capacitance values. It should be noted that for Fig. 11, the induction motor is always running under full load condition ($m_a = 1.1$, $I_m = 4.2\,\text{A} = 1.0\,\text{p.u.}$).

From Fig. 11, it can be seen that the experimental results match theory. Fig. 11 proves that the third harmonic component created by dc ripple voltage will cancel part of the third harmonic component generated by the SVPWM, causing the overall third harmonic component to dip under small dc capacitance regions.

D. Equivalent Modulation Index

According to (15), by measuring three dc capacitor voltages and motor current RMS, it is sufficient to estimate the equivalent modulation index for the H-bridge. Fig. 12 shows equivalent modulation index obtained from this method under very small dc capacitance ($C = 200\ \mu\text{F} = 3.3\,\text{p.u.}$) and full motor load condition ($m_a = 1.1$, $I_m = 4.2\,\text{A} = 1.0\,\text{p.u.}$).

It is interesting to point out that the equivalent modulation index ($m_a + m_b = 1.162$) has exceeded the upper limit of 1.1547 for the conventional SVPWM, as can be seen from Fig. 12. It is also worth noting that such a value agrees very well with theory, as is shown at the end of Section IV G. In the meanwhile, the dc /ac inversion is still in the linear region and the ac voltage injected by the H-bridge only contains the fundamental and third harmonic, as shown in Fig. 10. It is also worth noting that the conventional SVPWM increases the modulation index at the expense of more third harmonic injection. In contrast, modulation index boost caused by dc ripple voltage will cancel part of the third harmonic component generated by the SVPWM, causing overall third harmonic injection to dip under small dc capacitance regions, as shown in Fig. 11.

Fig. 13 is plotted to further prove (15) describing the modulation index boost of the H-bridge under ripple voltage condition. For Fig. 13, the induction motor is always running under full load condition ($m_a = 1.1$, $I_m = 4.2\,\text{A} = 1.0\,\text{p.u.}$).

From Fig. 13, it can be seen that the equivalent modulation index for the H-bridge is always higher than the conventional modulation index used in the SVPWM. For example, m_a is fixed at 1.1 for the SVPWM used in this paper. However, through experiments, it is found that $m_a + m_b$ is always higher than 1.1. The additional boost is caused by the second-order dc ripple voltage, as described in (15).

E. Motor Line Voltage

Fig. 14 shows an FFT analysis for motor line voltage under very small dc capacitance ($C = 200\ \mu\text{F} = 3.3\,\text{p.u.}$) and full motor load condition ($m_a = 1.1$, $I_m = 4.2\,\text{A} = 1.0\,\text{p.u.}$).

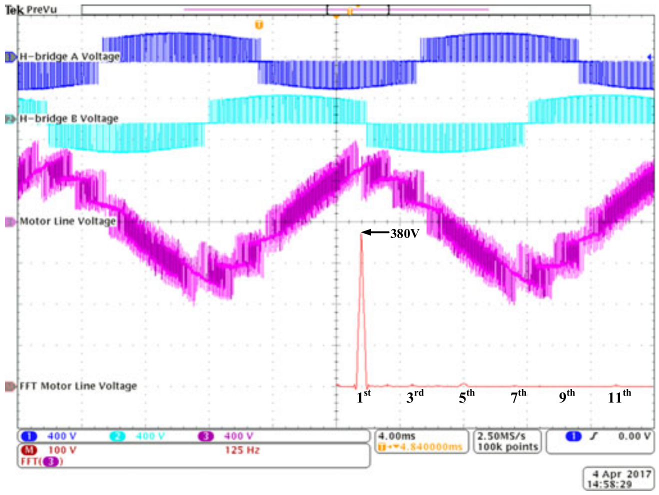


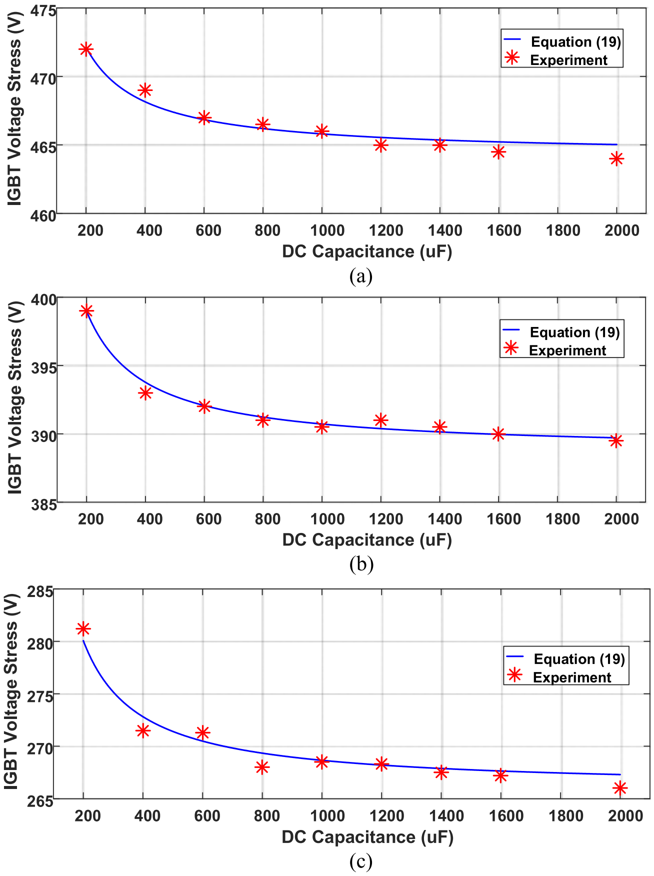
Fig. 14. FFT analysis for motor line voltage under very small dc capacitance and full motor load condition.

The proposed floating capacitor H-bridge motor drive system works on the principle of serial voltage injection. Therefore, the motor line voltage results from grid line voltage (not shown in Fig. 14) and line voltage produced by H-bridges. It can be seen that the third harmonic no longer exist in motor line voltage, leaving only fundamental component, which agrees well with (14). From Fig. 14, it can be seen that the proposed system can supply five-level line PWM waveforms to the induction motor. In contrast, a VFD system supplies induction motor with three-level line PWM waveforms and a much larger voltage step. This is one of the disadvantages for VFD because the higher voltage step introduces higher dV/dt stresses on the insulation of the motor windings. Moreover, the three-level line PWM output voltages from the VFD, using a higher dc link voltage, usually requires bulky 3%/5% reactors inserted between VFD and motor to mitigate the reflected wave or standing wave phenomenon. However, such practice affects the ability of the induction motor to produce rated torque due to voltage drops. In contrast, the proposed floating capacitor H-bridge motor drive does not require such reactors (see Fig. 1). Note that replacing iron with silicon is often considered advantageous.

F. IGBT Voltage Stress

Fig. 15 shows IGBT voltage stress (peak dc capacitor voltage) under various dc capacitance and various motor load conditions.

From Fig. 15, it can be seen that the experimental results match theoretical predictions well. Generally, the bigger the dc capacitance, the lower the IGBT voltage stress. Also, it can be observed from Fig. 15 that generally the higher motor load condition, the lower the IGBT voltage stress. This is because the size of V_b is a function of motor power factor angle ϕ_m [see (18)]. Under heavy motor load condition, the stator power factor of induction motor is usually high [39], which yields a low ϕ_m angle, which puts less demand on the dc capacitor voltage. In contrast, under light motor load condition, the stator power factor of induction motor is usually low [39], which yields a high ϕ_m angle, which puts more demand on the dc capacitor voltage.



(a)

(b)

(c)

Fig. 15. IGBT voltage stress versus dc capacitance under different motor load conditions: (a) quarter motor load $(m_a = 1.1,\ I_m = 2.55\,\mathrm{A},\ \phi_m = 63.85^\circ)$ (b) half motor load $(m_a = 1.1,\ I_m = 3.23\,\mathrm{A},\ \phi_m = 51.1^\circ)$ (c) full motor load $(m_a = 1.1,\ I_m = 4.2\,\mathrm{A},\ \phi_m = 37^\circ)$.

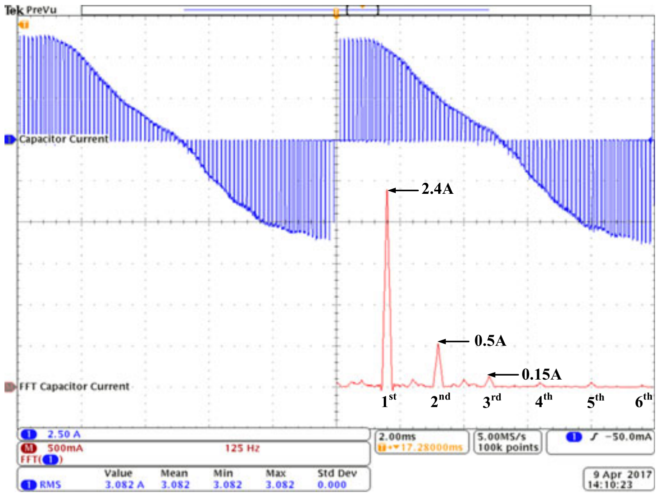


Fig. 16. FFT analysis for capacitor current under full motor load condition.

G. Capacitor Current

Fig. 16 shows an FFT analysis for capacitor current under very small dc capacitance $(C = 200\ \mu\mathrm{F} = 3.3\,\mathrm{p.u.})$ and full

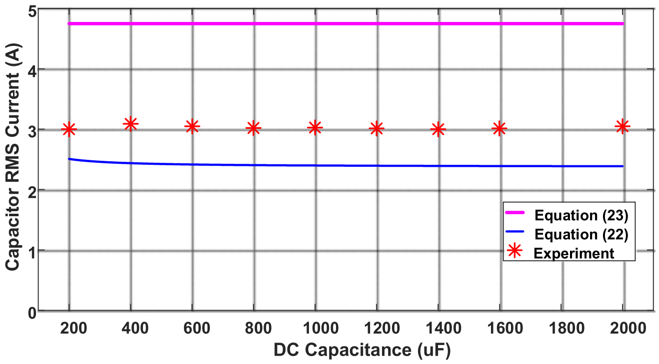


Fig. 17. RMS Capacitor current versus dc capacitance under full motor load condition.

motor load condition ($m_a = 1.1,\ I_m = 4.2\,\text{A} = 1.0\,\text{p.u.}$). Fig. 16 shows that the capacitor current is oscillating at 100 Hz, which agrees with (22). It can also be seen from Fig. 16 that the magnitude of the fundamental component (100 Hz) is 2.4 A, while (22) predicts this value to be 2.44 A, which is a good match. However, the RMS value of the capacitor current is 3.08 A, which is 25% higher than what (22) had predicted. The explanation for such deviation is that (22) is a rough approximation of capacitor current. From Fig. 16, it can be seen that there are other harmonic components (second, third) that cannot be captured by (22), which causes the actual RMS capacitor current to be higher than what (22) had predicted.

Fig. 17 is plotted where the RMS capacitor ripple current is recorded under various dc capacitance values. It should be noted that for Fig. 17, the induction motor is always running under full load condition ($m_a = 1.1,\ I_m = 4.2\,\text{A} = 1.0\,\text{p.u.}$).

From Fig. 17, it can be seen that the RMS capacitor current value remains almost flat despite large dc capacitance variation. The actual experiment value is always 25% higher than what (22) had predicted, but stays below the theoretical maximum value shown by (23). It should be noted that oversizing is commonly practiced in engineering and Fig. 17 proves that (23) can be used to select the capacitor current rating during design phase.

H. DC Ripple Effect Compensation

Due to the second order dc voltage ripple, instead of constant modulation index, the equivalent modulation index for the H-bridge is boosted (see Fig. 13). Such phenomenon will be taken into account in the control algorithm so that a more accurate motor voltage control can be achieved, as it is shown in Fig. 18. It should be noted that for Fig. 18, the induction motor is always running under full load condition ($m_a = 1.1,\ I_m = 4.2\,\text{A} = 1.0\,\text{p.u.}$) with its reference value fixed at 380 V ($|V_m^*| = 380\,\text{V} = 1.0\,\text{p.u.}$, see Fig. 3).

It can be seen from Fig. 18 that generally, with ripple effect compensation, a better motor terminal voltage control can be achieved. When the dc capacitance is relatively large, the difference between the two control schemes is small. This is because the modulation index boost can be neglected under relatively large dc capacitance conditions [see (15)]. However, as the dc capacitance value gets smaller, the previously proposed control scheme [19]–[21] begins to lose accuracy, while the advantage of taking the ripple effect into account becomes obvious.

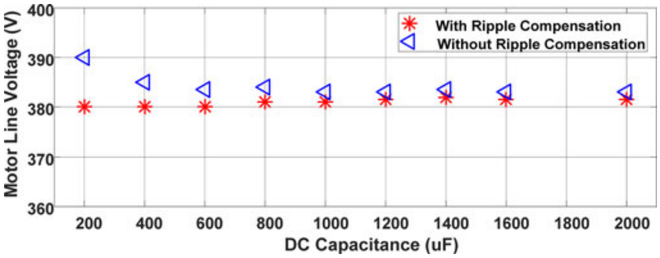


Fig. 18. Motor line voltage versus dc capacitance under full motor load condition.

I. Minimum DC Capacitance

According to (20), the theoretical minimum dc capacitance for the proposed system is 40 μF, where $I_m = 4.2\,\text{A}$, $m_a = 1.1$, $V_g = 330\,\text{V}$, $V_m = 380\,\text{V}$, $\phi_m = 37^\circ$, $V_b = 206.8\,\text{V}$ [see (18)]. In practice, according to (24), the minimum dc capacitance for the proposed H-bridge motor drive is k_a ($k_a = 3$–4) times higher than 40 μF, between 120 and 160 μF. Through experiments, it is found that when connecting three 400 μF capacitors in series ($C = 133\ \mu$F, $k_a = 3.325$), the proposed system can barely soft start and reach steady state condition. However, when connecting four 400 μF capacitors in series ($C = 100\ \mu$F, $k_a = 2.5$), the proposed system begins to oscillate and is never able to reach steady state. This proves that (24) can be used to roughly estimate the minimum dc capacitance during the design phase. For engineering practice, some margins are usually required, which is the reason that $C = 200\ \mu$F, $k_a = 5$ was chosen as the minimum dc capacitance value in this paper (see (25) and Fig. 12).

J. Power Loss Difference Due to ESR Variation

For an MPPF capacitor, its ESR is significantly smaller than that of an electrolyte capacitor, which is one of its advantages. The dc capacitors used in this paper are MPPF Capacitors made by EPCOS (B25620-B0407-K881) with a capacitance of 400 μF and ESR of 3.8 mΩ and a tolerance of 10%. The worst case scenario for power loss difference between phases is that under full motor load condition ($m_a = 1.1,\ I_m = 4.2\,\text{A} = 1.0\,\text{p.u.}$), the ESR of one phase is 20% higher than that of other phases. This will cause maximum power loss difference between phases, as shown in Fig. 19.

From Fig. 19, it can be seen that under the worst case scenario, the power loss difference between phases is in the range of 3.24 to 32.4 mW, which is almost negligible compared with maximum allowable ESR power loss of 7695 mW for this type of film capacitor. Therefore, it can be concluded that the way to handle ESR variation between different capacitors can be done by the following three means:

a) Use an MPPF capacitor instead of an electrolyte capacitor.
b) Choose MPPF capacitors that have relatively small tolerance in terms of capacitance.

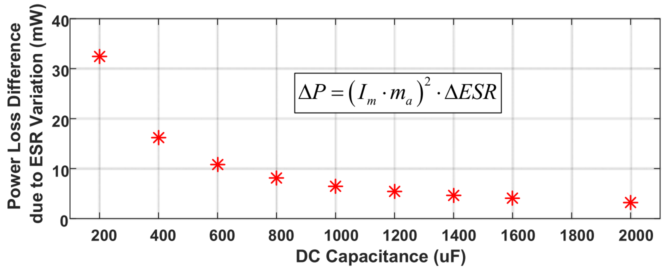


Fig. 19. Power loss difference due to ESR variation under full motor load condition.

c) Tight quality control during the manufacturing stage so that individual capacitor ESR variation can be compensated by a combination of different capacitors into equal capacitor banks.

VII. CONCLUSION

This paper examines the possibility of implementing slim dc capacitance on an induction motor drive under balanced grid voltage condition. Using rigorous mathematical formulations supported by hardware experiments, it is found that the second-order dc ripple voltage does not cause problematic low-order harmonics in motor line voltage. In fact, allowing the second-order dc ripple voltage to fluctuate can boost equivalent modulation index of the H-bridge to be higher than that of the conventional SVPWM. As a result, the theoretical boundary condition for the modulation index can be extended from 1.1547 to 2.3094, depending on the selection of the dc capacitance value. Accordingly, the motor terminal voltage control algorithm has been improved to take such a phenomenon into account. Interestingly, allowing the second-order dc ripple voltage to fluctuate will also generate an opposing third harmonic voltage to the one injected by the SVPWM. In addition, the worst case scenario for capacitor RMS current and IGBT voltage stress can be accurately predicted and the lower limit for dc capacitance suitable for engineering practice can also be quantified. Based on the above discoveries, it can be concluded that the proposed floating capacitor H-bridge motor drive can operate under slim dc capacitance condition. This means expensive, bulky, and unreliable electrolyte capacitor banks can be replaced with cheaper, small, and reliable MPPF capacitors, which greatly improves the competiveness of the proposed motor drive topology.

ACKNOWLEDGMENT

The authors would like to thank the Khalifa University of Science and Technology for use of the facilities.

REFERENCES

[1] R. F. McElveen and M. K. Toney, “Starting high-inertia loads,” *IEEE Trans. Ind. Appl.*, vol. 37, no. 1, pp. 137–144, Jan./Feb. 2001.

[2] J. C. Gomez and M. M. Morcos, “Voltage sag effects on sensitive equipment due to starting cycles of induction motor,” *IEEE Power Eng. Rev.*, vol. 22, no. 8, pp. 51–52, Aug. 2002.

[3] P. Waide and C. U. Brunner, “Energy-efficiency policy opportunities for electric motor-driven systems,” Int. Energy Agency, 2011 Working Pap. Energy Efficiency Ser., Paper OECD/IEA 201.1.

[4] I. Boldea and S. Nasar, *The Induction Machine Handbook*. Boca Raton, FL, USA: CRC Press, 2001.

[5] F. Blaabjerg, J. K. Pedersen, S. Rise, H.-H. Hansen, and A. M. Trzynadlowski, “Can soft-starters help save energy?,” *IEEE Ind. Appl. Mag,*, vol. 3, no. 5, pp. 56–66, Sep./Oct. 1997.

[6] P. Zhang, Y. Du, B. Lu, and T. G. Habetler, “A DC signal injection-based thermal protection scheme for soft-starter-connected induction motors,” *IEEE Trans. Ind. Appl.*, vol. 45, no. 4, pp. 1351–1358, Jul./Aug. 2009.

[7] K. LeDoux, P. W. Visser, J. D. Hulin, and H. Nguyen, “Starting large synchronous motors in weak power systems,” *IEEE Trans. Ind. Appl.*, vol. 51, no. 3, pp. 2676–2682, May/Jun. 2015.

[8] G. Seggewiss, J. Dai, and M. Fanslow, “Synchronous motors on grinding mills: The different excitation types and resulting performance characteristics with VFD control for new or retrofit installations,” *IEEE Ind. Appl. Mag*, vol. 21, no. 6, pp. 60–67, Nov./Dec. 2015.

[9] T. Isobe *et al.*, “Control of series compensated induction motor using magnetic energy recovery switch,” in *Proc. Eur..Conf. Power Electron. Appl.*, 2007, pp. 1–10.

[10] T. Isobe, F. D. Wijaya, K. Inoue, K. Usuki, T. Kitahara, and R. Shimada, “Improved performance of induction motor using magnetic energy recovery switch,” in *Proc. Power Convers. Conf.*, Nagoya, Japan, 2007, pp. 919–924.

[11] F. D. Wijaya, S. A. Kusumawan, and H. Prabowo, “Reducing induction motor starting current using magnetic energy recovery switch (MERS),” in *Proc. 6th Int. Conf. Inf. Technol. Elect. Eng.*, Oct. 7–8, 2014, pp. 1–6.

[12] J. A. Wiik, F. D. Wijaya, and R. Shimada, “Characteristics of the magnetic energy recovery switch (MERS) as a series facts controller,” *IEEE Trans. Power Del.*, vol. 24, no. 2, pp. 828–836, Apr. 2009.

[13] J. A. Wiik *et al.*, “Feasible series compensation applications using magnetic energy recovery switch (MERS),” in *Proc. Eur..Conf. Power Electron. Appl.*, 2007, pp. 1–9.

[14] C. F. DeSieno and B. J. Beaudoin, “A guide to the application of capacitors without induction motor self-excitation,” *IEEE Trans. Power App. Syst.*, vol. 84, no. 1, pp. 8–15, Jan. 1965.

[15] D. D. Robb and P. C. Krause, “The self-excitation of induction machines with application to motor starting,” *IEEE Trans. Power App. Syst.*, vol. PAS-90, no. 2, pp. 579–586, Mar. 1971.

[16] R. Subramanian and C. Chellamuthu, “A fast method of braking of induction motor by self-excitation,” *IEEE Trans. Energy Convers.*, vol. 7, no. 2, pp. 315–321, Jun. 1992.

[17] M. Ermis, Z. Cakir, I. Cadirci, G. Zenginobuz, and H. Tezcan, “Self-excitation of induction motors compensated by permanently connected capacitors and recommendations for IEEE std 141-1993,” *IEEE Trans. Ind. Appl.*, vol. 39, no. 2, pp. 313–324, Mar./Apr. 2003.

[18] S. Leng, R. Ul Haque, N. Perera, A. Knight, and J. Salmon, “Voltage control of grid connected induction motors using floating capacitor H-bridge converters,” in *Proc.7th IET Int. Conf. Power Electron., Mach. Drives*, Manchester, U.K., Apr. 2014, pp. 1–6.

[19] S. Leng, R. U. Haque, N. Perera, J. Salmon, and A. Knight, “Soft start and voltage control of grid connected induction motors using floating capacitor H-bridge converters,” in *Proc. IEEE Energy Convers. Congr. Expo.*, Sep. 14–18, 2014, pp. 1309–1316.

[20] S. Leng, R. Ul. Haque, N. Perera, A. Knight, and J. Salmon, “Soft start and voltage control of induction motors using floating capacitor H-bridge converters,” *IEEE Trans. Ind. Appl.*,vol. 52, no. 4, pp 3115–3123, Mar. 2016.

[21] S. Leng, R. Haque, N. Perera, A. Knight, and J. Salmon. “Smart grid connection of an Induction motor using a three-phase floating H-bridge system as a series compensator,” *IEEE Trans. Power Electron.*, vol. 31, no. 10, pp. 7053–7064, Dec. 2015.

[22] H. Wang and F. Blaabjerg, “Reliability of capacitors for DC-link applications in power electronic converters—An overview” *IEEE Trans. Ind. Appl.*, vol. 50, no. 5, pp. 3569–3578, Feb. 2014.

[23] S. Yang, A. Bryant, P. Mawby, D. Xiang, L. Ran, and P. Tavner, “An industry-based survey of reliability in power electronic converters,” *IEEE Trans. Ind. Appl.*, vol. 47, no. 3, pp. 1441–1451, May/Jun. 2011.

[24] H. Wang, M. Liserre, and F. Blaabjerg, “Toward reliable power electronics—Challenges, design tools and opportunities,” *IEEE Ind. Electron. Mag.*, vol. 7, no. 2, pp. 17–26, Jun. 2013.

[25] A. G. Abo-Khalil and D. C. Lee, “DC-link capacitance estimation in AC/DC/AC PWM converters using voltage injection,” *IEEE Trans. Ind. Appl.*, vol. 44, no. 5, pp. 1631–1637, Sep./Oct. 2008.

[26] J. W. Kolar *et al.*, “PWM converter power density barriers,” in *Proc. Power Convers. Conf.*, Nagoya, Japan, Apr. 2–5, 2007, pp. 9–29.

[27] G. Farivar, C. Townsend, B. Hredzak, J. Pou, and V. Agelidis, “A low capacitance cascaded H-bridge multilevel statcom,” *IEEE Trans. Power Electron.*, vol. 32, no. 3, pp. 1744–1754, Mar. 2017.

[28] J. I. Leon, S. Vazquez, A. J. Watson, L. G. Franquelo, P. W. Wheeler, and J. M. Carrasco, “Feed-forward space vector modulation for single-phase multilevel cascaded converters with any DC voltage ratio,” *IEEE Trans. Ind. Electron.*, vol. 56, no. 2, pp. 315–325, Feb. 2009.

[29] J. Vodden, P. Wheeler, L. G. Franquelo, J. I. Leon, and S. Vazquez, “One dimensional feed-forward modulation of a cascaded H-bridge multilevel converter including capacitor balancing with reduced switching frequency,” in *Proc. Eur.. Conf. Power Electron. Appl.*, 2011, pp. 1–10.

[30] H. Wen, W. Xiao, X. Wen, and P. Armstrong, “Analysis and evaluation of DC-link capacitors for high-power-density electric vehicle drive systems,” *IEEE Trans. Veh. Technol.*, vol. 61, no. 7, pp. 2950–2964, Sep. 2012.

[31] B. Karanayil, V.G. Agelidis, and J. Pou, “Evaluation of dc-link decoupling using electrolytic or polypropylene film capacitors in three-phase grid-connected photovoltaic inverters,” in *Proc. 39th Annu. Conf. IEEE Ind. Electron. Soc.*, Nov. 10–13, 2013, pp. 6980–6986.

[32] H.R. Andersen, R. Tan, and C. Kun, “3-phase AC-drives with passive front-ends with focus on the slim DC-link topology,” in *Proc. IEEE Power Elect. Specialists Confe.*, Jun. 10–13, 2008, pp. 3248–3254.

[33] R. Maheshwari, S. Munk-Nielsen, and S. Busquest-Monge, “Design of neutral-point voltage controller of a three-level NPC inverter with small dc-link capacitors,” *IEEE Trans. Ind. Electron.*, vol. 60, no. 5, pp. 1861–1871, May 2013.

[34] F. G. King, “A three phase transistor class-B inverter with sinewave output and high efficiency,” in *Proc. IEE Conf.*, 1974, vol. 123, pp. 204–209.

[35] L. J. Garces, “Current control of field oriented ac induction motordrives,” in *Proc. IEEE Tutorial: Mircoprocessor Control Motor Drives Power Converters*, Toronto, ON, Canada, 1993.

[36] S. L. Capitaneanu, B. de Fornel, M. Fadel, J. Faucher, and A. Almeida, “Graphical and algebraic synthesis for PWM methods,” *Eur. Power Electron. Drives J.*, vol. 11, no. 3, pp. 16–28, Aug. 2001.

[37] B. Wu, *High-Power Converters and AC Drives*Hoboken, NJ, USA: Wiley, Mar. 2006, Ch. 7.

[38] D. G. Holmes, “The significance of zero space vector placement for carrier-based PWM schemes,” *IEEE Trans. Ind. Appl.*, vol. 32, no. 5, pp. 1122–1129, Sep./Oct. 1996.

[39] A. Ukil, R. Bloch, and A. Andenna, “Estimation of induction motor operating power factor from measured current and manufacturer data,” *IEEE Trans. Energy Convers.*, vol. 26, no. 2, pp. 669–706, Jun. 2011.

[40] R. Errouissi, A. Al-Durra, S. M. Muyeen, S. Leng, and F. Blaabjerg, “Offset-free direct power control of DFIG under continuous-time model predictive control,” *IEEE Trans. Power Electron.*, vol. 32, no. 3, pp. 2265–2277, Mar. 2017.

Siyu Leng (S’09–M’14) received the B.Sc. degree in automation engineering from Tongji University, Shanghai, China, in 2006 and the Ph.D. degree in mechanical engineering from Florida State University, Tallahassee, FL, USA, in 2012. He was granted a full scholarship from the Florida State University to study in the U.S.A.

During the Ph.D. study, he joined the Center for Advanced Power Systems (CAPS) as a Graduate Research Assistant under the supervision of Prof. David A. Cartes. His research at CAPS was focused on power quality, especially active power filters. After receiving the Ph.D. degree in 2012, he went back to China to work as a Research Engineer at the State Grid Electric Power Research Institute. From May 2013, he has been working as a Postdoctoral Fellow at the University of Alberta under the supervision of Prof. John Salmon. His research at University of Alberta is focused on power electronics, especially induction motor drives. He joined Petroleum Institute as a Research/Teaching Associate in October 2014. His research interests include renewable energy, power electronics, motor drive, power quality, and power system analysis.

S. M. Muyeen (S’03–M’08–SM’12) received the B.Sc.Eng. degree from Rajshahi University of Engineering and Technology, Rajshahi, Bangladesh, formerly known as Rajshahi Institute of Technology, in 2000, and the M.Eng. and Ph.D. degrees from Kitami Institute of Technology, Kitami, Japan, in 2005 and 2008, respectively, all in electrical and electronic engineering.

He is currently working as an Associate Professor in the Department of Electrical and Computer Engineering, Curtin University, Perth, Australia. He has been a Keynote Speaker and an Invited Speaker at many international conferences, workshops, and universities. He has published more than 150 articles in different journals and international conferences. He has published five books as an author or editor. His research interests include power system stability and control, electrical machine, FACTS, energy storage system, renewable energy, and HVdc system.

Dr. Muyeen is a Fellow of Engineers Australia.

Ahmed Al-Durra (S’07–M’10–SM’14) received the B.S., M.S., and Ph.D. degrees in electrical and computer engineering from the Ohio State University (OSU), Columbus, OH, USA, in 2005, 2007, and 2010, respectively.

He conducted his PhD research at the Center for Automotive Research in OSU on the applications of modern estimation and control theories to automotive propulsion systems. He joined the Electrical Engineering Department, Petroleum Institute, Abu Dhabi, UAE, as an Assistant Professor in 2010. At present, he is an Associate Professor in the Electrical & Computer Engineering Department, Khalifa University of Science & Technology, PI Campus, Abu Dhabi, UAE. He has published more than 100 scientific articles in journals, international conferences, and book chapters. He has successfully accomplished several research projects at international and national levels. He has supervised/cosupervised over 20 Ph.D./Master students. His research interests include application of estimation and control theory in power system stability, micro and smart grids, renewable energy, and process control.

Mr. Al-Durra obtained the PI Research & Scholarship Award for Junior Faculty in 2014. He is the head of Energy Systems, Control & Optimization Lab , ADNOC Research & Innovation Center.

Frede Blaabjerg (S’86–M’88–SM’97–F’03) was working toward the Ph.D. degree in energy technology from Aalborg University, Aalborg, Denmark, from 1988 to 1992.

He was with ABB-Scandia, Randers, Denmark, from 1987 to 1988. He became an Assistant Professor in 1992, Associate Professor in 1996, and Full Professor of power electronics and drives in 1998. His current research interests include power electronics and its applications such as in wind turbines, PV systems, reliability, harmonics, and adjustable speed drives.

Mr. Blaabjerg has received 17 IEEE Prize Paper Awards, the IEEE PELS Distinguished Service Award in 2009, the EPE-PEMC Council Award in 2010, the IEEE William E. Newell Power Electronics Award 2014, and the Villum Kann Rasmussen Research Award 2014. He was an Editor-in-Chief of the IEEE TRANSACTIONS ON POWER ELECTRONICS from 2006 to 2012. He was nominated in 2014 and 2015 by Thomson Reuters to be between the most 250 cited researchers in engineering in the world.