Hybrid Nonisolated DC–DC Converters Derived From a Passive Switched-Capacitor Cell

Mauricio Dalla Vecchia, Marcos Antônio Salvador, and Telles Brunelli Lazzarin, *Member, IEEE*

***Abstract*—This paper presents a hybrid nonisolated dc–dc commutation cell, which is generated by the integration between conventional commutation cell and ladder-type passive switched capacitor (SC) cell. From the resulted hybrid cell are derived three different dc–dc converters: a buck-type, a boost-type, and a buck–boost-type. The three structures are analyzed in this paper and are presented the topological stages, static gain characteristics in continuous conduction mode and discontinuous conduction mode, steady-state analysis. The analyses are generalized in relation to the number of switched-capacitor cells employed, which allows the increase of the rated gain of the converters by adding more SC cells. In addition, the proposed hybrid nonisolated dc–dc commutation divides naturally the voltage stress among the semiconductors and capacitors of the power stage. A 1-kW prototype was developed to verify the operation of the three proposed converters and their theoretical analysis. For the buck-type topology, designed with an input voltage of 600 V and output voltage of 450 V, a peak efficiency of 99.2% and efficiency at rated power of 99% were obtained.**

***Index Terms*—Hybrid dc–dc commutation cell, nonisolated dc–dc converters, switched capacitor.**

I. Introduction

In RECENT years, considerable effort has been directed toward research in the fields of smart grids, microgrids, distributed power generation, renewable energy sources, electric vehicles, energy storage, and other related areas. All of these applications employ dc–dc converters and some of them use high-rated conversions. This scenario has created the need for new solutions for dc–dc converters that provide improvements in relation to gain and voltage stress. Different strategies have been used in this regard, such as, switched capacitor (SC) [1]–[7], switched inductor (SI) [8], couple inductor [9], multistage inductor cells, stack structure, series-connection of converters [10], and multilevel converters [11].

The switched-capacitor principle represents an attractive solution for dc–dc converters, mainly when higher voltage gain rates are desirable [12]–[14]. Initially, SC circuits were applied to low power systems (some milliwatt) [15]–[16]. However, with the evolution of power electronics in terms of component capability, this principle has been applied to higher powers (some kilowatt).

SC topologies are voltage multipliers or dividers and they usually operate in open loop, because the output voltage regulation remains a challenge. However, the SC can be integrated into conventional converters and the structures generated can maintain the characteristics of both topologies, such as multiplication and good regulation. Hence, the integration of SC topologies with conventional converters can provide new solutions that offer high-voltage gain rates and reduced voltage stress on the components (multilevel topologies) without causing significant changes in the shape of the static characteristic or in the dynamic models in relation to conventional dc–dc converters. Based on these advantages, the SC has also been applied in other areas such as inverters [17]–[20], rectifiers [21]–[22], and single- [23] and three-phase [24]–[25] ac–ac autotransformers.

Converters can be studied based on switching cells. This methodology analysis the switching cell and, thus, the converters generated from it are obtained. Following this approach, a hybrid dc–dc commutation cell that integrates the passive SC cell and the conventional commutation cell is proposed herein and, thus, three types of converters are derived from it, being one buck, one boost and one buck–boost. The commutation cell is referred to as a "hybrid cell" and the structures are referred to as "hybrid converters." These topologies improve the rated gain of the respective conventional converters, divide naturally the voltage stress among the semiconductors and capacitors of the power stage (no capacitors voltages balance control are need), and they can provide higher efficiencies.

Some relationships between two of the derived converters in this paper and the literature can be identified, as such as the case of the boost-type that coincide with the dc–dc multilevel boost [26]–[27]. Referring to the buck-type derived converter, some structural similarity can be verified with the three-level buck converters [28]–[30], for example, they have a common purpose in reducing the voltage stresses on the switches and in both topologies the distribution of voltage stresses on components are similar. However, they have different operating principles and static gain, since they have different voltages range at the input of the inductor buck. Furthermore, there are other differences from the point of view of implementation, as such as number of controlled switches and consequently different modulators should be applied. In relation to the buck–boost topology, it was not found similarity with others topologies.

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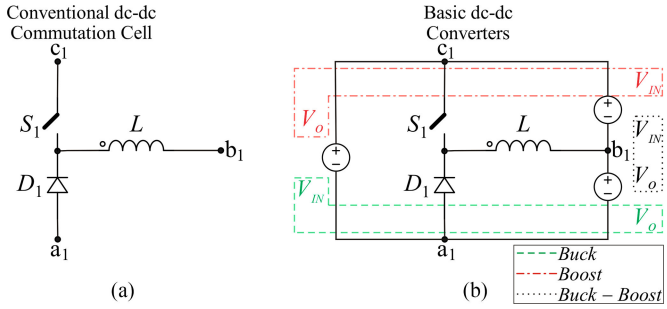

Fig. 1. (a) Basic dc–dc commutation cell and (b) basic dc–dc converters (buck, boost, and buck–boost) generated from the basic dc–dc commutation cell.

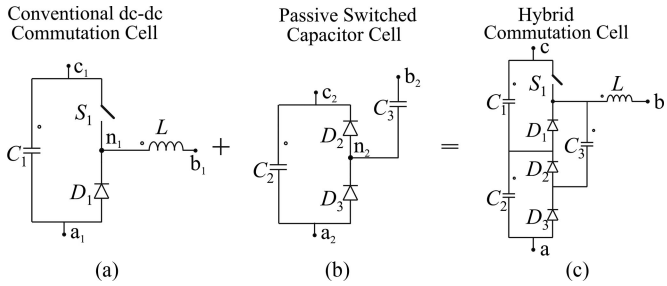

Fig. 2. (a) Conventional dc–dc commutation cell, (b) passive switched-capacitor cell, and (c) hybrid commutation cell proposed in this paper.

The three derived converters are investigated in this study by the theoretical analysis, generalization, steady-state analysis, prototype, and experimental results.

II. Proposed Topologies Derived From the Hybrid Commutation Cell

The conventional dc–dc commutation cell, shown in Fig. 1(a), is composed of one switch, one diode, and one inductor. It presents three terminals, "a_1", "b_1", and "c_1", which can be used as the input or output. The classical buck, boost, and buck–boost converters are generated from the conventional dc–dc commutation cell, as seen in Fig. 1(b) (the power flow in Fig. 1(b) is always from $V_{\rm IN}$ to V_o).

In this paper, a commutation cell that integrates the conventional commutation cell [see Fig. 2(a)] with a passive switched-capacitor cell [see Fig. 2(b)] is studied, which results in the commutation cell shown in Fig. 2(c). The SC cell [see Fig. 2(b)] uses only passive switches and, thus, it is named the passive switched-capacitor cell.

Three types of converters can also be generated from the proposed cell: a buck, a boost, and a buck–boost, as shown in Fig. 3(a)–(c). These structures will be referred to as hybrid converters, due to the integration between SC cells and the conventional converters.

The buck-type and buck–boost-type converters proposed herein are novel structures. The boost structure is well known in the literature as a multilevel boost converter [26]–[27]. Nevertheless, it will be also examined in this paper using the commutation cell concept proposed herein.

On considering the hybrid commutation cell as a box, where only the terminals *a*, *b*, and *c* are available to connect the input

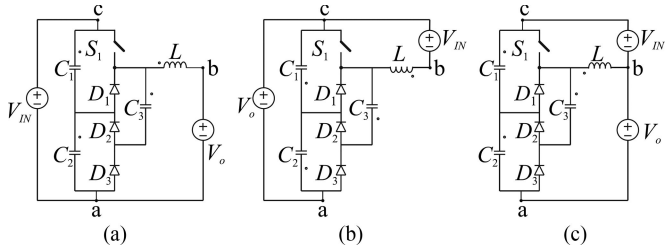

Fig. 3. Three converters generated for the hybrid commutation cell proposed in this paper: (a) hybrid dc–dc buck-type converter, (b) hybrid dc–dc boost-type converter, and (c) hybrid dc–dc buck–boost-type converter.

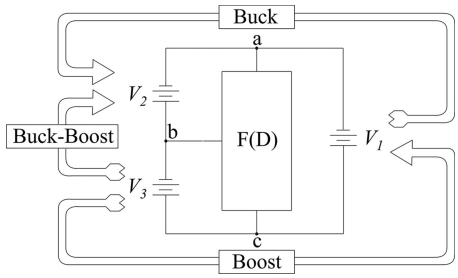

Fig. 4. Commutation cell with the connection terminals and the power flow to generate the converters for the cell.

and output, it is possible to illustrate the three converters as shown in Fig. 4. The *F(D)* is the commutation function and, thus, all static gains of the three converters can be derived from the *F(D)*, as described by

$$\begin{cases} G_{\rm Buck-type} = F(D) \\ G_{\rm Boost-type} = \dfrac{1}{1-F(D)} \\ G_{\rm Buck-Boost-type} = \dfrac{F(D)}{1-F(D)} \end{cases}. \tag{1}$$

III. Theoretical Analysis of the Proposed Topologies

The main characteristics of the proposed converters are analyzed in this section, including the topological stages, static gain in continuous conduction mode (CCM), static gain in discontinuous conduction mode (DCM), current and voltage stresses, and a generalization of the topologies.

A. Topological Stages

The topological stages for the three converters derived for the hybrid dc–dc commutation cell are shown in Fig. 5, which shows the converters buck-type [see Fig. 5(a)], boost-type [see Fig. 5(b)], and buck–boost-type [see Fig. 5 (c)].

In the first topological stage, the pulse width modulation (PWM) signal is at the high level and the switch S_1 is turned on [see first topological stage in Fig. 5(a)–(c)]. When this stage starts, the voltage across the capacitor C_1 is slightly higher than the voltage on the capacitor C_3 (SC of the structure). Thus, the diode D_2 is forward biased, connecting the capacitors C_1 and C_3 in parallel. The capacitors C_2 and C_3 are charging and the

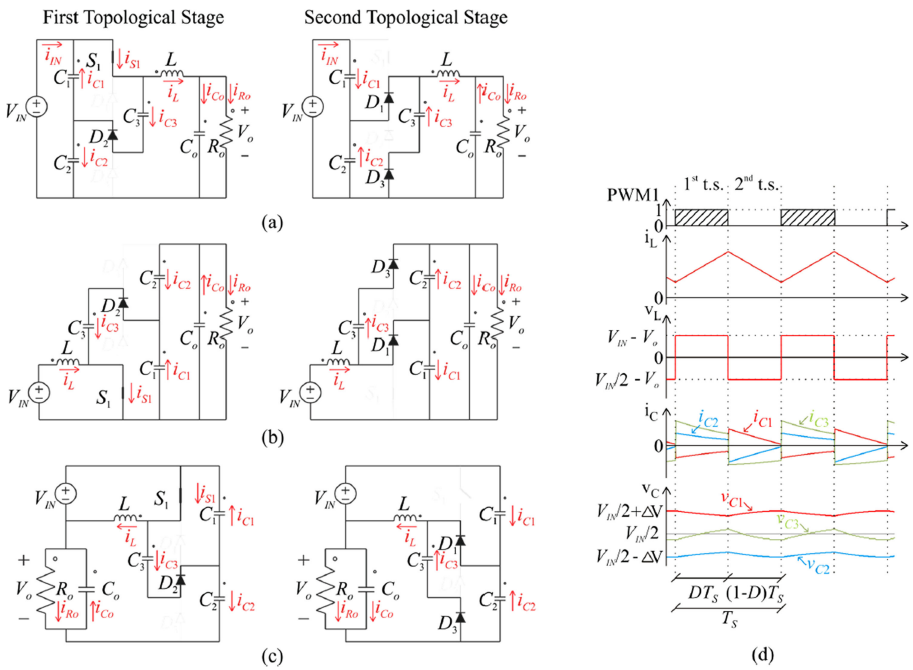

Fig. 5. Topological stages for the converters derived from the hybrid commutation cell: (a) hybrid buck converter; (b) hybrid boost converter; (c) hybrid buck-boost converter; and (d) the main waveforms for the hybrid buck converter.

capacitor C_1 is discharging during this stage. The inductor is storing energy.

In the second topological stage, the PWM signal changes to the low level and the switch S_1 is turned off [see second topological stage in Fig. 5(a)–(c)]. The diode D_1 is forward biased. The voltage across the capacitor C_3 is slightly higher than the voltage in the capacitor C_2. Thus, the diode D_3 is also forward biased, and it connects the capacitor C_3 in parallel with the capacitor C_2. The capacitors C_2 and C_3 are discharging while the capacitor C_1 is charging. The inductor provides energy for the load in this stage.

The waveforms for the PWM signal, inductor (i_L), and capacitor (i_C) currents, inductor (v_L) and capacitor (v_C) voltages related to the buck configuration can be seen in Fig. 5(d). The three converters show the same behavior and, thus, their main waveforms are similar. The differences are related to the voltage levels v_L and v_C, which differ for each topology. The waveforms in Fig. 5(d) consider the resistance series equivalent for the switched-capacitor (C_3) operating in partial charge mode [31].

B. CCM Gain

The voltage across the inductor (v_L) in *CCM* can be seen in Fig. 5(d). On considering the principle of inductor volt–second balance, all energy stored in the first topological stage (W_E) is provided to the load in the second topological stage (W_o). Hence

$$W_E + W_o = 0. \tag{2}$$

Expanding (2), gives

$$(V_{\mathrm{IN}} - V_o)\, I_o D T_S + \left(\frac{V_{\mathrm{IN}}}{2} - V_o\right) I_o\,(1-D)\,T_S = 0 \tag{3}$$

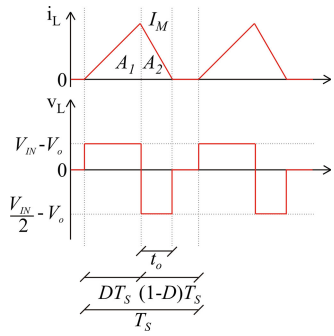

Fig. 6. Current and voltage across the inductor for DCM operation.

where V_{IN} is the input voltage, V_o is the output voltage, I_o is the output current, D is the duty cycle and T_S is the switching period.

From (3), the static gain in CCM for the proposed hybrid buck converter is given by

$$G_{\mathrm{buck\_CCM}} = F(D)_{\mathrm{CCM}} = \frac{1+D}{2}. \tag{4}$$

The commutation function *F*(*D*) can be defined from the buck-type converter gain, thus it is also defined by (4). Therefore, on substituting (4) in (1), the gains of the boost and buck–boost hybrid converters are defined by

$$\begin{cases} G_{\mathrm{boost\_CCM}} = \dfrac{2}{1-D} \\ G_{\mathrm{buck-boost\_CCM}} = \dfrac{1+D}{1-D} \end{cases}. \tag{5}$$

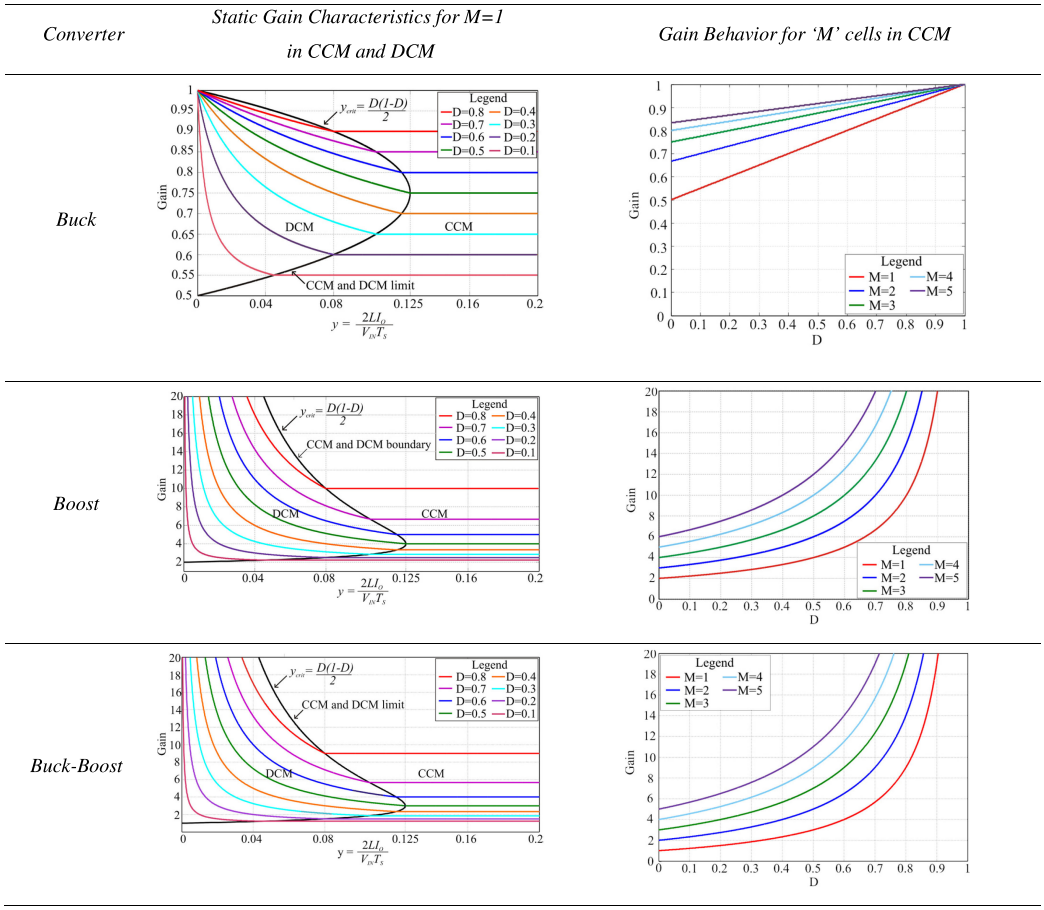

Fig. 7. Graphs showing the static characteristic behavior in CCM and DCM considering one switched-capacitor cell (M = 1), and graphs showing the gain behavior in CCM considering up to five switched cells.

C. DCM Gain

An analysis of the DCM gain was carried out for the hybrid buck converter and then expanded to the other two converters.

The current and voltage on the inductor terminals of the hybrid buck converter [see Fig. 5(a)], when operating in DCM, can be seen in Fig. 6, where IM is the inductor current peak value, tc is the time (DTS) required to magnetize the inductor before it reaches IM (peak current) and to is the time needed to completely demagnetize the inductor. Profiles similar to those in Fig. 6 were observed for the conventional buck converter.

On considering the principle of inductor volt–second balance, it is possible to obtain the average load current, which is defined by

$$\begin{cases} I_o = \dfrac{t_C^2}{2LT_S}\left((V_{\rm IN}-V_o)-\dfrac{(V_{\rm IN}-V_o)^2}{\left(\frac{V_{\rm IN}}{2}-V_o\right)}\right) \\ y = \dfrac{2LI_o}{V_{\rm IN}T_S} \end{cases}. \tag{6}$$

Following some manipulations, the DCM gain for the hybrid dc–dc buck converter is given by

$$G_{\rm buck\_DCM} = F(D)_{\rm DCM} = \frac{y+D^2}{2y+D^2} \tag{7}$$

where y is defined in (6).

Substituting (7) in (1), in DCM operation, the gain of the boost and buck–boost hybrid converters is provided by

$$\begin{cases} G_{\rm boost\_DCM} = \dfrac{D^2}{y}+2 \\ G_{\rm buck-boost\_DCM} = \dfrac{D^2}{y}+1 \end{cases}. \tag{8}$$

The static characteristics of the three converters in relation to y for different values of D, based on (4), (5), (7), and (8), are shown in Fig. 7 (column heading "*Static Gain Characteristics for M = 1 in CCM and DCM*"). The gain for the hybrid buck converter ranges from 0.5 to 1, that is, the proposed commutation cell decreases the voltage stress on the power component and it also lowers the gain range. The gains of the hybrid boost and hybrid buck–boost converters start at 2 and 1, respectively. In both cases, the commutation cell offers an off-set in the static characteristic in relation to conventional converters. The gains in CCM, DCM and at the boundary of both modes are seen in Fig. 7.

D. Generalization of the Proposed Hybrid Commutation Cell

Section II showed in detail how the hybrid dc–dc commutation cell was generated. Furthermore, it is possible to connect one set of SC cells in series (in the *ladder* configuration) with

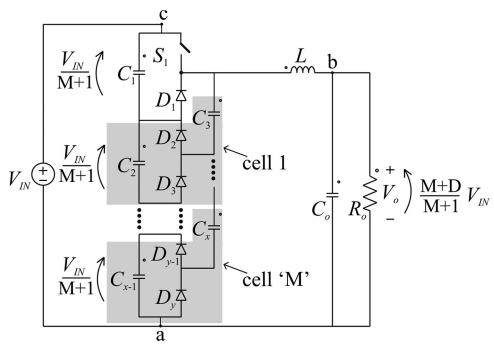

Fig. 8. Generalization of the switched-capacitor cell for the hybrid dc–dc buck converter.

the conventional commutation cell, as shown in Fig. 8. In this way, a generalized hybrid commutation cell is created, which supplies different gains for the proposed converters (buck-type, boost-type, and buck–boost-type).

The number of semiconductors increases when more SC cells are added to the system; however, the voltage stress on the components is divided. In other words, the generalized hybrid commutation cell can supply multilevel buck, boost [26]–[27], and buck–boost converters. Fig. 8 exemplifies the generalization of the cell for the hybrid dc–dc buck converter, where "M" is the number of cells added in the power stage.

The generalized gain for the hybrid buck converter is given by

$$G_{\text{buck\_gen}} = F(D)_{\text{gen}} = \frac{M+D}{M+1} \tag{9}$$

which also defines the commutation function for the generalized system. Substituting (9) in (1), the gain of the boost and buck-boost converters for the generalized cell are described by

$$\begin{cases} G_{\text{boost\_gen}} = \dfrac{M+1}{1-D} \\ G_{\text{buck-boost\_gen}} = \dfrac{M+D}{1-D} \end{cases}. \tag{10}$$

The generalized gain characteristics for CCM operation of the three converters are obtained from (9) and (10). They are shown in Fig. 7 (column heading "*CCM Gain Behavior for "M" cells*") in relation to *D* for different values of *M*. When the number of SCs increases, the gain range of the hybrid buck converter decreases and approaches a value of 1. On the other hand, the ideal static gains of the hybrid boost and buck–boost converters increase when more cells are employed (the curve for the gains presents an off-set in relation to the number of cells applied).

E. Steady-State Analysis

The topological stages in Fig. 5 ($M = 1$) can be described by the set of equations shown in Table I. This analysis considers all series resistances from the capacitors C_1, C_2, and C_3 to be equal to r_C.

The equations in Table I can be described by (11) and, subsequently, the coefficients of the matrixes A_1 and B_1, for the first topological stage, and A_2 and B_2 for the second topological stage, are found through a comparison between the equations in Table I and those in (11), shown at the bottom of the page. Considering the capacitances $C_1 - C_3$ to be equal, the results for the three converters are shown in Table II.

In steady state, (12), which represents the main variables of the system, can be simplified as

$$\dot{x} = Ax + Bu \qquad \xrightarrow{\text{steady state}} \qquad 0 = Ax + Bu \tag{12}$$

where

$$\begin{cases} A = A_1 D + A_2 (1-D) \\ B = B_1 D + B_2 (1-D) \end{cases} \tag{13}$$

and *u* considers the input voltage (V_{IN}) of the circuit.

Substituting the matrixes presented in Table II in (13) and then in (12) gives the steady-state equations for the inductor current and for the voltage across all the capacitors ($C_1 - C_3$, and C_o) for the buck-type, boost-type, and buck–boost-type converters. These are shown in detail in Table III. On comparing the expression related to the output voltage (V_{Co}), i.e., element X_{51} of the results vector in Table III, with (4) and (5), which represent the gain of the converters in CCM, the same expression is obtained for the three converters, corroborating the steady-state analysis and the gain obtained with the commutation function *F(D)* defined in (4).

$$\begin{cases} v_L = L\dfrac{di_L}{dt} = a_{11}i_L + a_{12}v_{C1} + a_{13}v_{C2} + a_{14}v_{C3} + a_{15}v_{Co} + b_{11}v_{\text{IN}} \\ i_{C1} = C_1\dfrac{dv_{C1}}{dt} = a_{21}i_L + a_{22}v_{C1} + a_{23}v_{C2} + a_{24}v_{C3} + a_{25}v_{Co} + b_{21}v_{\text{IN}} \\ i_{C2} = C_2\dfrac{dv_{C2}}{dt} = a_{31}i_L + a_{32}v_{C1} + a_{33}v_{C2} + a_{34}v_{C3} + a_{35}v_{Co} + b_{31}v_{\text{IN}} \\ i_{C3} = C_3\dfrac{dv_{C3}}{dt} = a_{41}i_L + a_{42}v_{C1} + a_{43}v_{C2} + a_{44}v_{C3} + a_{45}v_{Co} + b_{41}v_{\text{IN}} \\ i_{Co} = C_o\dfrac{dv_{Co}}{dt} = a_{51}i_L + a_{52}v_{C1} + a_{53}v_{C2} + a_{54}v_{C3} + a_{55}v_{Co} + b_{51}v_{\text{IN}} \end{cases} \tag{11}$$

TABLE I
SET OF EQUATIONS FOR THE FIRST AND SECOND TOPOLOGICAL STAGES FOR THE CONVERTERS SHOWN IN FIG. 5

Converter	First Topological Stage	Second Topological Stage
Buck	$\begin{cases} v_L = v_{IN} - v_o \\ v_{IN} = i_{C1} r_C + v_{C1} + i_{C2} r_C + v_{C2} \\ i_{C2} = i_{C1} + i_{C3} \\ i_{C1} r_C + v_{C1} = i_{C3} r_C + v_{C3} \\ i_L = i_{Co} + i_{Ro} \end{cases}$	$\begin{cases} v_L = i_{C2} r_C + v_{C2} - v_o \\ v_{IN} = i_{C1} r_C + v_{C1} + i_{C2} r_C + v_{C2} \\ i_{C1} = i_{C2} + i_{C3} + i_L \\ i_{C2} r_C + v_{C2} = i_{C3} r_C + v_{C3} \\ i_L = i_{Co} + i_{Ro} \end{cases}$
Boost	$\begin{cases} v_L = v_{IN} \\ v_o = i_{C1} r_C + v_{C1} + i_{C2} r_C + v_{C2} \\ i_{C2} = i_{C1} + i_{C3} \\ i_{C1} r_C + v_{C1} = i_{C3} r_C + v_{C3} \\ i_{C2} = -i_{Co} - i_{Ro} \end{cases}$	$\begin{cases} v_L = v_{IN} - i_{C1} r_C + v_{C1} \\ v_o = i_{C1} r_C + v_{C1} + i_{C2} r_C + v_{C2} \\ i_{C1} = i_{C2} + i_{C3} + i_L \\ i_{C2} r_C + v_{C2} = i_{C3} r_C + v_{C3} \\ i_{C2} = -i_{Co} - i_{Ro} - i_{C3} \end{cases}$
Buck-Boost	$\begin{cases} v_L = v_{IN} \\ v_{IN} + v_o = i_{C2} r_C + v_{C2} + i_{C3} r_C + v_{C3} \\ i_{C2} = i_{C1} + i_{C3} \\ i_{C1} r_C + v_{C1} = i_{C3} r_C + v_{C3} \\ i_{C2} = -i_{Co} - i_{Ro} \end{cases}$	$\begin{cases} v_L = v_{IN} - i_{C1} r_C + v_{C1} \\ v_{IN} + v_o = i_{C1} r_C + v_{C1} + i_{C2} r_C + v_{C2} \\ i_{C1} = i_{C2} + i_{C3} + i_L \\ i_{C2} r_C + v_{C2} = i_{C3} r_C + v_{C3} \\ i_{C2} = -i_{Co} - i_{Ro} - i_{C3} \end{cases}$

TABLE II
MATRIX ANALYSIS TO OBTAIN THE STEADY-STATE EQUATIONS WHICH REPRESENT THE MAIN CHARACTERISTICS OF THE HYBRID DC–DC CONVERTERS

Converter	A_1	A_2	B_1	B_2
Buck	$\begin{pmatrix} 0 & 0 & 0 & 0 & \frac{1}{L} \\ 0 & \frac{-2}{3r_C C} & \frac{-1}{3r_C C} & \frac{1}{3r_C C} & 0 \\ 0 & \frac{-1}{3r_C C} & \frac{-2}{3r_C C} & \frac{-1}{3r_C C} & 0 \\ 0 & \frac{1}{3r_C C} & \frac{-1}{3r_C C} & \frac{-2}{3r_C C} & 0 \\ \frac{1}{C_o} & 0 & 0 & 0 & \frac{-1}{R_o C_o} \end{pmatrix}$	$\begin{pmatrix} \frac{r_C}{3L} & \frac{-1}{3L} & \frac{1}{3L} & \frac{1}{3L} & \frac{-1}{L} \\ \frac{1}{3C} & \frac{-2}{3r_C C} & \frac{-1}{3r_C C} & \frac{-1}{3r_C C} & 0 \\ \frac{-1}{3C} & \frac{-1}{3r_C C} & \frac{-2}{3r_C C} & \frac{1}{3r_C C} & 0 \\ \frac{-1}{3C} & \frac{-1}{3r_C C} & \frac{1}{3r_C C} & \frac{-2}{3r_C C} & 0 \\ \frac{1}{C_o} & 0 & 0 & 0 & \frac{-1}{R_o C_o} \end{pmatrix}$	$\begin{pmatrix} \frac{1}{L} \\ \frac{1}{3r_C C} \\ \frac{2}{3r_C C} \\ \frac{1}{3r_C C} \\ 0 \end{pmatrix}$	$\begin{pmatrix} \frac{1}{3L} \\ \frac{2}{3r_C C} \\ \frac{1}{3r_C C} \\ \frac{1}{3r_C C} \\ 0 \end{pmatrix}$
Boost	$\begin{pmatrix} 0 & 0 & 0 & 0 & 0 \\ 0 & \frac{-2}{3r_C C} & \frac{-1}{3r_C C} & \frac{1}{3r_C C} & \frac{1}{3r_C C} \\ 0 & \frac{-1}{3r_C C} & \frac{-2}{3r_C C} & \frac{-1}{3r_C C} & \frac{2}{3r_C C} \\ 0 & \frac{1}{3r_C C} & \frac{-1}{3r_C C} & \frac{-2}{3r_C C} & \frac{1}{3r_C C} \\ 0 & \frac{1}{3r_C C_o} & \frac{2}{3r_C C_o} & \frac{1}{3r_C C_o} & \frac{-(3r_C+2R_o)}{3r_C R_o C_o} \end{pmatrix}$	$\begin{pmatrix} \frac{-r_C}{3L} & \frac{-1}{3L} & \frac{1}{3L} & \frac{1}{3L} & \frac{-2}{3L} \\ \frac{1}{3C} & \frac{-2}{3r_C C} & \frac{-1}{3r_C C} & \frac{-1}{3r_C C} & \frac{2}{3r_C C} \\ \frac{-1}{3C} & \frac{-1}{3r_C C} & \frac{-2}{3r_C C} & \frac{1}{3r_C C} & \frac{1}{3r_C C} \\ \frac{-1}{3C} & \frac{-1}{3r_C C} & \frac{1}{3r_C C} & \frac{-2}{3r_C C} & \frac{1}{3r_C C} \\ \frac{2}{3C_o} & \frac{2}{3r_C C_o} & \frac{1}{3r_C C_o} & \frac{1}{3r_C C_o} & \frac{-(3r_C+2R_o)}{3r_C R_o C_o} \end{pmatrix}$	$\begin{pmatrix} \frac{1}{L} \\ 0 \\ 0 \\ 0 \\ 0 \end{pmatrix}$	$\begin{pmatrix} \frac{1}{L} \\ 0 \\ 0 \\ 0 \\ 0 \end{pmatrix}$
Buck-Boost	$\begin{pmatrix} 0 & 0 & 0 & 0 & 0 \\ 0 & \frac{-2}{3r_C C} & \frac{-1}{3r_C C} & \frac{1}{3r_C C} & \frac{1}{3r_C C} \\ 0 & \frac{-1}{3r_C C} & \frac{-2}{3r_C C} & \frac{-1}{3r_C C} & \frac{2}{3r_C C} \\ 0 & \frac{1}{3r_C C} & \frac{-1}{3r_C C} & \frac{-2}{3r_C C} & \frac{1}{3r_C C} \\ 0 & \frac{1}{3r_C C_o} & \frac{2}{3r_C C_o} & \frac{1}{3r_C C_o} & \frac{-(3r_C+2R_o)}{3r_C R_o C_o} \end{pmatrix}$	$\begin{pmatrix} \frac{-r_C}{3L} & \frac{-1}{3L} & \frac{1}{3L} & \frac{1}{3L} & \frac{-2}{3L} \\ \frac{1}{3C} & \frac{-2}{3r_C C} & \frac{-1}{3r_C C} & \frac{-1}{3r_C C} & \frac{2}{3r_C C} \\ \frac{-1}{3C} & \frac{-1}{3r_C C} & \frac{-2}{3r_C C} & \frac{1}{3r_C C} & \frac{1}{3r_C C} \\ \frac{-1}{3C} & \frac{-1}{3r_C C} & \frac{1}{3r_C C} & \frac{-2}{3r_C C} & \frac{1}{3r_C C} \\ \frac{2}{3C_o} & \frac{2}{3r_C C_o} & \frac{1}{3r_C C_o} & \frac{1}{3r_C C_o} & \frac{-(3r_C+2R_o)}{3r_C R_o C_o} \end{pmatrix}$	$\begin{pmatrix} \frac{1}{L} \\ \frac{1}{3r_C C} \\ \frac{2}{3r_C C} \\ \frac{1}{3r_C C} \\ \frac{-2}{3r_C C_o} \end{pmatrix}$	$\begin{pmatrix} \frac{1}{3L} \\ \frac{2}{3r_C C} \\ \frac{1}{3r_C C} \\ \frac{1}{3r_C C} \\ \frac{-2}{3r_C C_o} \end{pmatrix}$

F. Current and Voltage Stress Analysis

The matrix coefficients for the first and second topological stages, shown in Table II, and the steady-state equations, shown in Table III, can be applied in (11) ($i_{C1} - i_{C3}$ equations) and, for this analysis, the current stress equations for all power components are obtained directly. Tables IV and V summarize the voltage and current stresses in all power components. The equations in Table IV can be applied in the three converters derived from the proposed hybrid commutation cell.

IV. PROTOTYPE IMPLEMENTATION AND EXPERIMENTAL RESULTS

A. Verification of the Proposed Converters

A prototype was built to verify the converters derived from the hybrid dc–dc commutation cell [see photograph in Fig. 9(a)]. The prototype was designed for the hybrid dc–dc buck-type converter (1 kW of rated power). The power density ability of the prototype built was about 0.508 W/cm^3 or 0.689 W/g. Furthermore, after adjusting the input/output voltages and rated power, the boost and buck–boost topologies were validated with the same prototype. The converter specifications are summarized in Table VI. The switch frequency (f_s) was set at 70 kHz and a list of the component is given in Table VII.

The main waveforms related to the hybrid buck, boost, and buck–boost converters are displayed in Fig. 10. The experimental waveforms are in agreement with the theoretical waveforms shown in Fig. 5.

The experimental steady-state values (shown in Fig. 10) are close to those obtained from Table III. The voltage stresses in the switch S_1 for the buck, boost, and buck–boost converters are, respectively, $V_{\rm IN}/2$, $V_o/2$, and $(V_{\rm IN} + V_o)/2$, which is in agreement with the theoretical analysis reported in Tables IV and V.

TABLE III
STEADY-STATE ANALYSIS FOR THE HYBRID DC–DC BUCK, BOOST, AND BUCK–BOOST CONVERTERS DERIVED FROM THE HYBRID COMMUTATION CELL PROPOSED IN THIS PAPER

Converter	X_o
Buck	$\begin{pmatrix} I_L \\ V_{C1} \\ V_{C2} \\ V_{C3} \\ V_{Co} \end{pmatrix} = \begin{pmatrix} \frac{12V_{IN}D(1+D)}{[if\,4DR_o+r_C(9+D(16D-25))]} \\ \frac{V_{IN}[12DR_o+r_C(9+D(5D-11))]}{[24DR_o+r_C(9+D(16D-25))]} \\ \frac{DV_{IN}[12R_o+r_C(11D-14)]}{[24DR_o+r_C(9+D(16D-25))]} \\ \frac{DV_{IN}[12R_o+r_C(14D-11)]}{[24DR_o+r_C(9+D(16D-25))]} \\ \frac{12V_{IN}DR_o(1+D)}{[24DR_o+r_C(9+D(16D-25))]} \end{pmatrix} \xrightarrow{\text{if } r_C=0} \begin{pmatrix} \frac{V_{IN}(1+D)}{2R_o} \\ \frac{V_{IN}}{2} \\ \frac{V_{IN}}{2} \\ \frac{V_{IN}}{2} \\ \frac{V_{IN}(1+D)}{2} \end{pmatrix}$.
Boost	$\begin{pmatrix} I_L \\ V_{C1} \\ V_{C2} \\ V_{C3} \\ V_{Co} \end{pmatrix} = \begin{pmatrix} \frac{8V_{IN}D}{(1-D)[2DR_o(1-D)+3r_C]} \\ \frac{V_{IN}[2DR_o(1-D)+r_C(3-2D)]}{(1-D)[2DR_o(1-D)+3r_C]} \\ \frac{V_{IN}[2DR_o(1-D)+r_C(2D-3)]}{(1-D)[2DR_o(1-D)+3r_C]} \\ \frac{V_{IN}[2DR_o(1-D)+r_C(4D-3)]}{(1-D)[2DR_o(1-D)+3r_C]} \\ \frac{4V_{IN}DR_o}{[2DR_o(1-D)+3r_C]} \end{pmatrix} \xrightarrow{\text{if } r_C=0} \begin{pmatrix} \frac{4V_{IN}}{R_o(1-D)^2} \\ \frac{V_{IN}}{1-D} \\ \frac{V_{IN}}{1-D} \\ \frac{V_{IN}}{1-D} \\ \frac{2V_{IN}}{1-D} \end{pmatrix}$.
Buck-Boost	$\begin{pmatrix} I_L \\ V_{C1} \\ V_{C2} \\ V_{C3} \\ V_{Co} \end{pmatrix} = \begin{pmatrix} \frac{4V_{IN}D(1+D)}{(1-D)[2DR_o(1-D)+3r_C]} \\ \frac{V_{IN}[2DR_o(1-D)+r_C(3-D(D+1))]}{(1-D)[2DR_o(1-D)+3r_C]} \\ \frac{V_{IN}[2DR_o(1-D)+r_C(D(D-2))]}{(1-D)[2DR_o(1-D)+3r_C]} \\ \frac{V_{IN}[2DR_o(1-D)+r_C(D(2D-1))]}{(1-D)[2DR_o(1-D)+3r_C]} \\ \frac{2V_{IN}D(1+D)R_o}{[2DR_o(1-D)+3r_C]} \end{pmatrix} \xrightarrow{\text{if } r_C=0} \begin{pmatrix} \frac{2V_{IN}(1+D)}{R_o(1-D)^2} \\ \frac{V_{IN}}{1-D} \\ \frac{V_{IN}}{1-D} \\ \frac{V_{IN}}{1-D} \\ \frac{V_{IN}(1+D)}{1-D} \end{pmatrix}$

TABLE IV
EQUATIONS FOR THE CURRENT AND VOLTAGE STRESS ON ALL SEMICONDUCTORS AND CAPACITORS IN THE POWER STAGE FOR ONE SWITCHED-CAPACITOR

	Stress		
		Current	
Components	Voltage	RMS	Average
C_1	$\frac{V_x}{2}$	$\frac{I_L}{4}\sqrt{\frac{(1-D)}{D}}$	–
C_2	$\frac{V_x}{2}$	$\frac{I_L}{4}\sqrt{\frac{(1-D)}{D}}$	–
C_3	$\frac{V_x}{2}$	$\frac{I_L}{2}\sqrt{\frac{(1-D)}{D}}$	–
S_1	$\frac{V_x}{2}$	$\frac{I_L}{2}\frac{(1+D)}{\sqrt{D}}$	$\frac{I_L}{2}(1+D)$
D_1	$\frac{V_x}{2}$	$\frac{I_L}{2}\sqrt{(1-D)}$	$\frac{I_L}{2}(1-D)$
D_2	$\frac{V_x}{2}$	$\frac{I_L}{2}\frac{(1-D)}{\sqrt{D}}$	$\frac{I_L}{2}(1-D)$
D_3	$\frac{V_x}{2}$	$\frac{I_L}{2}\sqrt{(1-D)}$	$\frac{I_L}{2}(1-D)$

TABLE V
PARAMETER DEFINITIONS FOR THE CURRENT AND VOLTAGE FOR THE HYBRID DC–DC CONVERTERS

Converter	V_X	I_L
Buck	V_{IN}	I_o
Boost	V_o	I_{IN}
Buck-Boost	$V_{\text{IN}} + V_o$	$I_{\text{IN}} + I_o$

TABLE VI
SPECIFICATIONS OF THE CONVERTERS

Buck	Boost	Buck-Boost
$V_{\text{IN}} = 600\,\text{V}$	$V_{\text{IN}} = 100\,\text{V}$	$V_{\text{IN}} = 150\,\text{V}$
$V_o = 450\,\text{V}$	$V_o = 400\,\text{V}$	$V_o = 450\,\text{V}$
$D = 0.5$	$D = 0.5$	$D = 0.5$
$Gain = 0.75$	$Gain = 4$	$Gain = 3$

TABLE VII
LIST OF COMPONENTS USED IN THE PROTOTYPE DESIGN

Components	Quantity	Characteristics
C_1, C_2, C_3	3	Panasonic – 100 µF – 500 V – 4.7 mΩ – 18 A
S_1	1	Infineon – IPW60R099 – 650 V – 0.099 mΩ – 24 A
D_1, D_2, D_3	3	CREE – C3D10060A – 600 V – 10 A
L	1	2.41 mH ($\Delta I_L = 20\%$)
Core	2	E 55/28/21 – EPCOS – N87
C_o	1	Kemet 20 µF – 600 V – 1.9 mΩ – 29 A
PWM	1	UC3525
Gate Driver (optocoupler)	1	DRO100S25A
Isolated Supplier to Gate Driver	1	S320-08A

The SC C_3 ensured the voltage balance between the capacitors C_1 and C_2. Thus, the proposed commutation cell and the three topologies described herein were validated experimentally

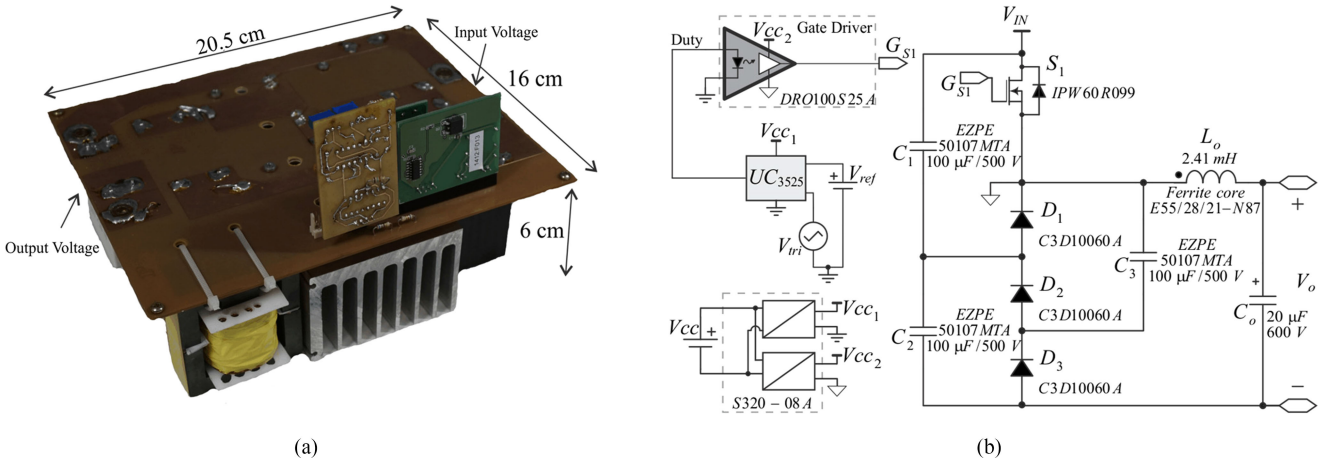

Fig. 9. (a) Prototype built to validate experimentally all converters derived from the hybrid dc–dc commutation cell and (b) schematic of the buck-type converter.

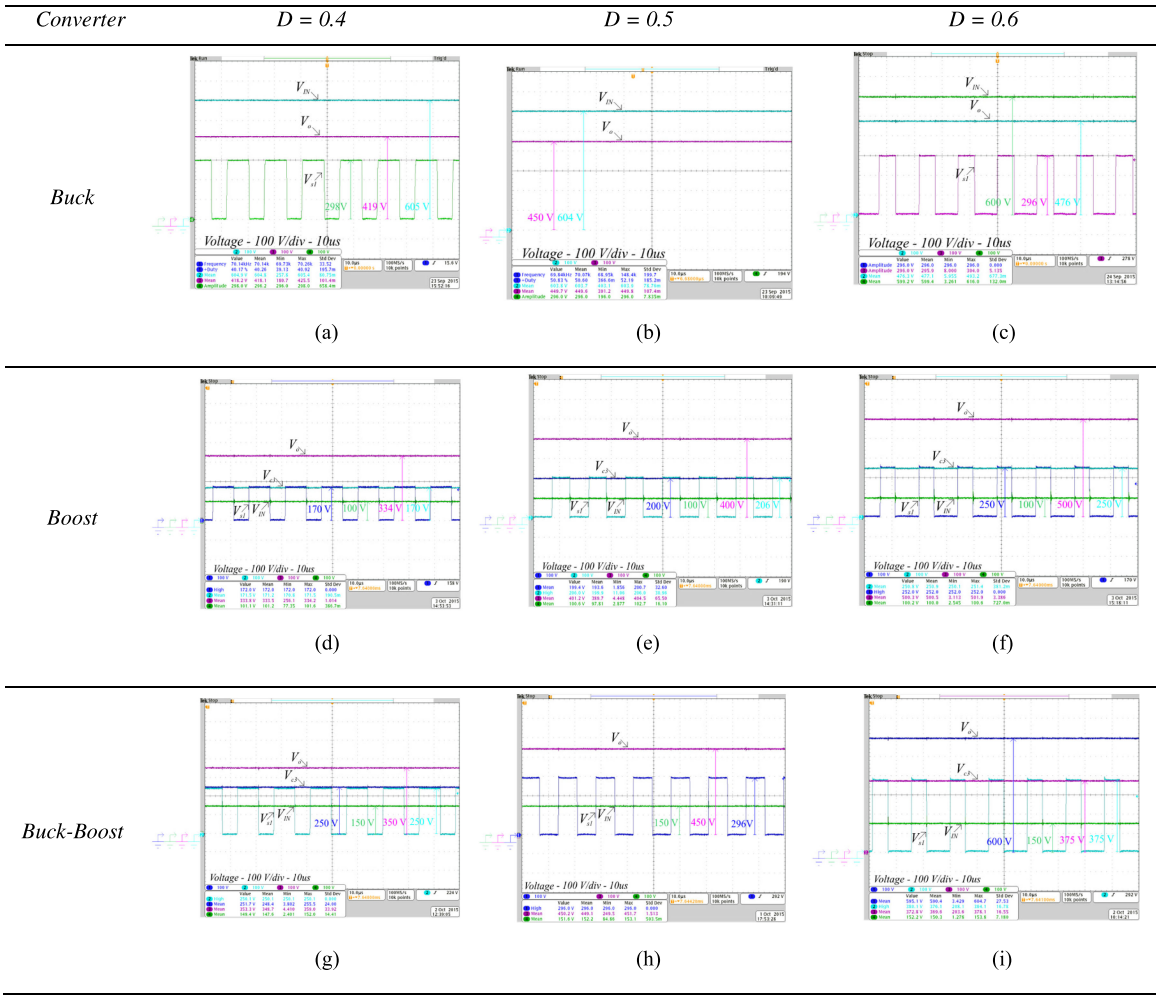

Fig. 10. Main waveforms obtained for the experimental validation of the hybrid dc–dc converters generated from the proposed hybrid dc–dc commutation cell: (a) buck-type converter with $D = 0.4$ ($V_{\text{in}} = 600$ V and $V_o = 420$ V); (b) buck-type converter with $D = 0.5$ ($V_{\text{in}} = 600$ V and $V_o = 450$ V); (c) buck-type converter with $D = 0.6$ ($V_{\text{in}} = 600$ V and $V_o = 480$ V); (d) boost-type converter with $D = 0.4$ ($V_{\text{in}} = 100$ V and $V_o = 333$ V); (e) boost-type converter with $D = 0.5$ ($V_{\text{in}} = 100$ V and $V_o = 400$ V); (f) boost-type converter with $D = 0.6$ ($V_{\text{in}} = 100$ V and $V_o = 500$ V); (g) buck–boost-type converter with $D = 0.4$ ($V_{\text{in}} = 150$ V and $V_o = 350$ V); (h) buck–boost-type converter with $D = 0.5$ ($V_{\text{in}} = 150$ V and $V_o = 450$ V); and (i) buck–boost-type converter with $D = 0.6$ ($V_{\text{in}} = 150$ V and $V_o = 600$ V).

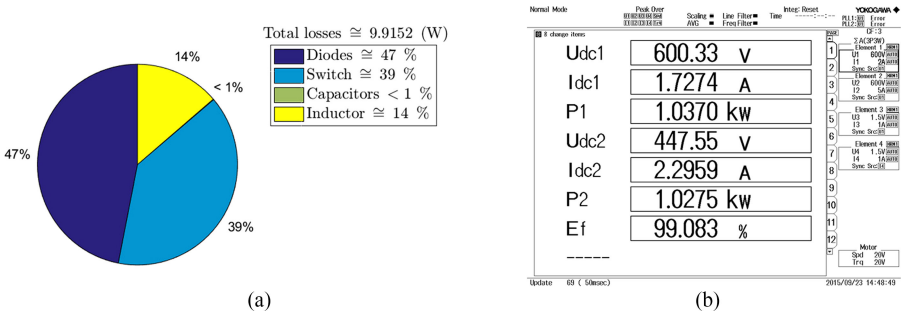

Fig. 11. (a) Estimated total losses and distribution losses by components of the buck-type converter and (b) experimental measured efficiency of the buck-type converter with $f_s = 70$ kHz, D = 0.5, and 1 kW.

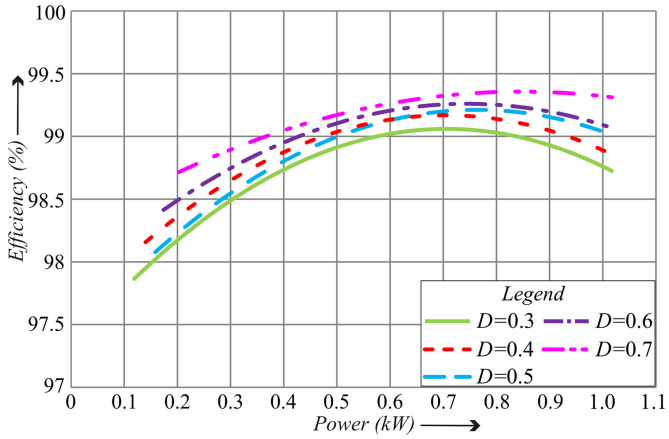

Fig. 12. Efficiency for different duty cycle values (switching frequency of 70 kHz).

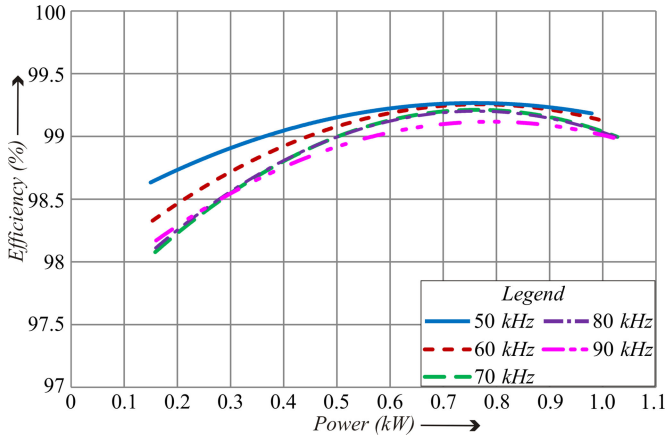

Fig. 13. Efficiency for different switching frequencies ($D = 0.5$).

and the results are consistent with all of the theoretical analysis presented in Section III. $I_{\rm IN}$ and I_o are, respectively, the input and output currents.

The prototype was designed using the partial charger mode to the switched capacitors, thus the currents could be considerate almost constants and the estimated efficiency of the hybrid converters can be derived from the conventional methodology. Knowing the component stresses of Table IV and component specifications of Table VII, the estimated conduction and commutation total losses and the portions these losses in each component are summarized in Fig. 11(a) for the buck-type converter with rated power (1 kW) and switching frequency ($f_s = 70$ kHz). Hence, a theoretical efficiency of the 99.02% can be calculated, and this value is nearly to the experimental efficiency measured by Yokogawa Power Analyzer showed in Fig. 11(b).

The efficiency curves obtained for the hybrid dc–dc buck converter (i.e., the structure used to design the prototype) are shown in Figs. 12 and 13. The tests were carried out using different values for the duty cycle and switching frequency.

The maximum efficiency ($f_s = 70$ kHz) seen in Fig. 12, with the converter operating with a duty cycle of $D = 0.5$, was 99.2% at 68% of load. For the rated power, the efficiency was 99.08% (this measure only accounts loss from the power stage). Moreover, the topology presented a high efficiency for a wide range of operation conditions. It was also observed in the efficiency tests that when the duty cycle of the system was increased, the efficiency also increased. This is because in the second topological stage only the diodes D_1 and D_3 are forward biased and, thus, since they have a conduction resistance lower than S_1, the efficiency increases. Fig. 13 shows the efficiency curves for different switching frequencies (with a constant duty cycle of 0.5). It can be observed that the efficiency increases at lower switching frequency. This is because the switching losses decrease and, when the switching frequency drops to 30%, the equivalent resistance value for the SC [32], [33] does not increase significantly for the design specification used. Therefore, the conduction loss increases only slightly. Thus, the whole efficiency increases for lower switching frequencies.

B. Comparison Between the Proposed Converters and Conventional Solutions

Table VIII shows a qualitative and quantitative comparison between the described topologies in this paper and other topologies in the literature with the same voltage gain. Table VIII shows a comparison of the aforementioned topologies in relation to the gain range, the voltage stress on the power semiconductors, and number of components. In the buck structure, the addition of one switched-capacitor cell to the conventional cell reduces the voltage stress on the power semiconductors to half in relation to the same topology generated by the conventional cell. If compared with the three-level buck [28]–[30], the

TABLE VIII
QUALITATIVE AND QUANTITATIVE COMPARISON BETWEEN THE TOPOLOGIES PRESENTED IN THIS PAPER AND OTHER SOLUTIONS IN THE LITERATURE (CONVENTIONAL BUCK, THREE-LEVEL BUCK [28]–[30] AND TOPOLOGIES PROPOSED IN [34]–[36])

Topology	Gain	V_{S1}	$V_{D\max}$	Number of C	S	D	L
C-Buck[1]	D	$V_{\rm IN}$	$V_{\rm IN}$	1	1	1	1
3-Level Buck [28]	$\frac{D}{2}\ to\ (D<0.5)$ and $\frac{1+D}{2}\ to\ (D>0.5)$	$\frac{V_{\rm IN}}{2}$	$\frac{V_{\rm IN}}{2}$	2	4	0	1
H-Buck[2]	$\frac{1+D}{2}\ to\ (0\le D\le 1)$	$\frac{V_{\rm IN}}{2}$	$\frac{V_{\rm IN}}{2}$	3	1	3	1
H-Boost[2]	$\frac{2}{1-D}$	$\frac{V_o}{2}$	$\frac{V_o}{2}$	3	1	3	1
Converter II [34]	$\frac{2}{1-D}$	$\frac{V_o}{2}$	V_o	2	2	2	2
Cuk Derived [35]	$\frac{2}{1-D}$	$\frac{V_o}{2}$	$\frac{V_o}{2}$	3	1	3	1
H- Buck-Boost[2]	$\frac{1+D}{1-D}$	$\frac{V_{\rm IN}+V_o}{2}$	$\frac{V_{\rm IN}+V_o}{2}$	3	1	3	1
Converter I [34]	$\frac{1+D}{1-D}$	$\frac{V_{\rm IN}+V_o}{2}$	$V_{\rm IN}+V_o$	1	2	1	2
Zeta Derived [35]	$\frac{1+D}{1-D}$	$\frac{V_o}{1+D}$	$\frac{V_{\rm IN}+V_o}{2}$	3	1	3	1
SL Boost [36]	$\frac{1+D}{1-D}$	V_o	V_o and $V_{\rm IN}$	1	1	4	2

[1]C—Conventional dc–dc converters;
[2]H—Hybrid dc–dc converters proposed in this paper.

proposed buck-type allows a more accurate output voltage variation, because the voltage gain $(1 + D)/2$ matches to all range of the duty cycle ($D = 0$ to 1), which does not happen in the three-level buck. This feature can be used when converters for preregulation stages are required. Furthermore, the proposed buck-type can be implemented employing only one controllable switch and, therefore, a simpler modulator is required (independently of the number of stacked SC cells). The hybrid boost topology is compared to the proposed converters in [34] (converter II) and [35]. The range of gain and the voltage stress on switch S is the same for the three topologies $(V_o/2)$. The voltage stresses on diodes are $V_o/2$ in the hybrid boost converter and structure Cuk [35]. Therefore, converter II presented in [34] has one diode (D_2) that the voltage stress is V_o. The proposed buck–boost-type converter was compared with the presented topologies in [34] (converter I), [35] and [36], as can be seen in Table VIII. Considering the same gain, the voltage stress on switch S is equal to the proposed buck–boost and converter I in [34] and, usually, it is higher in the approached structures in [35] and [36]. In relation to the voltage stress on the diodes, the proposed buck–boost and zeta derived converter in [35] have the same value and, both present a smaller value regarding to structures in [34] and [36].

Furthermore, the topologies described herein allow the addition of more switched-capacitor cells, which increase the range of gain, while maintaining the linear characteristic of the gain for the buck-type converter (see Fig. 7) and the nonlinear characteristics of the gain for the boost-type and buck–boost-type converters (see Fig. 7). Besides that, the voltage stresses on the semiconductors are maintained constant. Hence, the proposed topologies can be applied in systems with higher voltage levels using semiconductors with reduced voltage stress.

A quantitative comparison of the aforementioned topologies revealed that, comparing the buck-type topology with the conventional buck, there is an increase in the number of diodes (two) and capacitors (two). For the boost-type, the converter II proposed in [34] has fewer capacitors and diodes (one of each), but one more inductor and switch, while the cuk derived in [35] has the same number of components in the power stage. Finally, the buck–boost-type converter has the same number of components if compared with the zeta derived [35] and differs from the converter I [34] and SL Boost [36], as it can be seen in details in Table VIII.

V. CONCLUSION

The new hybrid dc–dc commutation cell proposed in this paper integrates a passive switched-capacitor cell with the conventional commutation cell. The three converters generated from the commutation cell are referred to as the hybrid dc—dc buck, hybrid dc–dc boost [26], [27], and hybrid dc–dc buck–boost converters. On applying the commutation cell concept, it was possible to analyze the three derived converters together. As approached in this paper, the proposed hybrid commutation cell was generalized for any number of SC cells in series-connection (ladder configuration). Thus, different gain rated for the proposed hybrid buck, boost, and buck–boost converters can be ascertained. As results, the generalized structures were also defined in this paper.

The main advantages of proposed topologies are the wide range of gains and reduced voltage stress on the components in comparison with the conventional dc–dc converters (for the same duty cycle). Furthermore, the voltage stresses are equally divided among the semiconductors and capacitors of the power

stage, thus no capacitors voltages balance control are need and the strategies of the control applied in conventional converters can be used to proposed converters.

The gain of the hybrid buck converter has a narrower range (from 0.5 to 1 for one SC), which is suitable for operation with a lower duty cycle and high gains (close to one). As this gain rate is valid to all range of duty cycle, the hybrid buck is limited to a little adjust range, but with a high precision. This characteristic can be used in converters applied in preregulation stages. The gains of the hybrid boost and buck–boost converters are multiplied by the number of SC cells, which improves the gain without changing the characteristic static shape. However, as shown in Fig. 7, increasing more and more the number of SC cells (M) it makes difficult to control the output voltage regulation to high duty cycle values. The buck-boost type derived offers a gain of $(M + D)/(1 - D)$ and the voltage stresses are equal on all switches. As shown in Tables IV and V, the hybrid buck–boost has higher stresses on components than the hybrid buck and boost, which also happens in the conventional buck–boost converter. If the number of SC cells increases (i.e., $M > 1$), the voltage stress on the components will decrease in relation to the total output voltage, but this will have impacts at the efficiency too. The proposed buck–boost extends the applicability of this topology for cases where a higher conversion rate and lower voltage stress are required.

The hybrid converters was designed using the partial charger mode [31] to the switched capacitors, since the currents may be considerate almost constant and losses in each component can be quantified [as shown in Fig. 14(a)] by classical methods. Since, a theoretical efficiency of 99.02% was calculated at the rated power (1 kW) and this value was close to the experimental efficiency measured of 99.08%, as shown in Fig. 14 (b). Experimental results obtained for the three converters corroborated the theoretical analysis. For the hybrid buck structure, the maximum efficiency was 99.2% in a power of 68% of the rated power (680 W). Based on these results, the topologies can be applied in dc–dc conversion that needs to operate with a higher voltage level and rated gain.

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