Evaluation of Carrier-Based Modulation Techniques With Common-Mode Voltage Reduction for Neutral Point Clamped Converter

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***Abstract*—Common-mode voltage output is closely associated with switching states in three-phase three-wire neutral point clamped converter. Detailed analysis shows avoiding redundant states can effectively improve the common-mode voltage, so this paper proposes a pulse width modulation (PWM) technique with zero redundant state to reduce the common-mode voltage output, and evaluates their performance with the conventional PWM schemes. This paper also takes the compensation of neutral point potential deviation into consideration. Laboratory test results are presented to verify the effectiveness of the proposed scheme.**

***Index Terms*—Common-mode voltage (CMV), neutral point clamped (NPC) converter, pulse width modulation (PWM).**

I. Introduction

NEUTRAL point clamped (NPC) converters provide a popular solution for the medium-voltage system. Fig. 1 shows a typical application of the three-level NPC converter, and this circuit can meet several requirements of customers with the reduced voltage stress on switching devices and the improved harmonics [1]–[3]. Nevertheless, the impact of common-mode voltage (CMV) must be addressed to prevent the bearing failures and electromagnetic interference noise [4].

The conventional solution, like common-mode elimination pulse width modulation (CMEPWM), has been presented in many studies, but the weak points include; linear modulation range is reduced to 86.6% of the full potential of NPC converter; minimum numbers of the synthesized vectors lead to a problem to the NPP deviation compensation [5]–[9]. Phase opposite deposition PWM (PODPWM) offered a substituted method with the reduced CMV output [10]–[12]. Unfortunately, the instantaneously switching an output for more than one level may occur, and the switching devices may be damaged [13]. Recently, Yuan *et al.* presented a discontinuous PWM (DPWM) to deal with this issue, but it traded off the NPP compensation capability [14], [15]. Many space-vector schemes were developed in [16]–[18], but those suffered from more calculation burden to synthesize modulation voltage and select switching states than the carrier-based ones.

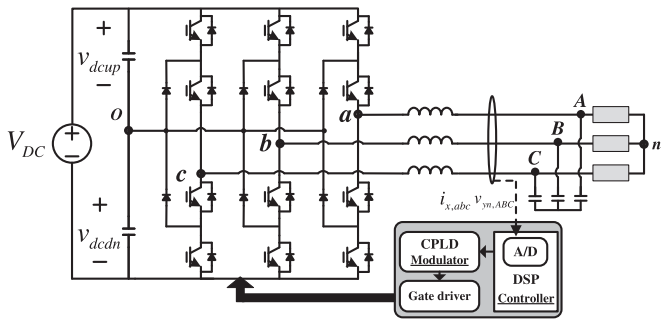

Fig. 1. Three-level NPC converter.

This paper proposes a zero redundant state PWM (ZRSPWM) to meet both demands with the reduced CMV output and the NPP balance, and the quad-carrier-based operation can effectively reduce the calculation burden. Besides, the instantaneous switching an output for more than one level can be avoided. This research also compares the performance of the proposed PWM with the other carrier-based reduced CMV PWMs, and the laboratory test results are presented to validate the aforementioned analysis.

II. CMV of NPC-Based Converter

Fig. 2 shows the space-vector plane of the NPC three-level converter, where P, O, and N respectively represent voltage outputs of $+V_{\rm dc}/2$, 0, and $-V_{\rm dc}/2$. On space-vector plane, the output voltage vectors can be classified as zero vectors (z), small vectors (u), medium vectors (v), and full vectors (w) according to the size of vector. Besides, a zero vector or small vector can be outputted from more than one switching states (i.e., redundant states).

CMV output ($v_{\rm CM}$) is defined as follows:

$$v_{\rm CM} = \frac{1}{3}\sum_{x=a,b,c} v_{xo},\ \text{where}\ v_{xo} = s_x\frac{V_{\rm dc}}{2}. \tag{1}$$

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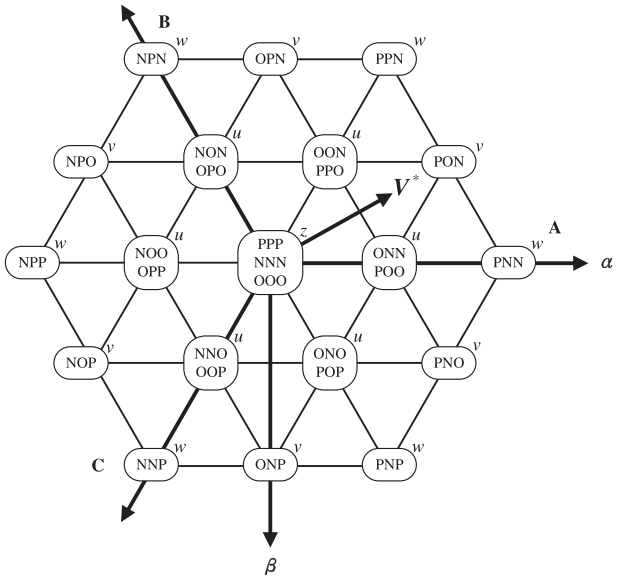

Fig. 2. Space-vector plane of the three-level NPC converter.

TABLE I
CMV LEVELS OF DIFFERENT SWITCHING STATES

Classification	Switching state	CMV level
Large (w)	PPN, NPP, PNP	$+V_{\rm dc}/6$
	NNP, NPN, PNN	$-V_{\rm dc}/6$
Medium (v)	PON, PNO, OPN	0
	ONP, NPO, NOP	
Small(u)	PPO, OPP, POP	$+V_{\rm dc}/3$
	ONN, NON, NNO	$-V_{\rm dc}/3$
	POO, OPO, OOP	$+V_{\rm dc}/6$
	OON, ONO, OON	$-V_{\rm dc}/6$
Zero (z)	PPP	$+V_{\rm dc}/2$
	NNN	$-V_{\rm dc}/2$
	OOO	0

Note that subscript x stands for the three legs of converter, and v_{xo} is the output voltage of each leg with respect to the reference node (o). s_x represents the switching states ($+1$, 0, and -1). As Table I indicates, the levels of CMV output expand to $\pm V_{\rm dc}/2$, $\pm V_{\rm dc}/3$, $\pm V_{\rm dc}/6$, and 0 depending on 27 switching states. Both maximum and minimum of CMV are respectively generated by PPP and NNN of zero vector, and zero CMV level occurs at OOO of zero vector and all medium vectors. Besides, the redundant states, such as ONN and POO, generate the same voltage output vector but the different CMV output.

III. CONVENTIONAL PWM SCHEME

A. Phase Deposition PWM

The phase deposition PWM (PDPWM) uses two carriers (Λ_1 and Λ_2) with phase deposition to synthesize voltage output [10], [11], and the unipolar modulation can effectively avoid PPP and NNN. Fig. 3(a) shows the pulse pattern of the PDPWM with unipolar modulation, where v^*_{ao}, v^*_{bo}, and v^*_{co} are the modulation voltages, and the generated states are POO, PON, PNN, and ONN. Synthesizing voltage outputs are without PPP and NNN, and the CMV output is reduced from $\pm V_{\rm dc}/2$ to $\pm V_{\rm dc}/3$.

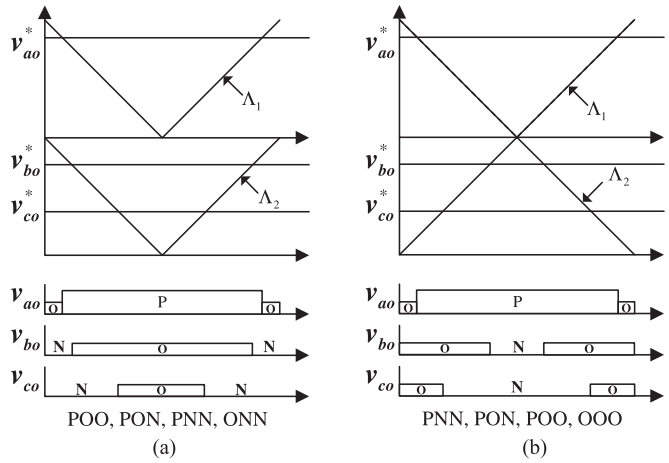

Fig. 3. Pulse pattern (a) PDPWM (b) PODPWM.

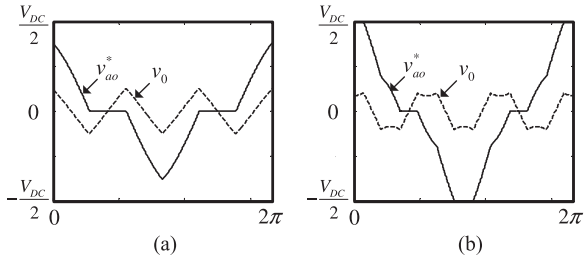

Fig. 4. Modulation voltage of DPWM scheme (a) $M_i = 0.4$ (b) $Mi = 0.65$.

B. Discontinuous PWM

Based on PDPWM, the DPWM injects an adequate offset into the three-phase modulation voltages to reduce CMV output to $\pm V_{\rm dc}/6$. Fig. 4 shows the waveforms of the modulation voltages and the injected offset, where M_i stands for the modulation index defined as follows:

$$M_i = \frac{\pi\,|V^*|}{2V_{\rm dc}}. \tag{2}$$

The modulation voltage for each phase has total 1/3 of fundamental cycle, which is clamped to the positive, negative, or zero dc rails [14]. Compared with sinusoidal PWM (SPWM), the switching number can be effectively decreased in a fundamental period, but balancing the NPP must be traded off. Among the modulation voltages (v^*_{ao}, v^*_{bo}, and v^*_{co}), the maximum and minimum are respectively denoted with $v_{\rm max}$ and $v_{\rm min}$, and the middle one is denoted with $v_{\rm mid}$. Then, the injected offset ($v^{\rm d}_0$) can be derived as follows:

$$v^{\rm d}_0 = \begin{cases} -v_{\rm mid} & \text{if } u_{\rm min} = |v_{\rm mid}| \\ u_{\rm min} & \text{elsewhere} \end{cases} \tag{3}$$

where $u_{\rm min} = \min(\frac{V_{\rm dc}}{2} - v_{\rm max}, |v_{\rm mid}|, \frac{V_{\rm dc}}{2} + v_{\rm min})$.

C. Phase Opposite Deposition PWM

The PODPWM uses two carriers with opposite deposition to synthesize the voltage output, and the pulse pattern is shown in Fig. 3(b) [10], [11]. As the figure indicates, this method can effectively reduce CMV levels to $\pm V_{\rm dc}/6$, but there is a risk in

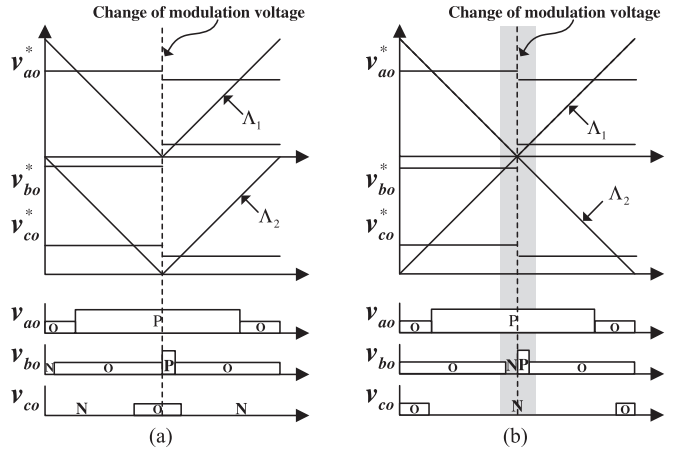

Fig. 5. Modulation operation when the modulation voltages are changed. (a) PDPWM. (b) PODPWM.

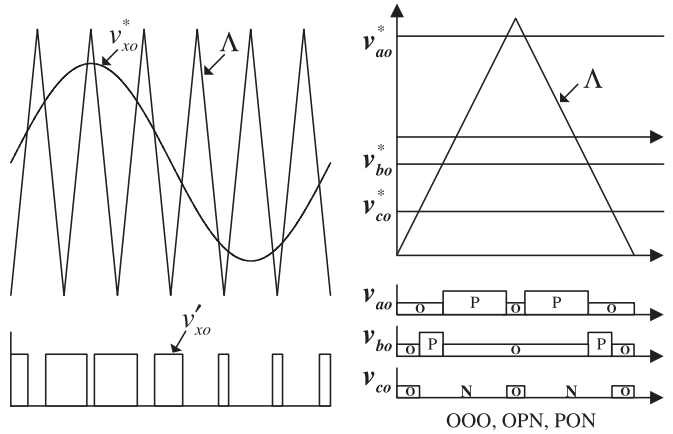

Fig. 6. Pulse pattern of CMEPWM.

switching an output for more than one voltage level when the modulation voltage is changed near zero cross point. Consequently, the switching devices may be damaged by a switching delay [12], [13]. Fig. 5 shows the modulation operation when the modulation voltage of b-phase is changed near zero cross point. Compared with the PDPWM, the b-phase voltage output of PODPWM shows a change from N to P, and two voltage levels are instantaneously switched as the modulation voltage alters.

D. Common-Mode Elimination PWM

Carrier-based CMEPWM was early presented in [5], and eliminating the CMV output can be achieved by synthesizing voltage output with the medium vectors (v). Fig. 6 shows the pulse pattern of CMEPWM, where v_{ao}, v_{bo}, and v_{co} are respectively derived as follows:

$$\begin{cases} v_{ao} = (v'_{ao} - v'_{bo})/2 \\ v_{bo} = (v'_{bo} - v'_{co})/2 \\ v_{co} = (v'_{co} - v'_{ao})/2 \end{cases} \tag{4}$$

where v'_{xo} is reference voltage derived by comparing modulation voltages with carrier (Λ). As the figure shows, this scheme

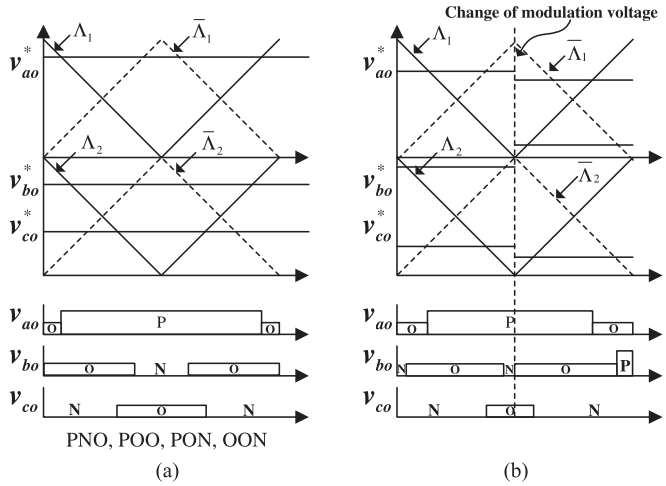

Fig. 7. Proposed ZRSPWM. (a) Pulse pattern. (b) Modulation operation when the modulation voltages are changed.

switches an output for more than once in a carrier's cycle, which increases overall switching loss, and the simultaneous switching an output for two legs is operated. Based on (4), the linear operation range is decreased to 86.6% of the conventional SPWM of NPC converter, and the NPP deviation compensation must depend on an additional circuit.

IV. Proposed ZRSPWM Scheme

Compared with two carriers (Λ_1 and Λ_2) in PDPWM, the proposed approach with four carriers (Λ_1, Λ_2, $\overline{\Lambda_1}$, and $\overline{\Lambda_2}$) can effectively avoid using the redundant states to synthesize voltage output, which $\overline{\Lambda_1}$ and $\overline{\Lambda_2}$ are respectively phase-shifted 180° from Λ_1 and Λ_2. Among the modulation voltages (v^*_{ao}, v^*_{bo}, and v^*_{co}), the maximum ($v_{\max}$) and the minimum ($v_{\min}$) are compared with a pair of carrier (Λ_1 and Λ_2), and the middle one (v_{mid}) is compared with the other pair ($\overline{\Lambda_1}$ and $\overline{\Lambda_2}$). Note that shifting the phase of carriers cannot affect volts-second balance in a switching cycle. As Fig. 7(a) shows, the middle voltage (v^*_{bo}) is compared with $\overline{\Lambda_1}$ and $\overline{\Lambda_2}$, and the others are compared with Λ_1 and Λ_2. Therefore, the generated switching states are PNO, POO, PON, and OON, which all states are not redundant. Based on Table I, these states give the further reduced CMV outputs compared with PDPWM, and the CMV output is reduced to $V_{\mathrm{dc}}/6$.

In addition, the proposed scheme can adequately adjust 19 switching states to address the NPP deviation issue, and avoid switching an output for two voltage levels in effect since the same pair of carriers are used for zero cross-point switching, as shown in Fig. 7(b).

V. Compensation for NPP Deviation

Zero sequence injection (ZSI) provides an effective solution for NPP deviation compensation [19]–[23], and this compensation signal (v_0) can be designed as follows:

$$v_0 = \mathrm{sgn}(v_0)|v_0|, \text{ where } \mathrm{sgn}(v_0) = \begin{cases} 1 & \text{if } v_0 > 0 \\ -1 & \text{if } v_0 \le 0 \end{cases}. \tag{5}$$

$|v_0|$ and sgn(v_0) respectively represent the magnitude and polarity of v_0, and sgn(v_0) can be defined as follows:

$$\begin{aligned}&\text{sgn}(v_0) = \text{sgn}(\Delta v_{\text{dc}})\text{sgn}(i_p)\\&\text{where } \Delta v_{\text{dc}} = v_{\text{dcup}} - v_{\text{dcdn}}, \text{and } i_p = \sum_{x=a,b,c} \text{sgn}(v_{xo}^*) i_x.\end{aligned} \tag{6}$$

Notice that i_p significantly affects the performance and polarity of NPP compensation, and the detail is shown in [23].

Moreover, v_0 must be bounded to prevent side effects, like overmodulation and opposite NPP compensation polarity, and the boundaries of PWM schemes are respectively calculated as follows.

The boundaries of PDPWM are shown as follows:

$$\begin{cases} v_0^{\text{ub}} = \frac{V_{\text{dc}}}{2} - \max(v'_{ao}, v'_{bo}, v'_{co}) \\ v_0^{\text{lb}} = -\min(v'_{ao}, v'_{bo}, v'_{co}) \end{cases}$$
$$\text{where } v'_{xo} = (v_{xo}^* + V_{\text{dc}}/2) \text{mod}(V_{\text{dc}}/2). \tag{7}$$

Note that v_0^{ub} and v_0^{lb} respectively represent the upper and lower boundaries, and v'_{xo} is considered for boundaries in order to keep sgn($v_{xo}^* + v_0$)=sgn(v_{xo}^*).

Compared with PDPWM, the ZSI of PODPWM and ZRSPWM must be bounded with an additional limit to keep a reduced CMV after ZSI, and v_0^{ub} and v_0^{lb} of both schemes are respectively expressed as follows.

A. PODPWM

$$\begin{aligned}&\text{If } v_{\text{mid}} > 0\\&\quad v_0^{\text{ub}} = \min\left(-\frac{v_{\text{mid}} + v_{\text{min}}}{2}, \frac{V_{\text{dc}}}{2} - v_{\text{max}}\right)\\&\quad v_0^{\text{lb}} = -v'_{\text{min}}\\&\text{If } v_{\text{mid}} \le 0\\&\quad v_0^{\text{ub}} = \frac{V_{\text{dc}}}{2} - v'_{\text{max}}\\&\quad v_0^{\text{lb}} = \max\left(-\frac{v_{\text{mid}} + v_{\text{max}}}{2}, -v_{\text{min}}\right).\end{aligned} \tag{8}$$

B. ZRSPWM

$$\begin{aligned}&\text{If } v_{\text{mid}} > 0\\&\quad v_0^{\text{ub}} = \min\left(\frac{V_{\text{dc}}}{4} - \frac{v'_{\text{mid}} + v'_{\text{min}}}{2}, \ \frac{V_{\text{dc}}}{2} - v'_{\text{max}}\right)\\&\quad v_0^{\text{lb}} = -v'_{\text{min}}\\&\text{If } v_{\text{mid}} \le 0\\&\quad v_0^{\text{ub}} = \frac{V_{\text{dc}}}{2} - v'_{\text{max}}\\&\quad v_0^{\text{lb}} = \max\left(\frac{V_{\text{dc}}}{4} - \frac{v'_{\text{mid}} + v'_{\text{max}}}{2}, \ -v'_{\text{min}}\right)\end{aligned} \tag{9}$$

where $v'_{\text{max}} = \max(v'_{ao}, v'_{bo}, v'_{co})$, $v'_{\text{mid}} = \text{mid}(v'_{ao}, v'_{bo}, v'_{co})$, and $v'_{\text{min}} = \min(v'_{ao}, v'_{bo}, v'_{co})$. Compared with PDPWM, ZSI in PODPWM and ZRSPWM takes more limit conditions into consideration, so the narrower ZSI range can be regulated.

In addition, there is no degree of freedom (DOF) of ZSI for CMEPWM and DPWM, so the NPP compensation cannot be achieved.

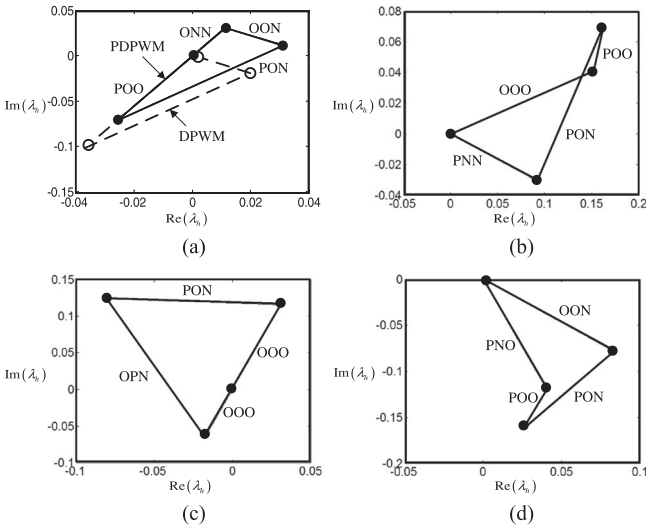

Fig. 8. Harmonic flux trajectories of PWM schemes at $\theta = 15^\circ$ and $M_i = 0.6$. (a) PDPWM and DPWM. (b) PODPWM. (c) CMEPWM. (d) ZRSPWM.

VI. Evaluation Among PWM Schemes

A. Waveform Quality

The waveform quality of current output can be investigated by harmonic flux over an Nth cycle [24], [25], which is calculated as follows:

$$\lambda_h(M_i, \theta) = \frac{\pi}{V_{\text{dc}} T_s} \int_{NT_s}^{(N+1)T_s} (V_m - V^*) dt. \tag{10}$$

Note that V_m and V^* are respectively the output voltage vector of the mth state and the modulation voltage vector, and T_s is the period of a switching cycle. Root mean square (rms) value of harmonic flux ($\lambda_{h\text{rms}}^2$) in a switching cycle can be expressed as follows:

$$\lambda_{h\text{rms}}^2(M_i, \theta) = \int_0^1 (\lambda_h)^2 d\delta \tag{11}$$

where δ stands for the duty cycle.

Fig. 8 shows the harmonic flux trajectories of the different PWM schemes at $\theta = 15^\circ$ and $M_i = 0.6$, and these flux trajectories are closely related to the switching states and the corresponding output voltage vectors. The PDPWM scheme uses four switching states to generate a triangular trajectory, where POO and ONN are the redundant states, and the DPWM and CMEPWM use three states that are not redundant to realize it. On the other hand, the trajectories of PODPWM and ZRSPWM respectively consist of four nonredundant switching states. Fig. 9 shows the comparison of the normalized rms harmonic flux among PWM schemes at different M_i. The results indicate the reduced CMVPWM schemes have larger harmonic distortion than the conventional PDPWM at two M_i, and CMEPWM outputs the less flux ripple than PODPWM and

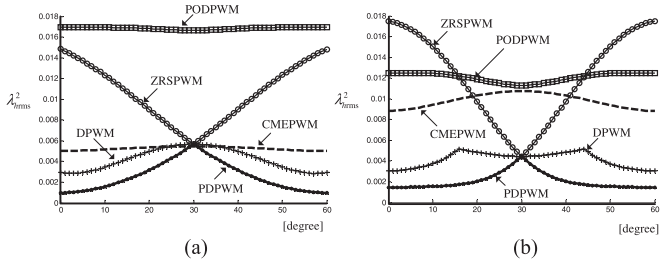

Fig. 9. Normalized RMS harmonic fluxes of PWM schemes. (a) $M_i = 0.4$. (b) $M_i = 0.65$.

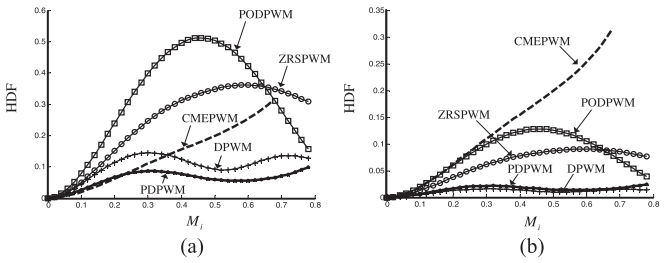

Fig. 10. HDFs of PWM schemes. (a) $K_f = 1:1:1$. (b) $K_f = 3:1:2$.

ZRSPWM. Subsequently, the PODPWM has the worse flux ripple at lower modulation index but better one at higher modulation index compared with ZRSPWM. For each modulation technique, the per fundamental cycle rms harmonic flux ($\lambda_{1f\text{rms}}$) can be expressed as a harmonic distortion function (HDF), as shown in the following equation:

$$\text{HDF} = \frac{288}{\pi^2}\lambda_{1f\text{rms}}^2, \text{ where } \lambda_{1f\text{rms}}^2 = \frac{1}{2\pi}\int_0^{2\pi} \lambda_{h\text{rms}}^2 dt. \quad (12)$$

HDF is an evaluation index of output current harmonics at different M_i, and the lower HDF represents that the smaller output filter can be chosen for current quality. Fig. 10 shows the HDFs of PWM schemes at different K_f, where K_f represents the ratio of carrier frequency among DPWM, CMEPWM, and the others (i.e., $K_f = f_{\text{DPWM}} : f_{\text{CMEPWM}} : f_{\text{other}}$).

As figures indicate, the maximum linear range of carrier-based CMEPWM is achieved at $M_i = 0.675$, but the range of other PWM schemes can reach 0.78 or above. Notice the maximum range of DPWM can be achieved at $M_i = 0.9$. The PDPWM has a superior performance in flux harmonics at different K_f and M_i. The DPWM provides the second output quality when $K_f = 1:1:1$, but it can strike a better performance than PDPWM scheme under consideration of the same switching number ($K_f = 3:1:2$). The CMEPWM provides a better output performance than PODPWM and ZRSPWM when $K_f = 1:1:1$, but there is an inferior output flux when $K_f = 3:1:2$. The ZRSPWM outputs smaller flux ripple than PODPWM when M_i is below 0.68, but the PODPWM has an better output when M_i is beyond 0.68.

B. Compensation Dynamics for NPP Deviation

Compensation dynamics of NPP is closely associated with $|v_0|$, so the maximum compensation charges can be obtained by designing v_0 at the boundaries. Then, the compensation charge ($q_c$max) in a switching cycle can be expressed as follows:

$$|q_{c\max}| = |i_p|\,|\,\mathrm{d}_{0\max}|T_s \quad (13)$$

where $d_{0\max}$ is the duty generated by the boundary of v_0, and T_s is the period of a switching cycle. In a fundamental cycle, the maximum ZSI compensation charge ($q_{1\max}$) is derived as follows:

$$q_{1\max} = \int_0^{T_1} \frac{1}{T_s}|q_{c\max}|dt \quad (14)$$

where $q_{c\max}$ represents maximum compensation charges in a switching cycle, and T_1 represents the period of a fundamental cycle. Fig. 11 shows $q_{1\max}$ of PWM schemes at different M_i and power factors (PFs). As figures indicate, $q_{1\max}$ becomes larger with PFs and M_i increasing, whose maximum can be achieved when $M_i = 0.6$ and PF=1. The PDPWM provides the most compensation charges since the available ZSI range of PODPWM and ZRSPWM are limited by the extra limitation, and this difference is more obvious at high power factor and M_i. Besides, the ZRSPWM has larger $q_{1\max}$ at low M_i than PODPWM, but they have the similar dynamics at high M_i. Note that the DPWM and the CMEPWM provide zero charges to compensate NPP deviation due to no DOF for ZSI.

Table II shows an evaluation among these PWM schemes. As the table indicates, the carrier-based CMEPWM can mostly reduce CMV output among these PWM schemes, but it cannot take full advantage of the modulation range, whose maximum modulation range is achieved only at $M_i = 0.675$. Besides, double switching an output is operated in a carrier's cycle, and simultaneous switching may also occur. Subsequently, the PODPWM and the ZRSPWM can reduce CMV output to $\pm V_{\text{dc}}/6$, and their modulation ranges can be achieved at $M_i = 0.9$ by injecting an adequate offset, which is offset-PWM. Compared with PODPWM, the ZRSPWM provides a better performance at low M_i, and switching an output for more than one level can be avoided effectively. The conventional PDPWM provides the largest CMV level but the superior output quality among five PWM schemes. The PDPWM-based DPWM can also reduce the CMV output to $\pm V_{\text{dc}}/6$, and provides the superior performance in switching number. However, the NPP compensation must also depend on the extra circuit.

VII. Laboratory Test Result

Fig. 1 shows the experimental platform, and their parameters are given in Table III. Note that the DSP is the digital signal processor (TEXAS INTRUMENT F28335), and the CPLD is complex programmable logic device (Lattice MXO2 7000E). Besides, the controller is designed in the DSP, and the carrier-based modulator is realized in the CPLD. For NPP deviation compensation, the experiment adopts the maximum charge compensation in order to evaluate the dynamics among the different schemes. The measured signals include the voltage of dc-link capacitors (v_{dcup} and v_{dcdn}), the load voltage of a-phase (v_{an}), the inductor current of a-phase (i_a), and the CMV output (v_{CM} or v_{on}).

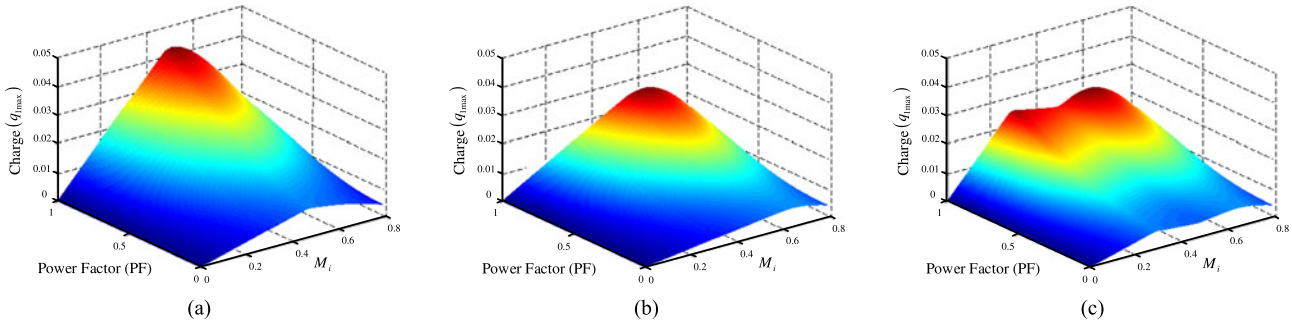

Fig. 11. Maximum compensation charges at different M_i and PFs. (a) PDPWM. (b) PODPWM. (c) ZRSPWM.

TABLE II
EVALUATION AMONG PWM SCHEMES

	PDPWM	DPWM	CMEPWM	PODPWM	ZRSPWM
CMV output	$\pm V_{\rm dc}/3$	$\pm V_{\rm dc}/6$	0	$\pm V_{\rm dc}/6$	$\pm V_{\rm dc}/6$
Linear range based on SPWM	0.78	×	0.675	0.78	0.78
Linear range based on offset PWM	0.9	0.9	0.675	0.9	0.9
Switching number over a fundamental cycle	1.5N	N	3N	1.5N	1.5N
NPP compensation	Yes(best)	No	No	Yes	Yes(better)
Switching an output for more than one level	No	No	No	Yes	No
Simultaneous switching an output for more than one leg	No	No	Yes	No	No

TABLE III
PARAMETER OF CIRCUIT

Parameter	Value	
Load	50	Ω
DC-link capacitor	2240	μF
DC bus voltage	400	V
Fundamental frequency	60	Hz
Filter inductor	2	mH
Dead time	1	μ s
Switching frequency		
DPWM	15/5	kHz
CMEPWM	5	kHz
Others	10/5	kHz

Fig. 12 shows a-phase output voltage when a 20 V change occurs at the zero cross point of modulation voltage, and the following figure shows the enlarged waveform of a-phase output voltage for PODPWM and ZRSPWM. The PODPWM scheme leads to instantaneous switching of a voltage output for more than one level (P to N), but the proposed ZRSPWM can effectively prevent this problem.

Fig. 13 shows the waveforms of the phase load voltage, the inductor current, and the CMV output for the different PWM schemes, where $M_i = 0.65$. As figures show, the CMEPWM can provide approximately zero CMV output. In addition, the DPWM, the PODPWM, and the ZRSPWM generate the reduced CMV between ±67 V ($\pm V_{\rm dc}/6$), and the PDPWM induces an inferior CMV output (± 133 V, $\pm V_{\rm dc}/3$). Fig. 14(a) shows a comparison of the current harmonics ($i^2_{h\rm rms}$) among these PWM schemes at $K_f = 1:1:1$, where $i_{h\rm rms}$ is defined as follows:

$$i^2_{h\rm rms} = \sum_{n=2} i_n^2 = \left[(\text{THD}_F)i_1\right]^2. \tag{15}$$

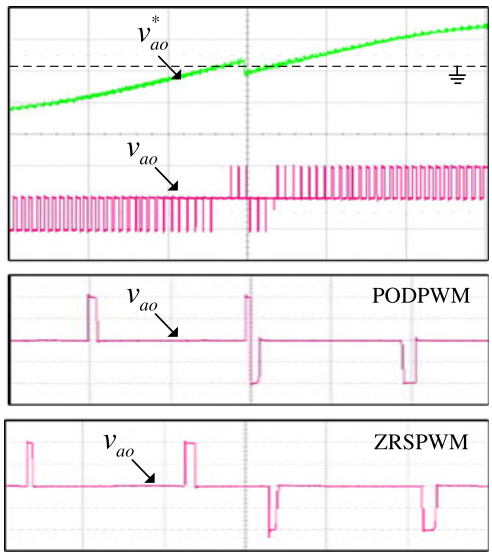

Fig. 12. Output voltage of a-phase when the modulation voltage is changed at zero cross point.

Note that i_n is the rms value of the nth harmonic current, where $n = 1$ is the fundamental frequency, and THD_F is the total harmonic distortion for the fundamental frequency. As the figure shows, the PDPWM shows a superior quality of current waveforms among these PWMs, and the PODPWM has an inferior current output. With M_i increased to 0.65, the PDPWM still keeps the best current quality among these PWMs, but the difference of the current quality among CMEPWM, PODPWM, and the ZRSPWM becomes smaller. When $M_i = 0.75$, the PODPWM has better performance in current quality than ZRSPWM. Fig. 14(b) shows a comparison of $i^2_{h\rm rms}$ among

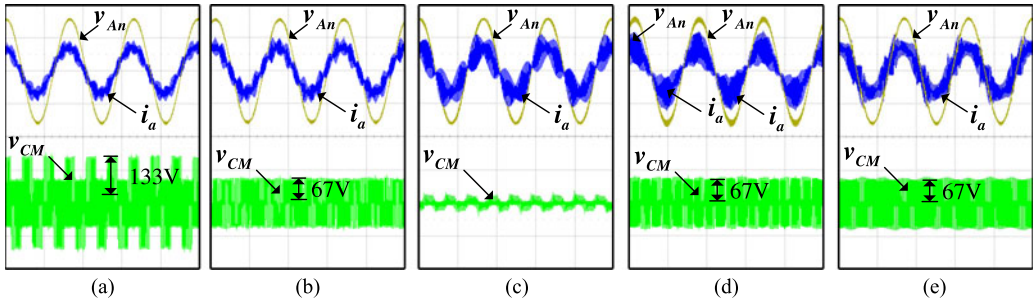

Fig. 13. Waveform of load voltage, inductor current, and CMV at $M_i = 0.65$. (a) PDPWM. (b) DPWM. (c) CMEPWM. (d) PODPWM. (e) ZRSPWM. Scales: $v_{\rm an}$: 100 V/div, i_a: 5 A/div, $v_{\rm CM}$: 100 V/div, and 5 ms/div.

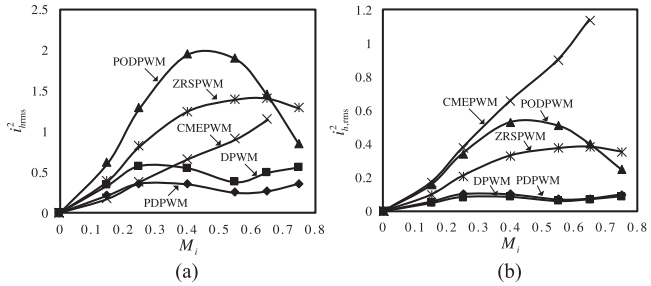

Fig. 14. Numerical result of current harmonics ($i_{h\,\rm rms}$) at different M_i. (a) $K_f = 1:1:1$. (b) $K_f = 3:1:2$.

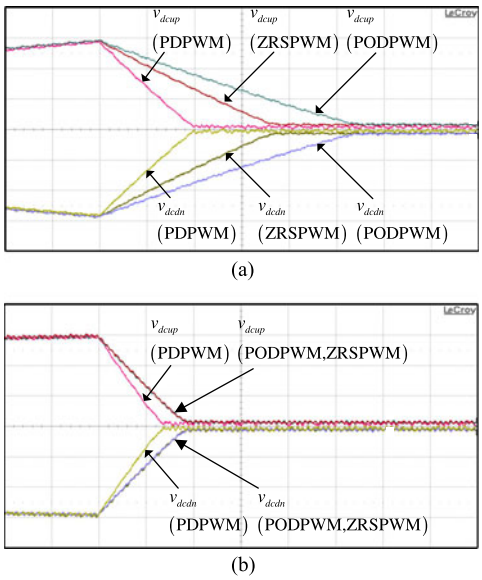

Fig. 15. Dynamics of NPP deviation compensation with maximum charges for different PWM schemes. (a) $M_i = 0.4$. (b) $M_i = 0.65$. Scales: $v_{\rm dcup}$: 10 V/div, $v_{\rm dcdn}$: 10 V/div, and 50 ms/div.

these PWM schemes at $K_f = 3:1:2$. In such case, the same switching number is considered for each PWM scheme, and the DPWM has more improved results than PDPWM due to higher switching frequency. Besides, the PODPWM and the ZRSPWM provide a better current quality compared with CMEPWM.

Fig. 15 illustrates the dynamics of NPP deviation compensation with the maximum charges for the different PWM schemes. The results clearly indicate the dynamics are closely related to the PWM strategies and their available ZSI range. Both of PODPWM and ZRSPWM provide more limited ZSI range than PDPWM, and result in less $q_{1\max}$, so their NPP compensation dynamics are slower. In addition, the PODPWM has worse dynamics than ZRSPWM at $M_i = 0.4$, but they have the similar NPP compensation dynamics at $M_i = 0.65$. These results are consistent with the evaluation in Section VI, and they can be supported to validate aforementioned analysis.

VIII. Summary

This paper proposes a ZRSPWM scheme to reduce CMV output by using four carriers to synthesize the output voltage, and all switching states in this scheme are not redundant, namely ZRSPWM. Besides, an comparison with the conventional PWM strategies is presented to evaluate their performance. Among these PWM schemes, the PDPWM provides the larger CMV output but the superior performance in the current quality and the NPP compensation. The PDPWM-based DPWM can reduce the CMV output to $\pm V_{\rm dc}/6$, but the NPP compensation must depend on an additional circuit. In addition, the CMEPWM provides zero CMV output, but the linear modulation range and the NPP compensation must be traded off. The PODPWM and the proposed ZRSPWM give substituted strategies to reduce CMV output, and overcome the disadvantages of the CMEPWM, but their CMV output are reduced to only $\pm V_{\rm dc}/6$. Besides, the proposed ZRSPWM can effectively avoid switching an output for more than one level compared with PODPWM, and provide better performance in NPP compensation. Finally, the laboratory test results are presented to validate the aforementioned evaluation.

References

[1] A. Nabae, I. Takahashi, and H. Akagi, "A new neutral-point-clamped PWM inverter," *IEEE Trans. Ind. Appl.*, vol. IA-17, no. 5, pp. 518–523, Sep. 1981.

[2] B. P. McGrath, D. G. Holmes, and T. Lipo, "Optimized space vector switching sequences for multilevel inverters," *IEEE Trans. Power Electron.*, vol. 18, no. 6, pp. 1293–1301, Nov. 2003.

[3] B. P. McGrath, D. G. Holmes, and T. Lipo, "Optimized space vector switching sequences for multilevel inverters," *IEEE Trans. Power Electron.*, vol. 18, no. 6, pp. 1293–1301, Nov. 2003.

[4] J. M. Erdman, R. J. Kerkman, D. W. Schlegel, and G. L. Skibinski, "Effect of PWM inverters on ac motor bearing currents and shaft voltages," *IEEE Trans. Ind. Appl.*, vol. 32, no. 2, pp. 250–259, Mar./Apr. 1996.

[5] H. Zhang, A. Von Jouanne, S. Dai, A. K. Wallace, and F. Wang, "Multilevel inverter modulation schemes to eliminate common-mode voltages," *IEEE Trans. Ind. Appl.*, vol. 36, no. 6, pp. 1645–1653, Nov./Dec. 2000.

[6] A. Bendre, S. Krstic, J. Vander Meer, and G. Venkataramanan, "Comparative evaluation of modulation algorithms for neutral-point-clamped converters," *IEEE Trans. Ind. Appl.*, vol. 41, no. 2, pp. 634–643, Mar./Apr. 2005.

[7] R. Cuzner, A. Bendre, P. Faill, and B. Semenov, "Implementation of a four-pole dead-time-compensated neutral-point-clamped three-phase inverter with low common-mode voltage output," *IEEE Trans. Ind. Appl.*, vol. 45, no. 2, pp. 816–826, Mar. 2009.

[8] X. Zhang, D. Boroyevich, R. Burgos, P. Mattavelli, and F. Wang, "Impact and compensation of dead time on common mode voltage elimination modulation for neutral-point-clamped three-phase inverters," in *Proc. IEEE ECCE Asia Downunder*, Jun. 2013, pp. 1016–1022.

[9] L. Kai, J. Zhao, W. Wu, M. Li, L. Ma, and G. Zhang, "Performance analysis of zero common-mode voltage pulse-width modulation techniques for three-level neutral point clamped inverters," *IET Power Electron.*, vol. 9, no. 14, pp. 2654–2664, 2016.

[10] G. Carrara, S. Gardella, M. Marchesoni, R. Salutari, and G. Sciutto, "A new multilevel PWM method: A theoretical analysis," *IEEE Trans. Power Electron.*, vol. 7, no. 3, pp. 497–505, Jul. 1992.

[11] V. G. Agelidis and M. Calais, "Application specific harmonic performance evaluation of multicarrier PWM techniques," in *Proc. 29th Annu. IEEE Power Electron. Spec. Conf.*, vol. 1, May 1998, pp. 172–178.

[12] H.-J. Kim, H.-D. Lee, and S.-K. Sul, "A new PWM strategy for common-mode voltage reduction in neutral-point-clamped inverter-fed ac motor drives," *IEEE Trans. Ind. Appl.*, vol. 37, no. 6, pp. 1840–1845, Nov./Dec. 2001.

[13] X. Zhang, D. Boroyevich, and R. Burgos, "Hybrid modulation for neutral point voltage ripple reduction in dc-fed three-level motor drive systems," in *Proc. 9th Int. Conf. Power Electron. ECCE Asia*, Jun. 2015, pp. 274–280.

[14] X. Yuan, Y. Li, and C. Wang, "Objective optimisation for multilevel neutral-point-clamped converters with zero-sequence signal control," *IET Power Electron.*, vol. 3, no. 5, pp. 755–763, Sep. 2010.

[15] X. Yuan, J. Yon, and P. Mellor, "Common-mode voltage reduction in three-level neutral-point-clamped converters with neutral point voltage balance," in *Proc. IEEE Int. Symp. Ind. Electron.*, May 2013, pp. 1–6.

[16] H. Alawieh, K. A. Tehrani, Y. Azzouz, and B. Dakyo, "A new active common-mode voltage elimination method for three-level neutral-point clamped inverters," in *Proc. 40th Annu. Conf. IEEE Ind. Electron. Soc.*, Oct. 2014, pp. 1060–1066.

[17] M. J. Ferdous, S. Kabir, M. R. A. Siddique, and U. Salma, "Split inductor based neutral point clamped inverter using improved modulation technique to reduce common mode voltage," in *Proc. 8th Int. Conf. Elect. Comput. Eng.*, Dec. 2014, pp. 623–626.

[18] T.-K. Tu Nguyen, N.-V. Nguyen, and N. R. Prasad, "Novel eliminated common-mode voltage PWM sequences and an online algorithm to reduce current ripple for a three-level inverter," *IEEE Trans. Power Electron.*, vol. 32, no. 10, pp. 7482–7493, Oct. 2017.

[19] S. Ogasawara and H. Akagi, "Analysis of variation of neutral point potential in neutral-point-clamped voltage source PWM inverters," in *Proc. IEEE Ind. Appl. Soc. Annu. Meeting*, Oct. 1993, vol. 2, pp. 965–970.

[20] N. Celanovic and D. Boroyevich, "A comprehensive study of neutral-point voltage balancing problem in three-level neutral-point-clamped voltage source PWM inverters," *IEEE Trans. Power Electron.*, vol. 15, no. 2, pp. 242–249, Mar. 2000.

[21] K. Yamanaka, A. M. Hava, H. Kirino, Y. Tanaka, N. Koga, and T. Kume, "A novel neutral point potential stabilization technique using the information of output current polarities and voltage vector," *IEEE Trans. Ind. Appl.*, vol. 38, no. 6, pp. 1572–1580, Nov./Dec. 2002.

[22] H. Akagi and T. Hatada, "Voltage balancing control for a three-level diode-clamped converter in a medium-voltage transformerless hybrid active filter," *IEEE Trans. Power Electron.*, vol. 24, no. 3, pp. 571–579, Mar. 2009.

[23] M.-J. Tsai, M.-R. Tsai, H.-C. Chen, Y.-B. Wang, and P.-T. Cheng, "A modulation technique of neutral point clamped converters with common-mode voltage reduction and neutral-point potential balance," in *Proc. IEEE Energy Convers. Congr. Expo.*, Sep. 2016, pp. 1–7.

[24] A. M. Hava, R. J. Kerkman, and T. A. Lipo, "Simple analytical and graphical methods for carrier-based PWM-VSI drives," *IEEE Trans. Power Electron.*, vol. 14, no. 1, pp. 49–61, Jan. 1999.

[25] C.-C. Hou, C.-C. Shih, P.-T. Cheng, and A. M. Hava, "Common-mode voltage reduction pulsewidth modulation techniques for three-phase grid-connected converters," *IEEE Trans. Power Electron.*, vol. 28, no. 4, pp. 1971–1979, Apr. 2013.

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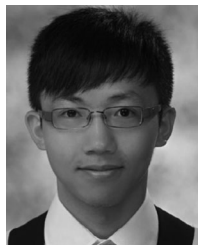

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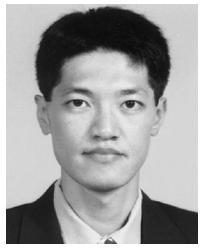

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