Characterization of a Countercurrent Injection-Based HVDC Circuit Breaker

René Sander, Michael Suriyah, *Member, IEEE*, and Thomas Leibfried, *Member, IEEE*

***Abstract*—The scope of this paper is a precise analysis of countercurrent injection-assisted HVDC circuit breaking. The considered topology consists of an outer diode rectifier for unipolar switching operations and an inner power electronic circuit breaker built using series-connected resonant circuits, which combine the Marx generator principle for voltage scaling and existing thyristor commutation circuitry for enhanced IGCT turn off. Toward the integration of an HVDC system, comparatively unique application demands such as current stresses, energy absorption characteristics, or transient voltage resilience during breaking operations require the evaluation of its fitness, including individual component rating limitations. Therefore, the characterization of the breaker's switching behavior at relevant abstraction levels is undertaken within this work, giving a detailed overview of technical features and even some specific dimensioning criteria. The advantageous features of the associated proposal in terms of adaptability are investigated, and the opportunity for an increase in the breaker's maximum current interruption capability is thereby outlined. General realization challenges are highlighted and verified by simulations using MATLAB Simulink and PLECS Blockset.**

***Index Terms*—Charge injection devices, dc circuit breakers (CB), dc power transmission, HVDC circuit breakers, pulse circuits.**

I. Introduction

THE integration of renewable energy sources into naturally grown electrical grids causes fluctuating in-feed power, which results in additional demand for flexibility in power transmission. Beyond conventional FACTS, VSC-HVDC Multi-Terminal-Systems (MTS) satisfy this need and provide further opportunities to offer promising grid stabilizing services.

The expansion of MTS is closely related to economic perspectives, which are influenced by the impact on ac grid stability in matters of realizing the "N−1 criterion" and derived necessities for additional spare capacities. This consequently increases sensitivity to dc side disturbances. At some point, ac transmission capacity will no longer be able to compensate for ordinary power outages within reasonable redundancy provisions. Then, ac grid stability also demands the reliable and prompt isolation of faulty parts on the dc side, helping to keep healthy transmission capacities online. HVDC Circuit Breakers (CBs) are a key element in the realization of fast and selective dc fault clearing. However, CBs have to cope with high voltage and high current stresses. This motivates a careful discussion of their feasibility.

Mechanical switching configurations from earlier proposals, which were mainly developed in the 1980s, do not meet current requirements for VSC HVDC. Clearing times and switching capabilities have been very limited [1]. A more recent concept presented in [2] shows test results with reduced opening times and an auxiliary circuit for countercurrent injection. Although faster zero-current crossings are achieved due to the use of capacitor discharge instead of passive resonant circuits, interruption problems for lower currents raise questions concerning reliability, and general usability of this scheme. Therefore, an enhanced solution with reduced breaking failure probability is achieved using a saw-tooth-shaped current injection, according to [3].

Despite improved motion drives and related mechanical breaking, where voltage insulation scalability and performance require detailed empirical evaluation for each advancement, the (statistical) predictability and modularization of semiconductor solutions may offer a beneficial simplified alternative. The realization of dc CBs in hybrid design, as proposed in [4] and refined for HVDC in [5], provide a general solution for acceptably low operation losses. Those breakers consist of an auxiliary breaker (AB) with a fast disconnector (FD) and load commutation switch (LCS) as well as a main breaker (MB) connected in parallel for final current interruption. A variety of power electronic breaker concepts based on this principle have been proposed, for example, in [5], [6] and [7].

In general, HVDC CBs must offer two basic features during breaking: the establishment of a dielectric withstand strength, which is equal to the system's protective voltage level and a reduction of the inductive current down to zero. One solution is the use of common high-power semiconductors and parallel-connected varistors for a simple implementation of the MB. Metal-oxide surge arresters can absorb magnetic field energy, realize predetermined voltage limitation and, therefore, suit both requirements. However, according to [8] and [9], metal-oxide varistors call for detailed knowledge of the expected material lifetime in order to guarantee an appropriate rating. The nonuniformity and characteristic stress dependencies of failure modes are major concerns in the individual application stress evaluation of ZnO varistors, as discussed in [10], [11], and [12]. Moreover, a careful consideration of the transmission line type within HVDC systems (overhead line, cable) and its ability to cope with polarity reversal should be undertaken. Both together might require a closer look at polarity selective fault clearing, as discussed in [13].

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The authors are with the Institute of Electric Energy Systems and High-Voltage Technology, Karlsruhe Institute of Technology, Karlsruhe 76131, Germany (e-mail: rene.sander@kit.edu; michael.suriyah@kit.edu; thomas.leibfried@kit.edu).

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In general, the dominating influences of the switching process as a source of transient voltage occurrence are the breaker's fault current limiter within the prebreaking phase, which is commonly proposed to be implemented using air-coils, and the arrester arrangement responsible for postbreaking behavior. Unless considering the fault-ride-through of a half-bridge MMC for STATCOM operation during a fault [14], specifications for this series-connected inductor result from the breaker's maximum turn-off capability and the expected maximum driving voltage. Whether the driving voltage equals the rated system voltage level [5], which is essentially the worst-case estimation, or a lower value which takes into consideration additional system characteristics, is a matter of short-circuit forecasting ability. Aspects such as the expected capacitive line discharge (overhead line or cable) and the converter design (full-bridge or half-bridge, arm inductor size, etc.) of nearby substations influence its behavior, as discussed in [15], [16], and [17].

Furthermore, during short-circuit situations, transients with peak values of up to a multiple of the rated converter current are expected. Consequently, this results in a rapid and pronounced temperature rise in semiconductor components; these are required to withstand this at least several hundred times without maintenance work. A highly robust thermal cyclic stability is therefore demanded, although good congruence of lifetime forecasts and failure rates is hard to obtain in this field. The operation conditions of HVDC CBs are fundamentally different from those of conventional converters. The maximization of breaking power through the use of turn-off abilities, for example, close to an IGBT saturation current, and in particular the short-term operation beyond conventional thermal cycling, raise questions as to whether commonly used testing procedures allow the simple extrapolation of lifetime forecasts to this field of application, or might involve at least a certain ambiguity. In addition to this, specific HVDC grid structures and algorithms for trip commands are generally unpredictable, meaning that stress forecasts of ordinary switching operations are rather imprecise.

The competitiveness of a specific design can be initially assessed using aspects of quality such as performance, reliability, and costs. Taking into account the abovementioned uncertainties, the assumption that HVDC CBs generally experience a greater variety of degradation phenomena than common ac CBs is natural. Consequently, a fundamental question in HVDC CB design considerations concerns the lifetime predictability and, as a previous step, the specification of performance characteristics. However, an evaluation of introduced breaker topologies at abstraction levels other than the top layer is generally absent. Following the detailed evaluation of Gate-Commutated-Thyristors (GCT) for use in medium voltage ac CBs as presented in [18], their application in HVDC should be considered. In this paper, the countercurrent injection-based hybrid HVDC CB concept presented in [19] using Integrated-GCT (IGCT) switches is examined in detail, with the aim of identifying performance characteristics and challenges in technical realization.

II. HVDC CB System Design

An overview of the hybrid HVDC CB examined in this paper is given in Fig. 1(a). By opening the AB, the current is commutated into the MB and concurrently rectified. The AB consists of

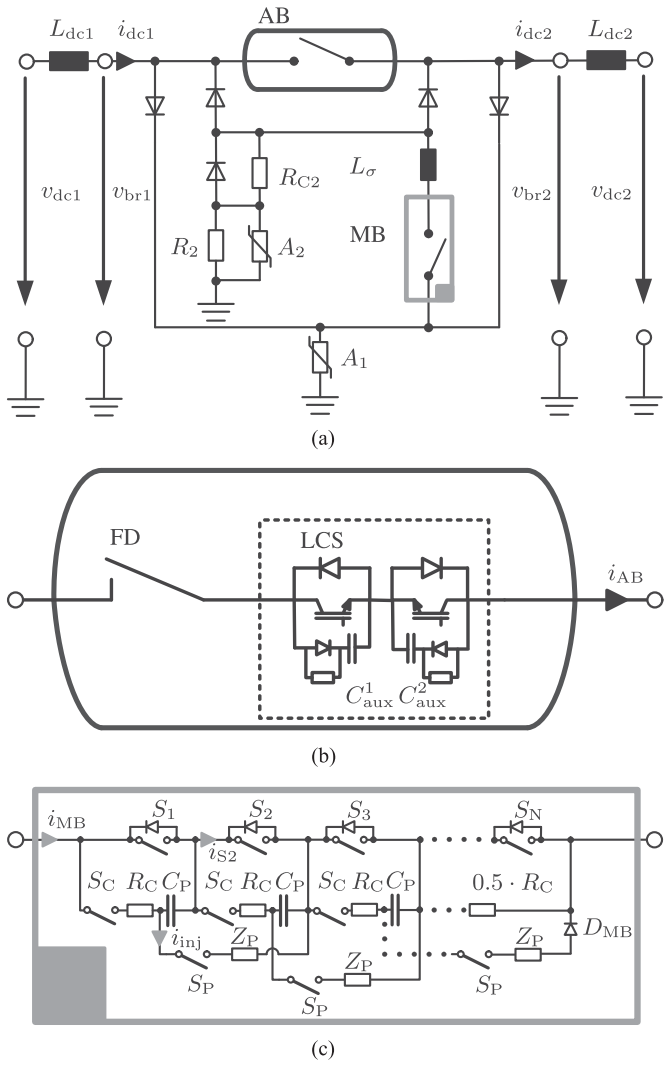

Fig. 1. HVDC CB design proposal. (a) Outer HVDC CB circuit [19]. (b) AB with LCS and FD [5], [20]. (c) MB design [19].

a FD and a series-connected LCS as shown in Fig. 1(b). In [20], a technical assessment of several LCS is made, in which the presented alternatives to the integrated RCD snubber may offer improvements in terms of unintended capacitor discharge during closing operations. However, in this paper, a nonoptimized frame is used for simplification purposes, since the opening operations are not (greatly) affected by the LCS design, and the closing attempts are not the main subject of this paper.

The inductor L_σ represents a parasitic inductance within the commutation path between AB and MB. A knowledge of this specific parameter is necessary for evaluation of the two breaker commutation processes.

The key element of any hybrid HVDC CB design is its MB, which commutates the dc current into energy absorbers in which full transient currents and voltages occur. Therefore, the design proposal shown in Fig. 1(c) uses a countercurrent injection path, which reduces the dc current to values within the turn-off capability of the applied IGCT $S_X, X \in [1, N]$. The current impulse itself is generated using an auxiliary circuit consisting of a capacitor, a turn-on switch, and an enclosed (distributed) ohmic-inductive impedance. This arrangement additionally in-

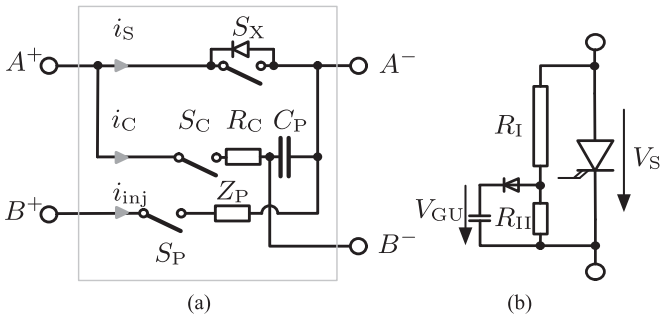

Fig. 2. Possible breaker implementation. (a) SBC of the MB. (b) Device supply.

cludes an integrated charging path and can be realized by series-connected Single Breaker Cells (SBC) according to Fig. 2(a); thus, enabling adaptive voltage scaling.

The switches S_P within the MB can be implemented in various ways, while the basic functionality of the interruption process remains the same. Triggered spark gaps or pulse thyristors are suitable examples. For a proper turn-off, low-current IGBTs S_C can be placed in the charging path, providing additional control opportunities for the energizing process.

The power consumption of individual semiconductor driver units is very low, due to the mostly passive operational state of the breaker. This offers further opportunities for supply such as proposed in Fig. 2(b) using typical grading resistors for voltage division. SBCs with relatively low voltage rating could even realize power supply using energy extraction from the pulse capacitor, which acts as a voltage source during the charged state.

III. Breaker Functionality

A. Interruption Process at Breaker Level

The inner interruption process is divisible into the commutation process from the AB to the MB at the moment the LCS is activated and afterward the commutation between the MB and related energy absorbers, which in this case is provoked by a countercurrent injection-assisted switching operation.

The time for commutation of the current into the MB is naturally specified by the AB's countervoltage and the inherent circuit impedance, which includes at least a parasitic inductance L_σ of the connectors involved. The specifications for semiconductors within the MB must be considered; in case of IGCTs, these particularly limit the rate of current rise. Therefore, the integration of additional air coils or the increase of RCD snubber capacitor size C_aux within the LCS describe optimizing parameters for handling the AB current i_AB according to

$$\frac{\mathrm{d}i_\mathrm{MB}}{\mathrm{d}t} = \frac{i_\mathrm{AB}}{\sqrt{L_\sigma \cdot C_\mathrm{aux}}} \cdot \sin\left(\frac{t}{\sqrt{L_\sigma \cdot C_\mathrm{aux}}}\right). \tag{1}$$

Alternatively, a reduced commutation voltage level and resulting commutation speed limitation can be achieved using surge arresters, as proposed in [7].

In terms of a proper breaking operation of the MB, the current must be commutated into parallel energy absorbers with their characteristic voltage protection levels. The MB therefore has to establish an appropriate insulation voltage, which is realized by IGCT blocking in this case. However, its limited turn-off current may require enhanced switching power in HVDC CB applications, and therefore, guides to the abovementioned turn-off support.

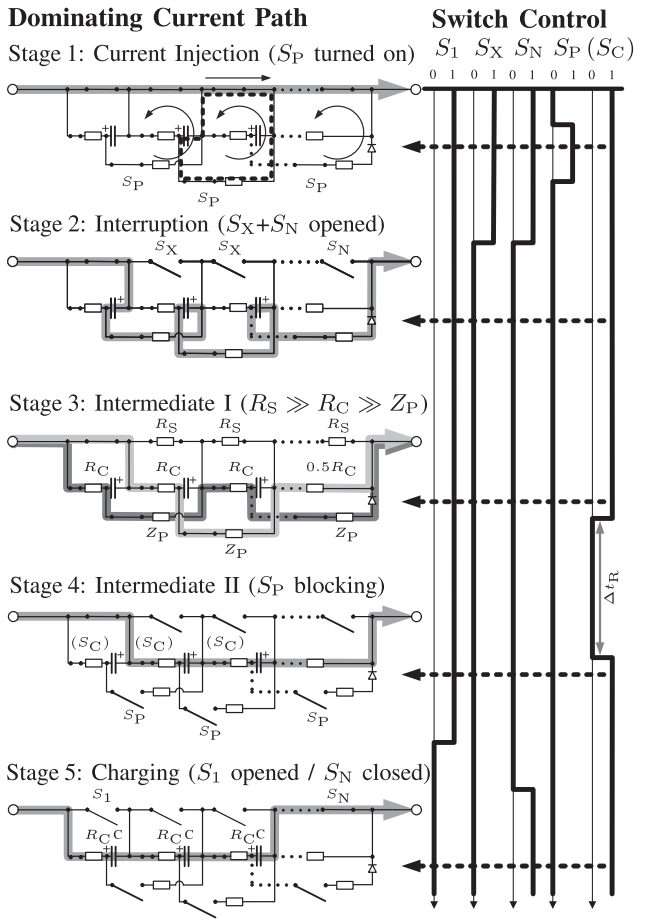

Fig. 3. Conduction paths and switching sequence of MB during interruption ($X \in [2, N-1]$).

The chronological order of switching stages and control commands within the interruption process is given in Fig. 3.

Stage 1: Turn off is initiated by closing all turn-on switches S_P. Thus, a resonant circuit is created, which consists of precharged capacitors C_P and the dominating ohmic-inductive impedances Z_P characterized by R_P and L_P, as shown in Fig. 1(c). The IGCT current stress will be lowered by superposition of the opposed currents and after an assigned time period, defined by the resonant circuit itself, the total IGCT current reaches its minimum, as shown in the uppermost curve of Fig. 4. At that moment, a turn-off signal is sent to the power electronic devices S_X ($X \in [2, N-1]$).

Stage 2: According to Stage 2, an internal current commutation takes place. The current is forced into an alternative path (compare Fig. 3). Since the charging resistors R_C are significantly higher than Z_P the fault current results in reversed capacitor charging. Its voltages v_C decrease approximately linearly to a value of about -40 kV as shown in Fig. 4. Its rate of rise is characterized by the capacitance and interruption current. Thus, the applied (derived) voltage stresses of the cell components can be limited and the mutual cell voltage balancing during the transient slope ensured. The resulting overall MB voltage then

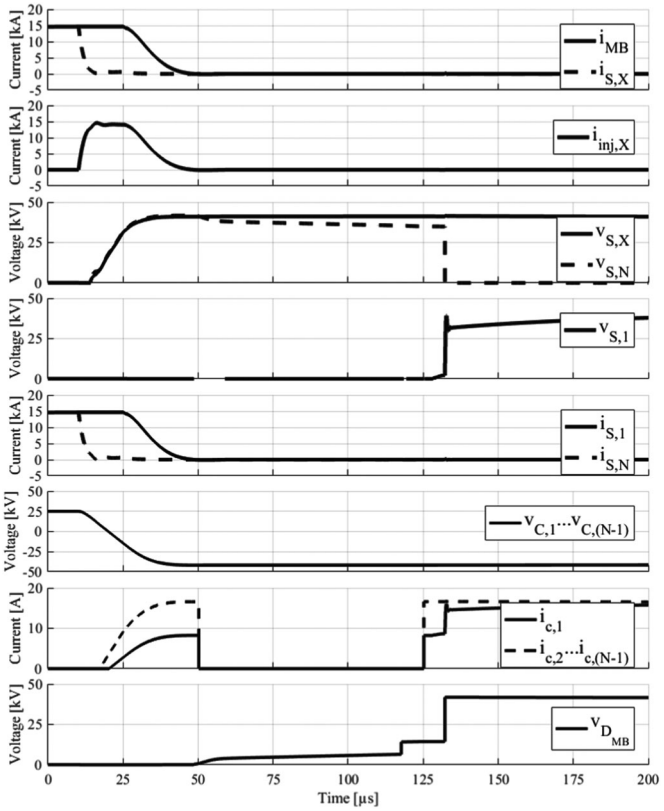

Fig. 4. Voltages and currents during breaking (from top to bottom: currents within S_{X} and MB; current within S_{P}; voltages over $S_{\mathrm{X}}\,(X \in [2, N-1])$ and S_{N}; voltage over S_1; currents within S_1 and S_{N}; voltages over $C_{\mathrm{j}}(j \in [1, N-1])$; charging currents [compare Fig. 2(a)] and voltage over D_{MB}).

drives the final commutation into related energy absorbers A_1 and A_2 by exceeding their OVP Level. At this point, the current i_{MB} starts decreasing, which finishes approximately 25 μs after IGCT turn off. Its duration mainly depends on the parasitic inductance L_σ, the resulting capacitor size of the $N-1$ series-connected capacitors C_{P} and the applied fault current. At this point, it should be noted that S_1 remains in on state until commutation is over, since this switch has no associated injection cell.

Stage 3: An additional switch S_{C} with marginal current carrying capability could be integrated, if S_{P} is based on turn-on switches such as spark gaps or thyristors, and expected stray currents become too high to pass them over into the blocking state. These two currents, which are almost balanced, pass through switches S_{P}, as shown in Stage 3 Intermediate I in Fig. 3. Switch S_{C} carries out the interruption of unintended stray currents, whereas for $Z_{\mathrm{P}} \ll R_{\mathrm{C}} \ll R_{\mathrm{S}} - R_{\mathrm{S}}$ represents the IGCT blocking resistance—the resulting steady-state turn-off currents can be approximated by

$$i_\sigma \approx \frac{v_{\mathrm{brX}}}{0.5 \cdot R_{\mathrm{C1}} + R_{\mathrm{C2}}}. \tag{2}$$

The recovery time of S_{P} characterizes the minimum duration Δt_{R} for which the switches S_{C} have to remain turned OFF.

Stage 4: The current i_{MB} has been successfully commutated and the injector switches S_{P} have recovered the blocking state. The last Breaker Cell includes an additional diode D_{MB} and a reduced resistor with half the value of the other charging resistors. The reason for these measures is due to the Intermediate Stage II. The (re-)charging current is almost doubled by the reverse-charged capacitors, and the resulting voltage drop across the resistor is also doubled. However, the cell's clamping voltage is compensated by the capacitor. Without a capacitor, the last Breaker Cell voltage would consequently remain twice as high, and the insulation voltage of S_{N} would need to be adapted. In order to avoid a cost-intensive adjustment of S_{N}, the resistor value is lowered. Again, the diode avoids an uncontrolled discharge of the capacitor of the second last Breaker Cell number $N-1$ at the moment S_{N} is closed. Thus, this diode is only necessary if a reverse conducting semiconductor switch is applied for S_{P}. Finally, the last switching operation results in first opening S_1 and then closing S_{N} to avoid overvoltages at the remaining switches S_2 to $S_{\mathrm{N}-1}$.

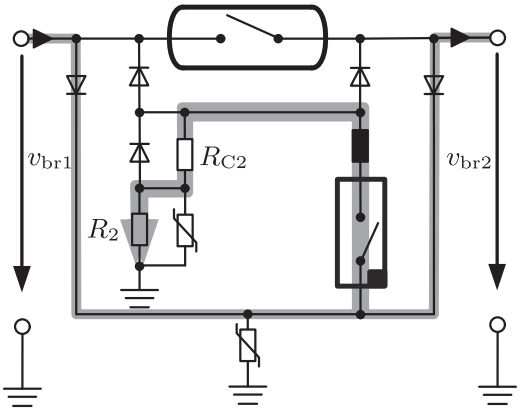

Fig. 5. Outer charging circuit supplied by v_{br1} and/or v_{br2}.

Stage 5: The final charging stage is activated again. This means that the breaker is opened and becomes re-energized. The inner circuit integrates a passive path to charge its injection capacitors C_{P}. During the charging process, a conduction path is developed according to Stage 5 in Fig. 3 and the outer circuit according to Fig. 5; this requires at least one connected line to be energized to the normal system operation voltage level. The resulting *RLC* circuit is driven with its voltage v_{brX} (v_{br1} or v_{br2}, respectively). Its charging time is determined according to relevant impedances by

$$\Delta t_{\mathrm{C}}\,(95\%) = 3 \cdot \tau_{\mathrm{C}} = 3 \cdot \frac{C_{\mathrm{p}}}{N-1}\,(R_{\mathrm{C1}} + R_{\mathrm{C2}} + R_2) \tag{3}$$

where $R_{\mathrm{C1}} = (N - 0.5) \cdot R_{\mathrm{C}}$. For adequate decoupling, R_C must be designed for relatively fast charging regarding a (re-) closure attempt and slow discharging in the MB conduction state. During a short-circuit situation, an unintended capacitor discharge occurs as given by

$$\Delta v_{\mathrm{C}} = v_{\mathrm{C}} \cdot \left[1 - \exp\left(-\frac{\Delta t}{R_{\mathrm{C}} C_{\mathrm{P}}}\right)\right] \tag{4}$$

within the time period Δt in which the MB is conducting. This must be considered for proper dimensioning.

The demand for open-close-open switching operations, as generally known from ac applications, may require a fast reaction of a HVDC CB device. The duration for arc extinction of overhead line flashovers and subsequent system voltage recovery can be considered a reasonable benchmark for the (re-) energization time of the MB, whereas expected voltage oscillations on the transmission line after a breaking event indicate

TABLE I
SIMULATION PARAMETERS

Parameter	Value	Description
N	21	Number of SBCs
V_{dc}	500 kV	Rated system voltage
A_1	750 kV	OVP Level of incoming current
A_2	40 kV	OVP Level of outgoing current
$L_{\mathrm{dc1}}, L_{\mathrm{dc2}}$	50 mH	Air coil
R_2	4 Ω	Pulse resistor rated to A_2
L_σ	15 μH	Stray inductance of MB
C_{aux}	10 μF	Snubber capacitor of LCS
Δt_{FD}	$<$ 2 ms [21]	Opening time of FD
C_{P}	4.8 μF	Capacitor of pulse circuit
R_{P}	1.3 Ω	Resistance of pulse circuit
L_{P}	3.3 μH	Inductance of pulse circuit
$(di_{\mathrm{inj}}/dt)_{\mathrm{max}}$	7.5 kA/μs	Maximum di/dt of pulse current
Δt_{R}	$<$ 75 μs	Pulse switch recovery time
R_{C}	5 kΩ	Charging resistor within SBC
R_{C2}	10 kΩ	Charging resistor rated to V_{dc}

even longer durations for reclosure. The charging duration for the applied scenario is $\Delta t_{\mathrm{C}} \approx 80\,\mathrm{ms}$ according to the parameters obtained from Table I and (3). This energizing time therefore seems acceptable. In addition, shorter energizing durations are possible as long as the decoupling of charging and discharging paths is adequately realized.

B. Interruption Process at Breaker Cell Level

The countercurrent injection is intended to assist the IGCT turn off. Its fundamental principle was initially proposed in [22] and has been widely used since then, e.g., in [23] and [24]. However, instead of completely bypassing a thyristor current and eliminating charge carriers, here turn off is performed using the power electronic breaking ability. The current to be interrupted may be beyond the device's natural turn-off capability, and may lead to higher charge carrier densities within the semiconductor. In combination with the almost zero-voltage IGCT switching operation, increased and longer lasting tail currents may appear. Zero-voltage switching has been investigated in [25], which gives an overview of this issue. Pulse capacitors and (stray) inductances result in a high-frequency resonant circuit. Current distribution and voltage stresses at device level must be considered carefully, and two issues require special attention: the utilization of the injected current and voltage stresses.

The first of these refers to the injected current itself. During normal IGCT turn off, the internal NPN transistor starts blocking, if its base current is lowered to zero by the integrated gate unit. This essentially characterizes the device's maximum turn-off capability [26]. The outer pulse current aims to reduce the instantaneous current stress, and the protective antiparallel diode may take over a certain share, which cannot support the breaking process anymore. The utilized injection current $\tilde{i}_{\mathrm{P}}$ is therefore defined, which has to reduce $i_{\mathrm{S}}(t=0) = I_0$ to a value $\tilde{I}_{\mathrm{S}}$ below the turn-off limit. An utilization factor u for the pulse current peak $\widehat{I}_{\mathrm{P}}$ can be deduced according to

$$u = \frac{I_0 - \tilde{I}_{\mathrm{S}}}{\widehat{I}_{\mathrm{P}}} = \frac{\max(\tilde{i}_{\mathrm{P}})}{\widehat{I}_{\mathrm{P}}} \tag{5}$$

for better performance evaluation. Before switches S_2 to S_{N} are allowed to open, switches S_{P} are closed. Consequently, C_{P}

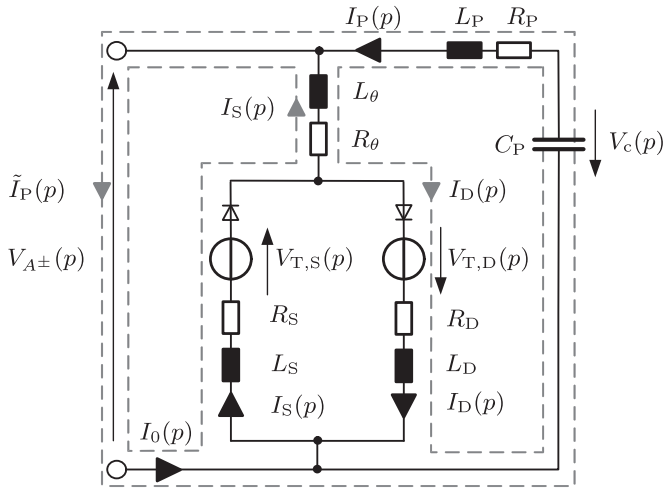

Fig. 6. Injection circuit including parasitic parameters for current distribution estimations.

starts discharging into the IGCT-diode configuration. In terms of utilization analysis, the equivalent circuit for this current reduction is given in Fig. 6. The forward voltages of the IGCT and diode are represented by $V_{\mathrm{T,S}}(p)$ and $V_{\mathrm{T,D}}(p)$, respectively. The voltage $V_{A^{\pm}}(p)$ can be interpreted as the resulting voltage stress of an SBC between clamps A^+ and A^- during interruption, compare Fig. 2(a). The aim of keeping C_{P} small results in a circuit with a high resonance frequency, in which the pulse impedance is dominated by geometries and the related frequency-dependent proximity and skin effect. Due to an increased ac resistance, the resistors may become relevant in pulse current control and damping. However, if the (parasitic) resistances are still low compared to the inductive circuit impedance, according to $f_0 \approx 40\,\mathrm{kHz}$ and $L_{\mathrm{P}} \approx 1\,\mu\mathrm{H}$, we obtain

$$R \ll \omega_0 L_{\mathrm{P}} = \sqrt{\frac{L_{\mathrm{P}}}{C_{\mathrm{P}}}} \approx 250\,\mathrm{m\Omega}. \tag{6}$$

Furthermore, the connector impedance $Z_\theta = pL_\theta + R_\theta$ can be neglected for basic behavior evaluation to a good approximation, and the simplified impedance network can be expressed in the Laplace domain by

$$Z(p) = \begin{Bmatrix} Z_{\mathrm{S}}(p) & 0 & 0 & -1 \\ 0 & \frac{1}{pC_{\mathrm{P}}} + Z_{\mathrm{P}}(p) + Z_{\mathrm{D}}(p) & \frac{1}{pC_{\mathrm{P}}} + Z_{\mathrm{P}}(p) & 0 \\ 0 & \frac{1}{pC_{\mathrm{P}}} + Z_{\mathrm{P}}(p) & \frac{1}{pC_{\mathrm{P}}} + Z_{\mathrm{P}}(p) & -1 \\ 1 & 0 & 1 & 0 \end{Bmatrix} \tag{7}$$

with $Z_{\mathrm{k}}(p) = R_{\mathrm{k}} + pL_{\mathrm{k}}$ $(k \in \{P, D, S\})$ and

$$Z(p) \cdot \begin{pmatrix} I_{\mathrm{S}}(p) \\ I_{\mathrm{D}}(p) \\ \tilde{I}_{\mathrm{P}}(p) \\ V_{\mathrm{A}^{\pm}}(p) \end{pmatrix} = \begin{pmatrix} L_{\mathrm{S}} I_0 - V_{\mathrm{T,S}}(p) \\ V_{\mathrm{C},0}/p - V_{\mathrm{T,D}}(p) \\ V_{\mathrm{C},0}/p \\ I_0(p) \end{pmatrix}. \tag{8}$$

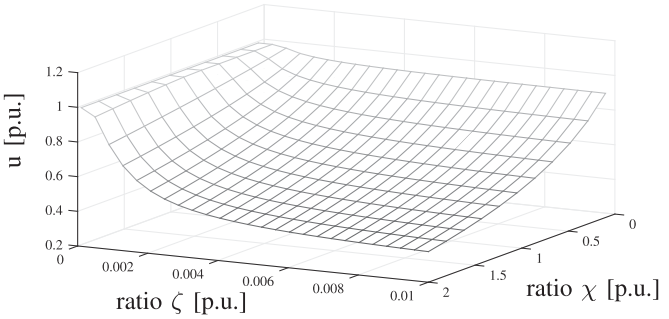

Fig. 7. Dependence of the utilization factor u, ratio ζ, and ratio χ on the parameters stated in Table I ($f_0 \approx 40$ kHz).

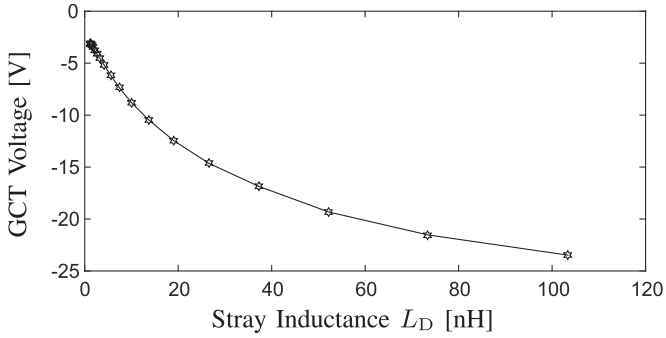

Fig. 8. Relationship of stray inductance L_D and GCT's reverse voltage peak ($L_S = 1$ nH).

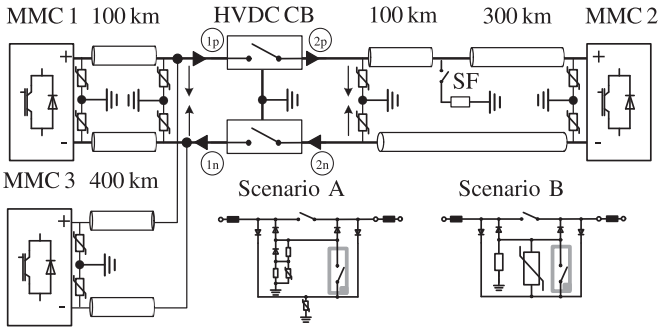

Fig. 9. HVDC system configuration consisting of three symmetric monopoles, a bipolar CB, and positive pole-to-ground fault.

The utilization factor of a corresponding pulse is given in Fig. 7. This was simulated in MATLAB Simulink according to the specifications provided in Table I. A parameter sweep on the ratio $\chi = L_S/L_D$ and the inductance ratio

$$\zeta = \frac{L_S||L_D}{L_S||L_D + L_P + L_\theta} \tag{9}$$

is shown. It can be stated, that both the ratio χ and the overall current dividing stray inductance between the diode and IGCT have an influence on utilization for values below 1% of the overall circuit inductance. Consequently, RC-IGCTs with low overall stray inductance result in the ratio ζ becoming small, which supports utilization. With regard to externally connected diodes with higher L_D and resulting lower χ, an advantageous trend can also be shown.

The second issue to be examined concerns critical voltages during the breaking process. For the harmonization of voltage distribution within an IGCT fall time variation in the 10% range and a turn-off time jitter of up to 50 ns, an *RC* snubber circuit with a 200 nF capacitor per IGCT device was added. This was sufficient to keep the resulting voltage imbalance within semiconductor specifications for given circuit parameters from Table I. The current slope-limiting inductance L_P for the commutation of $\tilde{I}_S$ into C_P is the dominant dimensioning criterion. Moreover, it should be noted, that tail current characteristics change noticeably if reduced device currents are applied during the charge carrier sweep-out phase, as shown for varying snubber capacitor configurations in [25]. In this case, increased snubber capacitance values may become necessary.

Further causes for the occurrence of transient voltages at device level are mainly current changes within inductors, due to reverse recovery and forward recovery effects of diodes. Except for solutions with added diode behavior at semiconductor-wafer level (RB-IGCT, BGCT), GCTs are asymmetric devices with a very limited reverse-blocking capability. The IGCT's gate unit capacitor is discharged by low-impedance MOSFETs which contain a reverse conducting diode [26]. If the voltage exceeds the gate capacitor voltage, typically around 20 V, a charging path is established, which is beyond the manufacturer specifications and may lead to destruction of the device, just as overstraining the GCTs reverse blocking ability would do after turn off. Therefore, the influence of the reverse diode's stray inductance on voltage development at the IGCT device must be kept accurate. As shown in Fig. 8, the individual, absolute GCT voltage remains below 20 V for inductance values of below 50 nH. This relationship also competes with the diode's forward recovery effect, which limits the allowable current steepness. Since a dependency on its blocking voltage is natural for Si diodes, as described in, e.g., [26], further opportunities might arise from semiconductor improvements to SiC diodes or the BGCT.

C. Interruption Process at System Level

The outer interruption process characterizes transient breaking behavior and resulting transmission system oscillations. Due to the surrounding inductors L_{dc1} and L_{dc2}, the transmission system is mostly decoupled from inner commutation processes of the breaker until the final interruption is initiated. The main difference between this scheme and other HVDC CB proposals lies in the subdivision of inductive energy absorption through the separation of incoming and outgoing currents i_{dc1} and i_{dc2} after MB opening. Thus, oscillations on the line require special attention after breaking, while each HVDC transmission system topology has its own characteristics. To facilitate the evaluation of its breaking behavior, a monopolar MTS HVDC system configuration is shown in Fig. 9 with a branching point 100 km apart from MMC 1. A breaker enabling MTS subdivision for point-to-point power transfer between MMC 1 and MMC 3 is inserted. The converters and CB are equipped with external surge arresters for Over Voltage Protection (OVP), which are rated to 1.5 per unit, here 750 kV. The breaker can be implemented for both positive and negative polarity by exchanging energy absorber arrangements among themselves and the

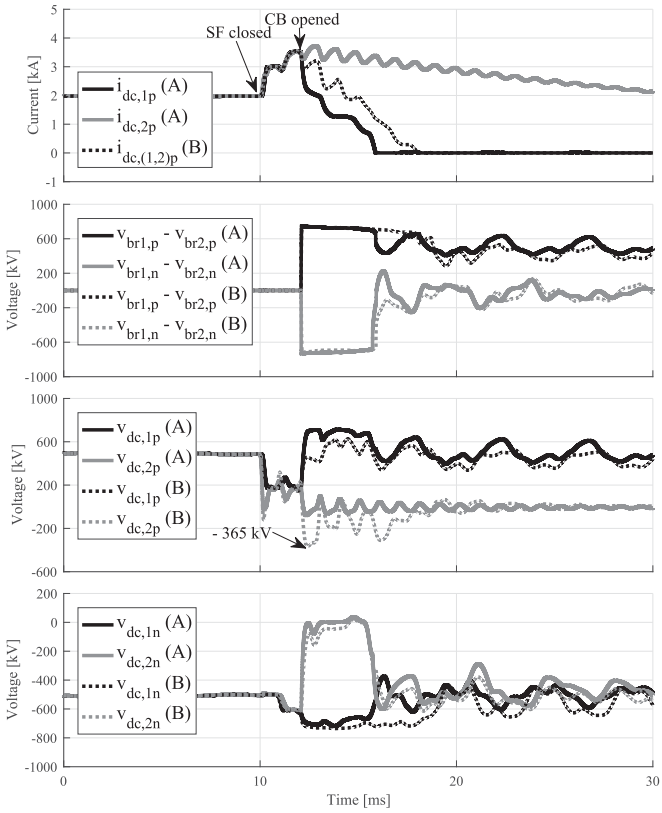

Fig. 10. Simulation results for Scenario A and B: incoming and outgoing CB currents (top), inner CB voltages $v_{\mathrm{br,X}}$ (upper middle), positive pole-to-ground voltages (lower middle) and negative pole-to-ground voltages (bottom).

charging path. In Scenario A, the proposed arrester arrangement with ground connection is used, while Scenario B offers a current decrease using a single arrester in parallel to the MB, as shown in Fig. 9. A single line-to-ground fault is created by closing SF, which is interrupted by the bipolar breaker specified in Table I. For simplification purposes, a transmission line model with 300 π—sections per 100 km is used. The simulation results are given in Fig. 10, showing adequate OVP for the healthy transmission line parts and suitable current decrease. Taking into account the maximum appearing breaker voltage $\max(|v_{\mathrm{br1}} - v_{\mathrm{br2}}|) = A_1 + A_2$ as the dimensioning criterion for the MB's voltage rating, the current decrease rate within a faulty line can be freely adjusted using A_2 and R_2 in Scenario A. This results in lower negative voltage stresses for Scenario A—here -8 kV compared with -365 kV for Scenario B—with likely benefits for cable configurations, where stored space charges are expected to influence polarity-reversed breakdown voltages.

IV. Performance Considerations

State-of-the-art HVDC CB proposals provide dc interruption using either mechanical CBs in combination with resonant circuit turn-on switching or the inherent turn-off capabilities of self-commutating semiconductors. Typical breaking performance values are within 10–20 kA, as shown in Table II, whereas higher ratings generally allow superimposing load current interruption or reduction of series-connected inductors L_{dc1} and L_{dc2}.

TABLE II
Breaker Performance Comparison

Breaker type	Current rating	Voltage rating	Main issue
Mech. RLC breaker [2]	5–16 kA	120 kV	Low current interruption and voltage scalability
Mech. three-stage RLC breaker [3]	10 kA	30 kV	voltage scalability
Hybrid IGBT breaker	9 kA [5]	Scalable	IGBT saturation
Hybrid BIGT breaker	16 kA [27]	Scalable	BIGT saturation
Hybrid IGCT breaker	15 kA	Scalable	Pulse circuit design and complexity

Mechanical breaking is proven for dc interruption for certain test configurations, but still has to demonstrate its voltage scalability for breaking times within a few milliseconds, in contrast to solid-state switches. Thyristor-based solutions, offering comparatively high current ratings, require a complete charge carrier reduction during time intervals of at least 50–100 μs. Therefore, the minimum capacitor size for forced commutation can be estimated according to

$$C_{\mathrm{min}} = \frac{i_0 \cdot \Delta t_{\mathrm{R}}}{V} = \frac{15\,\mathrm{kA} \cdot 1.5 \cdot 50\,\mu\mathrm{s}}{500\,\mathrm{kV}} \approx 2.25\,\mu\mathrm{F}. \quad (10)$$

This is rather a theoretical value, but remains still almost ten times the value of

$$C_{\mathrm{P,500\,kV}} = \frac{C_{\mathrm{P}}}{N-1} = \frac{4.8\,\mu\mathrm{F}}{20} = 240\,\mathrm{nF}. \quad (11)$$

Consequently, even for well-fitting devices such as medium voltage thyristors, comparatively massive capacitor banks are necessary to commutate fault currents sufficiently. In contrast, IGCTs with turn-off times of a few microseconds and turn-off current specifications of 4 to 5 kA (see for example [28]) might represent an opportunity for improvement. The development of reverse-conducting IGCTs with claimed current ratings of up to 8 kA according to [29] and Bi-Mode GCTs with a collaborative conduction area of diode and GCT, as proposed in [30], promises further upgrades not only in terms of the turn-off current, but also in allowable conduction times. Fig. 11 shows the simulation results of an IGCT junction temperature modeled according to [31] with thermal impedance values from [28]. The device is clamped between two copper plates and exposed to varying current stresses. For all three scenarios, an increase in junction temperature of less than 20 °C within 2 ms is observable. Scenario A, which is similar to the current slope design in [5], shows the lowest temperature rise rate. Scenario B describes an adjusted maximum current steepness curve due to lower inductor values (di/dt = 7.5 kA/ms) offering, for example, higher control dynamics of the transmission system. Scenario C considers a superpositioning load flow or tripping delay on a line using an increased initial current of 6 kA. Since the rate of temperature rise becomes high in Scenarios B and C, an influence on lifetime cannot be ruled out for breaking times of greater than 2 ms. The higher temperature rise resulting from the increased turn-off capabilities of the breaker allows a reliable assumption

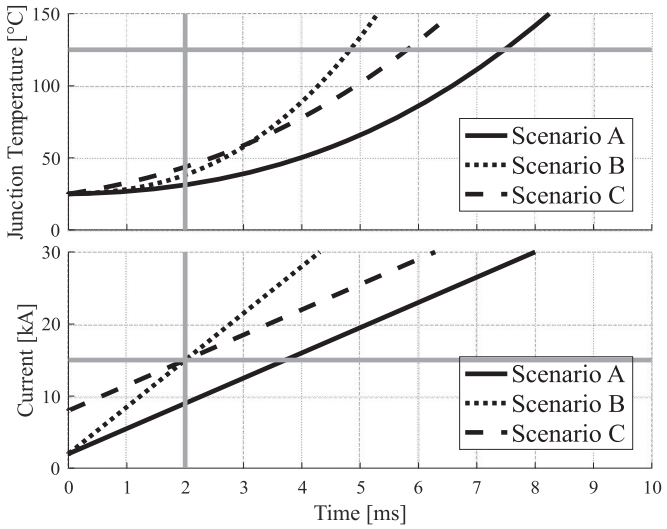

Fig. 11. Estimates of junction temperature curves of passively cooled IGCT [28] using an extended Foster model according to [31] for the presented current stress scenarios (boundaries are the maximum junction temperature of $125\,^{\circ}\mathrm{C}$ and the maximum turn-off capability of 15 kA applied to this proposal).

of an emerging negative correlation. This would require further predictability analysis and a differentiation between the most severe breaking event for sufficient breaking power design and the statistically typical breaking event for accurate lifetime forecasts. However, for the shorter clearing times as facilitated by an FD according to [21] and slope rates according to Scenario A, the temperature rise is likely to have a moderate influence on breaker degradation. In general, those high performance demands may require individual semiconductors to be tested under stresses comparable with the real application, which is possible due to the reduced number of switching operations during lifespan.

The increased design complexity caused by the power circuit of the MB and related control features within the proposal have to compete with the upscaling of breaking power, for example, by parallelization of semiconductor components. This benefits from a simple circuit and probable similarities to existing converter design, but in turn creates other difficulties and cost catalysts; doubling the breaking power in this context involves at least a doubling of semiconductor costs. In general, a certain inhomogeneity in current distribution between parallelized devices must be expected; this requires a well-coordinated turn off to avoid individual devices violating its safe operating areas. In IGBT-based solutions, which are attractive due to availability, cost, and technical improvements in recent years, breaking limitations are closely related to saturation currents. Compared with this, the investigated HVDC CB topology implements adjustable current ratings according to technical and economic objectives. First, IGCTs with nonsaturation behavior, high thermal cyclability, and high current ratings offer considerable advantages in an HVDC CB application environment. However, the main benefit may be the possibility for countercurrent injection-assisted turn off. The pulse circuit directly affects the achievable breaking power and no longer shows a direct correlation with component costs.

Further benefits can be assumed from the breaker's integrated rectifying principle and the earlier mentioned implementation of polarity selective fault clearing. Last but not least, subsequent extensibility toward bus bar applications with multiple interconnected transmission lines becomes feasible. This kind of centralized bus bar breaker topology, as introduced in [32], provides potential cost savings and more flexibility regarding protective transmission line branching at a later stage. Finally, the combination of both the inner countercurrent injection-based MB and the outer bus bar concept offers a solution for differing protection concerns by generally focusing on adaptability and scalability for a competitive HVDC fault protection strategy.

V. Conclusion

A protection scheme within a HVDC grid structure is likely to consist of a combination of fault current limiters, converter control measures and, where appropriate, HVDC CBs. In addition to a certain short-circuit breaking capability and the reduction of voltage transients during interruption, further application demands may become relevant in the future. For example, an intended delay function for HVDC CB tripping might be considered, when cascaded protection zones become indispensable due to system expansion. Within an HVDC system, fault current slope limitation can be adapted in matters of secure interruption as long as coil losses and reduced control dynamic behavior remain within acceptable discrimination limits; these are mainly defined by customer prioritization.

The scheme proposed in this paper focuses on an IGCT-based solution, due to the aim of adjustable breaking power beyond nominal current turn-off specifications. The HVDC CB concept is evaluated in terms of basic functionality and design interdependencies. In addition, an analytic description of processes at relevant abstraction levels is undertaken, and further considerations are supported by simulations using MATLAB Simulink and PLECS Blockset. It is shown for the proposal that voltage and current oscillations within an HVDC system with (in this case) monopolar converters result in low-reverse voltage stresses, which can be beneficial for relatively sensitive cables. Furthermore, the relevant correlations between component ratings, inner currents, and voltage distributions are highlighted, thereby demonstrating the relevance of a low-inductive pulse circuit design according to voltage restrictions and dependencies with the pulse current utilization factor. The general stress factors and the dimensioning criterion for components for adjustable breaker characteristics are identified, enabling further examination of reliability and lifetime or the development of realistic testing conditions in the future. Since specific insulation geometries and components are part of the system design process, more resilient parameters are hard to obtain. However, the basic characterization of this topology using appraised values shows good conformity with estimates of current requirements and introduces a framework for future evaluations.

References

[1] C. M. Franck, "HVDC circuit breakers: A review identifying future research needs," *IEEE Trans. Power Del.*, vol. 26, no. 2, pp. 998–1007, Apr. 2011.

[2] S. Tokoyoda *et al.*, "DC circuit breakers for HVDC grid applications HVDC and power electronics technology and developments," in *Proc. Cigre Conf.,*, Lund, Sweden, 2015, pp. 1–9.
[3] T. Heinz, V. Hinrichsen, S. Kosse, J. Teichmann, and E. Taylor, "Direct current interruption by a current zero impulse of constant steepness," in *Proc. 19th Int. Symp. High Voltage Eng.*, 2015, pp. 1–6.
[4] P. van Gelder and J. A. Ferreira, "Zero volt switching hybrid DC circuit breakers," in *Proc. IEEE Conf. Rec. Ind. Appl. Conf.*, vol. 5, Oct. 2000, pp. 2923–2927.
[5] J. Haefner and B. Jacobson, "Proactive hybrid HVDC breakers—A key innovation for reliable HVDC grids," in *Proc. Cigre Symp.*, Bologna, Italy, 2011, pp. 1–9.
[6] D. Schmitt, Y. Wang, T. Weyh, and R. Marquardt, "DC-side fault current management in extended multiterminal-HVDC-grids," in *Proc. 9th Int. Multi-Conf. Syst., Signals Devices*, 2012, pp. 1–5.
[7] W. Grieshaber, J.-P. Dupraz, D.-L. Penache, and L. Violleau, "Development and test of a 120 kV direct current circuit breaker," in *Proc. Cigre*, 2014, B4-301, pp. 1–11.
[8] C. Salles, M. L. B. Martinez, and Q. A., "Ageing of metal oxide varistors due to surges," in *Proc. Int. Symp. Lightning Protection*, 2011, pp. 171–176.
[9] K. Ringler, P. Kirkby, and C. Erven, "The energy absorption capability and time-to-failure of varistors used in station-class metal-oxide surge arresters," *IEEE Trans. Power Del.*, vol. 12, no. 1, pp. 203–212, Jan. 1997.
[10] A. Mizukoshi, J. Ozawa, S. Shirakawa, and K. Nakano, "Influence of uniformity on energy absorption capabilities of zinc oxide elements as applied in arresters," *IEEE Trans. Power App. Syst.*, vol. PAS-102, no. 5, pp. 1384–1390, May 1983.
[11] J. He and J. Hu, "Discussions on nonuniformity of energy absorption capabilities of ZnO varistors," *IEEE Trans. Power Del.*, vol. 22, no. 3, pp. 1523–1532, Jul. 2007.
[12] M. Bartkowiak, M. Comber, and G. Mahan, "Failure modes and energy absorption capability of ZnO varistors," *IEEE Trans. Power Del.*, vol. 14, no. 1, pp. 152–162, Jan. 1999.
[13] R. Sander and T. Leibfried, "Considerations on energy absorption of HVDC circuit breakers," in *Proc. 49th Int. Universities Power Eng. Conf.*, Sep. 2014, pp. 1–6.
[14] D. Döring, D. Ergin, K. Würflinger, J. Dorn, F. Schettler, and E. Spahic, "System integration aspects of DC circuit breakers," *IET Power Electron.*, vol. 9, no. 2, pp. 219–227, Oct. 2016.
[15] G. Asplund *et al.*, "HVDC grid feasibility study," Cigre - B4.52, 2013.
[16] M. K. Bucher and C. M. Franck, "Analysis of transient fault currents in multi-terminal HVDC networks during pole-to-ground faults," in *Proc. Int. Conf. Power Syst. Transients*, 2013, pp. 1–7.
[17] M. K. Bucher and C. Franck, "Analytic approximation of fault current contributions from capacitive components in HVDC cable networks," *IEEE Trans. Power Del.*, vol. 30, no. 1, pp. 74–81, Feb. 2015.
[18] C. Meyer, S. Schroeder, and R. W. De Doncker, "Solid-state circuit breakers and current limiters for medium-voltage systems having distributed power systems," *IEEE Trans. Power Electron.*, vol. 19, no. 5, pp. 1333–1340, Sep. 2004.
[19] R. Sander, M. Suriyah, and T. Leibfried, "A novel current-injection based design for HVDC circuit breakers," in *Proc. Int. Exhib. Conf. Power Electron., Intell. Motion, Renewable Energy Energy Manage.*, 2015, pp. 1–7.
[20] A. Hassanpoor, J. Haefner, and B. Jacobson, "Technical assessment of load commutation switch in hybrid HVDC breaker," *IEEE Trans. Power Electron.*, vol. 30, no. 10, pp. 5393–5400, Oct. 2015.
[21] P. Skarby and U. Steiger, "An ultra-fast disconnecting switch for a hybrid HVDC breaker," in *Proc. CIGRE Canada Conf.*, Sep. 2013, pp. 1–9.
[22] R. Troeger, *Technische Grundlagen und Anwendung der Stromrichter*. Elektrische Bahnen 8, 1932.
[23] M. Meyer, *Thyristor in der technische Anwendung Band 1: Stromrichter mit erzwungener Kommutierung*. Berlin, Germany: Siemens Verlag, 1967.
[24] C. Meyer and R. W. De Doncker, "Solid-state circuit breaker based on active thyristor topologies," *IEEE Trans. Power Electron.*, vol. 21, no. 2, pp. 450–458, Mar. 2006.
[25] R. Lenke, H. van Hoek, S. Taraborrelli, R. De Doncker, J. San-Sebastian, and I. Etxeberria-Otadui, "Turn-off behavior of 4.5 kV asymmetric IGCTs under zero voltage switching conditions," in *Proc. 4th Eur. Conf. Power Electron. Appl.*, 2011, pp. 1–10.
[26] J. Lutz, H. Schlangenmnotto, U. Scheuermann, and R. De Doncker, *Short Introduction to Power Device Technology*. New York, NY, USA: Springer-Verlag, 2011.
[27] L. Storasta, M. Rahimo, J. Haefner, F. Dugal, E. Tsyplakov, and M. Callavik, "Optimized power semiconductors for the power electronic based HVDC breaker application," in *Proc. Int. Exhib. Conf. Power Electron., Intell. Motion, Renewable Energy, Energy Manage.*, May 2015, pp. 1–7.
[28] ABB Std., "Asymmetric integrated gate commutated thyristor 5shy 35l4522," Doc. No. 5SYA1249-00, Feb. 2012. [Online]. Available: http://new.abb.com/semiconductors/integrated-gate-commutated-thyristors-(igct)
[29] ABB Std., "IGCT integrated gate-commutated thyristors," Doc. 5SYA 2023-13, Apr. 2015. [Online]. Available: http://new.abb.com/semiconductors/integrated-gate-commutated-thyristors-(igct)
[30] U. Vemulapati *et al.*, "An experimental demonstration of a 4.5 kV bi-mode gate commutated thyristor" (BGCT)," in *Proc. IEEE 27th Int. Symp. Power Semicond. Devices IC's*, 2015, pp. 109–112.
[31] K. Ma, N. He, M. Liserre, and F. Blaabjerg, "Frequency-domain thermal modeling and characterization of power semiconductor devices," *IEEE Trans. Power Electron.*, vol. 31, no. 10, pp. 7183–7193, Oct. 2016.
[32] R. Sander, M. Suriyah, and T. Leibfried, "Selective HVDC transmission line breaking for bus bar applications under reduced expenses," in *Proc. Int. Exhib. Conf. Power Electron., Intell. Motion, Renewable Energy Energy Manage.,* 2016, pp. 363–370.

René Sander was born in Munich, Germany, in 1987. He received the M.Sc. degree in electrical engineering from the Karlsruhe Institute of Technology, Karlsruhe, Germany, in 2012, where he is currently working toward the Ph.D. degree in electrical engineering.

His research interests include characterization and optimization of HVDC Circuit Breakers, dc interruption techniques and cost-effective HVDC fault handling strategies. He is member of VDE and CIGRE.

Michael Suriyah (M'14) was born in Kuala Lumpur, Malaysia, in 1982. He received the Diploma and M.Sc. degrees in electrical engineering from the University of Applied Sciences, Karlsruhe, Germany, in 2007 and 2008, respectively, and the Ph.D. degree in electrical engineering from the Karlsruhe Institute of Technology, Karlsruhe, Germany, in 2013.

He is currently the Head of the Department for Power Networks, Institute of Electric Energy Systems and High-Voltage Technology. His research interests include aging diagnostics and onsite testing of power transformers, high-voltage testing methods, analysis of electric power networks as well as planning of future power systems. He is also a member of VDE.

Thomas Leibfried (M'96) was born in Neckarsulm, Germany, in 1964. He received the Dipl.-Ing. and Dr.-Ing. degrees from the University of Stuttgart, Stuttgart, Germany, in 1990 and 1996, respectively.

From 1996 to 2002, he was with the Siemens AG, Nuremberg, Germany, working in the power transformer business in various technical and management positions. In 2002, he joined the University of Karlsruhe (now KIT), Karlsruhe, Germany, as the Head of the Institute of Electric Energy Systems and High-Voltage Technology. He is a member of VDE and CIGRE.