Cascaded Dual-Buck Inverter With Reduced Number of Inductors

Ashraf Ali Khan, *Student Member, IEEE*, Honnyong Cha, *Member, IEEE*, and Jih-Sheng (Jason) Lai, *Fellow, IEEE*

***Abstract*—A dual-buck inverter (DBI) possesses no shoot-through worries and can boost efficiency by using power MOSFETs. The main drawback of a DBI is the use of more inductors than in a traditional full-bridge inverter. This greater number of inductors decreases the power density and increases system cost. In this paper, a modified cascaded full-bridge DBI is proposed. It retains all the advantages of the conventional cascaded full-bridge DBI, possesses no shoot-through issues, and can be operated with no pulse-width-modulation dead-times. It can be implemented with power MOSFET without reverse recovery issues of a body diode to boost efficiency. The cascaded modules in the proposed inverter share current limiting inductors. Therefore, the number of inductors and inductor footprints, the complexity of the circuit layout, required inductance, and magnetic volume can all be decreased. To show the advantages of the proposed inverter, detailed theoretical analysis and experimental results are provided.**

***Index Terms*—Cascaded, dual-buck, H-bridge, inductor, inverter, MOSFET, multilevel, reliability.**

I. Introduction

FULL-BRIDGE inverter, shown in Fig. 1, is widely used for dc–ac power inversion. However, it has shoot-through problem of the input voltage source or capacitor. The shoot-through occurs when S_1 and S_2, or S_3 and S_4, or all switches $S_1 - S_4$ conduct simultaneously. The shoot-through problem has been the primary source of failure of the traditional H-bridge inverter. To reduce the risk of current shoot-through, a small dead-time is set between the switches in phase-leg. The dead-time causes distortion in output waveforms and reduces the achievable voltage gain. During the dead-time, the inductor current flows through the body diodes of switching devices, which causes significant reverse recovery related losses [28].

Power MOSFET, unlike the IGBT having fixed voltage drop, has resistive voltage drop and has no turn-OFF tail current. These features make MOSFET attractive at lower power level to boost efficiency and allow higher switching frequencies. However, the body diode of power MOSFET has severe reverse recovery issues especially at high-voltage and hard-switching converters [1], [2].

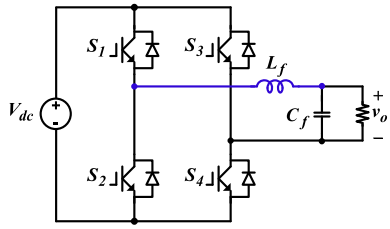

Fig. 1. Traditional full-bridge inverter.

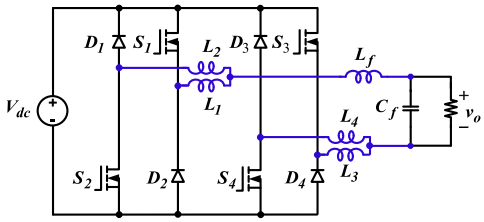

Fig. 2. Full-bridge DBI [4].

For this reason, power MOSFET is normally not recommended for traditional full-bridge or similar hard switching inverters. The soft-switching inverters can utilize the benefits of MOSFETs at the cost of more components count and auxiliary switches [3].

In [29], the concept of dual-buck inverter (DBI) was introduced. Full-bridge DBI [4] is shown in Fig. 2. It is composed of four MOSFETs $S_1 - S_4$, four external diodes $D_1 - D_4$, four shoot-through limiting inductors $L_1 - L_4$, and an output filter inductor L_f. Besides filtering, the $L_1 - L_4$ protect shoot-through in the converter. In each buck circuit, one MOSFET is connected in series with an external diode. Thus, the DBI does not suffer from the shoot-through problem, and therefore dead-times in switching signals can be eliminated. In this topology, current does not flow through the body diodes of $S_1 - S_4$, but freewheels through $D_1 - D_4$, which enables the use of power MOSFETs without reverse recovery issues of body diodes. The $D_1 - D_4$ can be selected externally with good reverse recovery features to decrease the reverse recovery and conduction losses, which contribute to increased efficiency. The dual-buck type dc–ac inverters [5]–[15], dc–dc converters [15]–[17], and ac–ac converters [18]–[22] have been researched. One of the

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A. A. Khan and H. Cha are with the School of Energy Engineering, Kyungpook National University, Daegu 41566, South Korea (e-mail: 08beeashrafa@seecs.edu.pk; chahonny@knu.ac.kr).

J.-S. Lai is with the Future Energy Electronics Center, Virginia Tech, Blacksburg, VA 24061 USA (e-mail: laijs@vt.edu).

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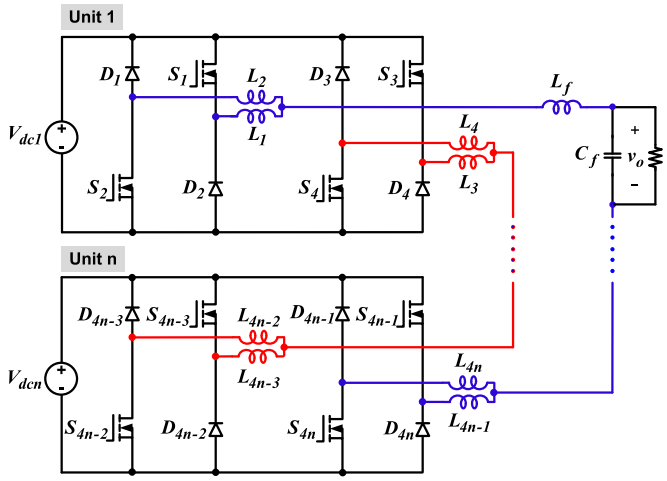


Fig. 3. Conventional CHB DBI [7].

noticeable drawbacks of the DBI is the use of a greater number of inductors.

In high-voltage applications, using two-level inverters as shown in Figs. 1–2 is impractical because of the limited voltage rating of semiconductor devices. To work with high voltages, multilevel inverters have evolved as a viable solution. Among the multilevel inverters, the flying capacitor [23], neutral point clamped [24], and cascaded H-bridge (CHB) [25] inverters are well known. It is also known that the cascaded multilevel inverter can reach high-output voltage. It is constructed with series connection of many single-phase two-level inverters using separate dc sources. The cascaded multilevel inverter is highly modular because each module has the same circuit configuration, control, and modulation scheme [26]. Its maintenance is relatively easy because the faulty module can easily be replaced and corrected. Moreover, a faulty module can be bypassed without disturbing the operation of healthy modules [27]. The cascaded inverters are very attractive for use in photovoltaic (PV) applications, in which each PV panel serves as a separate dc voltage source. In addition, they are highly desirable for the utility interface of various energy sources such as biomass, PV, and fuel cells.

A cascaded multilevel inverter based on the traditional H-bridge inverter also possesses the shoot-through worries and reverse recovery issues. To overcome the drawbacks of the traditional CHB inverter, cascaded half-bridge [7] and full-bridge [6]–[8] DBIs have been proposed. They have no shoot-through risks and no reverse recovery issues of body diode. The CHB DBI is obtained by a series connection of single-phase DBIs as shown in Fig. 3. The single-phase DBI has zero crossing distortion problems with hybrid bipolar pulse width modulation (PWM) strategy [11], [13]. The CHB DBI with phase-shift control solves the zero crossing distortion problem of single-phase DBI [7]. The main drawback of the CHB DBI is the use of four current limiting inductors for each module (or unit), which decreases power density.

This paper proposes an improved CHB DBI with reduced number of inductors while retaining all the aforementioned benefits of the conventional CHB DBI. The reduction is made by sharing limiting inductors in consecutive modules. Therefore,

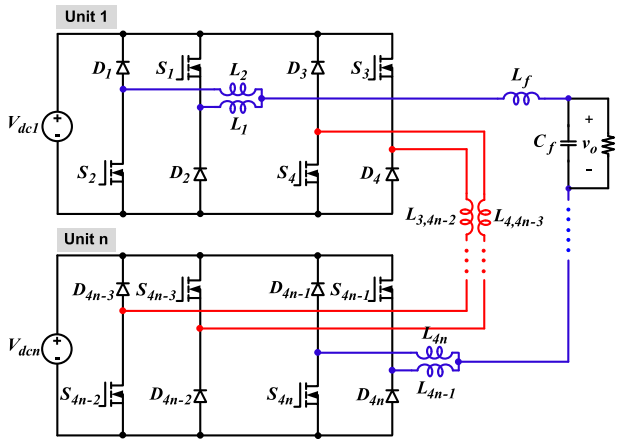


Fig. 4. Proposed CHB DBI.

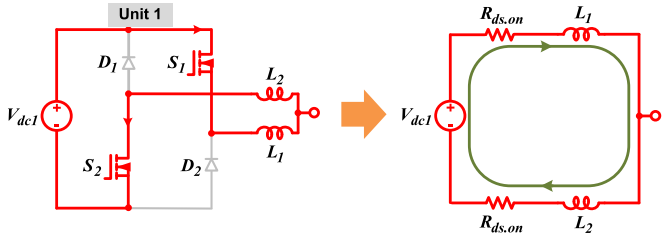


Fig. 5. Opposition to shoot-through during an overlap-time of S_1 and S_2.

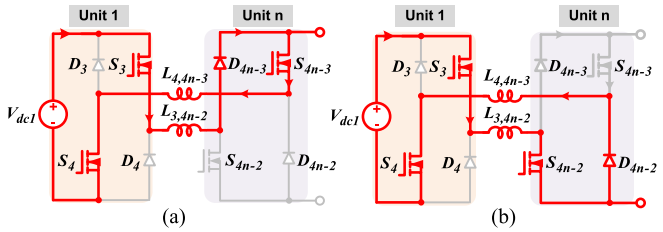


Fig. 6. Opposition to shoot-through during an overlap-time of S_3 and S_4. (a) S_{4n-3} ON. (b) S_{4n-2} ON.

not only the number of inductors but also the required inductance and magnetic volume can be reduced. In addition, the number of inductor footprints and complexity of the circuit layout can be reduced.

II. Proposed CHB DBI

The circuit topology of the proposed n-unit CHB DBI is shown in Fig. 4. Similar to the conventional CHB DBI, it takes the dual-buck structure, but the consecutive modules in the proposed inverter share current limiting inductors. For example, the two inductors (L_3 and L_{4n-2}) in Fig. 3 are merged into a single inductor $L_{3,4n-2}$ in Fig. 4. Similarly, the L_4 and L_{4n-3} are merged into inductor $L_{4,4n-3}$ in the proposed inverter. As a result, the number of current limiting inductors can be reduced and this reduction is maximized as more units are cascaded.

Ideally, the two switches in a phase-leg can operate without overlap-time. However, in practically, it can occur

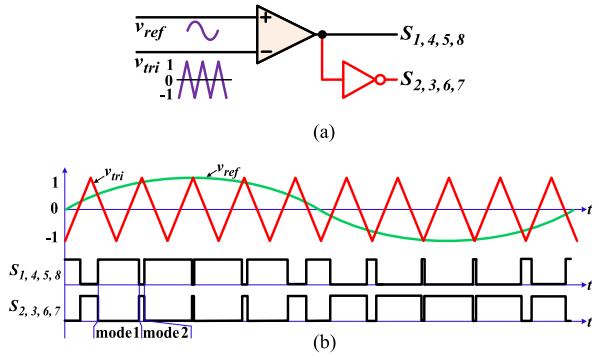


Fig. 7. TBPS. (a) Block diagram. (b) Gate signals.

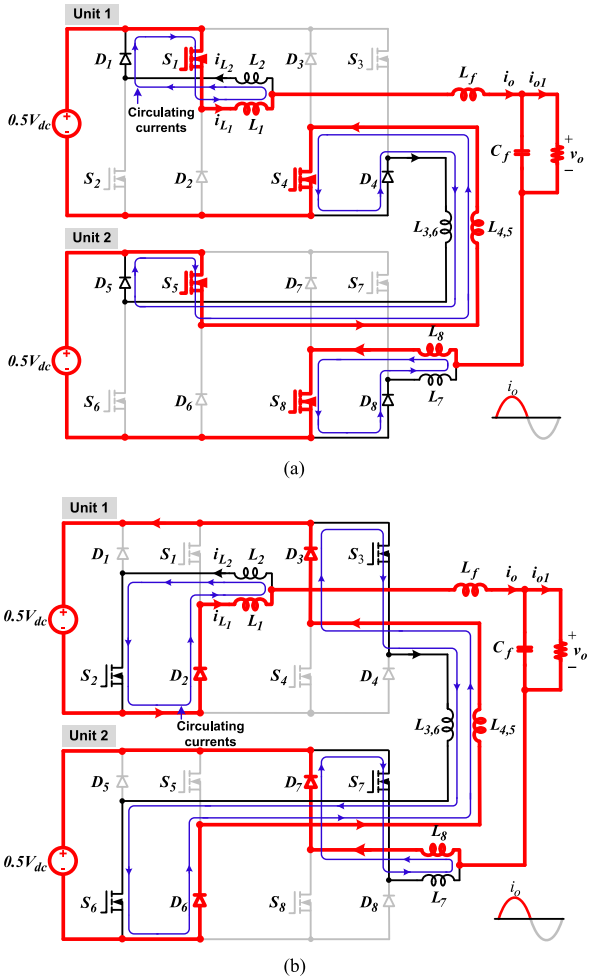


Fig. 8. Operation with TBPS. (a) Mode 1 (mode 1 and 3 of TUPS). (b) Mode 2.

although not desired. When an overlap between S_1 and S_2 occurs, L_1, L_2, and the conduction voltage drop of two MOSFETs oppose the shoot-through current as shown in Fig. 5. Similarly, when an overlap between S_3 and S_4 occurs, $L_{4,4n-3}$, $L_{3,4n-2}$, and the conduction voltage drop of three MOSFETs and one diode oppose the rise in current as shown in Fig. 6. In the proposed inverter, only the first (S_1 and S_2 in unit 1) and last (S_{4n-1} and S_{4n} in unit n) phase-legs experience the same opposition as depicted in Fig. 5, while all the other

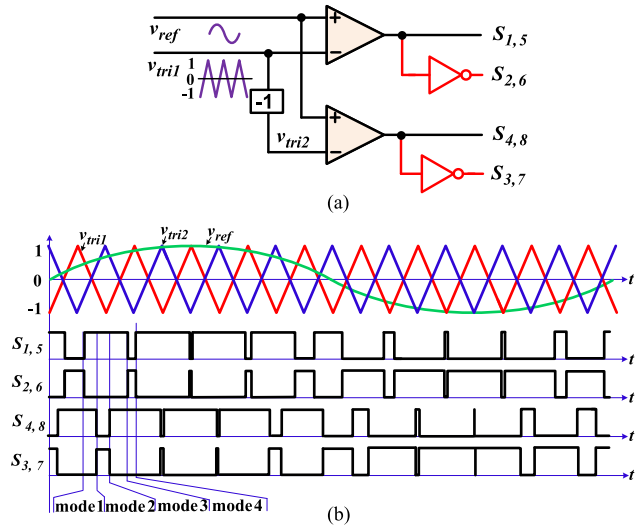


Fig. 9. TUPS. (a) Block diagram. (b) Gate signals.

phase-legs experience the opposition depicted in Fig. 6. On the other hand, all phase-legs in the conventional CHB DBI experience opposition depicted in Fig. 5. Thus, in each phase-leg of both types of CHB DBIs, shoot-through current is opposed by two current limiting inductors. Therefore, for the same inductance of current limiting inductors, the opposition of current limiting inductors to shoot-through current is the same in both inverters. In other words, the proposed inverter provides the same opposition with reduced number of inductors.

III. Operation of the Proposed Inverter

In this section, operational modes of the proposed inverter are analyzed. For the sake of simplicity, only two units are cascaded and all the current limiting inductors (L_1, L_2, $L_{3,6}$, $L_{4,5}$, L_7, and L_8) are assumed to have the same inductance L. Four PWM strategies without phase-shift control are discussed in this section and the similar analysis with phase-shift control will be given in Section IV.

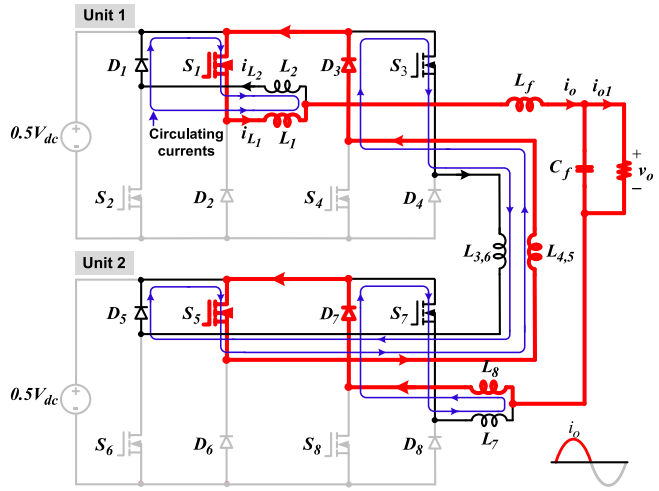
A. Traditional Bipolar PWM Strategy (TBPS)

The block diagram of the TBPS is shown in Fig. 7(a) and its gate signals are shown in Fig. 7(b). This strategy requires one reference signal $v_{\rm ref}$ and one carrier signal v_{tri}. In the TBPS, the duty ratio (D) defined as the ON-time duration of S_1 varies between 0 and 1. The TBPS has the following two operating modes within a switching cycle.

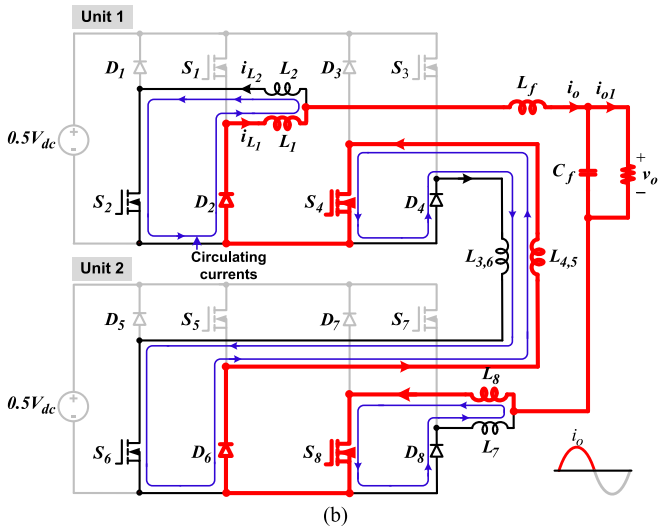
Mode 1: As shown in Fig. 8(a), S_1, S_4, S_5, and S_8 are ON, and S_2, S_3, S_6, and S_7 are OFF in this mode. D_1, D_4, D_5, and D_8 are forward-biased, and D_2, D_3, D_6, and D_7 are reverse-biased. The inductor current is expressed as

$$\frac{di_{L_1}}{dt} = \frac{V_{\rm dc} - v_o}{3L + L_f}. \tag{1}$$

Mode 2: This mode is shown in Fig. 8(b). S_1, S_4, S_5, and S_8 are OFF, and S_2, S_3, S_6, and S_7 are ON. D_1, D_4, D_5, and D_8 are reverse-biased, and D_2, D_3, D_6, and D_7 are forward-biased.



(a)



(b)

Fig. 10. Operation with TUPS. (a) Mode 2. (b) Mode 4.

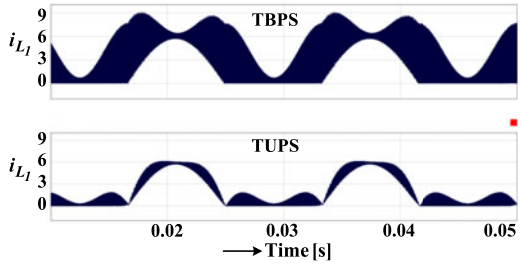


Fig. 11. Inductor current i_{L_1} with TBPS and TUPS.

The inductor current is expressed as

$$\frac{di_{L_1}}{dt} = \frac{-V_{\rm dc} - v_o}{3L + L_f}. \tag{2}$$

As shown in Fig. 8, the TBPS generates circulating currents, therefore, $i_{L_1} = i_o + i_{L_2}$ for $i_o > 0$. When the circulating currents are eliminated, i_{L_1} is the same as i_o for $i_o > 0$.

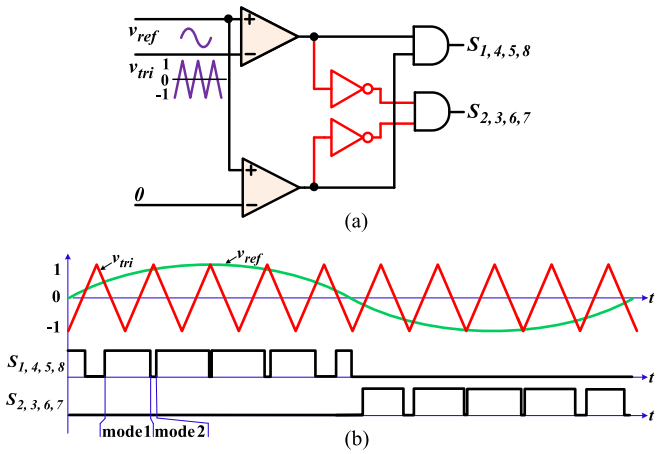
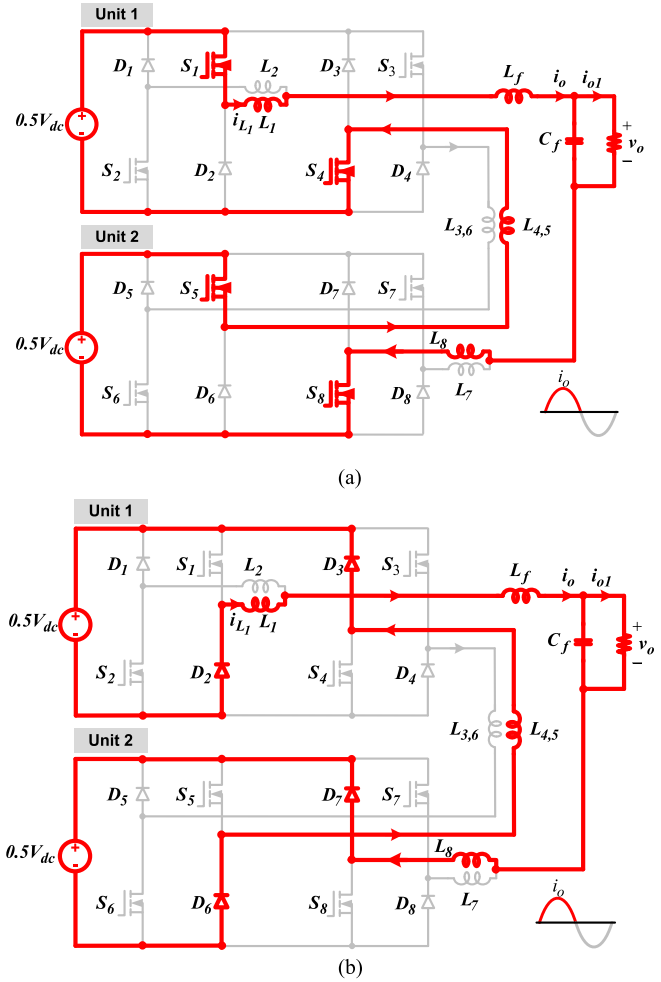


Fig. 12. HBPS. (a) Block diagram. (b) Gate signals.



(a)

(b)

Fig. 13. Operation with HBPS. (a) Mode 1 (mode 1 of HUPS). (b) Mode 2.

B. Traditional Unipolar PWM Strategy (TUPS)

The block diagram of the TUPS is shown in Fig. 9(a) and Fig. 9(b) shows the gate signals. It requires two carrier signals ($v_{\rm tri1}$, $v_{\rm tri2}$) shifted by 180°. In this strategy, D varies between 0 and 1. The TUPS has the following four operating modes.

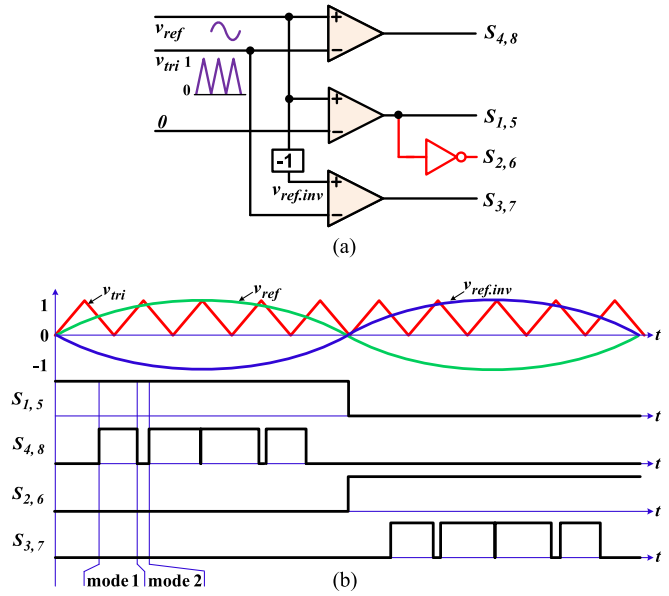


Fig. 14. HUPS. (a) Block diagram. (b) Gate signals.

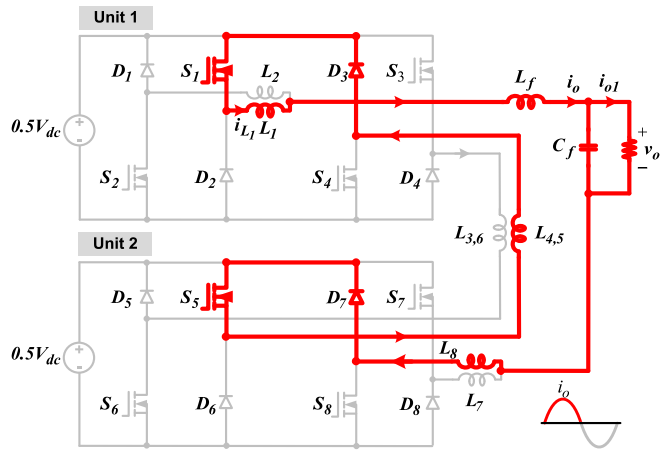


Fig. 15. Operation with the HUPS: mode 2.

Mode 1: This mode is the same as mode 1 of the TBPS.

Mode 2: This mode is depicted in Fig. 10(a). In this mode, S_1, S_3, S_5, and S_7 are ON, and S_2, S_4, S_6, and S_8 are OFF. D_1, D_3, D_5, and D_7 are forward-biased, and D_2, D_4, D_6, and D_8 are reverse-biased. The inductor current is expressed as

$$\frac{di_{L_1}}{dt} = \frac{-v_o}{3L + L_f}. \tag{3}$$

Mode 3: This mode is the same as mode 1 of the TUPS and TBPS.

Mode 4: This mode is shown in Fig. 10(b), where S_2, S_4, S_6, and S_8 are ON, and S_1, S_3, S_5, and S_7 are OFF. D_2, D_4, D_6, and D_8 are forward-biased, and, D_1, D_3, D_5, and D_7 are reverse-biased. The inductor current has the same slope as (3).

Similar to the TBPS, the TUPS also generates circulating currents, and $i_{L_1} = i_o + i_{L_2}$ for $i_o > 0$.

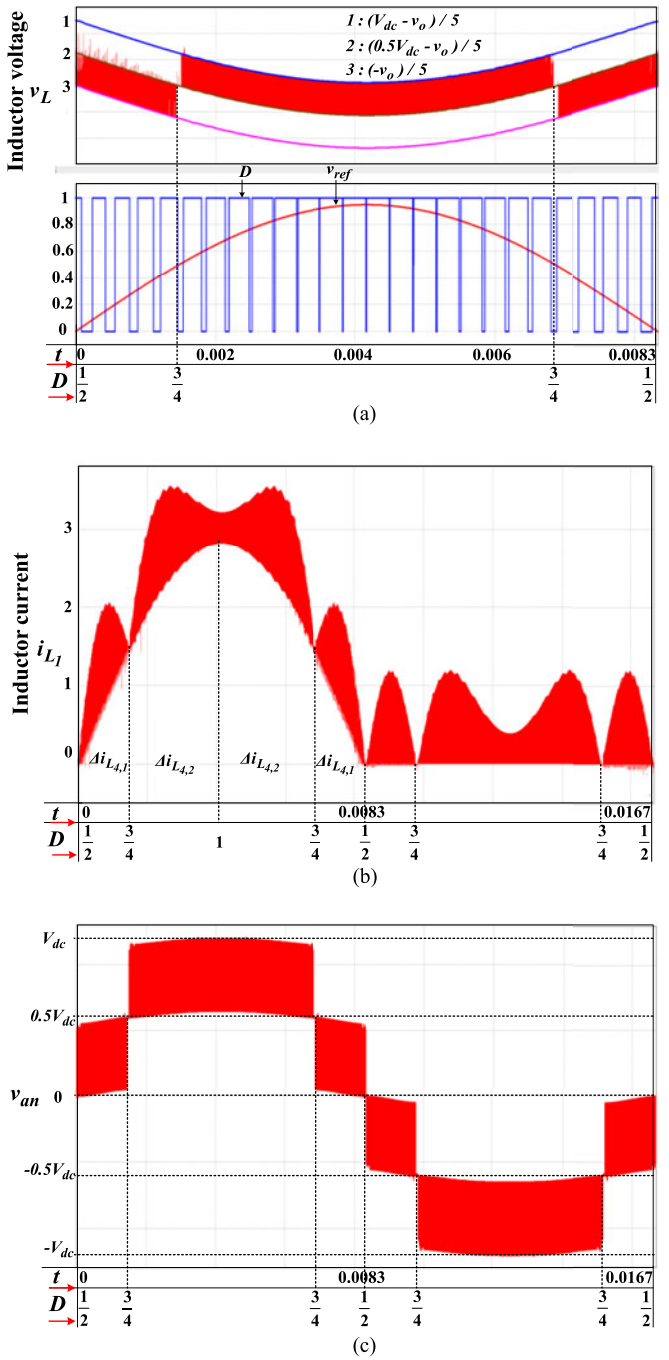


Fig. 16. Simulation results of the proposed 4-unit inverter using HBPS. (a) Inductor voltage. (b) Inductor current. (c) Voltage between the source of S_1 and drain of S_{16}.

As mentioned, both the TBPS and TUPS generate circulating currents, which increase the power loss and current stresses of switches. To decrease the circulating currents, a finite PWM dead-time between the switches should be inserted.

Fig. 11 compares the inductor current i_{L_1} with the TBPS and TUPS. In TUPS, the inductors experience twice of the inverter switching frequency and have lower voltage across them. Therefore, the TUPS results in a smaller inductor current ripple than the TBPS.

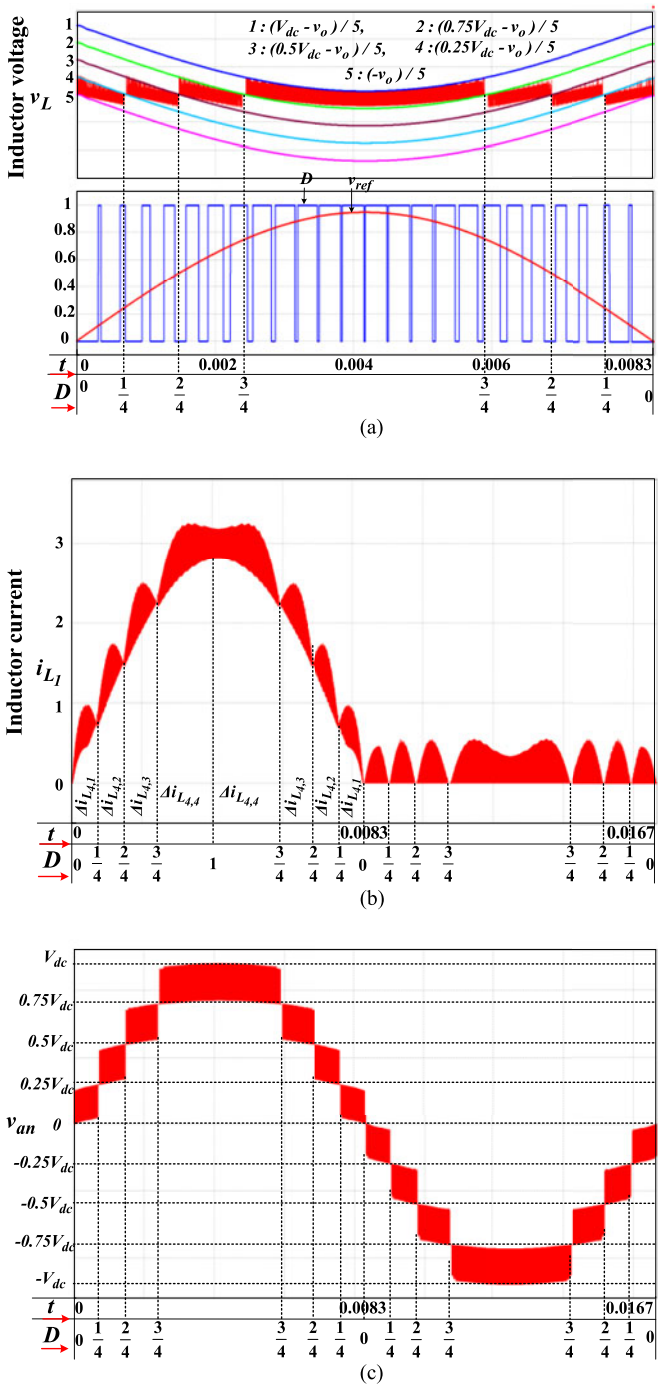


Fig. 17. Simulation results of the proposed 4-unit inverter using HUPS. (a) Inductor voltage. (b) Inductor current. (c) Voltage between the source of S_1 and drain of S_{16}.

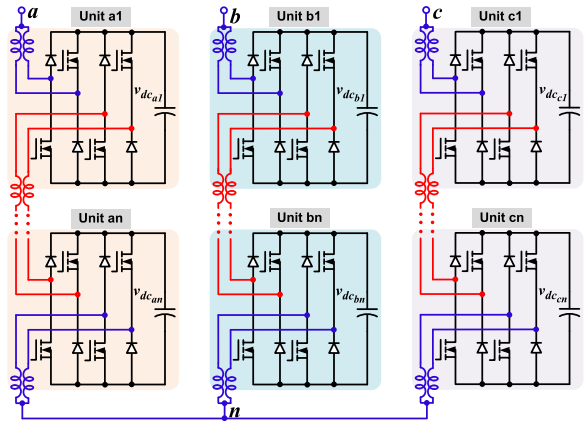


Fig. 18. Proposed three-phase CHB DBI.

C. Hybrid Bipolar PWM Strategy (HBPS)

To eliminate the circulating currents and reduce switching loss of the TBPS, a HBPS is used. The block diagram of the HBPS is given as Fig. 12(a) and the gate signals are shown in Fig. 12(b). In this strategy, two switches per module are switching at any given time, and D defined the ON-time duration of S_1 varies between 0.5 and 1. Assume that $v_{\rm ref}$ is in-phase with the output current. As shown in Fig. 12(b), for $v_{\rm ref} > 0$, S_1, S_4, S_5, and S_8 are switched at high frequency while S_2, S_3, S_6, and S_7 remain OFF. Similarly, for $v_{\rm ref} < 0$, S_2, S_3, S_6, and S_7 are switched at high frequency while S_1, S_4, S_5, and S_8 remain OFF. The two operating modes of the HBPS are described as follows.

Mode 1: As shown in Fig. 13(a), S_1, S_4, S_5, and S_8 are ON in this mode. The expression for inductor current is the same as (1).

Mode 2: All switches are OFF in this mode and D_2, D_3, D_6, and D_7 freewheel the inductor current. Fig. 13(b) shows the operation in this mode. The expression for inductor current is the same as (2).

In the HBPS, there are no circulating currents. Thus, $i_{L_1} = i_o$ for $i_o > 0$ and $i_{L_2} = i_o$ for $i_o < 0$.

D. Hybrid Unipolar PWM Strategy (HUPS)

The block diagram and gate signals of the HUPS are depicted in Fig. 14. In this strategy, D is the ON-time duration of S_4 and varies between 0 and 1. As shown in Fig. 14(b), for $v_{\rm ref} > 0$, S_2, S_3, S_6, and S_7 are always OFF. S_1 and S_5 are always ON, and S_4 and S_8 are switched at high frequency. Therefore, in the HUPS, only one switch per module switches at high frequency.

Mode 1: This mode is the same as Fig. 13(a).

Mode 2: As shown in Fig. 15, S_4 and S_8 are OFF, and D_3 and D_7 freewheel the current. The inductor current expression is the same as in (3). However, due to the absence of circulating currents in the TUPS $i_{L_1} = i_o$ for $i_o > 0$. Compared to the TBPS, TUPS, and HBPS, the HUPS can realize the highest efficiency due to the reduction of switching loss.

IV. Phase-Shift Control and Current Ripple Analysis

In this section, the proposed inverter is operated with phase-shift control. In this technique, the gate signals of high-frequency switches in the n-unit cascaded inverter are phase-shifted by $360°/n$. The phase-shift control increases the effective switching frequency of the passive components by the times of the cascaded modules. Therefore, the size of passive components can be reduced significantly without increasing the actual

TABLE I
INDUCTOR CURRENT RIPPLES UNDER THE HBPS

Unit (n)	Current Ripple ($\Delta i_{L_{n\,N}}$)		
1	$\frac{(V_{dc}-v_o)DT_s}{2L+L_f}, \frac{1}{2}\le D\le 1$		
2	$\frac{(V_{dc}-v_o)\left(D-\frac{1}{2}\right)T_s}{3L+L_f}, \frac{1}{2}\le D\le 1$		
3	$\frac{\left(\frac{V_{dc}}{3}-v_o\right)\left(D-\frac{1}{3}\right)T_s}{4L+L_f}, \frac{1}{2}\le D\le \frac{2}{3}$	$\frac{(V_{dc}-v_o)\left(D-\frac{2}{3}\right)T_s}{4L+L_f}, \frac{2}{3}\le D\le 1$	
4	$\frac{\left(\frac{V_{dc}}{2}-v_o\right)\left(D-\frac{2}{4}\right)T_s}{5L+L_f}, \frac{2}{4}\le D\le \frac{3}{4}$	$\frac{(V_{dc}-v_o)\left(D-\frac{3}{4}\right)T_s}{5L+L_f}, \frac{3}{4}\le D\le 1$	

TABLE II
INDUCTOR CURRENT RIPPLES UNDER THE HUPS

Unit (n)	Current Ripple ($\Delta i_{L_{n\,N}}$)			
1	$\frac{(V_{dc}-v_o)DT_s}{2L+L_f}, N=1,\ 0\le D\le 1$			
2	$\frac{\left(\frac{V_{dc}}{2}-v_o\right)DT_s}{3L+L_f}, N=1,\ 0\le D\le \frac{1}{2}$	$\frac{(V_{dc}-v_o)(D-\frac{1}{2})T_s}{3L+L_f}, N=2,\ \frac{1}{2}\le D\le 1$		
3	$\frac{\left(\frac{V_{dc}}{3}-v_o\right)DT_s}{4L+L_f}, N=1,\ 0\le D\le \frac{1}{3}$	$\frac{\left(\frac{2V_{dc}}{3}-v_o\right)(D-\frac{1}{3})T_s}{4L+L_f}, N=2,\ \frac{1}{3}\le D\le \frac{2}{3}$	$\frac{(V_{dc}-v_o)(D-\frac{2}{3})T_s}{4L+L_f}, N=3,\ \frac{2}{3}\le D\le 1$	
4	$\frac{\left(\frac{V_{dc}}{4}-v_o\right)DT_s}{5L+L_f}, \begin{cases} N=1 \\ 0\le D\le \frac{1}{4}\end{cases}$	$\frac{\left(\frac{2V_{dc}}{4}-v_o\right)(D-\frac{1}{4})T_s}{5L+L_f}, \begin{cases} N=2 \\ \frac{1}{4}\le D\le \frac{2}{4}\end{cases}$	$\frac{\left(\frac{3V_{dc}}{4}-v_o\right)(D-\frac{2}{4})T_s}{5L+L_f}, \begin{cases} N=3 \\ \frac{2}{4}\le D\le \frac{3}{4}\end{cases}$	$\frac{(V_{dc}-v_o)(D-\frac{3}{4})T_s}{5L+L_f}, \begin{cases} N=4 \\ \frac{3}{4}\le D\le 1\end{cases}$

TABLE III
ELECTRICAL SPECIFICATIONS

Output Voltage	420 Vrms/60 Hz
Input voltage of each module	310 V_{dc}
Output power	2 kW
Switching frequency	35 kHz
MOSFET	47N60CFD
Diode	RHRG3060
Shoot-through limiting inductors	0.2 mH
Output filter inductor	1 mH
Output capacitor	1.5 μF

switching frequency of semiconductor devices and switching loss. Figs. 16 and 17 show the simulation results with the phase-shift control for the proposed 4-unit inverter. The modulation index is set to 0.95. The individual dc source voltage is $V_{\rm dc}/4$. In the proposed inverter, all the shoot-through limiting inductors serve as filter inductors, thus, the output filter inductor L_f can be eliminated if sufficient units are cascaded. When L_f is removed, then five shoot-through limiting inductors are seen in series and only one-fifth of the total voltage appears across each shoot-through limiting inductor. Fig. 16(a) shows voltage (v_L) across a shoot-through limiting inductor under the HBPS when $v_{\rm ref} > 0$.

As shown, v_L has three levels: $-v_o/5$, $(0.5V_{\rm dc}-v_o)/5$, and $(V_{\rm dc}-v_o)/5$. Therefore, there are two inductor current ripples ($\Delta i_{L_{4,1}}$,$\Delta i_{L_{4,2}}$) as shown in Fig. 16(b). The inductor current ripples of 1- to 4-unit cascaded inverters under the HBPS are summarized in Table I. Fig. 16(c) shows the voltage (v_{an}) between the source of first switch S_1 and the drain of last switch S_{16} in a low-frequency (60 Hz) cycle. As shown, v_{an} is five-level staircase wave with a voltage step of $0.5V_{\rm dc}$. Fig. 17(a) shows v_L under the HUPS, and it has five voltage levels: $-v_o/5$, $(0.25V_{\rm dc}-v_o)/5$, $(0.5V_{\rm dc}-v_o)/5$, $(0.75V_{\rm dc}-v_o)/5$, and $(V_{\rm dc}-v_o)/5$.

Therefore, there are four inductor current ripples as shown in Fig. 17(b). The inductor current ripples of 1- to 4-unit cascaded inverters under the HUPS are summarized in Table II. The *n*-unit cascaded inverter with the HUPS has $(n+1)$ levels of v_L and has *n* inductor current ripples. The generalized inductor current ripple of the proposed *n*-unit cascaded inverter under the HUPS can be expressed as:

$$\Delta i_{L_{n\,N}} = \frac{\left(N\frac{V_{\rm dc}}{n}-v_o\right)\left(D-\frac{N-1}{n}\right)T_s}{(n+1)L+L_f}, \quad \frac{N-1}{n}\le D\le \frac{N}{n}. \tag{4}$$

In (4), *N* is the number of inductor current ripple for an *n*-unit cascaded inverter. For example, the 4-unit cascaded inverter has four inductor current ripples ($\Delta i_{L_{4,1}}$, $\Delta i_{L_{4,2}}$, $\Delta i_{L_{4,3}}$, and

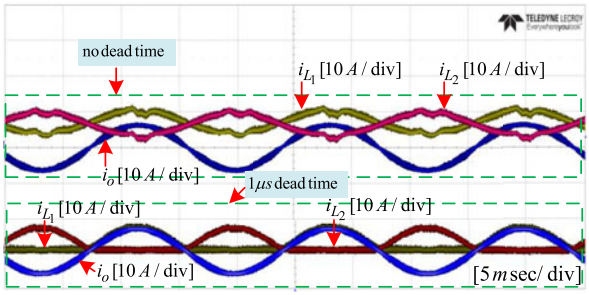


Fig. 19. Effect of dead- and overlap time on currents for TBPS.

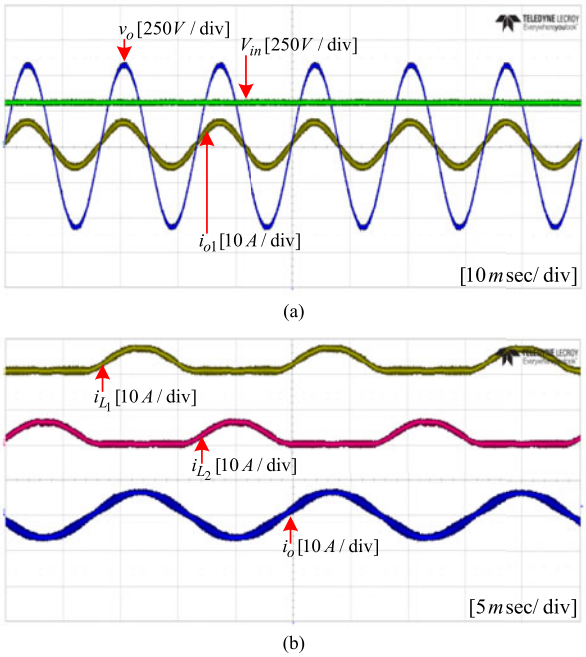


Fig. 20. TBPS. (a) Input, output voltages, and current. (b) Inductor currents.

$\Delta i_{L_{4,4}}$). The first one is obtained by putting $n = 4$ and $N = 1$ in (4). The second one is obtained by putting $n = 4$ and $N = 2$, and so on. From Figs. 16(b) and 17(b), it can be seen that the inductor current ripple under the HUPS is considerably smaller because of more levels in v_L. Fig. 17(c) shows v_{an} under the HUPS, and it is nine-level staircase wave with a voltage step of $0.25V_{\rm dc}$. Thus, the output waveforms with the HUPS can be more sinusoidal. In conclusion, for HUPS inductor current ripple is smaller, output voltage is more sinusoidal, and power loss is lower.

V. Comparison With the Conventional CHB DBI

In this section, the number of inductors and total inductance required in both the converters are compared.

1) The conventional n-unit CHB DBI requires $4n$ shoot-through limiting inductors, while the proposed inverter requires $(2n + 2)$ inductors. Thus, the proposed inverter requires $(2n–2)$ less limiting inductors.

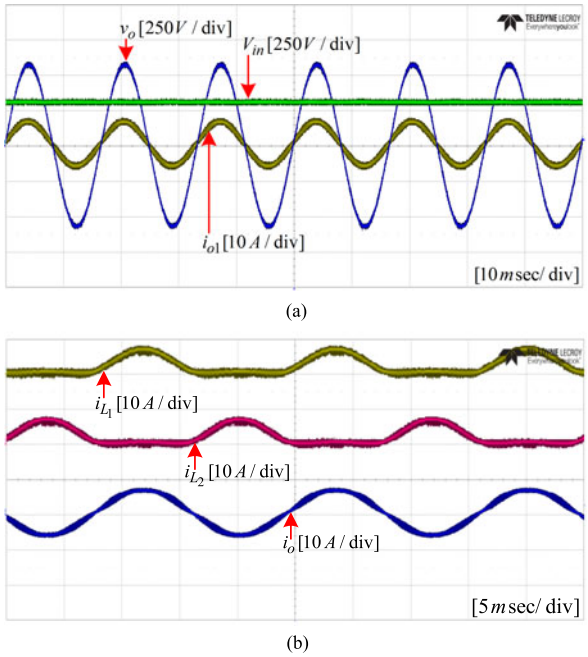


Fig. 21. TUPS. (a) Input, output voltages, and current. (b) Inductor currents.

2) During the conduction of the conventional n-unit CHB DBI, $2n$ limiting inductors and an output filter inductor $(L_{f.\rm conv})$ are always in series. Therefore, the inductor current undergoes an equivalent inductance of $L_{\rm eq.conv} = 2nL + L_{f.\rm conv}$, where L is defined as the inductance of limiting inductor in both inverters. In the proposed inverter, $(n + 1)$ limiting inductors and an output filter inductor $(L_{f.\rm prop})$ are always in series during the conduction. Thus, the inductor current undergoes an equivalent inductance of $L_{\rm eq.prop} = (n + 1)L + L_{f.\rm prop}$. In order to maintain the same inductor current ripple in both the inverters, $L_{\rm eq.conv}$ must equal to $L_{\rm eq.prop}$, which implies that the $L_{f.\rm prop}$ should be bigger than $L_{f.\rm conv}$ by $(n–1)L$. However, the total inductances of the proposed and conventional inverters are $(3n + 1)L + L_{f.\rm conv}$ and $4nL + L_{f.\rm conv}$, respectively. As a result, the proposed inverter requires $(n–1)L$ less inductance.

From the above mentioned analysis, it can finally be concluded that the proposed inverter requires $(2n–2)$ less limiting inductors in number and $(n–1)L$ less inductance.

Fig. 18 shows the proposed three-phase CHB DBI.

VI. Experimental Results

A 2-kW hardware prototype of the proposed single-phase 2-unit CHB DBI was fabricated and tested using the phase-shift control. The electrical specifications are shown in Table III.

Fig. 19 shows the inductor currents i_{L_1}, i_{L_2}, and output current i_o with the TBPS. The top waveforms show the results with no dead-time. Although no dead-time is used from the controller, due to the time delay in gate drive circuit and finite switching speed in semiconductor devices, there exists an unwanted overlap-time in gate signals. This overlap-time generates extra currents in the converter. This is the reason why

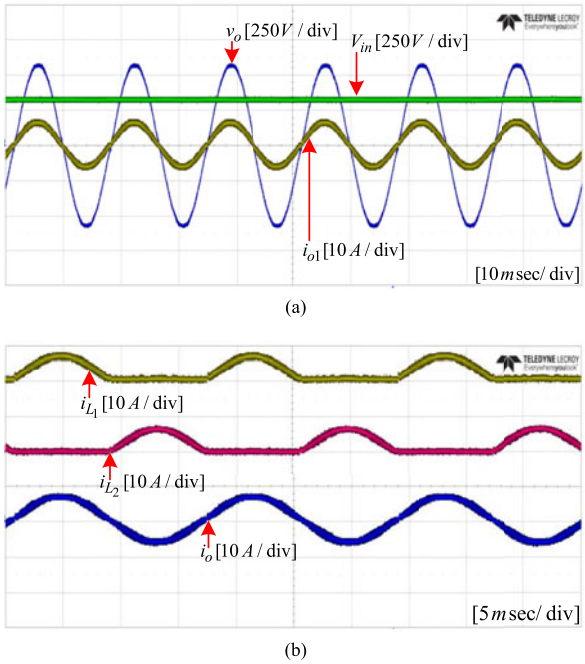


Fig. 22. HBPS. (a) Input, output voltages, and current. (b) Inductor currents.

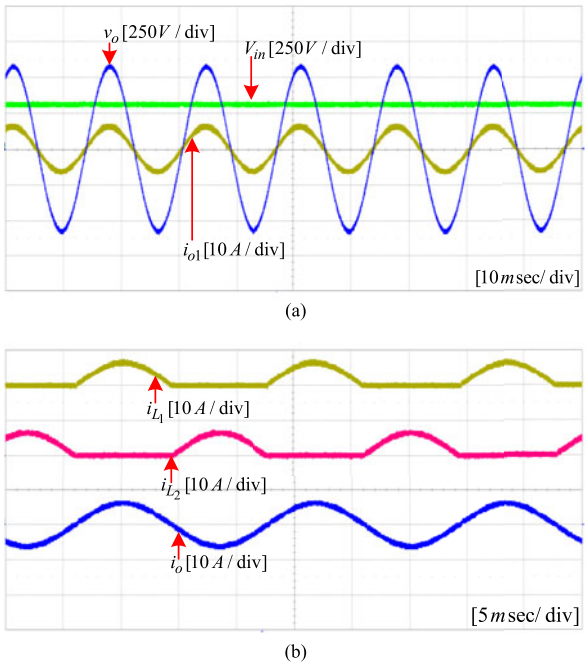


Fig. 23. HUPS. (a) Input, output voltages, and current. (b) Inductor currents.

i_{L_1} and i_{L_2} have offset. In order to reduce this, 1-μs dead-time is inserted between the switches and the results are shown in the bottom waveforms in Fig. 19. As shown, the extra currents are decreased considerably, and i_{L_1} is nearly the same as i_o for $i_o > 0$. Thus, the experimental results with the TBPS and TUPS are reported in this paper with 1-μs dead-time.

Fig. 20 shows the experimental results with the TBPS, where V_{in} is the dc source voltage in each module and v_o is the output ac voltage. The i_o and i_{o1} are the output currents before and after the output filter capacitor, respectively. Fig. 21 shows the

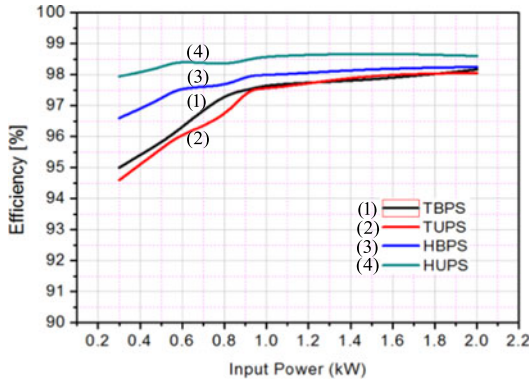


Fig. 24. Measured efficiency of the proposed 2-unit cascaded inverter.

experimental results with the TUPS. The circulating current is negligible because 1-μs dead-time is used between the switches. Figs. 22 and 23 show the waveforms with the HBPS and HUPS, respectively. For the HBPS and HUPS, no dead-time is used between the switches, and the circulating current has been eliminated completely. The current ripple of i_o with the HUPS in Fig. 23(b) is smaller than that of with the HBPS, which verifies the analysis in Section IV.

Fig. 24 compares the measured efficiencies of the TBPS, TUPS, HBPS, and HUPS. The circulating currents and simultaneous switching of all switches over the entire cycle of output voltage decrease the efficiencies of the TBPS and TUPS. The efficiency of the HBPS is higher than those of the TUPS and TBPS because of the absence of circulating currents and the fact that two switches per module are switched at high frequency. As expected, the HUPS showed the highest efficiency because of the absence of circulating currents and the fact that only one switch per module are switched at high frequency.

VII. Conclusion

This paper proposed a CHB DBI with reduced number of inductors. The proposed inverter requires fewer inductors than the conventional CHB DBI, thereby reducing the total required inductance, magnetic volume, inductor footprints, and layout complexity. Thus, the power density is improved and cost is reduced. A detailed analysis of the proposed inverter was presented and the analysis was verified by experimental results. Finally, the operation of the proposed inverter with bipolar and unipolar PWM schemes was presented and the measured efficiencies are compared.

References

[1] A. Fiel and T. Wu, "MOSFET failure modes in the zero-voltage-switched full-bridge switching mode power supply applications," in *Proc. Int. Conf. IEEE Appl. Power Electron.*, 2001, pp. 1247–1252.

[2] Q. Zhao and G. Stojcic, "Characterization of cdv/dt induced power loss in synchronous buck dc–dc converters," *IEEE Trans. Power Electron.*, vol. 22, no. 4, pp. 1508–1513, Jul. 2007.

[3] P. Sun *et al.*, "Efficiency evaluation of a 55 kW soft-switching module based inverter for high temperature hybrid electric vehicle drives application," in *Proc. 25th IEEE Appl. Power Electron. Conf. Expo.*, Feb. 2010, pp. 474–479.

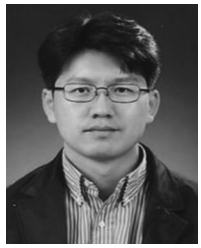
[4] D. Garabandic, "Method and apparatus for reducing switching losses in a switching circuit," U.S. Patent 6 847 196, Aug. 28, 2002.

[5] P. Sun, C. Liu, J.-S. Lai, C.-L. Chen, and N. Kees, "Three-phase dual-buck inverter with unified pulse width modulation," *IEEE Trans. Power Electron.*, vol. 27, no. 3, pp. 1159–1167, Mar. 2012.
[6] C. Liu *et al.*, "Cascaded dual-boost/buck active-front end converter for intelligent universal transfer," *IEEE Trans. Ind. Electron.*, vol. 59, no. 12, pp. 4671–4680, Dec. 2012.
[7] P. W. Sun, C. Liu, J.-S. Lai, and C.-L. Chen, "Cascade dual buck inverter with phase-shift control," *IEEE Trans. Power Electron.*, vol. 27, no. 4, pp. 2067–2077, Apr. 2012.
[8] P. Sun, C.-L. Chen, J.-S. Lai, and C. Liu, "Cascaded dual-buck full-bridge inverter with hybrid PWM technique," in *Proc. 27th Annu. IEEE Appl. Power Electron. Conf. Expo.*, 2012, pp. 113–119.
[9] Z. Yao and L. Xiao, "Two-switch dual-buck grid-connected inverter with hysteresis current control," *IEEE Trans. Power Electron.*, vol. 27, no. 7, pp. 3310–3318, Jul. 2012.
[10] Z. Yao, L. Xiao, and Y. Yan, "Dual-buck full-bridge inverter with hysteresis current control," *IEEE Trans. Ind. Electron.*, vol. 56, no. 8, pp. 3153–3160, Aug. 2009.
[11] B. F. Chen, B. Gu, J.-S. Lai, C.-Y. Ling, and C. Zheng, "Current distortion correction in dual buck photovoltaic inverter with a novel PWM modulation and control method," in *Proc. 28th IEEE Appl. Power Electron. Conf. Expo.*, Long Beach, CA, USA, Mar. 2013, pp. 727–731.
[12] L. Zheng, K. Sun, Y. Xing, and J. Zhao, "A family of five-level dual-buck full-bridge inverters for grid-tied applications," *IEEE Trans. Power Electron.*, vol. 31, no. 10, pp. 7029–7042, Oct. 2016.
[13] B. F. Chen, P. W. Sun, C. Liu, C.-L. Chen, J.-S. Lai, and W. Yu, "High efficiency transformerless photovoltaic inverter with wide-range power factor capability," in *Proc. 27th IEEE Appl. Power Electron. Conf. Expo.*, Orlando, FL, USA, Feb. 2012, pp. 575–582.
[14] X. Zhang and C. Gong, "Dual-buck half-bridge voltage balancer," *IEEE Trans. Ind. Electron.*, vol. 60, no. 8, pp. 3157–3164. Aug. 2013.
[15] A. A. Khan, H. Cha, H. F. Ahmed, and H.-G. Kim, "A family of high efficiency bidirectional dc-dc converters using switching cell structure," in *Proc. 8th Int. Conf. IEEE Power Electron. Motion Control* , May 2016, pp. 1177–1183.
[16] L. M. Tolbert, F. Z. Peng, F. H. Khan, and S. Li, "Switching cells and their implications for power electronic circuits," in *Proc. Int. Conf. IEEE Int. Power Electr. Motion*, 2009, pp. 773–779.
[17] F. H. Khan, L. M. Tolbert, and F. Z. Peng, "Deriving new topologies of DC–DC converters featuring basic switching cells," *Proc. IEEE Workshop Comput. Power Electron.*, 2006, pp. 328–332.
[18] A. A. Khan, H. Cha, and H.-G. Kim, "Three-phase three-limb coupled inductor for three-phase direct PWM AC-AC converters solving commutation problem," *IEEE Trans. Ind. Electron.*, vol. 63, no. 1, pp. 189–201, Jan. 2016.
[19] A. A. Khan, H. Cha, and H. F. Ahmed, "High efficiency single-phase AC-AC converters without commutation problem," *IEEE Trans. Power Electron.*, vol. 31, no. 8, pp. 5655–5665, Aug. 2016.
[20] H. Shin, H. Cha, H. Kim, and D. Yoo, "Novel single-phase PWM AC-AC converters solving commutation problem using switching cell structure and coupled inductor," *IEEE Trans. Power Electron.*, vol. 30, no. 4, pp. 2137–2147, Apr. 2015.
[21] A. A. Khan, H. Cha, and H. F. Ahmed, "An improved single-phase direct PWM inverting buck-boost ac-ac converter," *IEEE Trans. Ind. Electron.*, vol. 63, no. 9, pp. 5384–5393, Sep. 2016.
[22] A. A. Khan, H. Cha, and H. Kim, "Magnetic integration of discrete coupled inductors in single-phase direct PWM AC-AC converters," *IEEE Trans. Power Electron.*, vol. 31, no. 3, pp. 2129–2138, Mar. 2016.
[23] T. A. Meynard, H. Foch, P. Thomas, J. Courault, R. Jakob, and M. Nahrstaedt, "Multicell converters: Basic concepts and industry applications," *IEEE Trans. Ind. Electron.*, vol. 49, no. 5, pp. 955–964, Oct. 2002.
[24] A. Nabae, I. Takahashi, and H. Akagi, "A new neutral-point-clamped PWM inverter," *IEEE Trans. Ind. Appl.*, vol. IA-17, no. 5, pp. 518–523, Sep./Oct. 1981.
[25] P. W. Hammond, "A new approach to enhance power quality for medium voltage AC drives," *IEEE Trans. Ind. Appl.*, vol. 33, no. 1, pp. 202–208, Jan./Feb. 1997.
[26] J. Wen and K. M. Smedley, "Synthesis of multilevel converters based on single- and/or three-phase converter building block," *IEEE Trans. Power Electron.*, vol. 23, no. 3, pp. 1247–1256, May 2008.
[27] P. Lezana and G. Ortiz, "Extended operation of cascade multicell converters under fault condition," *IEEE Trans. Ind. Electron.*, vol. 56, no. 7, pp. 2697–2703, Jul. 2009.
[28] W. Yu *et al.*, "High-efficiency inverter with H6-type configuration for photovoltaic non-isolated AC module applications," in *Proc. 25th Annu. IEEE Appl. Power Electron. Conf.*, 2010, pp. 1056–1061.
[29] N. R. Zargari, P. D. Zargari, and G. Joos, "Two switch high performance current regulated DC/AC converter module," in *Proc. Conf. Rec. IEEE Ind. Appl. Soc. Annu. Meet.*, 1995, pp. 929–934

Ashraf Ali Khan (S'15) received the B.E. degree in electronics engineering from the National University of Sciences and Technology, Islamabad, Pakistan, in 2012. He is currently working toward the M.S. combined Ph.D. degree in energy engineering from the School of Energy Engineering, Kyungpook National University, Daegu, South Korea.

His current research interests include high efficiency and high reliability power converters, magnetics, grid connected inverters, and multilevel converter systems.

Mr. Khan received third Best Paper Award in ECCE-ASIA 2015, and scholarships from NICT R&D Fund Pakistan, BISE SWAT, NUST, and Kyungpook National University. In 2015–2017, he received Best Research Contribution Awards from BK.



Honnyong Cha (S'08–M'10) received the B.S. and M.S. degrees in electronics engineering from Kyungpook National University, Daegu, South Korea, in 1999 and 2001, respectively, and the Ph.D. degree in electrical engineering from Michigan State University, East Lansing, MI, USA, in 2009.

From 2001 to 2003, he was a Research Engineer with the Power System Technology Company, Ansan, South Korea. From 2010 to 2011, he worked as a Senior Researcher at the Korea Electrotechnology Research Institute, Changwon, South Korea. In 2011, he joined the School of Energy Engineering, Kyungpook National University. In 2017, he was with the Future Energy Electronics Center, Virginia Polytechnic Institute and State University, Blacksburg, VA, USA, as a Visiting Scholar. His current research interests include high power dc–dc converters, dc–ac inverters, Z-source inverters, and power conversion for electric vehicles and wind power generation.

Jih-Sheng (Jason) Lai (S'85–M'89–SM'93–F'07) received the M.S. and Ph.D. degrees in electrical engineering from the University of Tennessee, Knoxville, TN, USA, in 1985 and 1989, respectively.

In 1989, he joined the Electric Power Research Institute (EPRI) Power Electronics Applications Center, where he managed EPRI-sponsored power electronics research projects. In 1993, he then joined the Oak Ridge National Laboratory as the Power Electronics Lead Scientist, where he initiated a high-power electronics program and developed several novel high-power converters including multilevel converters and soft-switching inverters. In 1996, he joined the Virginia Polytechnic Institute and State University. He is currently the James S. Tucker Professor at the Department of Electrical and Computer Engineering and Director of Future Energy Electronics Center, Blacksburg, VA, USA. He also holds Honorary International Chair Professorship at National Taipei University of Technology, Taipei, Taiwan, and serves as a Visiting Professor at Nanyang Technological University, Singapore. His main research interests include high efficiency power electronics conversions for high power and energy applications. He published more than 380 refereed technical papers and 2 books, and received 25 U.S. patents.

Dr. Lai received the Technical Achievement Award in Lockheed Martin Award Night, 2 Journal Paper Awards, 12 Best Paper Awards from IEEE sponsored conferences, and Virginia Tech Dean's Award on Research Excellence. He led the student teams to win Top Three Finalist in Google Little Box Challenge in 2016, the Grand Prize Award from International Future Energy Challenge (IFEC) in 2011, and the Grand Prize Award from Texas Instruments Engibous Analog Design Competition in 2009. He is the founding chair of 2001 IEEE Future Energy Challenge and 2016 IEEE Asian Conference on Energy, Power, and Transportation Electrification, General Chairs of IEEE Workshop on Computers in Power Electronics (COMPEL 2000), and IEEE Applied Power Electronics Conference and Exposition (APEC 2005). He received the 2016 IEEE IAS Gerald Kliman Innovator Award.