An Efficient DSP–FPGA-Based Implementation of Hybrid PWM for Electric Rail Traction Induction Motor Control

Lijun Diao, *Member, IEEE*, Jing Tang, Poh Chiang Loh, Shaobo Yin, Lei Wang, *Member, IEEE*, and Zhigang Liu

***Abstract*—Low switching frequency is always used in an electric rail traction induction motor control system, in order to reduce switching losses and increase system reliability. But under low switching frequency, the conventional single pulse width modulation (PWM) technique for the whole speed region will produce a large number of harmonic components, which in turn cause motor heating, torque ripple, and other adverse effects. In this paper, a hybrid PWM technique formed by merging carrier-based asynchronous and synchronous modulation and optimal synchronous modulation is proposed to achieve low losses and total harmonics based on very low switching frequency. A simple low-cost and low-power digital signal processor (DSP) and field programmable gate array (FPGA) hybrid hardware structure is then adopted for implementing the technique, which fully utilizes advantages and resources of each processor. Total harmonic distortion of the system can hence be reduced by operating with the high-precision hybrid PWM, while not compromising the multirate and multitask processing requirements of traction control. Detailed implementations in both DSP and FPGA with high accuracy, low usage of resources, and computational burden are then described, focusing particularly at the smooth transitions among different PWM schemes. Simulations and experiments are eventually performed with results captured for validating the presented hybrid PWM technique.**

***Index Terms*—Digital signal processor (DSP), field programmable gate arrays (FPGA), hybrid pulse width modulation (PWM), low switching frequency, smooth transition, traction motor.**

I. Introduction

CURRENTLY, most electric rail traction systems are driven by induction motors fed by voltage source inverters (VSIs) [1]. These inverters are still mostly implemented with silicon (Si) semiconductors, such as insulated-gate bipolar transistors (IGBTs). It is certainly true that wide-bandgap semiconductor devices, such as silicon carbide, can be used for assembling improved inverters with lower losses and smaller sizes [2], [3], but their present costs and power levels are not likely to promote immediate wide-spread usage. Si devices are, therefore, still the main building blocks for inverters. No doubt, the doping process of Si devices has greatly improved their controllability and stability within a certain temperature range, but high switching and ON-state losses will still lead to excessive junction temperature that can cause the devices to fail. It is thus common to use low switching frequencies in rail traction systems to lower switching losses of IGBTs, and hence improving their thermal life and capacity.

Since introduced to the field of electric drive in 1964 by Schonung and Stemmler [4], pulse width modulation (PWM) techniques are developing very quickly, the general used PWM techniques have been studied and compared for induction motor drives in [5]–[10]. PWM techniques produce the desired voltage as the basic goal, and by optimizing the switching modes, they achieve better dc bus voltage utilization, optimize converter harmonics and losses, and improve the output frequency spectrum of three-phase converters and other indicators [5], [7], [8]. Electric rail traction converters have characteristics such as large power, low switching frequency, wide speed range, etc. If a single conventional continuous modulation method such as sinusoidal PWM (SPWM) or space vector PWM (SVPWM) is used for the whole speed range control of traction induction motor, the carrier frequency ratio $N_{\rm cr}$ in the middle to high frequency regions decreases as the motor frequency increases, which will cause the converters produce a large number of harmonic components, resulting in motor heating, torque ripple, and other adverse effects [7]. Compared to this, the discontinuous PWM (DPWM) methods are well known to reduce the harmonic distortion at high $N_{\rm cr}$ at a given average switching frequency [10]. Based on the aforementioned reasons, while taking into account the dc voltage utilization, real applications of electric rail traction converters often use hybrid PWM methods, i.e., low-frequency region using conventional continuous modulation, medium to high-frequency region using overmodulation or synchronous modulation, and finally transiting to square-wave [11].

At present, electric rail traction converters mostly use hybrid PWM techniques. There are mainly three methods for medium frequency transition zone: overmodulation, central 60°

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synchronous modulation, and optimal synchronous modulation. Mitsubishi and Toshiba adopted synchronous SVPWM for low-frequency region, then used overmodulation I and II regions to smoothly transfer to square-wave [12]. The proposed method is simple, but has high fifth and seventh subharmonics [13], [14], which makes it necessary to establish an accurate motor model to observe the fundamental current for closed-loop current control [15], and will cause low frequency oscillation problem when $N_{\rm cr}$ is not higher than 11 [16]. Early German ICE high-speed trains and China's first ac electric locomotive AC4000 used central 60° synchronous SPWM modulation technology [17]; it just modulates at central 60° area for each half-period (can be seen as opposite with conventional 60°-DPWM presented in [18]), which can be easily implemented and has low switching losses, but has very high peak motor currents and low-frequency harmonics. In contrast, optimized synchronous modulation methods can achieve different optimization goals [7], the representatives are selected harmonic minimum PWM (SHEPWM) [17]–[22] and current harmonic minimum PWM (CHMPWM) [23], [24]. ALSTOM and GE adopted the more mature SHEPWM technology [25], whereas SIEMENS used offline harmonic current optimization synchronous modulation technology [26]. Based on the high performance and fast development of processors in control systems, the optimized synchronous modulation methods will be more widely adopted.

A control system of electric rail traction converter is in fact a multitask and multirate system; the tasks include modulation, motor control algorithm, traction logic, protection logic, communication, diagnosis, etc., under different rates. To meet these requirements, over the last few years, three main implementation structures have been reported [27], [28]:

1) on-chip structures based on microcontrollers (MCUs) or digital signal processors (DSPs) [11], [17], [29]–[31], where natural sequence based operation and high-level programming languages are used;
2) on-chip structures based on field-programmable gate arrays (FPGAs) [32]–[34], where parallel operation and hardware description languages are used; and
3) hybrid structures which combine both type of processes connected through external memory interfaces [27], [28], [35]–[38], where more complicated operation can be implemented in an easier way.

In MCUs or DSPs, it is easy to implement carrier-based PWMs (CBPWMs), such as SPWM, SVPWM, and central 60°, by using up/down time-base counter and compare logic of built-in PWM modules [16], [17], [39]. But for optimal synchronous PWM (OSPWM), pulses must be generated by forced levels and strictly updated on the edge of the time-base counter [11]. In order to avoid timing conflicts among modulation, main control, and other algorithms [41], more complicated multitask and multirate management strategies using DSP/BIOS [40] or preemptible interrupt service routines (ISRs) must be taken into account [28], [37], even though the resolution of the PWMs is not very high [34], [37]. Comparatively, from [33], [42], and other literature, it seems that hardware concept based FPGAs can perfectly solve all of these problems under the following merits: better real-time, higher resolution, higher flexibility, etc. In spite of this, to implement the multitask control software of electric rail traction converter, sophisticated programming is necessary, and an expensive chip with a large number of logic elements is needed [28]. Considering the software and hardware flexibility and capability, cost, etc., a hybrid structure is a much better choice. One approach is using FPGA with embedded DSP [43], but the complex implementation limits its usage. The second approach is provided by Xilinx, Microsemi and Intel FPGAs (formerly Altera), which called all programmable system on chip (SoCs), where advanced RISC machines processors, DSP slices, and programmable logic are all included in a single chip [44]–[46]. This hybrid solution using all three types of computational blocks may therefore (maybe) work better than just using DSP or FPGA alone. But it is a brand new product which needs more man hours to migrate, where the developer's past experience and previous work will seriously influence the migration time. As a result, in this paper, the hybrid structure of a DSP in conjunction with an FPGA is chosen for electric rail traction converters. In this framework, low-cost DSP and FPGA are adopted, with fully utilized resources, DSP is used to deal with complex algorithm and low-rate tasks, and FPGA is used to implement higher real-time tasks.

The main contribution of this paper is related to a more advanced explanation about the hybrid PWM implementation for rail traction motor control, based on a relative simple and low-cost hybrid DSP–FPGA structure. The rest of this paper is organized as follows. Section II presents the basic hybrid PWM algorithms which are more suitable for the proposed hybrid structure. Section III provides the hardware implementation of the hybrid structure, and the programming implementations in DSP and FPGA. The smooth transitions are discussed in Section IV. Finally, some simulation and experimental results are presented in Section V, followed by conclusions in Section VI.

II. Hybrid PWM Algorithms

As discussed above, considering IGBTs' losses, harmonics, modulation index, etc., a hybrid PWM technique is optimized choice for a real rail traction induction motor control. In low-frequency region, the amplitudes of traction induction motor currents are always high; a low switching frequency is often used to avoid high losses; and an constant-frequency asynchronous PWM (APWM) is used to avoid complex calculation and transitions among synchronous PWMs with different $N_{\rm cr}$. But when fundamental frequency increases, PWM waveform asymmetry becomes serious with decreasing $N_{\rm cr}$; then, a conventional synchronous PWM (CSPWM) with triple and odd $N_{\rm cr}$ must be used to ensure the symmetry of the three-phase current waveform, until the linear modulation index is out of its range or subharmonic components are high [13], where OSPWM must be used instead.

In this section, the algorithm of different PWMs will be discussed, then hybrid PWM plan is given for a real electric traction motor control.

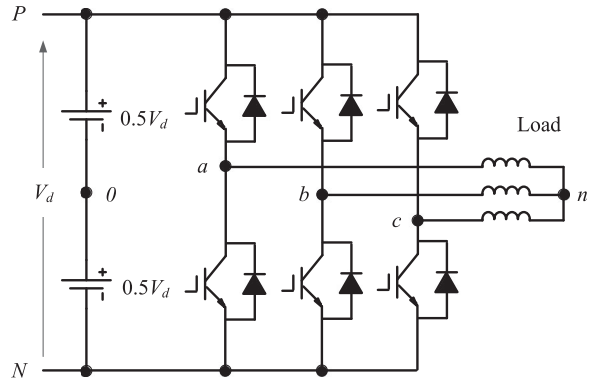

Fig. 1. Topology of VSI for electric rail traction.

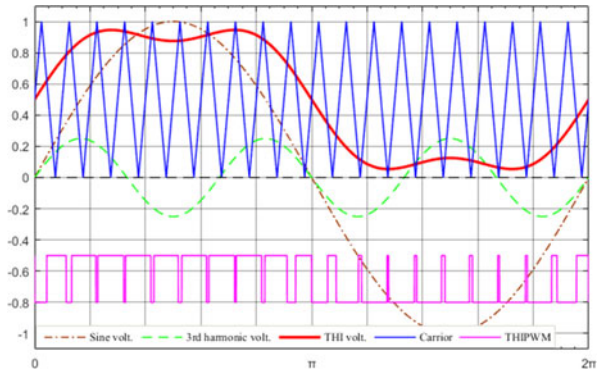

Fig. 2. THIPWM schematic for CBPWM.

A. Asynchronous THIPWM Algorithm

For high $N_{\rm cr}$ modulation, conventional SVPWM (CSVPWM) is the most popular modulation technique for three-phase VSIs, for its combined objective of higher dc bus utilization and lower total harmonic distortion (THD) [7], [8]. But in CSVPWM, three-phase pulses must be modulated at the same time, which sometime makes it not flexible enough for smooth transition where current or torque impact must be avoided. This paper uses one-fourth third-harmonic injection PWM (THIPWM4) in a hybrid structure of the motor control system. The THD of THIPWM4 is quite close to that of CSVPWM, at the cost of slight reduction of the maximum dc bus utilization [7] that has negligible effect in the low-frequency regions with high $N_{\rm cr}$ modulation. Using this method, it is much easier to achieve smooth transition for three-phase pulses independently, and the algorithm without triangular calculation is easy for FPGA to implement [8].

The general voltage source converter for electric rail traction is shown in Fig. 1.

From the figure, with respect to dc bus negative point *N,* the one-fourth third-harmonic injection three-phase voltages $v_{\rm xN}$ can be derived [7]

$$\begin{aligned} v_{\rm xN} &= v_{x0} + v_{0N} \\ &= \frac{V_d}{2} + \frac{2V_d M}{\pi}\left(\sin\left(\omega t - \delta_x + \phi\right) + \frac{\sin 3\omega t}{4}\right) \end{aligned} \quad (1)$$

where v_{x0} is phase voltages with respect to the fictitious dc center tap 0, V_d is dc bus voltage;ω is the fundamental angle frequency, ϕ is the initial phase, δ_x is the phase shift among three-phase voltages, which is 0, $\frac{2\pi}{3}$, $\frac{4\pi}{3}$ for phases a, b, and c, respectively;

M is modulation index, which is defined by fundamental peak phase-to-neutral voltage $v_{\rm pn}$ to the peak voltage (which is $\frac{2V_d}{\pi}$ [13]) of the square-wave modulation as $M = \pi v_{\rm pn}/2V_d$. In the linear modulation range, the maximum value of M is 0.907 for THIPWM [13].

In order to implement the modulation algorithm in FPGA more easily, the three-phase reference modulation voltages $v_{\rm mx}$ can be written as

$$v_{\rm mx} = \frac{1}{2}\left(1 + \sin\left(\omega t - \delta_x\right) + \frac{1}{4}\sin 3\omega t\right). \quad (2)$$

$v_{\rm ma}$ is shown as red wave in Fig. 2 as an example, the THIPWM4 modulation wave ranges within 0.093–0.907. Then, the initial PWM pulse can be produced by active-high comparison as the pink one.

B. Synchronous THIPWM Algorithm

As aforementioned above, synchronous THIPWM is used as a transition modulation to connect APWM and OSPWM. The modulation algorithm is quite similar with that of asynchronous THIPWM, the difference is that synchronous control is based on fundamental frequency, i.e., the carrier frequency is not constant but changed according to fundamental frequency and $N_{\rm cr}$. Besides, the value of $N_{\rm cr}$ must be maintained as a multiple of three because triple subharmonics are of no concern in isolated neutral load of three-phase converter [13]. The presented technique uses 15-$N_{\rm cr}$ for the synchronous modulation zone.

CSPWM has the continuity criterion of the carrier with that of APWM, which makes it possible to link up easily with each other at any phase position, and no additional transition strategy has to be used.

C. CHMPWM Algorithm

At present, SHEPWM and CHMPWM are the most popular OSPWMs for the elimination of low-order harmonics, and SHEPWM technique is much more widely used for applications in the literature. But SHEPWM has a drawback of boosting the next higher level harmonics near the eliminated harmonics, which will cause nonoptimal harmonic loss in a motor where the root-mean-square (rms) ripple current is emphasized [13], which will also make the smooth transition more difficult (will be discussed in Section IV). Therefore, CHMPWM is adopted in this paper to achieve minimum current weighted THD ($\rm WTHD_i$).

The CHMPWM algorithm is based on that of SHEPWM, and its expression can be deduced from the wave shown in Fig. 3.

The wave has half-wave and quarter-wave symmetry; it has only odd harmonics with sine components, then the phase-to-*N* voltage can be expressed by a Fourier series as [7], [13]

$$\begin{cases} v_{\rm xN} = \frac{V_d}{2} + \sum_{k=1,5,7\ldots}^{\infty} V_k \sin(k\omega t) \\ V_k = \pm\frac{2V_d}{k\pi}\left(1 + 2\sum_{i=1}^{K}(-1)^i \cos k\alpha_i\right) \end{cases} \quad (3)$$

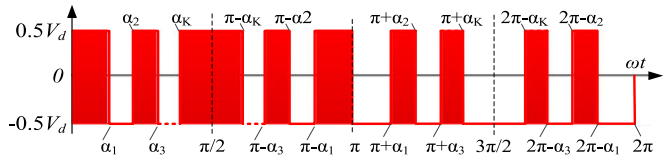

Fig. 3. Phase voltage wave for SHEPWM with *K* number of angles.

TABLE I
MAIN PARAMETERS OF THE TRACTION INDUCTION MOTOR

Parameters	Value
Rated dc bus voltage	1650 V
Rated line voltage of motor	1287 V_{rms}
Rated/maximum stator current of a motor	88/150 A_{rms}
Rated power of four traction motors	4 × 160 kW
Rated/maximum stator frequency of motor	84.5/176 Hz
Pole pairs of motor	2
Maximum switching frequency	630 Hz

where k is order of harmonic, K is number of notch angles, α_i is the number i notch angle, V_k is phase voltage peak value of kth-order harmonic, and $+1$ and -1 are taken for even and odd values of K, respectively.

The optimal object of CHMPWM technique is to minimize the THD of line current, which can be calculated from the phase voltage divided by the effective leakage impedance of the traction motor [13]. Furthermore, WTHD_i, which is expressed as a per unit of the fundamental component of line current [7], is more convenient for the expression. Then, CHMPWM algorithm can be expressed as

$$\begin{cases} \min: \ \mathrm{WTHD_i} = \frac{1}{k}\sqrt{\sum_{k=5,7,11\ldots}^{\infty}\left(\frac{V_k}{V_1}\right)^2} \\ \text{s.t.}: \ M = \pm\frac{1}{k}\left[1+2\sum_{i=1}^{K}(-1)^i\cos k\alpha_i\right] \\ \text{s.t.}: \ 0<\alpha_1<\alpha_2<\ldots<\alpha_K<\pi/2 \end{cases} \cdot \quad (4)$$

The notch angles can then be iterated in a computer program and saved in look-up tables (LUTs) [25]. With K number of notch angles, the fundamental magnitude can be controlled and number of $K-1$ harmonics can be eliminated. For low-frequency region, the number of notch angels can be increased to minimize WTHD_i, but the LUT will be unusually large, and much more logic elements of FPGA will be needed; at the same time, N_{cr} of CSPWM and APWM is high enough to keep good quality modulation performance. So in this presented implementation, only 1, 2, 3, 4 are adopted for K.

D. Hybrid PWM Plan

In this study, the proposed modulation strategy for the whole speed range will be APWM, CSPWM, OSPWM, and square-wave, on behalf of reducing the THD in motor line current, and resulting in lower pulsating torque than the individual methods concerned.

For an electric rail traction system with the main parameters presented in Table I, the proposed hybrid PWM can be planed as shown in Fig. 4, where the modulation methods (carrier frequencies), dc bus voltage V_d, rms line voltage $V_{\mathrm{ll(rms)}}$, and calculated total loss of the converter P_{pass} are characterized versus fundamental frequency.

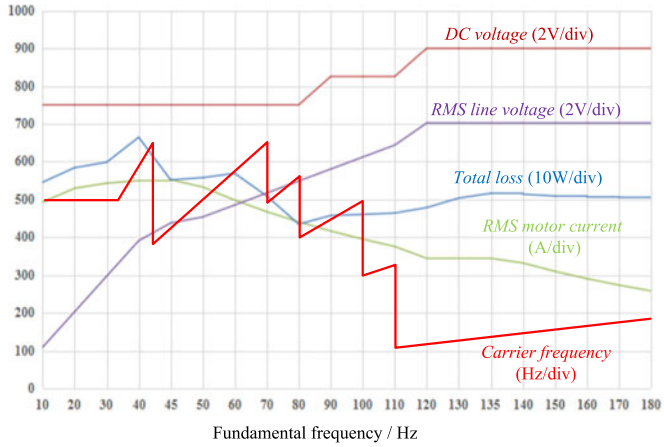

Fig. 4. Envelopes of VSI variables versus fundamental frequency.

From Fig. 4, it can be seen that for the whole speed region, the proposed APWM will transit to square-wave through 15-switch CSPWM (15-CSPWM), and 4–1 notch angles OSPWMs (9-CHM to 3-CHM). The line voltage changes by fundamental frequency to meet the flux and torque demand, and finally reaches a maximum level by square-wave ($M = 1$), which has minimum switch operations and reduces the effective motor current and losses. The dc bus voltage changes according to the requirement of the output line voltage. The modulation modes are changed not only according to the maximum available switching frequencies, but also the maximum available modulation indexes. The total loss is reduced with the decreasing carrier frequency, but when it finally transits to square-wave mode, the conduction loss is significant and the total loss is increased.

The proposed hybrid PWM plan has made it possible to keep good traction motor control in the full speed range, where each PWM must be characterized by the following requirements:

1) limited peak current to reduce current stress on IGBT;
2) respect the limitation of switching frequencies and relatively low switching frequencies to limit converter losses and boost maximum available current capacity of IGBT;
3) harmonic content is acceptable;
4) the range of M and notch angle LUTs must meet the feasibility of PWMs and FPGA resource;
5) smooth transition among different PWMs.

III. HYBRID PWM IMPLEMENTATION IN DSP AND FPGA

A low cost and low power consumption hybrid DSP–FPGA structure consisting of a DSP and an FPGA is proposed for the electric rail traction motor control. In the structure, floating point TMS320F28335 of Delfino series from Texas Instruments and EP1C12Q240 of Cyclone FPGA series from Intel FPGAs are used.

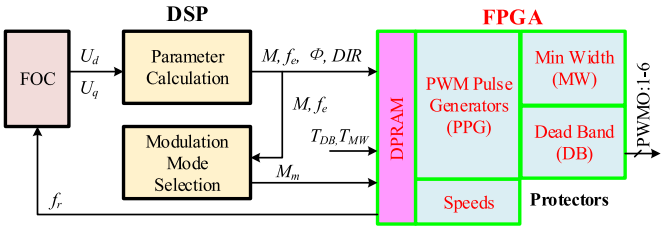

Fig. 5. Block diagram of hybrid PWM implementation.

A. Overview of the Implementation

Hybrid PWM implementation includes four parts:

1) parameter calculation;
2) modulation mode (M_m) selector;
3) pulse generator;
4) protector.

The often modified parts 1) and 2) are executed in the DSP, whilst the repetitive parts 3) and 4) that rarely changed will be programmed in the FPGA. Then, the proposed hybrid PWM will be implemented using the pattern shown in Fig. 5.

Parameters of PWM implementation include stator frequency (f_e), initial phase (ϕ) in deg (°), M, and rotation direction (DIR) which are calculated from field oriented control (FOC) output voltages (U_d, U_q) and rotor frequency (f_r) from FPGA. These parameters are also used for M_m selection. Two PWM protection submodules, minimum width (MW) and dead band (DB), are also used, where the protection conditions can be set by DSP through two reference times $T_{\rm DB}, T_{\rm MW}$. As shown in the figure, all related parameters are transmitted between the two devices through dual-port RAM (DPRAM) in FPGA.

B. DSP Implementation

As aforementioned low-cost and easy-handling reason, the integrated analog to digital converters (ADCs) in DSP are used for analog sampling and thus FOC algorithm is finished by DSP. The parameters obtained from the output voltages of FOC can be expressed as

$$\begin{cases} M = \sqrt{U_d^2 + U_q^2} \Big/ \frac{2V_d}{\pi} \\ \phi = \frac{360}{2\pi} \text{arctg} \dfrac{U_q}{U_d} \\ |f_e| = |f_r + f_{\rm sl}| \\ \text{DIR} = \text{sign}(f_e) \end{cases} \tag{5}$$

where $f_{\rm sl}$ is slip frequency calculated from the FOC algorithm.

There are square (SQRT) and inverse trigonometric (ARC) function operations, and execution comparison between DSP and FPGA is presented in Table II.

The operations can be easily handled by using floating point unit of DSP, and it is fast enough to modify the operations within each FOC operation cycle. Obviously, too many resources are need if SQRT or ARC is directly handled in FPGA. CORDIC or intellectual property (IP) cores can be used for optimization, but nearly 10% resource of the presented FPGA and much more complicated method will be required [47], [48], which is hardly

TABLE II
EXECUTION COMPARISON BETWEEN DSP AND FPGA

Algorithm	DSP C28x		FPGA uses pipeline or IP core		
	Max CPU Cycles	Code Size (Byte)	Max CPU Cycles	Register Number	LUT Number
SQRT	28	18	1	0	1120
ARC	50	18	1–2	747	1265

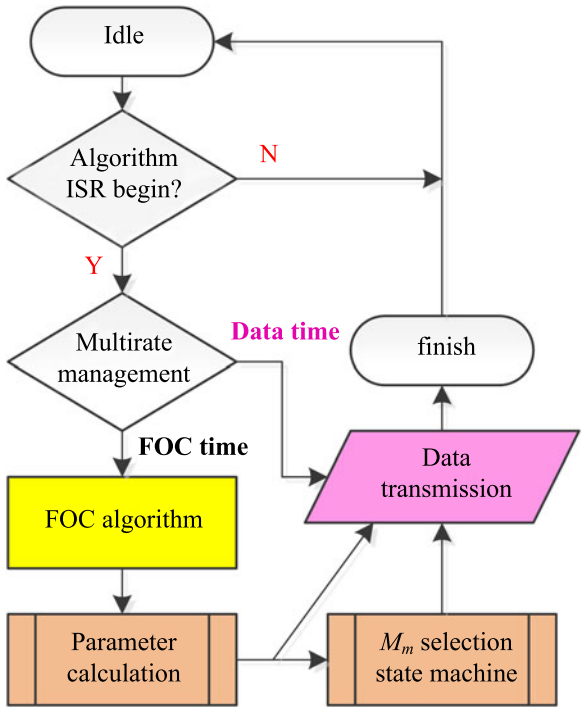

Fig. 6. DSP operation for the hybrid PWM algorithm.

acceptable by the low-cost FPGA, even if the calculation speed is much higher. As a result, the parameters are calculated in DSP according to the tradeoff between speed and resources.

Then, arithmetic left shifting is also used to improve the accuracy of the transmitted analog signals and reduce the burden of FPGA computing as follows:

$$\begin{cases} f_e^Q = |f_e| \times 2^7 \\ \varphi^Q = \varphi \times 2^7 \\ M^Q = M \times 2^{10} \end{cases} \tag{6}$$

where superscript "Q" denotes fixed-point format used in FPGA.

The flowchart of DSP for hybrid PWM is shown in Fig. 6, where different counters based on 4k-ISR and "switch-case" statement are used for multirate task management. The parameters of hybrid PWM are sent to FPGA immediately to reduce the delay time after the calculation is completed, but general data transmission will be processed periodically. M_m can then be selected based on the values of f_e and M; the state machine of the selection in DSP is shown in Fig. 7 for acceleration and deceleration conditions.

In other words, the presented DSP implementation method considered the low cost of the system architecture and made

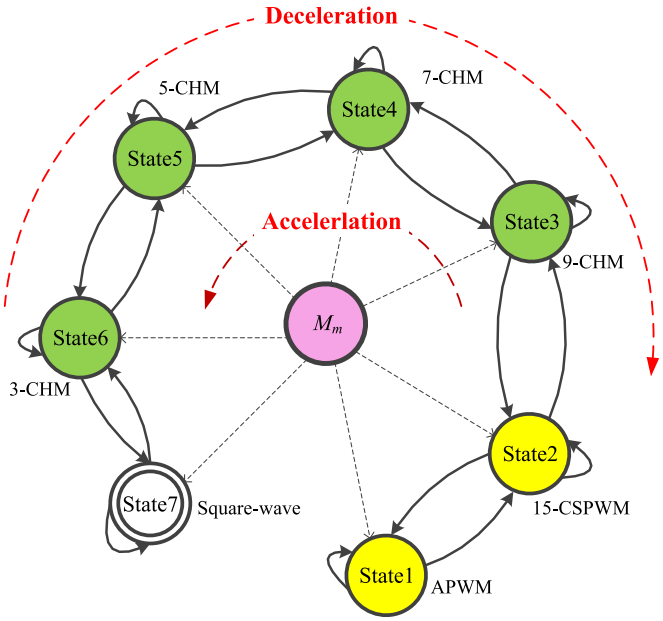

Fig. 7. State machine of modulation mode selection.

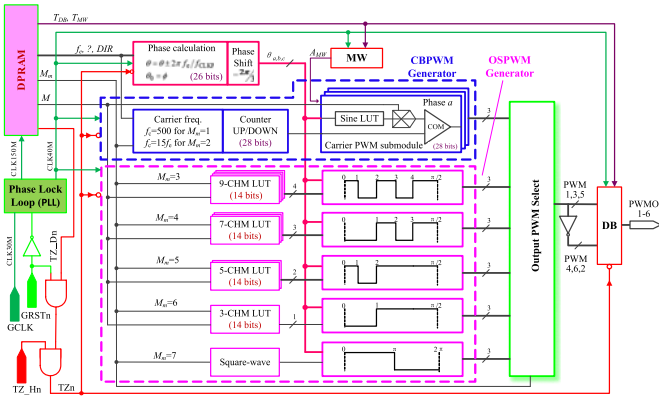

Fig. 8. Hybrid PWM implementation module in FPGA.

full use of the advantages of DSP, and matched the processing speed and system control needs. Furthermore, calculating the parameter in DSP is much more flexible than that in FPGA, especially during the test period, for it is much easier to modify DSP programming.

C. FPGA Implementation of Hybrid PWM Pulses

Hybrid PWM implementation in FPGA is shown in Fig. 8, where GCLK is 30 MHz global clock input, GRSTn is active low global reset signal from the power supply management electronic circuit, and TZn is active low trip zone signals with "_Dn" from DSP software protection and "_Hn" from hardware protection.

The module can be divided into four main parts: clocks, communication, pulse generators, and protections. Clocks are generated by a built-in phase-locked loop (PLL) IP core, where a 150 MHz clock is used for communication, and a 40 MHz clock is used for the implementation. The communication is based on DPRAM, which can be easily implemented by the built-in IP cores too. This section will mainly describe the pulse generation; the protections will be discussed in the next section.

1) Position Calculation of Modulation Waves: A global three-phase position calculation of the modulation waves is needed for all pulse generators. The positions are defined in deg to access the LUTs easily, which can be expanded by shifting left 17 bits. Considering the integrating algorithm by arithmetic left shift in DSP, the actual clock for position calculation must be $f_{\mathrm{CLKP}} = f_{\mathrm{CLK40M}}/2^7$. Then, the basic position calculation can be modified by combining (6) to fit for FPGA fixed-point characteristics as

$$\begin{cases} \theta_a^Q = \theta_a^Q \pm (360 << 17) f_e^Q / f_{\mathrm{CLK40M}} \\ \theta_{a0}^Q = \varphi^Q << 10 \text{ when DIR} = 1 \text{ or} \\ \theta_{a0}^Q = (360 << 17) + (\varphi^Q << 10) \text{ when DIR} = 0 \\ \theta_b^Q = \theta_a^Q - (120 << 17) \\ \theta_c^Q = \theta_a^Q - (240 << 17) \end{cases} \tag{7}$$

where the subscript "0" denotes an initial value, and $+1$ and -1 are taken for positive (DIR $= 1$) and negative (DIR $= 0$) directions, respectively.

2) CBPWM Generator: A Sine LUT and a carrier wave generator are the two main parts for CBWPM generation. The Sine LUT includes 360 numbers of sine values of one period THIPWM4 wave. It must be noticed that the values of Sine LUT must cover the modulation index range from 0 to 1 for the multiplication calculation between M from DSP and Sine LUT in FPGA. When looking up the table, the nodes are usually not integers but between two points, then linear interpolation method can be used to reduce the error. But the linear interpolation will bring additional multiplication computing and need more space of FPGA (shown in Table IV), which should be avoided in the presented low-cost FPGA with heavy burden. Therefore, LUT values can be obtained by approximation, and the relative errors can be reasonably accepted. Then, the output multiplied by M^Q can be written as

$$A_{M\sin}^Q = M^Q \mathrm{Sine}(\mathrm{int}(\theta_x^Q >> 17)). \tag{8}$$

Defining the maximum amplitude of the Sine LUT is 10e5, the equation shows that the maximum value of $A_{M\sin}^Q$ will be $A_{M\sin\_\max}^Q = (2^{10} \times 10^5)$ when M and the Sine LUT both reach their peak values.

For the carrier wave generator, the maximum value of the carrier amplitude A_{carrier}^Q must be equal to $A_{M\sin\_\max}^Q$ from the active-high pulse generation method point of view. Defining the cumulative step size of the carrier wave generator is h_c and the cumulative clock is $f_{\mathrm{CLK\_C}} = f_{\mathrm{CLK40M}}/25$, then the following equation holds

$$h_c f_{\mathrm{CLK40M}} \Big/ \left(50 N_r \frac{f_e^Q}{2^7}\right) = A_{M\sin\_\max}^Q. \tag{9}$$

Substituting all the related values yields

$$h_c = N_r f_e^Q. \tag{10}$$

TABLE III
CALCULATION PERFORMANCE PARAMETERS OF PWM GENERATION

Algorithm	Control frequency divider by f_{CLK40M}	Bit-width	Accuracy
Phase positions	128	26	$1/2^{17}$ deg
Sine LUT	128	17	$1/10^5$
Carrier counter	25	28	$h_c/(2^{10} \times 10^5)$
M for CBPWM	128	10	$1/2^{10}$
M for OSPWM	128	7	1/100
CHM LUTs	128	14	$1/2^7$ deg

The differences between APWM and CSPWM can be reflected through h_c such as

$$\begin{cases} h_c = 500 << 7 & \text{for } M_m = 1, (i.e.,\ \text{APWM}) \\ h_c = 15 f_e^Q & \text{for } M_m = 2, (i.e.,\ \text{CSPWM}) \end{cases}. \quad (11)$$

Then, the CBPWMs for high-side switches are generated by active-high comparing between A^Q_{carrier} and $A^Q_{M\sin}$.

3) OSPWM Generator: OSPWM waves have half-wave and quarter-wave symmetry, so only angles of the first quarter-wave have to be saved in the offline LUTs, which are defined by the format *array*[*K*][100] according to the relationship of the notch angle versus *M*. Considering the tradeoff between accuracy and FPGA resource, the notch angles and *M* will be magnified 128 and 100 times in the LUTs. Then, the output of the LUTs can be achieved by

$$\alpha_K^Q = \mathrm{array}[K][\mathrm{int}(100M^Q >> 10)] \in [0,\ 90 \times 2^7]. \quad (12)$$

Then, OSPWM pulses can be easily generated by comparing the notch angle α_K^Q and the position calculator output θ_x^Q. Giving the first quarter-wave of 9-CHM as an example, the logic in FPGA can be written on every rising_edge of f_{CLKP} as

$$\begin{cases} \theta^Q = \theta_x^Q >> 10; \\ \theta^Q \le \alpha_1^Q :\ \mathrm{OSPWM}_x = 1; \\ \theta^Q \le \alpha_2^Q :\ \mathrm{OSPWM}_x = 0; \\ \theta^Q \le \alpha_3^Q :\ \mathrm{OSPWM}_x = 1; \\ \theta^Q \le \alpha_4^Q :\ \mathrm{OSPWM}_x = 0. \end{cases}$$

Finally, the initial hybrid PWMs for high-side switches are selected by multiplexer switch according to the modulation mode. And the PWMs for low-side switches can be easily generated by inverting the high-side pulses.

4) Performance Comparison With Other Options: Main calculation performance parameters including clocks, bit-width, and accuracy are listed in Table III for convenience. It can be seen that the accuracy of each parameter is very high, which will lead to much more precise PWMs than that implemented in DSP, this is advantageous for different mode transitions which require successive parameter changes.

For further performance evaluation of PWM generation, a comparative analysis with other possible options in terms of resources, accuracy, and computational burden can be summarized in Table IV. The table mainly focuses on the algorithms for analog parameters, sine magnitudes, and OSPWM, which have the most important impact.

TABLE IV
PERFORMANCE COMPARISON OF MAIN ALGORITHMS

Analog parameters	Options	Proposed shifting		Method in [32]
	Usage comparison	Easy handle, but calibration requires high consistency.		A little complicated, but more independent.
Sine LUT	Options	Proposed	Linear interpolation [49]	CORDIC (17bits) [50]
	One-phase resource (LEs)	1320	1320 + 182	1000
	Relative error (%)	0.0038–0.888	0.0035–0.357	0.0021 [51]
	f_{MAX} (MHz)	150	150	220
OSPWM Generation	Options	Proposed offline LUT		Online calculation [52]
	Computational burden	low		much higher

Fixed point is the best choice to reduce the computational burden of the low-cost FPGA, amongst the possible options for transferring the floating point analog parameters, such as the method given in [32]; the proposed shifting method is the easiest way, but high consistency is required for the programming design of FPGA and DSP. Altera provides an IP core of ALTFP_SINCOS for sine algorithm [48], which can be very easily handled, but its input width is fixed and very high resource is needed. Sine LUT without linear interpolation is proposed in this study to avoid the additional resource requirement for multiplications, where the relative error can be accepted for this research. But Cordinate Rotation Digital Computer (CORDIC) algorithm looks better, which can be considered for further optimization. High frequency clock and high resolution angles are the most important items for OSPWM generation. The lowest OSPWM resolution (%) in this study is at the beginning of 9-CHM with the value calculated as 100% × 9 × 42/40 MHz = 0.001%. Saied *et al*. [52] proposed an artificial neural network online optimization angle calculation method in FPGA that works well, but the computational burden is quite high. So this paper uses an offline method and improves the angle accuracy by 128 times.

D. Pulse Protections in FPGA

Pulse protections include TZ for error or reset trig, DB for shoot-through protection, and MW for avoiding transient abnormal actions. TZ trig and DB are very common in VSI protections; this part mainly focuses on the MW protection.

As described in [13], when *M* approaches 1, the notch and pulse widths near the center tend to vanish, which is not enough to complete switching operation. For inductive loads such as motor, the antiparallel diode of the other side IGBT in the same leg will have to turn OFF immediately after the not completely turning-ON, which will cause serious *dv*/*dt* and oscillation that is harmful for IGBT reliability. So, the minimum-width notches

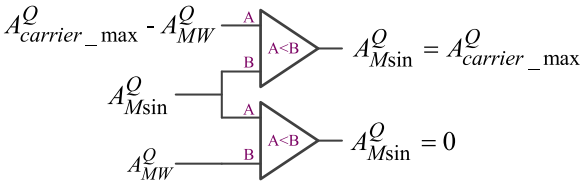

Fig. 9. Minimum width protection logic.

TABLE V
RESOURCES SUMMARY IN FPGA

Device	Cyclone EP1C12Q240I7
Total logic elements	11 626/12 060 (96%)
PWM generation	8896 (7435)
Speeds calculation	1546
Communication	340
Protections	1272
Total pins	138/173 (80%)
Total PLLs	1/2 (50%)

or pulses must be avoided. According to the algorithm, MW protection is more likely to occur in CBPWM generation.

In order to ensure the real-time of the pulse from calculation, generation to output, MW algorithm is not easy to finish after DB submodule, it should be carried out during the initial pulse generation. At the same time, DB time $(T_{\rm DB})$ has to be added to the MW limit time $(T_{\rm MW})$ for consideration, where both times are transmitted from DSP in the unit of μs. Let $A_{\rm MW}$ be the peak amplitude difference between the carrier wave and the modulation wave, it can be deduced from Fig. 2 that

$$A_{\rm MW} = \frac{T_{\rm DB} + T_{\rm MW}}{10^6} f_c A_{\rm carrier\_max}. \tag{13}$$

Rewriting in the integer form of FPGA yields

$$A^Q_{\rm MW} = \frac{T_{\rm DB} + T_{\rm MW}}{10^6} \frac{N_r f^Q_e}{2^7} A^Q_{\rm carrier\_max}. \tag{14}$$

Then, the following logic shown in Fig. 9 is used to modify the comparison input for the CBPWM generation.

E. FPGA Resource Usage Summary

The FPGA resource usage of the proposed control system in this paper is summarized in Table V according to Quartus II. It shows that PWM generation uses most of the resources, as there are several high resolution LUTs in it, which may be implemented in the ROM for future optimization. The speed calculations (without division or multiplication algorithms) and system protections use nearly the rest of the resources.

IV. SMOOTH TRANSITION DISCUSSION

Hybrid PWM technique needs to transit between different modulation modes; the carrier ratio decreases with the gradually increasing frequency when traction accelerates, and vice versa. The carrier ratio's significant change will affect the precise phase control of the PWM output voltage. In addition, the dead time and microprocessor digital control error can also easily lead to the phase deviation of the inverter between the actual output voltage and the reference voltage. All these factors will cause the traction motor current and torque shock in the transition [53].

In this section, the general transition rules will be given first, then more discussion on transitions, including transition methods, performance comparisons between a single DSP and the proposed structure, SHEPWM and CHMPWM, will be presented.

A. General Rules of Smooth Transition

In order to keep the stability of motor currents and torques, when transiting between different PWM modulation modes, the following aspects need to be considered to keep the succession of PWMs from slow speeds to square-wave.

First, try to keep the fundamental succession, including smooth changes of phase and amplitude. Fundamental succession depends mainly on the accuracy of switching angle and control algorithm.

Then, the impact of harmonics cannot be ignored. Harmonic phases are not guaranteed to be continuous in different modes of switching, because the harmonic content is different for each mode, and phase mutations are inevitable. So the transition should avoid too large overall harmonic mutation, in order not to cause the harmonic current impact.

Finally, hysteresis must be included at each transition so that the system does not cycle continuously between two different modulation modes at a certain speed. In the proposed strategy, a hysteresis of 0.5 Hz is used.

B. More Discussion on Smooth Transition

There are several different transitions for the hybrid PWM in the whole speed range. The first transition occurs between two CBPWMs of APWM and CSPWM, where the carrier frequencies are nearly similar and *M* is continuous, which make it easy to achieve smooth transition. The transition will also become very easy when it happens between three-pulse OSPWM and square-wave [11], as the angle of the three-pulse OSPWM will decrease to zero according to the increasing *M*, which is square-wave. The motor currents and torque can be kept stable during this transition.

But the fundamental succession and harmonic impact become more significant when the transitions occur between CSPWM and OSPWM, or inside OSPWMs, especially when only a single MCU or DSP is used or SHEPWM is used for OSPWM.

1) Transition Comparison Between a Single DSP and the Proposed Structure: The fundamental succession relies on high precision OSPWMs, to achieve which there are two methods in a single DSP.

The first one uses forced pulse levels through general IOs based on relatively much higher frequency interrupt. This method does not need complex calculation, but it will easily cause time conflict between different tasks as presented in [41]. Take the transition point from 15-CSPWM to 9-OSPWM as an example, where the fundamental frequency equals 42 Hz. For the switching angle accuracy of 0.01°, a fundamental period requires to count 36 000 (360/0.01) times, which means that the

DSP timer interrupt frequency needs to be 1512 kHz (36 000 $*$ 42). The frequency will become much higher when the fundamental frequency increases. In fact, it is nearly impossible to realize so high frequency in DSPs, which makes the accuracy of OSPWMs to be reduced. But the modulation does not depend on the instantaneous voltage or current, so it is possible to solve the problem that all the parameters can be precalculated based on the last higher level control algorithm ISR and scheduled using the PWM module.

Wei *et al*. [11] presented another easier idea to generate OSPWMs through PWM modules of a DSP, where continuous up/down counter is used and the compare values are calculated and reloaded according to the switching angles in each sample period. By this way, very high frequency interrupt is not needed, and time conflicts will not occur, but there are still some drawbacks as follows:

1) The pulse level can only be modified one time in each sample period, which means the difference of every two adjacent switching angles must be larger than the period. For example, if the angle difference is less than 5° for the fundamental frequency of 50 Hz, the sample frequency must be not less than 3.6 kHz ($2\pi * 50/(5\pi/180)$). In order to avoid this conflict, higher sample frequency is needed or minimum angle difference must be limited. Both will affect the control performance of the DSP. The problems can be solved by separating pre-emptible sampling ISR and PWM update ISR, and a better solution is provided by TI's new version DSPs.
2) The compare values and comparison modes are reloaded in each sample interrupt; it may cause some angle error if the pulse level happens to change in the period or underflow point of the time counter.
3) The OSPWMs are still generated based on the PWM modules built-in the DSP, which means the accuracy of the OSPWM is still dependent on the accuracy of the PWM modules.

The above-mentioned reasons will weaken the succession of the fundamental amplitude and harmonic optimization effect, even cause additional problem in transition. Then, more complicated transition methods have to be taken into account for transitions between CSPWM and OSPWM, or inside OSPWMs.

But in the proposed structure, DSP is just used for modulation mode selection, much higher frequency and parallel processing FPGA can easily solve these problems, which makes the transition more easy to control. The later simulation and experimental results validate this merit.

2) Transition Comparison Between SHEPWM and CHMPWM: When transitions are taken for SHEPWMs, fundamental succession is not enough and harmonic impact affects more significantly. The transitions are better to be processed at phase positions of $\pi/2$ and $3\pi/2$, where theoretically the current harmonics are zero according to the calculations in [11] and [53]. Otherwise, the low harmonic mutations will cause serious current and torque vibrations when transiting from CSPWM to OSPWM, or inside OSPWMs, which can be seen from the simulation results shown in Fig. 10.

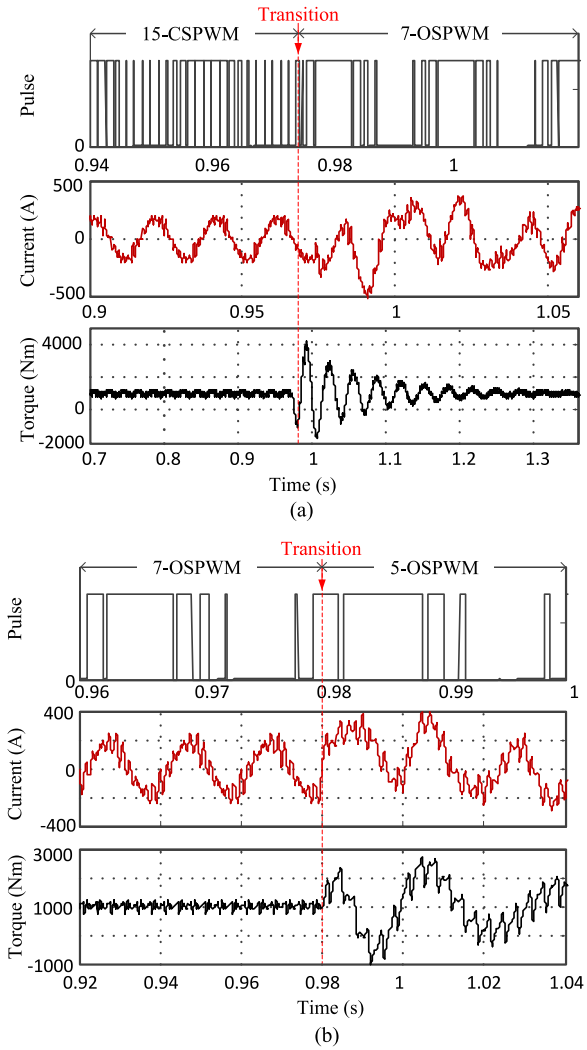

Fig. 10. Transition vibration simulation for SHEPW. (a) 15-CSPWM to 7-OSPWM. (b) 7-OSPWM to 5-OSPWM.

More simulation of SHEPWM and CHMPWM are done for comparison, and the harmonic spectrum of 9-OSPWM and 7-OSPWM is shown in Fig. 11 as an example to explain the different harmonic impacts for transition. It can be seen from the figures that though the THD differences from 9-OSPWM to 7-OSPWM of SHEPWM and CHMPWM are quite similar (both are 10%), SHEPWM has a serious harmonic mutation of 11th order harmonic, which easily cause current vibration. But CHMPWM aims to realize the optimization of the total current harmonics. Although it cannot completely eliminate some current harmonics, the whole harmonic content distribution is even, which results in no significant sudden change of the harmonics in the process of transitions.

In other words, CHMPWM can easily realize the smooth transition when combining the high precision PWM generator in FPGA with its harmonic characteristics, without complicated software process in a single DSP and strict harmonic phase or amplitude control that is used for SHEPWM.

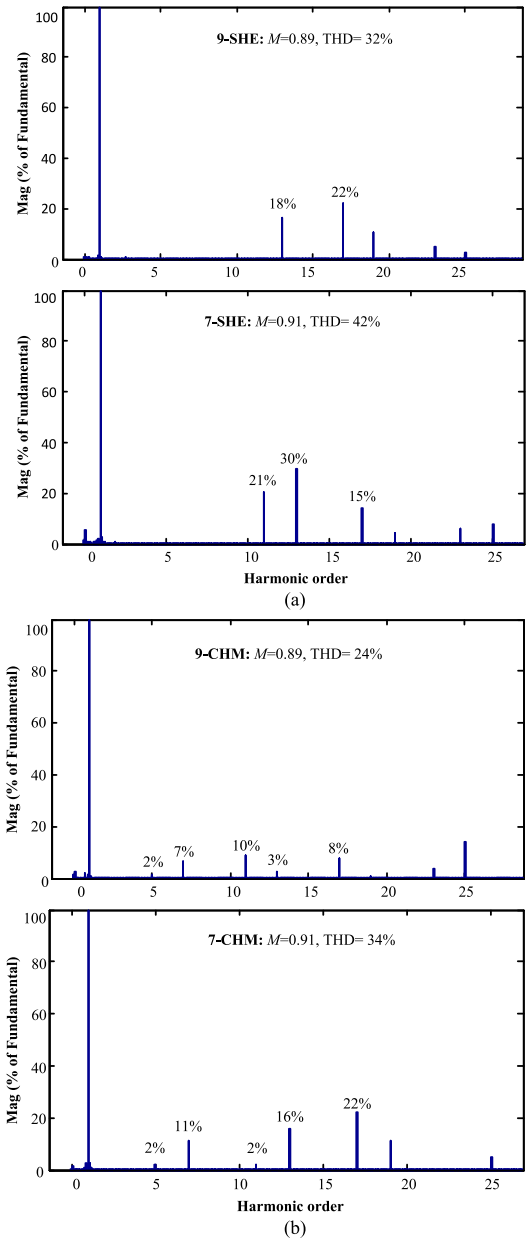

Fig. 11. Different harmonic examples for SHEPWM and CHMPWM. (a) 9-SHE to 7-SHE (b) 9-CHM to 7-CHM.

V. Simulation and Experimental Validation

In this section, the proposed hybrid PWM technique will be validated through simulations and experiments based on test-rig. The Quartus II and MATLAB/Simulink are chosen to simulate the performance of the proposed hybrid PWM. A real electric rail traction system of parameters presented in Table I is selected in the simulation and the experiment.

A. Simulation Analysis

Quartus II software is easily used to validate the basic function of pulse generation in FPGA. Here, only the proposed hybrid PWM technique in MATLAB/Simulink is given as an example shown in Fig. 12. It can be seen that there is no obvious current

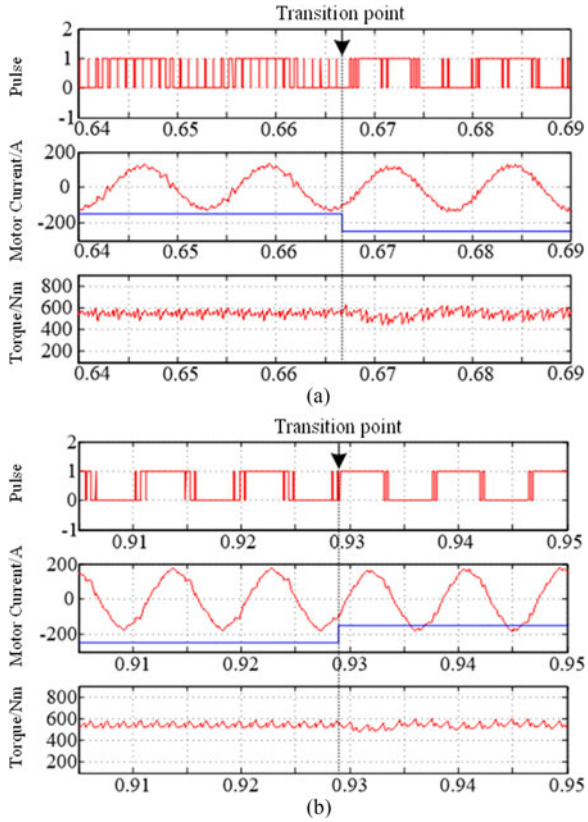

Fig. 12. Hybrid PWM transition examples: (a) 15-CSPWM to 9-CHM and (b) 5-CHM to 3-CHM.

and torque oscillation, that is to say: the PWMs clearly succeed each other when it is used for the traction motor control.

B. Experimental Analysis

Experimental results were taken from two different test rigs: static test rig and rolling test rig. The former was fixed in the test lab to validate the basic performance of the electric traction system, and the latter was used to validate the dynamic performance in the whole frequency region with full electric rail vehicle logic, where the traction system has been fixed in the vehicle, and the rolling wheels driven by converter–motor system are used as loads. The static test rig is shown in Fig. 13.

The transition and harmonic test results in the static test rig are shown in Fig. 14, where transition from 15-CSPWM to 9-CHM is given as an example, no current or dc voltage oscillation occurred. The harmonic spectra indicate that low subharmonics are not fully eliminated by CHMPWM as that in SHEPWM. It is also seen from the current THD comparison between CHMPWM and SHEPWM in the OSPWM region shown in Fig. 15.

It can be seen from Fig. 15 that the CHM optimization effect is significant when the number of notch angle is relatively high, i.e., the THD of 9-CHM and 7-CHM is about 10% lower than that of SHE with the same modulation ratio. But when the number of notch angle is small, the optimization effect is limited: 5-CHM has only about 3% lower rate, and 3-CHM has exactly the same rate with that of SHE. Because in the three-pulse

Fig. 13. Static test rigs.

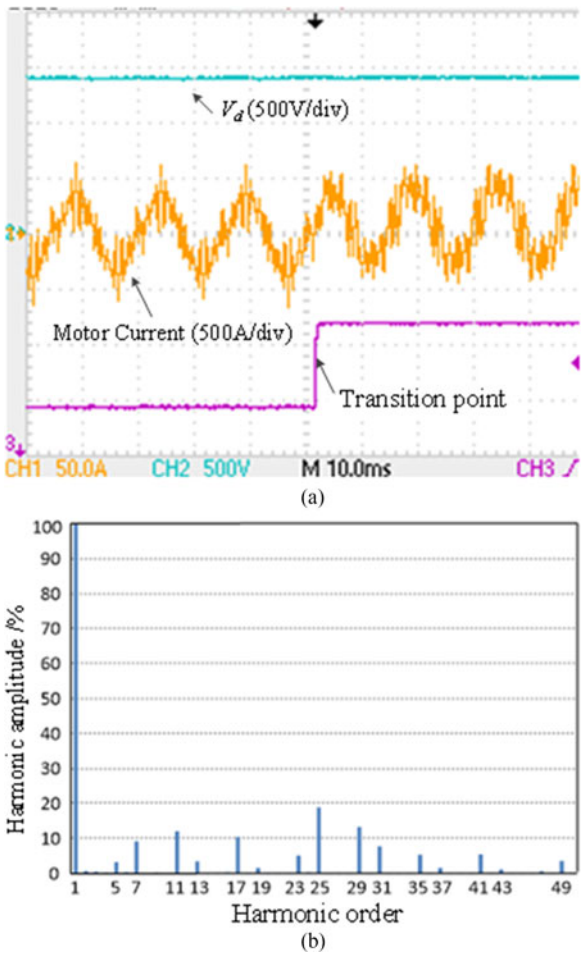

Fig. 14. (a) Current transition from 15-CSPWM to 9-CHM and (b) harmonic spectrum of 9-CHM.

mode, both have only one notch angle, which can only meet the constraint of modulation index, but cannot achieve harmonic optimization.

In the rolling test rig, three-phase current waveform of real vehicle traction system under acceleration and deceleration is shown in Fig. 16, where the zoom-in details of positive transitions are also given in the subfigures. It can be seen that all transitions can ensure a smooth transition of motor currents without

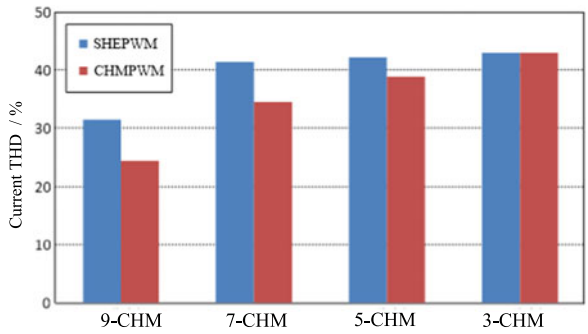

Fig. 15. Comparison of current THD between SHEPWM and CHMPWM.

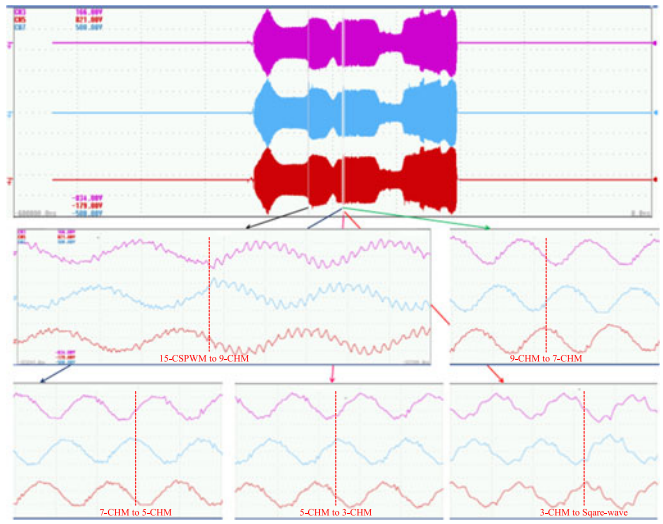

Fig. 16. Dynamic current waveform of rolling test rig (Time axis: total wave—60 s/div, subwaves—5 ms/div).

any significant impact, which ensure the smooth transition of the torque and operational stability.

VI. Conclusion

This paper proposes a much easier DSP–FPGA-based implementation method of the hybrid PWM scheme for electric traction motor control. The overview of the compact, low-cost, and low-power control platform is described. By fully utilizing the advantages and resources of each processor, high-precision hybrid PWMs are implemented whereas satisfying the multirate and multitask processing of the traction control. The implementation methods of the presented hybrid PWM technique, where asynchronous and synchronous THIPWM4, CHMPWMs are used for transiting from low-speed to square-wave, are discussed in detail, including algorithms between the two processors, smooth transition, etc. From the simulation results of Quartus II and MATLAB/Simulink, and experimental results of static and rolling test rigs, it can be seen that through the proposed technique, PWM generation with high accuracy, low usage of resources, and computational burden in FPGA is well implemented, and the merits of low losses, low total harmonics based on very low switching frequency are achieved, which help

to improve the performance of the motor control and increase the system reliability.

REFERENCES

[1] D. Doncker, D. Rik, W. J. Pulle, and A. Veltman, *Advanced Electrical Drives: Analysis, Modeling, Control*. New York, NY, USA: Springer, 2010.

[2] J. Holtz, M. Höltgen, and J. O. Krah, "A space vector modulator for the high-switching frequency control of three-level SiC inverters," *IEEE Trans. Power Electron.*, vol. 29, no. 5, pp. 2618–2626, May 2014.

[3] Z. Zhang, F. Wang, L. M. Tolbert, B. J. Blalock, and D. J. Costinett, "Evaluation of switching performance of SiC devices in PWM inverter-fed induction motor drives," *IEEE Trans. Power Electron.*, vol. 30, no. 10, pp. 5701–5711, Oct. 2015.

[4] A. Schonung and H. Stemmler, "Static frequency changers with subharmonic control in conjunction with reversible variable speed ac drives," *Brown Boveri, Rev.*, vol. 55, pp. 555–557, 1964.

[5] H. W. van der Broeck, H.-C. Skudelny, and G. V. Stanke, "Analysis and realization of a pulse width modulator based on voltage space vectors," *IEEE Trans. Ind. Appl.*, vol. 24, no. 1, pp. 142–150, Jan./Feb. 1988.

[6] J. Holtz, "Pulse width modulation for electronic power conversion," *Proc. IEEE*, vol. 82, no. 8, pp. 1194–1214, Aug. 1994.

[7] D. G. Holmes and T. A. Lipo, *Pulse Width Modulation for Power Converters: Principles and Practice*. Hoboken, NJ, USA: Wiley, 2003.

[8] D. Zhao, V. S. S. P. K. Hari, G. Narayanan, and R. Ayyanar, "Space-vector-based hybrid pulse width modulation techniques for reduced harmonic distortion and switching loss," *IEEE Trans. Power Electron.*, vol. 25, no. 3, pp. 760–774, Mar. 2010.

[9] K. Basu, J. S. S. Prasad, G. Narayanan, H. K. Krishnamurthy, and R. Ayyanar, "Reduction of torque ripple in induction motor drives using an advanced hybrid PWM technique," *IEEE Trans. Ind. Electron.*, vol. 57, no. 6, pp. 2085–2091, Jun. 2010.

[10] S. Das, G. Narayanan, and M. Pandey, "Space-vector-based hybrid pulse width modulation techniques for a three-level inverter," *IEEE Trans. Power Electron.*, vol. 29, no. 9, pp. 4580–4591, Sep. 2014.

[11] K. K. Wei, T. Q. Zheng, R. Wang, and C. C. Wang, "Study on a hybrid PWM method under low switching frequency," in *Proc. Int. Conf. Electr. Mach. Syst.*, Beijing, China, 2011, pp. 1–4.

[12] T. Ando *et al.*, "Apparatus and method for controlling induction motor," *U.S. Patent 6 166 514*, Dec. 26, 2000.

[13] B. K. Bose, *Modern Power Electronics and AC Drives*. Upper Saddle River, NJ, USA: Prentice-Hall, 2002.

[14] T. H. Nguyen and D. C. Lee, "Improvement of current control in over-modulation range for vector controlled induction machine drives," in *Proc. IEEE 8th Int. Conf. Power Electron. ECCE Asia*, 2011, pp. 421–426.

[15] A. Tripathi and A. M. Khambadkone, "Dynamic control of torque in overmodulation and in the field weakening region," *IEEE Trans. Power Electron.*, vol. 21, no. 4, pp. 1091–1098, Jul. 2006.

[16] K. Dong and L. J. Diao, "Research on over-modulation algorithm based on basic bus clamping strategy," *J. China Railw. Soc.*, vol. 36, no. 4, pp. 35–40, 2014.

[17] C. C. Wang, M. L. Zhou, and X. J. You, "Research on the PWM method of high power ac electrical locomotive," *Trans. China Electrotech. Soc.*, vol. 27, no. 2, pp. 173–178, 2012.

[18] P. C. Loh, G. H. H. Pang, and D. G. Holmes, "Multi-level discontinuous pulse width modulation: Common mode voltage minimisation analysis," *IEE Proc. Electr. Power Appl.*, vol. 151, no. 4, pp. 477–486, Jul. 2004.

[19] H. S. Patel and R. G. Hoft, "Generalized techniques of harmonic elimination and voltage control in thyristor inverters : Part 1—Harmonic elimination," *IEEE Trans. Ind. Appl.*, vol. IA-9, no. 3, pp. 310–317, May 1973.

[20] H. S. Patel and R. G. Hoft, "Generalized techniques of harmonic elimination and voltage control in thyristor inverters : Part 2-Voltage control techniques," *IEEE Trans. Ind. Appl.*, vol. IA-10, no. 5, pp. 666–673, Sep. 1974.

[21] Z. Zhao, Y. Zhong, H. Gao, L. Yuan, and T. Lu, "Hybrid selective harmonic elimination PWM for common-mode voltage reduction in three-level neutral-point-clamped inverters for variable speed induction drives," *IEEE Trans. Power Electron.*, vol. 27, no. 3, pp. 1152–1158, Mar. 2012.

[22] Y. Zhang, Y. W. Li, N. R. Zargari, and Z. Cheng, "Improved selective harmonics elimination scheme with online harmonic compensation for high-power PWM converters," *IEEE Trans. Power Electron.*, vol. 30, no. 7, pp. 3508–3517, Jul. 2015.

[23] G. S. Buja and G. B. Indri, "Optimal pulse width modulation for feeding ac motors," *IEEE Trans. Ind. Appl.*, vol. IA-13, no. 1, pp. 38–44, Jan. 1977.

[24] K. Akshay and J. Holtz, "Synchronous optimal pulse width modulation for low-switching frequency control of medium voltage multilevel inverters," *IEEE Trans. Ind. Electron.*, vol. 57, no. 7, pp. 2374–2381, Jul. 2010.

[25] B. K. Bose and H. A. Sutherland, "A high-performance pulse width modulator for an inverter-fed drive system using a microcomputer," *IEEE Trans. Ind. Appl.*, vol. 19, no. 2, pp. 235–243, Mar. 1983.

[26] D. Horstmann and G Stanke, "Die Stromrichternahe Antriebsregelung des Steuergerates fur Bahnauto-matisierungssysteme SIBAS32," *Sonderdruck Elektr. Bahnen*, vol. 1, no. 1, pp. 1–8, 1992.

[27] L. J. Diao *et al.*, "Dual DSPs-FPGA structured traction control system for urban rail transit vehicle," *Trans. China Electrotech. Soc.*, vol. 29, no. 1, pp. 174–180, Jan. 2014.

[28] E. J. Bueno, A. Hernandez, F. J. Rodriguez, C. Giron, R. Mateos, and S. Cobreces, "A DSP- and FPGA-based industrial control with high-speed communication interfaces for grid converters applied to distributed power generation systems," *IEEE Trans. Ind. Electron.*, vol. 56, no. 3, pp. 654–669, Mar. 2009.

[29] C. Charumit and V. Kinnares, "Discontinuous SVPWM techniques of three-leg VSI-fed balanced two-phase loads for reduced switching losses and current ripple," *IEEE Trans. Power Electron.*, vol. 30, no. 4, pp. 2191–2204, Apr. 2015.

[30] A. Kirubakaran, S. Jain, and R. K. Nema, "DSP-controlled power electronic interface for fuel-cell-based distributed generation," *IEEE Trans. Power Electron.*, vol. 26, no. 12, pp. 3853–3864, Dec. 2011.

[31] J. D. B. Ramírez, J. J. R. Rivas, and E. Peralta-Sanchez, "DSP-based simplified space-vector PWM for a three-level VSI with experimental validation," *J. Power Electron.*, vol. 12, no. 2, pp. 285–293, 2012.

[32] M. Lakka, E. Koutroulis, and A. Dollas, "Development of an FPGA-based SPWM generator for high switching frequency dc/ac inverters," *IEEE Trans. Power Electron.*, vol. 29, no. 1, pp. 356–365, Jan. 2014.

[33] Ó. López *et al.*, "Comparison of the FPGA implementation of two multilevel space vector PWM algorithms," *IEEE Trans. Ind. Electron.*, vol. 55, no. 4, pp. 1537–1547, Apr. 2008.

[34] D. Navarro, Ó Lucía, L. A. Barragán, J. I. Artigas, I. Urriza, and Ó. Jiménez, "Synchronous FPGA-based high-resolution implementations of digital pulse-width modulators," *IEEE Trans. Power Electron.*, vol. 27, no. 5, pp. 2515–2525, May 2012.

[35] R. V. Nair, S. A. Rahul, R. S. Kaarthik, A. Kshirsagar, and K. Gopakumar, "Generation of higher number of voltage levels by stacking inverters of lower multilevel structures with low voltage devices for drives," *IEEE Trans. Power Electron.*, vol. 32, no. 1, pp. 52–59, Jan. 2017.

[36] R. Dubey, P. Agarwal, and M. K. Vasantha, "Programmable logic devices for motion control—A review," *IEEE Trans. Ind. Electron.*, vol. 54, no. 1, pp. 559–566, Feb. 2007.

[37] M. Hamouda, H. F. Blanchette, K. Al-Haddad, and F. Fnaiech, "An efficient DSP-FPGA-based real-time implementation method of SVM algorithms for an indirect matrix converter," *IEEE Trans. Ind. Electron.*, vol. 58, no. 11, pp. 5024–5031, Nov. 2011.

[38] R. Morales-Caporal and M. Pacas, "Digital implementation of a direct mean torque control for ac servo drives based on a hybrid DSP/FPGA controller system," in *Proc. 11th IEEE Int. Power Electron. Congr.*, 2008, pp. 77–83.

[39] Texas Instruments, "Flexible PWMs enable multi-axis drives, multi-level inverters," Technical Brief SPRT723, May 2016.

[40] Texas Instruments, "DSP/BIOS real-time operating system (RTOS)," 2016. [Online]. Available: http://www.ti.com/tool/dspbios

[41] L. J. Diao, D. N. Sun, K. Dong, L. T. Zhao, and Z. G. Liu, "Optimized design of discrete traction induction motor model at low-switching frequency," *IEEE Trans. Power Electron.*, vol. 28, no. 10, pp. 4803–4810, Oct. 2013.

[42] B. B. Carvalho *et al.*, "Multi-rate DSP/FPGA-based real-time acquisition and control on the ISTTOK tokamak," *IEEE Trans. Nucl. Sci.*, vol. 55, no. 1, pp. 54–58, Feb. 2008.

[43] M. Langhammer and B. Pasca, "Design and implementation of an embedded FPGA floating point DSP block," in *Proc. IEEE 22nd Symp. Comput. Arithmetic*, Lyon, France, 2015, pp. 26–33.

[44] All Programmable SoC With Hardware and Software Programmability. [Online]. Available: https://www.xilinx.com/products/silicon-devices/soc/zynq-7000.html

[45] SmartFusion2 SoC FPGA Family. [Online]. Available: https://www.microsemi.com/products/fpga-soc/soc-fpga/smartfusion2

[46] Intel SoCs. [Online]. Available: https://www.altera.com/products/soc/overview.html
[47] X. Liu, Y. Xie, H. Chen, and B. Li, "Implementation on FPGA for CORDIC-based computation of arcsine and arccosine," in *Proc. IET Int. Radar Conf.*, Hangzhou, China, 2015, pp. 1–4.
[48] Altera Inc., Floating-Point IP Cores User Guide,UG-01058, Dec. 2016.
[49] G. J. Chen, M. K. Wan, and D. M. Wang, "Serial implementation of multiplication, division and square root operation based on FPGA," *Micro Comput. Inf.*, vol. 24, no. 22, pp. 167–168, 192, 2008.
[50] Altera Inc., "Application Note 263: CORDIC reference design v1.4," Jun. 2005. [Online]. Available: http://www.altera.com/literature/an/an263.pdf
[51] T. Ashrita and R. K. Chidambara, "Sine wave generation using CORDIC algorithm," *Int. J. Electron. Commun. Technol.*, vol. 3, no. 4, pp. 224–227, Oct./Dec. 2012.
[52] B. M. Saied, S. A. Dawwd, and A. S. Al-Soufi, "FPGA based selective harmonic elimination pulse width modulation technique," in *Proc. 2009 4th Int. Des. Test Workshop*, Riyadh, Saudi Arabia, 2009, pp. 1–6.
[53] D. N. Sun, "Research on key control technologies of electric traction drive system for metro cars," Ph.D. dissertation, Beijing Jiaotong Univ., Beijing, China, 2012 (in Chinese).

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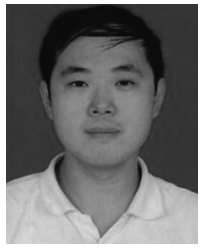

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