A Triple-Mode Wireless Power-Receiving Unit With 85.5% System Efficiency for A4WP, WPC, and PMA Applications

Young-Jun Park, ByeongGi Jang, Seong-Mun Park, Ho-Cheol Ryu, Seong Jin Oh, Sang-Yun Kim, *Student Member, IEEE*, YoungGun Pu, Sang-Sun Yoo, Keum Cheol Hwang, *Senior Member, IEEE*, Youngoo Yang, *Member, IEEE*, Minjae Lee, *Member, IEEE*, and Kang-Yoon Lee, *Senior Member, IEEE*

***Abstract*—This paper presents the design of a triple-mode wireless power-receiving unit (TWPRU) for battery charger with high efficiency. The TWPRU is proposed based on Alliance for Wireless Power (A4WP), Wireless Power Consortium (WPC), and Power Matters Alliance (PMA) standards. An adaptive alignment gate controller technique is proposed in the triple-mode active rectifier to block the reverse leakage current and improve the power conversion efficiency (PCE). This technique can compensate for the delays in the gate control signals of the main switching MOSFETs at different operating frequencies for A4WP, WPC, and PMA. The dead time of a dc–dc converter is optimally determined depending on the voltage and the temperature variations by phase calibration circuit. This chip with an active area of 5.0 mm × 3.5 mm is implemented in 0.18-μm BCD technology. The maximum PCEs of the triple-mode active rectifier are 91.7% in the A4WP mode and 92.7% in the WPC/PMA mode, respectively. The maximum PCE of the dc–dc converter is 92.3% at a load current of 500 mA, while the system efficiencies of TWPRU at A4WP and WPC/PMA modes are about 84.5% and 85.5%, respectively.**

***Index Terms*—Active rectifier, Alliance for Wireless Power (A4WP), delay compensation, magnetic induction, magnetic resonance, Power Matters Alliance (PMA), wireless power-receiving unit, Wireless Power Consortium (WPC).**

Manuscript received December 18, 2016; revised March 31, 2017; accepted May 4, 2017. Date of publication May 10, 2017; date of current version January 3, 2018. This work was supported by Institute for Information and Communications Technology Promotion (IITP) grant funded by the Korea Government (MSIP) (B0717-16-0057, Development of MST integrated 15 W magnetic induction/resonance wireless charging technology). This work was supported by the National Research Foundation of Korea (NRF) grant funded by the Korean government (MSIP) (2014R1A5A1011478). Recommended for publication by Associate Editor O. Lucia. *(Corresponding author: Kang-Yoon Lee.)*

Y.-J. Park, B. Jang, S.-M. Park, H.-C. Ryu, S.-J. Oh, S.-Y. Kim, Y. Pu, K. C. Hwang, Y. Yang, and K.-Y. Lee are with the College of Information and Communication Engineering, Sungkyunkwan University, Suwon 440-746, South Korea (e-mail: pyj88@skku.edu; seeys17@skku.edu; psm7289@skku.edu; smart5653@skku.edu; geniejazz@skku.edu; ksy0501@skku.edu; hara1015@konkuk.ac.kr; khwang@skku.edu; yang09@skku.edu; klee@skku.edu).

S.-S. Yoo is with the College of Information and Communication Engineering, Sungkyunkwan University, Suwon 440-746, South Korea, and also with the Department of Smart Automobile, Pyeongtaek University, Pyeongtaek-si 450-701, South Korea (e-mail: rapter@kaist.ac.kr).

M. Lee is with the School of Information and Communications, Gwangju Institute of Science and Technology, Gwangju 61005, South Korea (e-mail: minjae@gist.ac.kr).

Digital Object Identifier 10.1109/TPEL.2017.2703153

I. Introduction

WIRELESS power transfer (WPT) has emerged as one of the best solutions among the recent improvements. Researchers have developed the most useful method of wireless charging of electric vehicles. Also, the wireless battery charging technique can be applied to mobile and wearable devices to improve user convenience and flexibility. The two WPT methods are inductive coupling and magnetic resonance [1]. Wireless Power Consortium (WPC) and Power Matters Alliance (PMA) standards are based on the inductive coupling method and are commercially available to supply wireless chargers for the consumer. In WPC/PMA standards, the frequency of the WPT system is adjustable from 87 to 357 kHz for power control and enhanced efficiency [2]–[5]. On the other hand, the Alliance for Wireless Power (A4WP) standard is based on the magnetic resonance method, which can transfer the power over a few centimeters more than the inductive coupling method. The operation frequency of A4WP is 6.78 MHz, which is much higher than those of WPC/PMA [6]. The A4WP standard can be the target for battery charging of laptop, tablet, automotive, and USB devices applications. In addition, WPC and PMA standards can be used for battery charging of smart phone, small device, tablet, laptop, furniture, and video gaming accessories. Therefore, a wireless charger that can operate in all standards makes use of wireless charging in various applications more conveniently.

Fig. 1(a) and (b) shows the conceptual diagram of the prior WPT system and the proposed triple-mode WPT system, respectively. Fig. 1(a) shows the prior WPT system supporting WPC, PMA, and A4WP standards. Using separate systems for each standard increases the area and costs because of the increased use of redundant circuits and external components. Therefore, triple-mode WPT systems are proposed in this paper. Fig. 1(b) shows the conceptual diagram of the triple-mode WPT system. In order to implement the triple-mode WPT system, the external matching networks for the three modes can be designed [9]. For the active rectifier and dc–dc converter, the building blocks for each mode should be shared to reduce the area. However, the rectifier has the following difficulties in sharing the circuit. First, since the frequencies of the transmitted signals are different for each standard, accurate synchronous rectifier

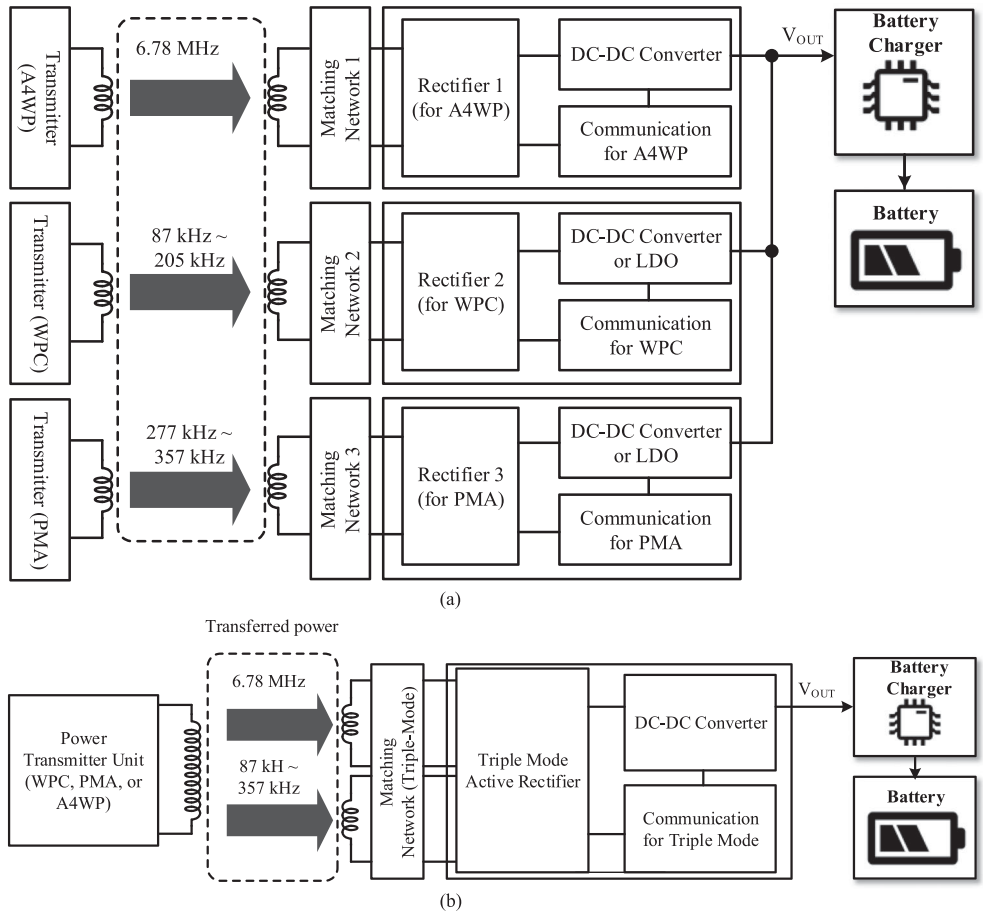

Fig. 1. Conceptual diagram of the (a) prior WPT system and (b) proposed triple-mode WPT system.

operation is difficult to implement. Second, the communication and control methods for each standard differ according to the inductive coupling and the magnetic resonant methods. In addition, the output power level of the WPT receiver should be increased in order to efficiently reduce the charging time. Therefore, the triple-mode active rectifier proposed in this paper supports the three standards by using a single shared active rectifier for smaller area and high efficiency. Also, it automatically changes the configuration and modes for high efficiency by detecting the three standards' operating frequencies. In the dc–dc converter of the WPT receiver, the output power level has been increased to reduce the charging time recently. As the output power level is increased, the heat from the circuit will be more serious if the power efficiency is kept the same. Therefore, to reduce the heat caused by the power loss, a high-efficiency dc–dc converter has been designed and its malfunction is prevented by optimizing the dead time, which depend on the temperature and load current. A high switching frequency has also been adopted to minimize the inductor size for mobile phones [10].

Table I presents the list of acronyms used in this paper.

TABLE I
LIST OF ACRONYMS

Acronyms	Definition	Acronyms	Definition
A4WP	Alliance for Wireless Power	NMOS	n-type metal–oxide–semiconductor
AAGC	Adaptive alignment gate controller	PMA	Power Matters Alliance
BCD	Bipolar–CMOS–DMOS	PTU	Power transfer unit
CCM	Continues current mode	PC	Phase calibration
DCM	Discontinues current mode	SAR	Successive approximation register
EMI	Electromagnetic interference	SOVP	Soft overvoltage protection
EPT	End power transfer	TWPRU	Triple-mode wireless power-receiving unit
ESR	Equivalent series resistance	VCDL	Voltage controlled delay line
HOVP	Hard overvoltage protection	WPC	Wireless Power Consortium
ICPT	Inductively coupled power transfer	WPT	Wireless power transfer
PMOS	p-type metal–oxide–semiconductor	ZCS	Zero current sensing

II. Proposed Triple-Mode Wireless Power-Receiving System Architecture

Fig. 2 shows a block diagram of the triple-mode wireless power-receiving unit (TWPRU) of this paper, which can be used to wirelessly charge mobile devices. The A4WP power transmitting unit (PTU) and WPC/PMA PTU deliver ac power to the receiver's coils of A4WP and WPC/PMA, respectively. A TWPRU can receive power from all types of PTU (WPC, PMA, and A4WP), since it can select the type of PTU, and receive power through the communication. The TWPRU is composed of triple-mode active rectifier, dc–dc converter, frequency detector, SAR analog to digital converter (ADC), power-up circuit,

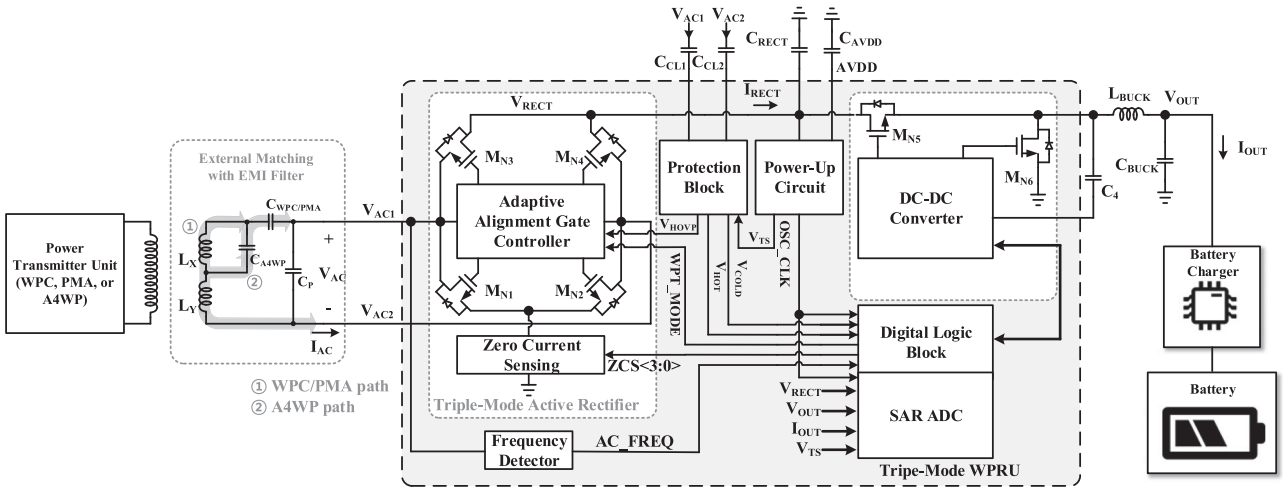

Fig. 2. Block diagram of the TWPRU.

protection block, and digital logic block. The triple-mode active rectifier generates the dc power supply (V_{RECT}) from the received V_{AC} with high efficiency. The dc–dc converter generates an output voltage (V_{OUT}) of 5 or 9 V, depending on the modes of the battery charger (normal or fast charging). The power-up circuit generates voltages analog VDD (AVDD) and V_{TS}. AVDD supplies voltage to the internal circuits and the voltage of V_{TS} is used to check the thermal shutdown condition. The protection block has overvoltage protection and thermal shutdown functions. The SAR ADC senses the information such as V_{RECT}, V_{OUT}, I_{OUT}, V_{TS}, and converts them into 10-b data to transfer to the digital logic block.

External matching with the electromagnetic interference (EMI) filter is designed with an architecture for matching the WPC and PMA frequency band and the A4WP frequency band [9]. The magnetic resonators (L_X and L_Y) ensure the maximum power delivery between the PTU and TWPRU. When the output power is 5 W in the WPT system, with a diode type of the rectifier, the efficiency of the diode type rectifier is lower than that of the active rectifier. Therefore, some additional devices are essential in order to minimize the heat, which is not suitable for mobile application. So, high-efficiency system is needed to minimize the heat caused by the power loss. Also, since the output power should be higher to support quick charging, the issues about heat and efficiency are more important. The adaptive alignment gate controller (AAGC) circuit in the active rectifier is proposed and designed as the switching type to increase its efficiency and mitigate the heat problem.

In Fig. 2, high *dv/dt* of V_{AC1} and V_{AC2} nodes can occur by the high frequency switching of M_{N1} to M_{N4}, which can raise the conductive EMI from 150 kHz to 30 MHz, and radiative EMI from 30 MHz to 1 GHz. As a way to reduce EMI, adding an EMI filter in the matching circuit can reduce the conductive EMI [11]. There are several ways to reduce the radiated EMI. First, the radiation from the antenna is generated by the loop of the current path. Therefore, the radiated EMI can be reduced by using a smaller radiated antenna to minimize the path of high *di/dt*. The printed circuit board (PCB) for measuring the integrated circuit (IC) is designed to have the minimum loop between V_{AC1}, ground, and V_{AC2} in Fig. 2. Second, the radiated EMI is reduced by using the capacitors, C_{A4WP}, $C_{\mathrm{WPC/PMA}}$, and C_P with small equivalent series resistances (ESRs) to maximize the decoupling effect. Third, the radiated EMI is reduced with a Faraday cage to shield the noise. Material such as copper foil tape can be used for the Faraday cage [12], [13].

Fig. 3 shows a flowchart of the TWPRU IC. When the PTU starts to transfer power, the triple-mode active rectifier starts to operate in passive mode. Thereafter, the internal voltage is generated and supplied to operate the internal building blocks of the TWPRU by a power-up circuit. The operating mode of the TWPRU is automatically selected among three standards (A4WP, WPC, and PMA). The frequency ranges of the V_{AC1} are from 87 to 205 kHz for the WPC standard and from 277 to 357 kHz for the PMA standard. The frequency of V_{AC1} is 6.78 MHz for the A4WP standard. As can be seen in Fig. 3, the F_{AC1} is counted value that the frequency of V_{AC1} is counted for the predetermined time by the frequency detector. When the count of F_{AC1} is larger than the reference values of N_{A4WP}, the A4WP mode is selected. On the other hand, if F_{AC1} is larger than N_{WPC}, then the PMA mode is selected. Otherwise, the WPC mode is selected. When the input power level is sufficiently high, the rectifier operates in synchronous mode. When the output voltage of the rectifier is high enough, the dc–dc converter is enabled, and delivers the power to the battery charger. During the operation of TWPRU IC, the SAR ADC converts the V_{RECT}, V_{OUT}, and I_{OUT} into digital codes and transfers them to the digital logic block. It estimates the received power and produces the signals to be transferred to the PTU. When the protection conditions are detected, the TWPRU sends the end power transfer (EPT) information to the PTU.

III. Building Blocks

A. Proposed Triple-Mode Active Rectifier

One of the most important performance parameters of the triple-mode active rectifier is the power conversion efficiency (PCE). In this paper, the triple-mode active rectifier is proposed to actively turn ON and turn OFF the MOS transistors, depending

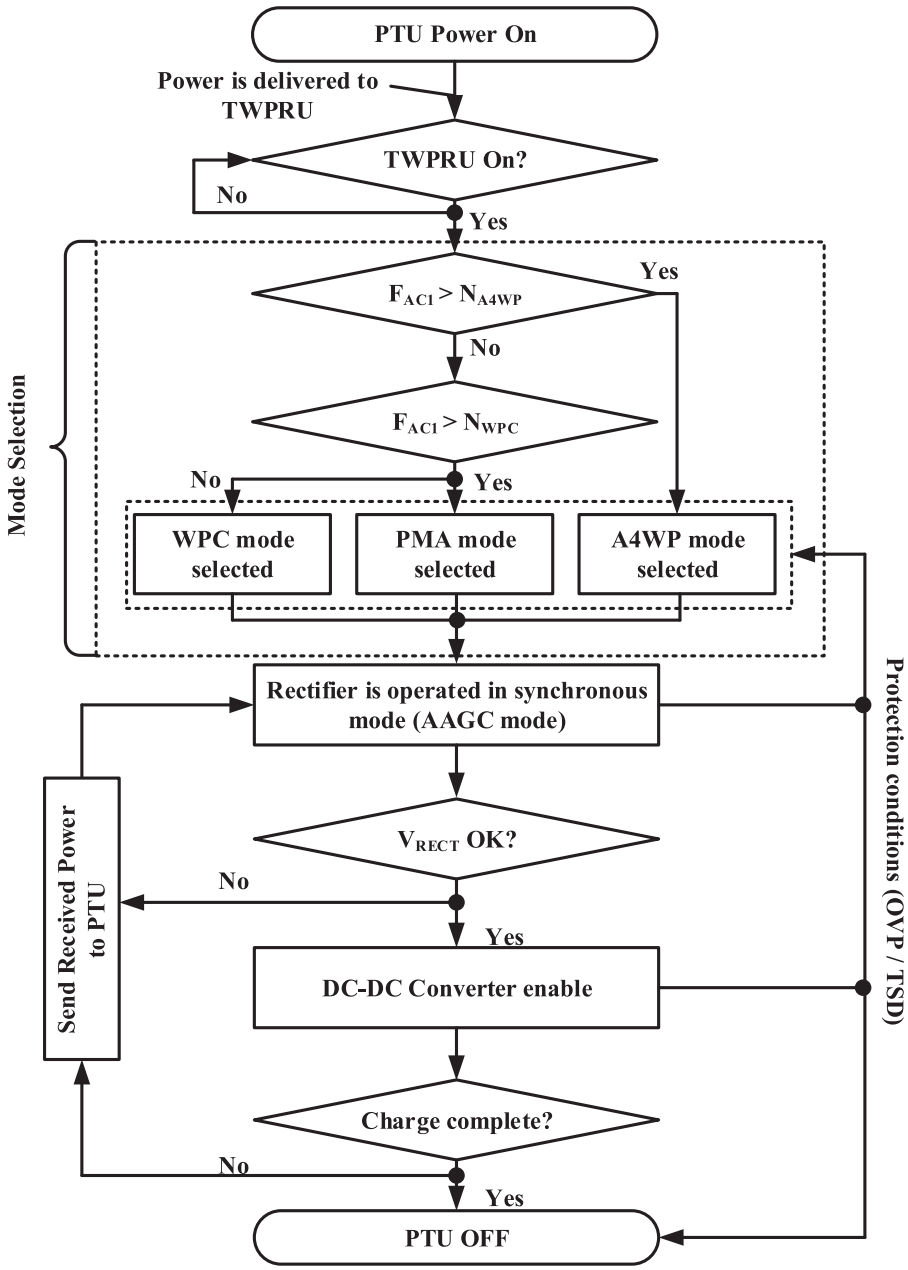

Fig. 3. Flowchart of the operation of the TWPRU.

on the polarity of V_{AC}. The voltage drops across the MOS transistors can be controlled to be much smaller than that of a diode-based passive rectifier, to achieve higher PCE.

Fig. 4(a)–(c) shows the active rectifier structure used in prior works. Fig. 4(a) shows a p-channel metal–oxide–semiconductor (PMOS) diode connection structure with the bootstrap technique. This structure has the critical drawback of large conduction loss generated by the threshold voltage of 0.7 V from the diode connection structure [17]. Fig. 4(b) shows the comparator-based gate control structure. The comparator is used to control a gate signal of active rectifier [8]. Since the delay caused by the comparator cannot be compensated for in this structure, a reverse leakage current occurs and efficiency is decreased.

Fig. 4(c) shows the structure of active rectifier with a zero delay circuit to compensate for the delay of the comparator. The high-side MOSFET of this structure, however, consists of a PMOS cross-coupled structure, so that the size would be extremely large if the same on-resistance was used as in an n-channel metal–oxide–semiconductor (NMOS) [14]. As can be seen from the structures, PMOS is used as high-side MOSFET. However, MOSFET involves a break issue since the maximum V_{SG} voltage of PMOS is designated as 5 V in the recent BCD process, which means that high voltage cannot be generated by the rectifier.

Since the frequency of the input power for the A4WP standard is 6.78 MHz, the propagation delays of the gate control circuits cause a reverse leakage current and reduce the PCE [14]–[16]. The frequencies of both the WPC and PMA are changeable

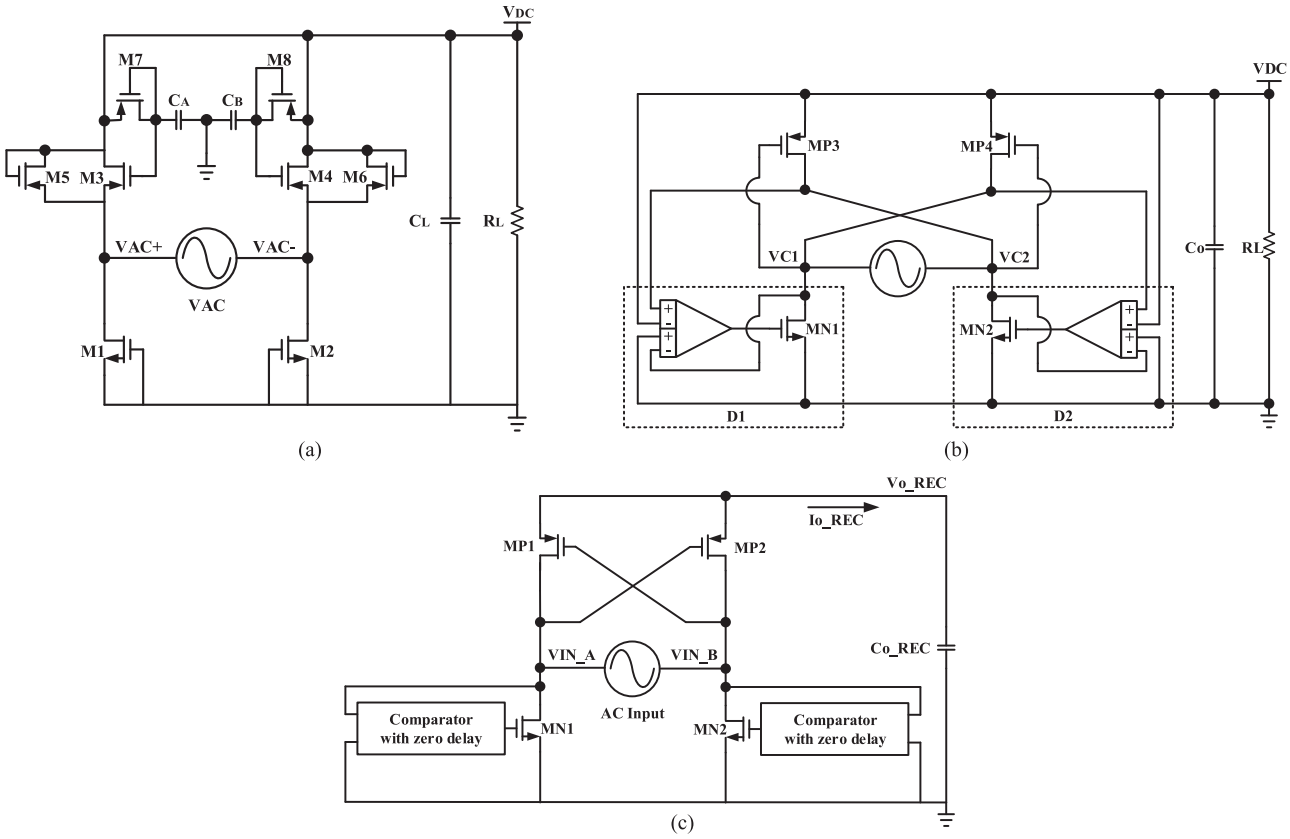

Fig. 4. Active rectifier circuits in prior works (a) PMOS diode connection circuits, (b) comparator-based gate control circuit, and (c) active rectifier with zero delay circuit.

within from 87 to 357 kHz. The triple-mode active rectifier is designed to be reconfigurable depending on the input frequency. In the WPC and PMA standards, the transferred power is controlled by the frequency of transferred power. The differences between frequencies of transferred power in WPC and PMA are not so large that, in this paper, the active rectifier can be operated synchronously with the current by sensing the frequency of transferred power.

Fig. 5 shows a block diagram of the simplified triple-mode active rectifier. This consists of a voltage limiter, an A4WP alignment gate controller, the WPC and PMA alignment gate controller, level shifter, HS_Driver, and LS_Driver.

Unlike low-side power MOSFETs (M_{N2_2}, M_{N2_1}), the high-side power MOSFETs (M_{N3_1}, M_{N3_2}) require the level shifter for driving, which leads to an inevitable delay. As shown in Fig. 5, M_{N2} and M_{N3} consist of $M_{N2\_1} - M_{N2\_2}$ and $M_{N3\_1} - M_{N3\_2}$, respectively. In order to prevent the reverse leakage current, the current through the active rectifier is sensed by the zero current sensing (ZCS) circuit shown in in Fig. 5. Source voltages (V_{IZCD}) of the sensing MOSFETs are sensed by the ZCS circuit to generate the gate signals (V_{G2_SR} and V_{G3_SR}).

Fig. 6(a) and (b) shows the simplified circuit of active rectifier for loss analysis. The loss of active rectifier is composed of the conduction loss and switching loss. The conduction loss and switching loss of M_{N2} can be represented as follows:

$$P_{\mathrm{LOSS\_RECT}} = P_{\mathrm{COND}} + P_{\mathrm{SW}} \tag{1}$$

where $P_{\mathrm{LOSS_{RECT}}}$, P_{COND}, and P_{SW} are the power loss of active rectifier, conduction loss of active rectifier, and switching loss of active rectifier, respectively.

The conduction loss (P_{COND}) can be decomposed to two terms when M_{N2} is turned ON and turned OFF as

$$P_{\mathrm{COND}} = \left(\frac{T_{\mathrm{on}}}{T_{\mathrm{SW}}} \times {I^2}_{\mathrm{AC.on}} \times R_{\mathrm{on}}\right) + \left(\frac{T_{\mathrm{off}}}{T_{\mathrm{SW}}} \times {I^2}_{\mathrm{AC.off}} \times R_{\mathrm{off}}\right) \tag{2}$$

where T_{sw}, T_{on}, T_{off}, $I_{\mathrm{AC.on}}$, $I_{\mathrm{AC.off}}$, R_{on}, and R_{off} are the switching period of M_{N2}, turned-ON time of M_{N2}, turned-off time of M_{N2}, averaging value of input current at turned-ON M_{N2}, averaging value of input current at turned-off $M_{N2,}$ turned-ON resistance of M_{N2}, and turned-off resistance of M_{N2}, respectively. R_{on} is inversely proportional to total width (W_{MN2}) of M_{N2}.

Also, the switching loss (P_{SW}) can be decomposed to the switching loss of M_{N2} and gate driver as follows:

$$P_{\mathrm{SW}} = \left(\frac{V_{\mathrm{DS}} \times I_{\mathrm{AC}}}{2}(T_{\mathrm{rise}} + T_{\mathrm{fall}}) + ((Q_{g1} + Q_{g2}) \times V_{\mathrm{driver}})\right) \times f_{\mathrm{sw}} \tag{3}$$

where V_{DS}, I_{AC}, T_{rise}, T_{fall}, Q_{g1}, Q_{g2}, V_{driver}, and f_{sw} are the drain to source voltage of M_{N2}, input current of active

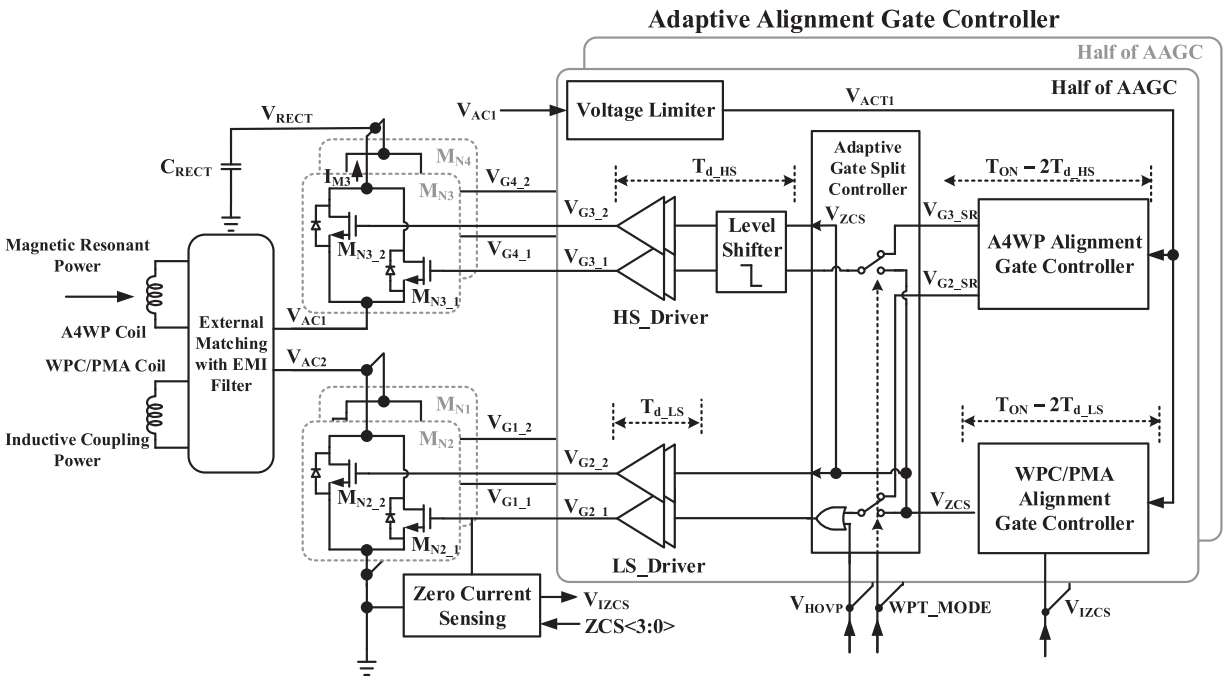

Fig. 5. Block diagram of the simplified triple-mode active rectifier.

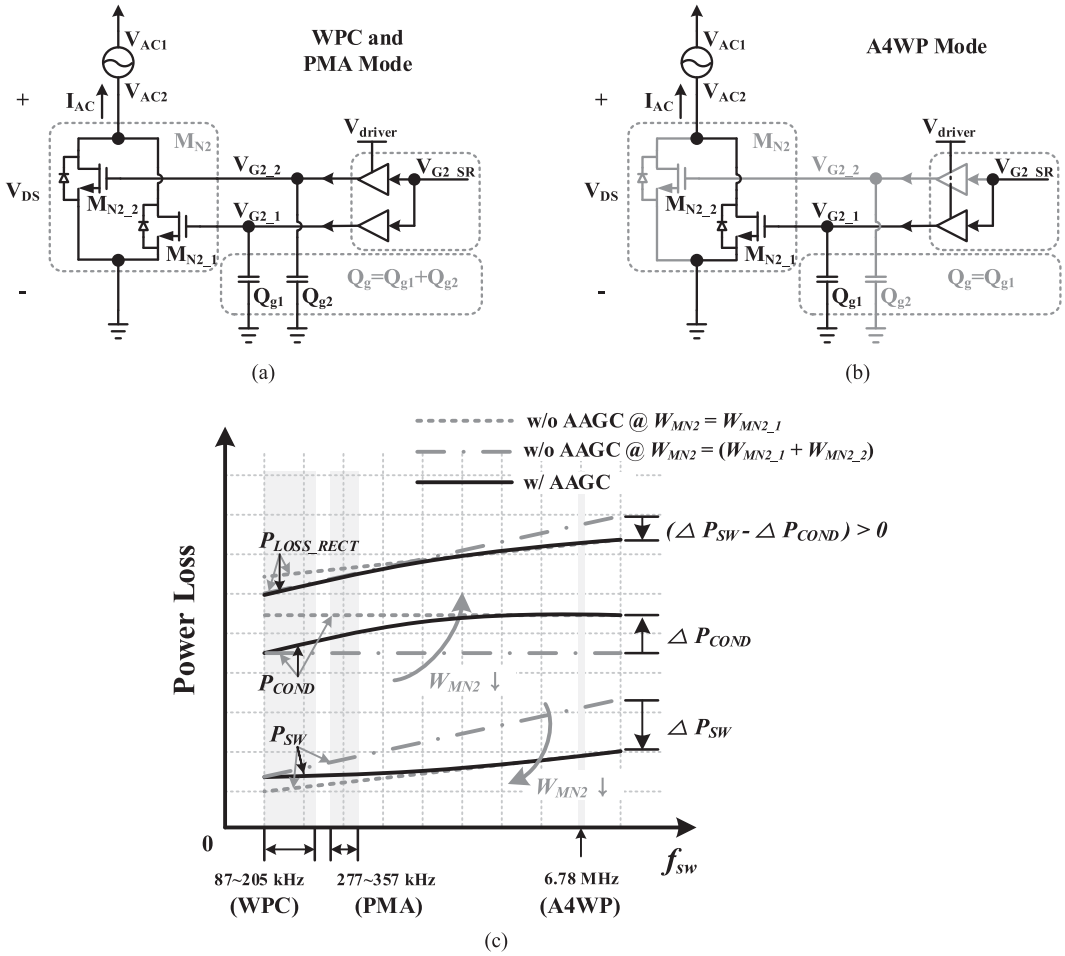

Fig. 6. Simplified circuit of active rectifier for loss analysis of: (a) WPC and PMA mode, (b) A4WP mode, and (c) conduction losses and switching losses of M_{N2} at WPC, PMA, and A4WP modes depending on the sizes of M_{N2}.

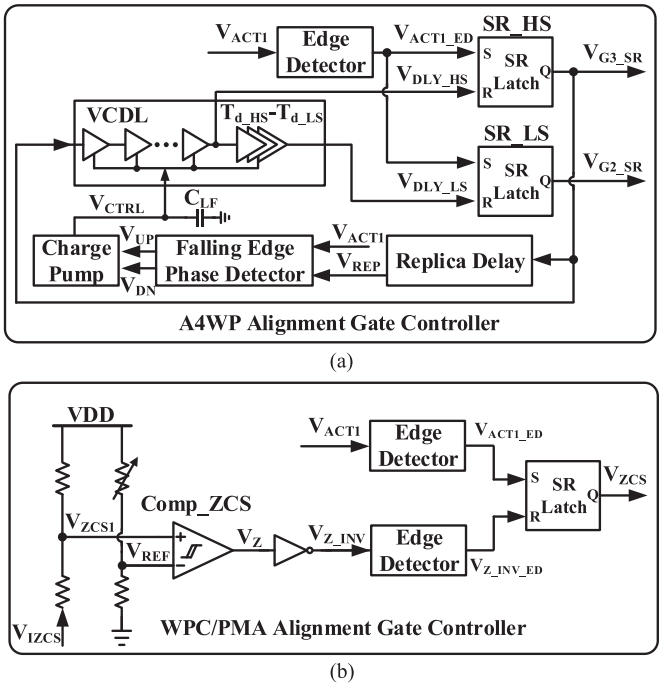

Fig. 7. (a) Detailed adaptive A4WP alignment gate controller. (b) Detailed adaptive WPC/PMA alignment gate controller.

rectifier, rising time of V_{G2} node, falling time of V_{G2} node, charge at the parasitic capacitance of V_{G2_1} node, charge at the parasitic capacitance of V_{G2_2} node, driving voltage, and switching frequency of M_{N2}, respectively.

Thus, the sizes of switching MOSFET (M_{N2}) should be controlled automatically depending on the switching frequency since the switching loss is proportional to the switching frequency and the conduction loss is inverse proportional to it.

Fig. 6(c) shows the conduction losses and switching losses of M_{N2} at WPC, PMA, and A4WP modes depending on the sizes of M_{N2}. When the switching frequency is high, the switching loss is dominant. Thus, the size of M_{N2} (W_{MN2}) needs to be decreased at the frequency of 6.78 MHz since the reduced amount of switching loss ($-\Delta P_{\mathrm{SW}}$) is larger than the increased amount of conduction loss ($+\Delta P_{\mathrm{COND}}$). In this paper, the efficiency of active rectifier is optimized by the AAGC that can change the sizes of Core MOSFETs depending on the modes (WPC, PMA, and A4WP).

Fig. 7(a) shows the detailed adaptive alignment gate controller. In A4WP alignment gate controller, the replica delay is designed to be the same as the delay of the level shifter, and V_{REP} is the output signal of the replica delay. The phase difference between V_{REP} and V_{ACT1} using a falling edge phase detector and the charge pump generates V_{CTRL}. The voltage controlled delay line (VCDL) controls delay time depending on V_{CTRL}. Fig. 7(b) shows the detailed WPC/pma adaptive alignment gate controller, which compares V_{ZCS1} with V_{REF} to generate the ZNS signal V_{ZCS}. In order to enhance the PCE, the AAGC scheme is proposed in the triple-mode active rectifier to achieve synchronization between ac input voltage, current, and gate control signals ($V_{G1\_1} - V_{G4\_2}$) for switching MOSFETs ($M_{N1} - M_{N4}$). This can also adaptively change the configuration by selecting the optimal sizes of drivers and power MOSFETs ($M_{N1} - M_{N4}$). When the A4WP mode is detected, the WPT_MODE signal goes to low and M_{N1_2}, M_{N2_2}, M_{N3_2}, and M_{N4_2} are disabled.

When the A4WP Alignment Gate Controller is enabled, the turn-ON times of M_{N3_1} (T_{t_HS}) and M_{N2_1} (T_{t_LS}), respectively, are generated as

$$T_{t\_\mathrm{HS}} = T_{ON} - 2T_{d\_\mathrm{HS}} + T_{d\_\mathrm{HS}} = T_{\mathrm{ON}} - T_{d\_\mathrm{HS}} \quad (4)$$

$$T_{t\_LS} = T_{\mathrm{ON}} - 2T_{d\_LS} + T_{d\_LS} = T_{\mathrm{ON}} - T_{d\_LS} \quad (5)$$

where T_{ON}, T_{d_HS}, and T_{d_LS} are the half-period of 6.78 MHz, delay times of the level shifter, and HS_Driver, and delay time of LS_Driver, respectively. When the WPC and PMA mode is selected, the signal level of WPT_MODE goes to high. M_{N1}, M_{N2}, M_{N3}, and M_{N4} can be turned ON by gate signals ($V_{G1\_1} - V_{G4\_2}$). When the I_{AC} current is positive, AAGC turns ON M_{N1} and M_{N4}. However, when the current level of I_{AC} is negative, it turns ON M_{N2} and M_{N3}. The comparator in Fig. 5, Comp_ZCS, detects the polarity of I_{AC}.

Fig. 8(a) shows the timing diagram of the triple-mode active rectifier with the A4WP alignment gate controller. When the V_{ACT1} becomes high, $V_{\mathrm{G3_1}}$ and $V_{\mathrm{G2_1}}$ become high after the delay times of T_{d_HS} and T_{d_LS}, respectively. When $V_{\mathrm{DLY_HS}}$ and $V_{\mathrm{DLY_LS}}$ become high after the delay times of T_{t_HS} and T_{t_LS}, respectively, $V_{\mathrm{G3_1}}$ and $V_{\mathrm{G2_1}}$ are low.

Fig. 8(b) shows the timing diagram of the triple-mode active rectifier with the WPC and PMA alignment gate controller. When V_{ACT1} is high, V_{ZCS} becomes high. When V_{ZCS1} voltage is lower than V_{REF} voltage, V_{ZCS} becomes low.

B. DC–DC Converter

Fig. 9 shows a block diagram of the dc–dc converter needed to compensation of switching frequency and dead time. The input voltage of the dc–dc converter is connected to V_{RECT}, which is the voltage rectified by the triple-mode active rectifier. Therefore, the operation of the dc–dc converter is not directly related to the WPT (WPC, PMA, and A4WP) systems. However, the output (V_{RECT}) of the rectifier has the voltage ripple whose frequency is double that of the frequency of V_{AC} in the WPT system. Thus, operation of the dc–dc converter needs to be more stable with respect to the input voltage variation. In this paper, the dc–dc converter is designed to support the fast-charging mode with the maximum output power level of 9 W, which requires the high PCE since the heat from it can be increased as the output power level is higher. Thus, the dead-time generator is proposed to optimize the dead time for improved efficiency. In [18]–[21], variable turn-on delay generators are used for an adaptive dead-time control circuit. However, this scheme is sensitive to the delay mismatch due to the variations of process, temperature, voltage, and parasitic capacitances [18]. Continuous-time comparator generally needs several hundreds of nanoseconds from the off-state to the active operation, and hence it is not always available for instant sensing and comparison during different V_X node signal excursions, which results in significant conduction power loss through the body diode

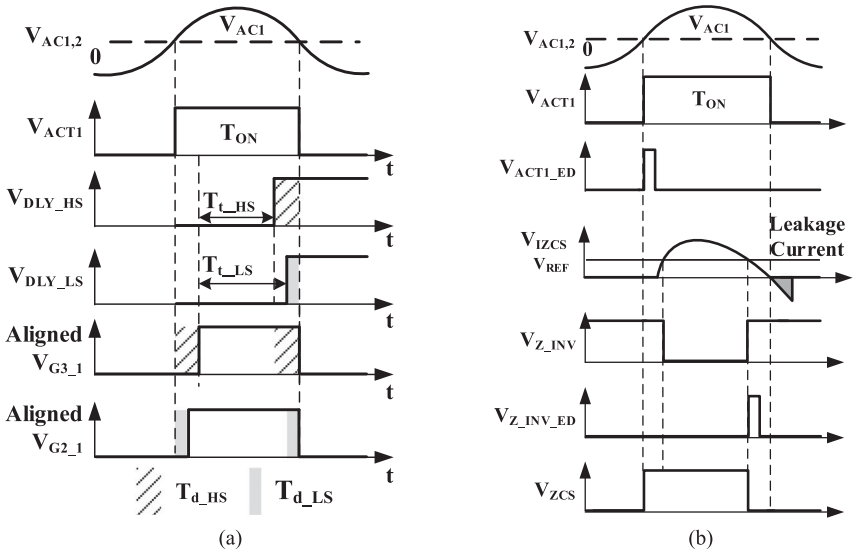

Fig. 8. Timing diagram of the triple-mode active rectifier: (a) with A4WP alignment gate controller; and (b) with WPC/PMA alignment gate controller.

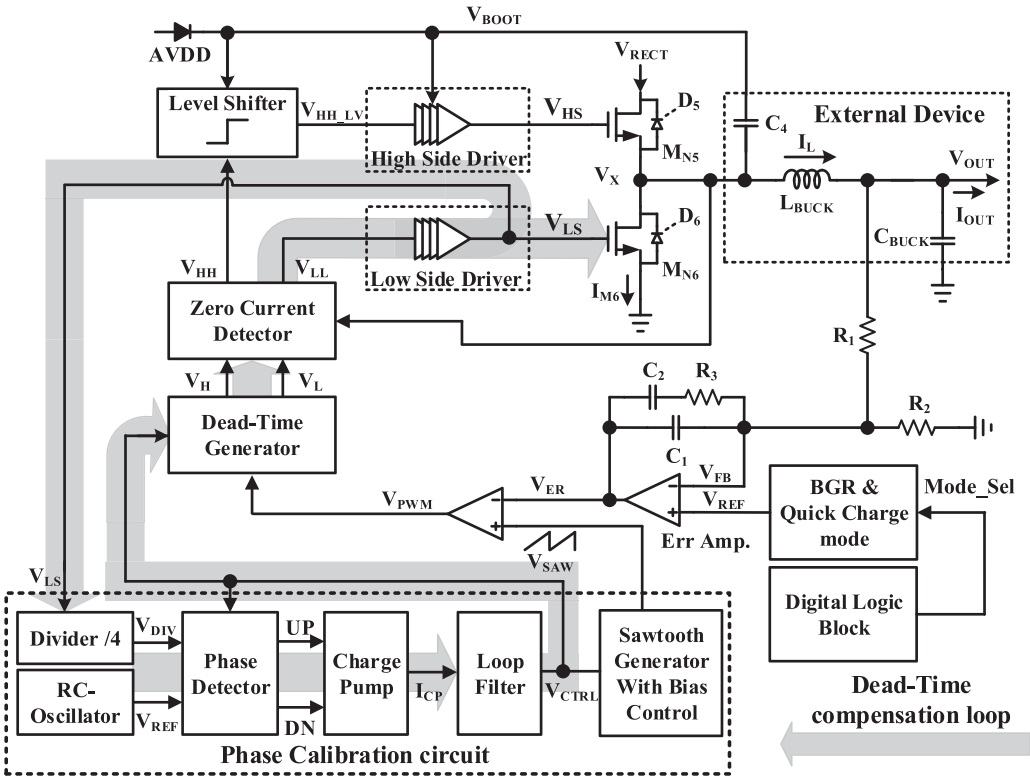

Fig. 9. Block diagram of the dc–dc converter for compensation of variation of switching frequency and dead time.

of M_{N6} [18]. In [19], automatic dead-time is generated by the phase of V_X and low-side gate signal. However, this structure can be used if V_X voltage is lower than 5 V [19]. The way sensing V_X node with diode can also be used, but there is serious power loss in the light load due to some leakage current through the power path. Also, the process, voltage, and temperature (PVT) variation makes the approach difficult to be used for the commercial products [20], [21]. In order to mitigate the above issues, adaptive dead-time controller that can adjust the dead time adaptively with respect to the temperature variations even though V_X node is not directly sensed is proposed in the dc–dc converter.

The dc–dc converter, which employs a phase calibration (PC) circuit, consists of a bandgap reference (BGR), which generates the internal reference voltage; an error amplifier (Err Amp.), which amplifies the voltage difference between the output voltage and reference voltage; a PC circuit consisting of *RC* oscillator, divider/4, phase frequency detector, charge pump, loop

filter, and sawtooth generator with bias control, which generates a constant frequency irrespective of the PVT and external circumstances; a zero current detector; and drivers for the power MOSFETs (M_{N5} and M_{N6}).

In Fig. 9, C_{BUCK}, L_{BUCK}, and C_4 are the output capacitance, inductance of the dc-dc converter, and the boosting capacitor, respectively. R_1, R_2, R_3, C_1, and C_2 are used for a compensation feedback loop. V_{RECT} is the input voltage to the dc–dc converter. V_{HS} and V_{LS} are the gate voltage signals for M_{N5} and $M_{N6,}$ respectively. The dc–dc converter operates in the CCM region or DCM region when the load current is from 300 mA to 1.0 A or below 300 mA, respectively. As mentioned earlier, the widths of power MOSFETs (M_{N5} and M_{N6}) are increased to reduce their conduction losses. As a result, the parasitic capacitances at V_{LS} and V_{HS} nodes are also increased. The heat due to the power loss causes the variation of parasitic capacitance depending on the temperature, which affects the switching operation and efficiency of the dc–dc converter [22].

Therefore, it would reduce the slew rate of each driver and increase the mismatch between delays of the high-side driver and low-side driver in Fig. 9. If the slew rate is too small, there may be the overlap between high durations of V_{HS} and V_{LS}, which can cause the shoot-through current and drastically decrease the PCE of the dc–dc converter when the dead time is too short. Therefore, this paper proposes a dead-time compensation circuit to overcome the problem caused by the process, voltage, and temperature variations [23], [24].

In this paper, the dead time of the dc–dc converter is adaptively controlled by a dead-time generator with PC circuit, which is designed to minimize the duration of dead time. This has the advantage that its dead time is optimally controlled regardless of the voltage and temperature variations. Thus, the PCE of the dc–dc converter can be maximized by automatically selecting the optimum dead time through the dead-time compensation loop.

The V_{SAW} is generated by the sawtooth generator with bias controller, which is compensated by the PC circuit. Therefore, the frequency of V_{SAW} is compensated to frequency of V_{REF}. The dead-time generator generates dead time between V_{LS} and V_{HS} depending on the level of V_{CTRL}. If the level of V_{CTRL} is increased or decreased, the dead time is also increased or decreased.

Fig. 10 shows the proposed phase detector and charge pump in the PC circuit. An UP signal is generated based on the phase difference between V_{REF} and V_{DIV}. The current of I_{VDN} is inverse proportional to the V_{CTRL} voltage. The loop in Fig. 10 operates to make the I_{UP} and I_{DN} the same.

Fig. 11 shows the block diagram of the dead-time generator. The proposed dead-time generator consists of a rising/falling one shoot trigger, hysteresis comparator, D flip-flop (D-FF), and logic gates. The output of PC (V_{CTRL}) is applied to the proposed dead-time generator to change I_{DEAD}. Also, $V_{\mathrm{ONE_S}}$ is generated by the rising edge and falling edge of V_{PWM} through the rising/falling one shoot trigger. When $V_{\mathrm{ONE_S}}$ is high, C_{DEAD} is discharged and V_{D} goes to low by the hysteresis comparator. V_D determines the duty of dead time. The output of V_D is connected to D-FF and AND gates to generate the dead time.

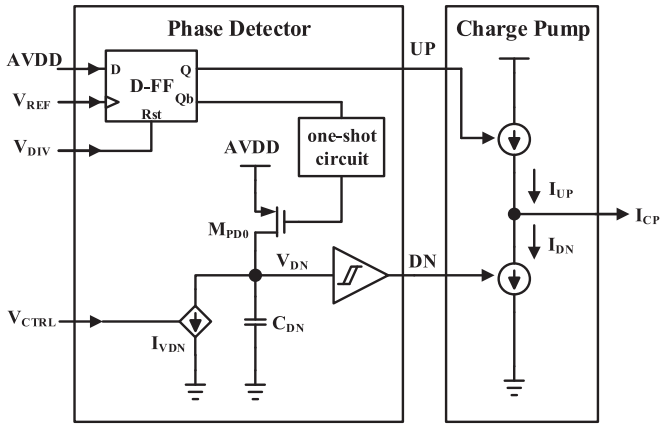

Fig. 10. Block diagram of the proposed phase detector and charge pump in the PC circuit.

The zero current detector senses the V_X node, to prevent reverse leakage current in the DCM mode.

Fig. 12(a) illustrates the operation of the PC circuit in the dc–dc converter with respect to the frequency variation. The switching frequency is controlled by the control voltage, V_{CTRL}, when the switching frequency is changed because of voltage, temperature variations and the external environment. V_{CTRL} is changed by the PD, charge pump, and loop filter of the PC circuit. As the phase difference ($\Delta\Phi$) is increased, PD detects it and V_{CTRL} is increased by the charge pump and loop filter to compensate for the variation of dead time.

Fig. 12(b) shows the operation of the PC circuit in the dc–dc converter with respect to the dead-time variation. When the dead time is small, the high durations of gate driving signals (V_{HS} and V_{LS}) for high-side driver and low-side driver can be overlapped causing the shoot-through current. In this case, V_{CTRL} is increased by the PC circuit and I_{DEAD} is gradually reduced, lowering the charging slope of V_{DEAD}. As a result, the high duration of V_D and dead time are increased. The extended dead time does not generate the shoot-through current. In this way, constant a dead time is generated, which solves the problems of shoot-through current and body diode loss.

C. Power-Up Circuit

When the voltage of V_{RECT} is supplied by V_{AC}, the power-up circuit generates power and a reference voltage for the internal circuit. Moreover, the power-up circuit checks the rectifier voltage, which can operate the circuits of the TWPRU, such as the triple-mode active rectifier, dc–dc converter, SAR ADC, and digital logic block, in a standby state.

Fig. 13 shows a block diagram of the power-up circuit, which consists of a limiter, BGR, internal Low Drop Out (LDO), reference voltage generator, under voltage lock out (UVLO), power on reset (POR), and oscillator conditions [25]–[27]. If the voltage of V_{RECT} is higher than 5 V, the limiter clamps the voltage of V_{RECT} to V_{LIMIT}. Thus, because of the limiter circuit, it is possible to design the BGR, internal LDO, and reference voltage generator block using a 5-V process. The BGR block generates the reference voltage to supply the internal LDO or reference

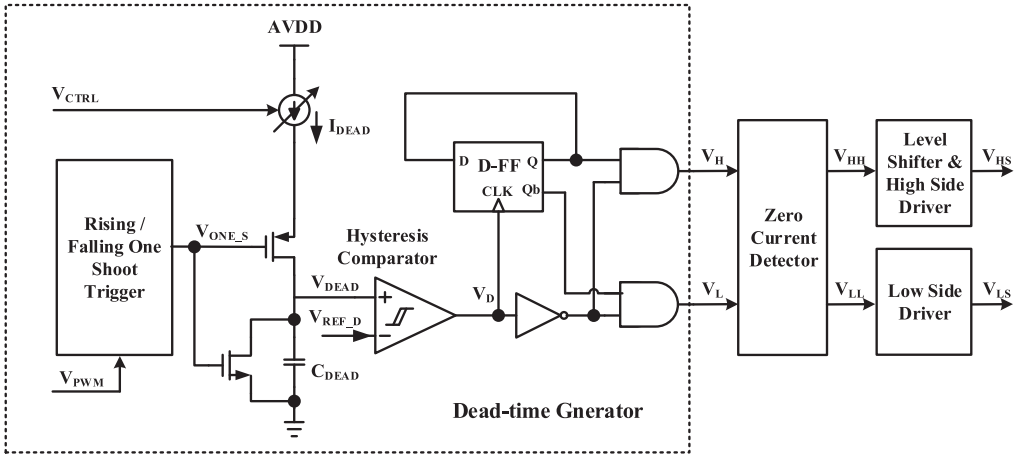

Fig. 11. Block diagram of the dead-time generator.

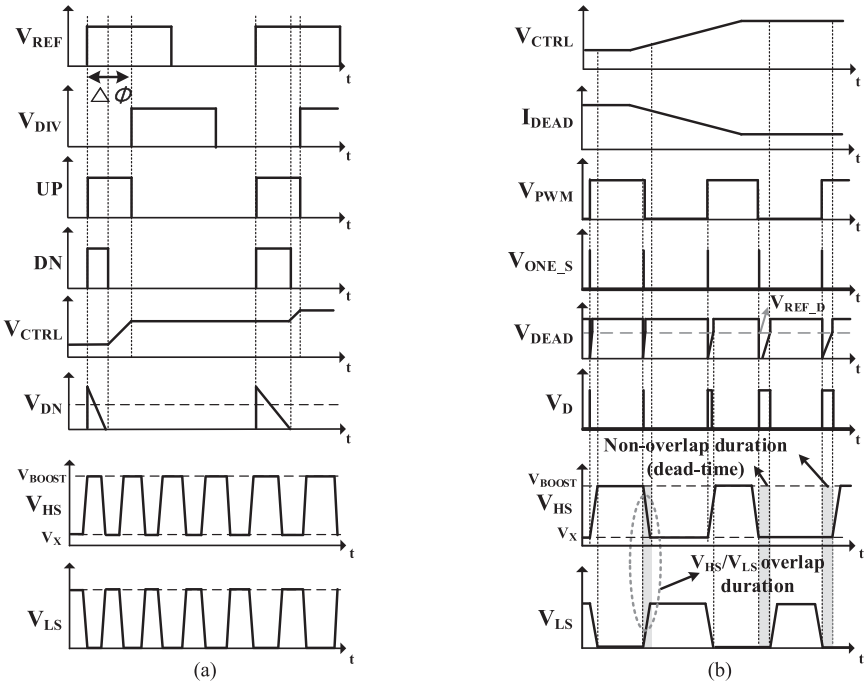

Fig. 12. Operation of the PC circuit in the dc–dc converter with respect to (a) frequency variation, and (b) dead-time variation.

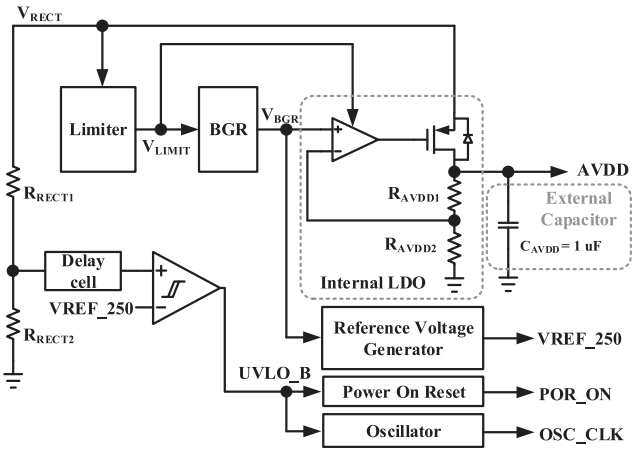

Fig. 13. Block diagram of the power-up circuit.

voltage generator block. The internal LDO is the power supply for the internal circuit of the TWPRU; the reference voltage generator generates the reference voltage of TWPRU. In the UVLO circuit, if the V_{RECT} voltage is lower than VREF_250, the UVLO_B node goes to low, in order to prevent malfunction. The POR generates the power enable signal of the triple-mode active rectifier, dc–dc converter, SAR ADC, and digital logic block. The oscillator generates the clock signal OSC_CLK to inputs of the SAR ADC and Digital Block.

Fig. 14 shows the conditions for the power-up sequence of TWPRU with respect to the voltage of the rectifier. When the V_{RECT} voltage is 2.5 V, UVLO is released and the POR_ON signal becomes high. The V_{RECT} voltage that is over 2.5 V regulates the VREF_250 voltage to 2.5 V. When V_{RECT} voltage is over 5 V, the power supply of AVDD is regulated at 5 V. Soft overvoltage protection (SOVP) and hard overvoltage protection

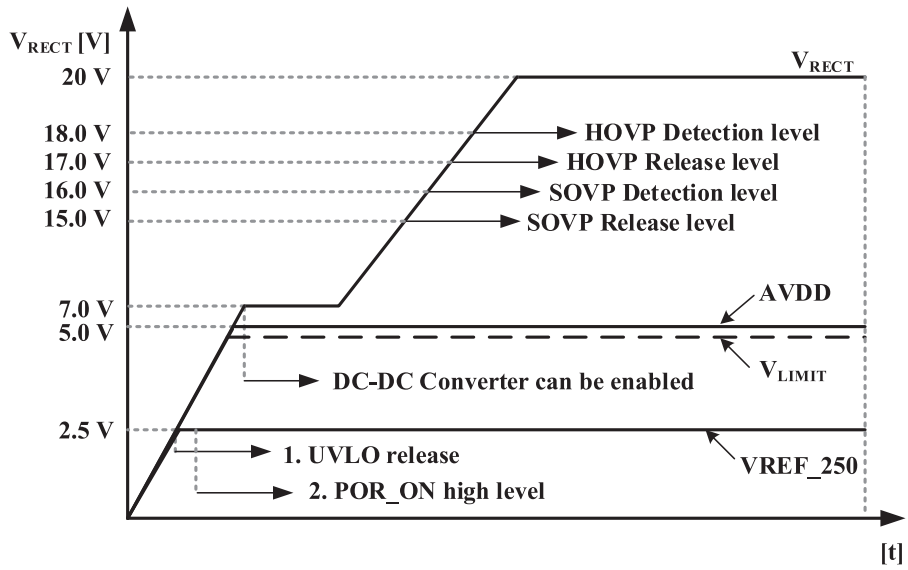

Fig. 14. Conditions for the power-up sequence of TWPRU with respect to the rectifier output voltage.

(HOVP) are detected at 16 V and 18 V, respectively. These are released at 15 V and 17 V, respectively. These values are taken from the commercial datasheets and specifications from industrial companies [27].

D. Protection block

The protection block of TWPRU IC consists of two protection circuits. First, the overvoltage protection (OVP) is designed to cut off the $V_{\rm AC}$ voltage when the $V_{\rm RECT}$ voltage becomes higher than the reference voltage.

Power MOSFETs $(M_{N1} - M_{N8})$ are designed using 20 V laterally diffused metal–oxide–semiconductor (LDMOS) in bipolar–CMOS–DMOS (BCD) process. Therefore, the maximum voltage of $V_{\rm RECT}$ is limited to 20 V to protect the power MOSFETs and internal circuits. The OVP reference voltage is lower than 20 V. In this paper, the SOVP and HOVP detection levels are determined as 16 V and 18 V, respectively. Second, when the temperature of the TWPRU IC is too high or too low, there may be a malfunction in the circuit, so a thermal shutdown function is added. The reference voltages for OVP and thermal shut-down (TSD) are generated by the reference voltage generator block in the power-up circuit.

Fig. 15 shows the system configuration of the protection block. $V_{\rm RECT}$ and $V_{\rm TS}$ are applied to the inputs of the comparator block. The outputs of the comparator block are $V_{\rm SOVP}$, $V_{\rm HOVP}$, $V_{\rm HOT}$, and $V_{\rm COLD}$ signals. The drain nodes of M_{N7} and M_{N8} are connected to the external clamp capacitors ($C_{\rm CL1}$ and $C_{\rm CL2}$). The OVP function is implemented in two ways, SOVP and HOVP, which are design parameters for TWPRU. SOVP changes the effective input capacitance of the rectifier in TWPRU. Therefore, the matching impedance between PTU and TWPRU is changed, and the delivered power is also changed. HOVP cut off the input power to $V_{\rm RECT}$ by connecting the $V_{\rm AC1}$ and $V_{\rm AC2}$ to ground during the turn-ON time of M_{N1} and M_{N2}. When SOVP is enabled, M_{N7} and M_{N8} are turned ON

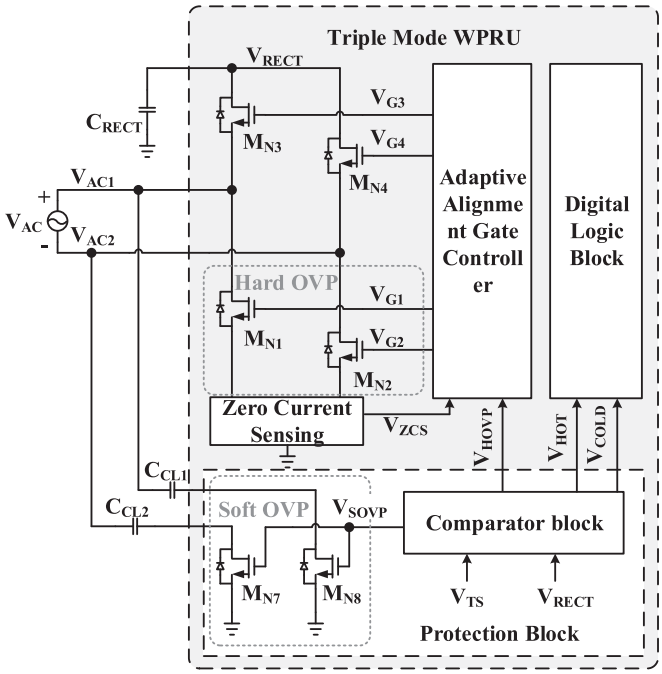

Fig. 15. System configuration of the protection block.

at the same time. In this case, other pins of $C_{\rm CL1}$ and $C_{\rm CL2}$ are connected to nodes $V_{\rm AC1}$ and $V_{\rm AC2}$, respectively.

Other pins of $C_{\rm CL1}$ and $C_{\rm CL2}$ connected to ground so that the impedance across the input, $V_{\rm AC}$, is changed to reduce the input power. Therefore, the requirement of the input voltage range of the dc–dc converter can be relaxed. When HOVP is activated, M_{N1} and M_{N2} are simultaneously turned ON, and the $V_{\rm AC1}$ and $V_{\rm AC2}$ nodes fall to the ground voltage level. The detection level for the HOVP is designed to be 18 V with a margin of 2 V, because the breakdown voltages of devices are 20 V. Capacitances of 2.2 nF are used for $C_{\rm CL1}$ and $C_{\rm CL2}$ [25]. These values can shift the resonance frequency in A4WP systems. Therefore, a

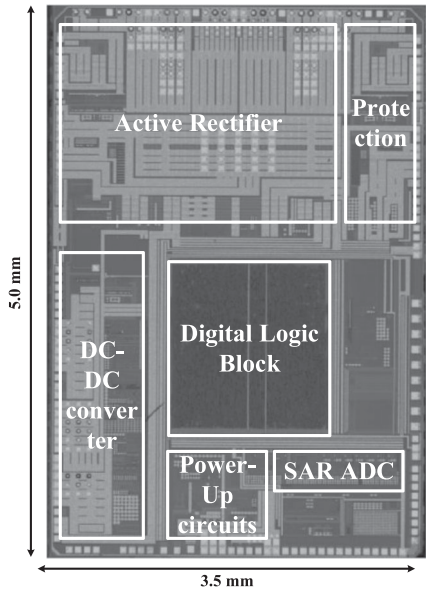

Fig. 16. Microphotograph of the chip.

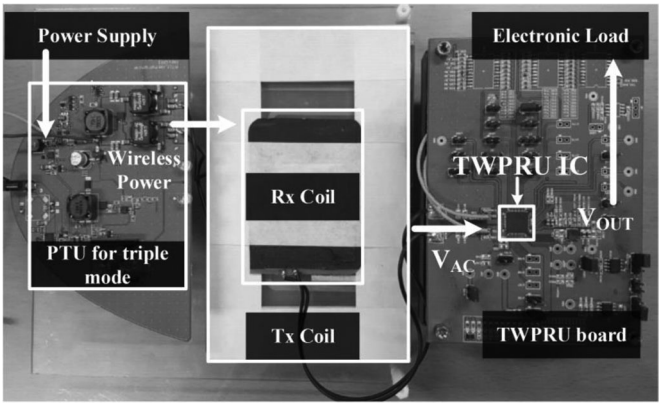

Fig. 17. Measurement environments of the TWPRU.

two-stage OVP operation strengthens protection for the circuit. TSD uses the $V_{\rm TS}$ voltage, which varies linearly with temperature and a comparator, to sense and respond to the temperature of the TWPRU IC. If the increase or decrease in temperature becomes excessive, the thermal shutdown outputs $V_{\rm HOT}$, and the $V_{\rm CLOD}$ signal becomes high.

IV. Experimental Results

The chip was fabricated using the BCD process in 0.18 μm technology using one poly, four metal, and the high-voltage MOSFET option. Fig. 16 shows a microphotograph of the chip. The die area of the TWPRU IC is 5.0 mm $\times$ 3.5 mm.

Fig. 17 illustrates the measurement environments of the TWPRU. The PTU generates the triple-mode frequency, and modifies the matching network for input matching to A4WP, WPC, and PMA. The Tx coil is located under the Rx coil. The power supply is the supply voltage of PTU; the electronic load is that of $V_{\rm OUT}$.

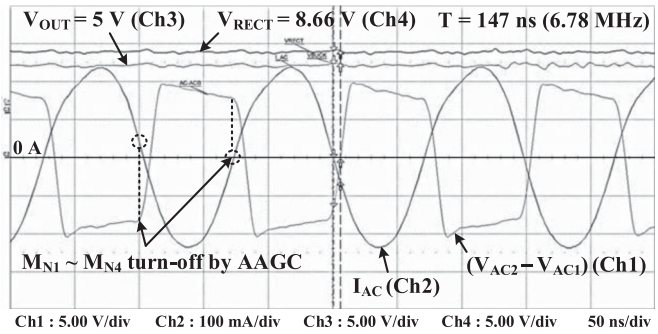

Fig. 18. Measurement results of the triple-mode active rectifier in the A4WP mode.

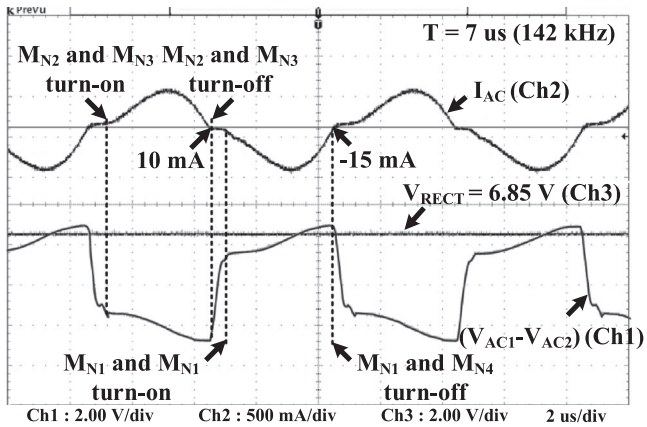

Fig. 19. Measurement results of the triple-mode active rectifier in the WPC and PMA modes.

Fig. 18 shows measurement results of the triple-mode active rectifier in the A4WP mode. The measured output of the rectifier is 8.66 V with the input matching and output of the dc–dc converter is 5.01 V. It shows that the reverse current is blocked by the AAGC function control.

Fig. 19 shows the measurement results of the triple-mode active rectifier in the WPC mode. The AAGC block in the triple-mode active rectifier senses the $I_{\rm AC}$ current. When the $I_{\rm AC}$ current is 10 mA, $M_{\rm N2}$ and $M_{\rm N3}$ are turned ON. On the other hand, when the $I_{\rm AC}$ current is -15 mA, $M_{\rm N1}$ and $M_{\rm N4}$ are turned ON. Therefore, there is no reverse current thanks to the AAGC block.

Fig. 20 shows the measurement results of the dc–dc converter in the DCM mode with zero current detector. When the load current I_L is 200 mA, $V_{\rm OUT}$ is regulated to 5 V, and the dc–dc converter is operated in the DCM region. When the current of I_L is 0 A, M_{N5} and M_{N6} are turned OFF by the zero current detector. Therefore, the dc–dc converter is not damaged by the reverse current in the DCM mode.

Fig. 21 shows the measurement results of the dc–dc converter in the CCM mode. When the load current is 600 mA, the duty ratio of V_{G5} is 80%. There is no shoot-through current in the

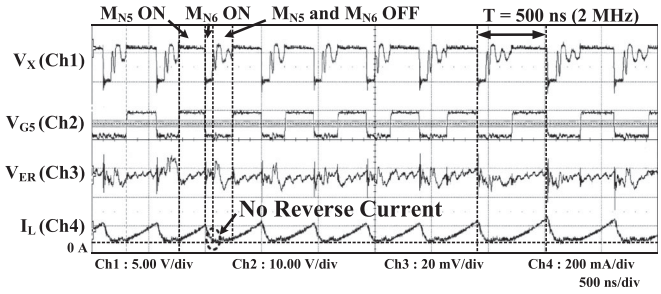

Fig. 20. Measurement results of the dc–dc converter in DCM mode with zero current detector.

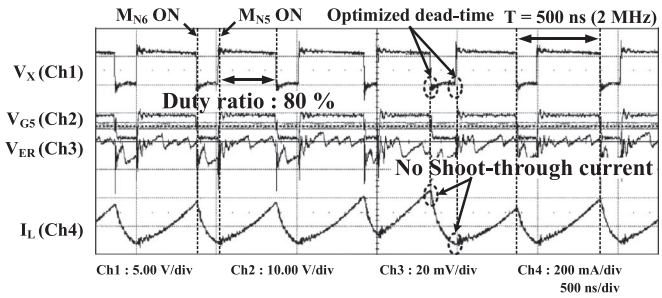

Fig. 21. Measurement results of the proposed dc–dc converter in the CCM mode.

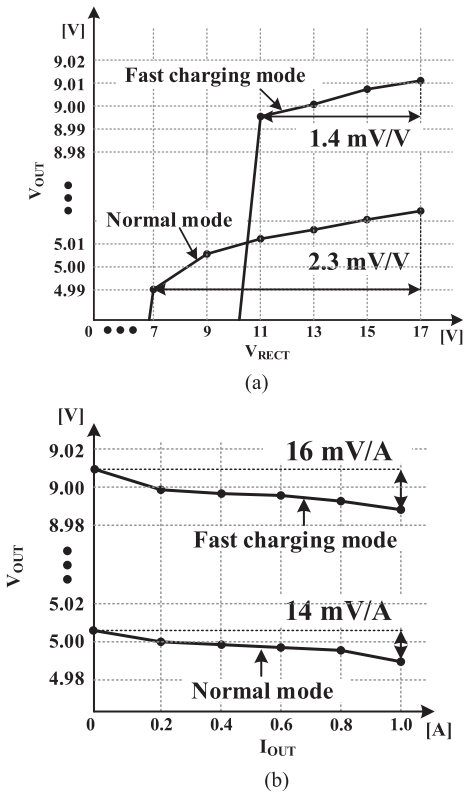

Fig. 22. Measurement results of the dc–dc converter: (a) line regulation and (b) load regulation.

waveform of $I_{\rm L}$ current because the dead time is optimized by the PC circuit.

Fig. 22(a) shows the measurement result of the dc–dc converter line regulation. When the dc–dc converter is in the normal or fast-charging mode, the output voltage is measured by sweeping the voltage of $V_{\rm RECT}$ from 7 to 17 V. The line regulation characteristic is 2.3 mV/V in normal mode, and 1.4 mV/V in fast-charging mode.

Fig. 22(b) shows the measurement results of the dc–dc converter load regulation. When the dc–dc converter is in normal- or fast-charging mode, the output voltage is measured by sweeping the current of $I_{\rm OUT}$ from 0 to 1 A.

Fig. 23 shows the measured PCE of the proposed triple-mode active rectifier with respect to the output current. When the AAGC function is used, the maximum efficiency of the triple-mode active rectifier in the A4WP mode and WPC/PMA are 91.7% and 92.7% in WPC/PMA mode, respectively.

Table II summarizes the power losses of the triple-mode active rectifier when the input power is 7.5 W.

The conduction loss comes from the turn-ON resistances of the low side ($M_{N1} - M_{N2}$) and the high side ($M_{N3} - M_{N4}$). The switching loss and gate drive loss come from the loss of $M_{N1} - M_{N4}$ and the loss to drive $V_{G1.(1,2)} - V_{G4.(1,2)}$, respectively. In addition, the power consumption of the internal circuits of the triple-mode active rectifier contributes to internal circuit losses.

Fig. 24 shows the measured PCE of the proposed dc–dc converter with respect to the output current. When the PC circuit

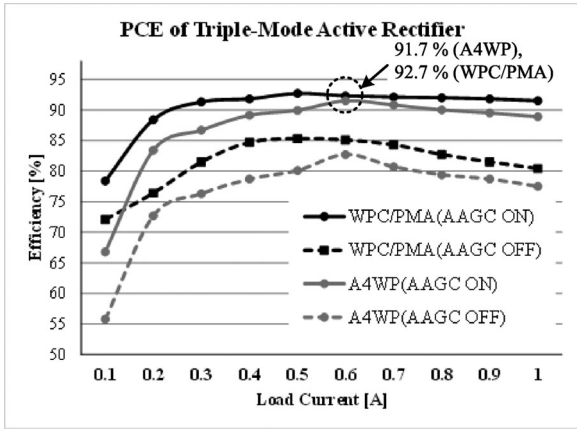

Fig. 23. Measured power efficiency of the proposed triple-mode active rectifier with respect to the output current.

TABLE II
ANALYSIS OF POWER LOSSES OF TRIPLE-MODE ACTIVE RECTIFIER

Parameters	WPC/PMA Mode (@ 150 kHz)	A4WP Mode (@ 6.78 MHz)
Input power	7.5 W	7.5 W
Conduction losses	6.4%	5.7%
Switching losses	0.1%	1.5%
Gate drive losses	0.05%	0.1%
Internal circuits losses	0.75%	1.0%
Total losses	7.3%	8.3%
Output power	6.95 W	6.87 W
Efficiency	92.7%	91.7%

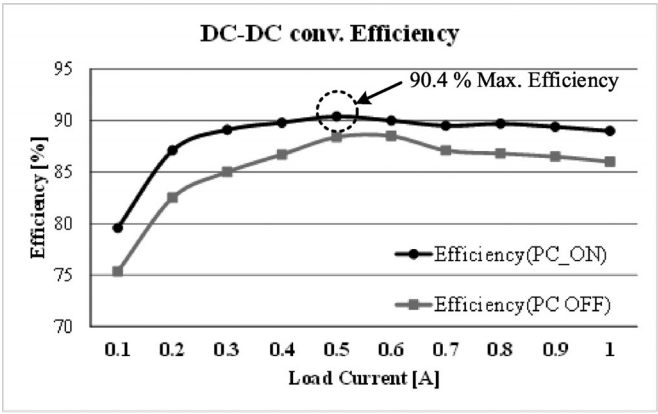

Fig. 24. Measured power efficiency of the proposed dc–dc converter with respect to the output current.

TABLE III
COMPARISON OF REPORTED RELATED TWPRUS AND THIS PAPER

Parameters	[14]	[15]	[16]	**This Paper**
Technology	0.35 μm BCD	0.35 μm CMOS	0.18 μm BCD	**0.18 μm BCD**
Supported standards	A4WP	–	A4WP	**A4WP, WPC and PMA**
Input frequency	3.23 MHz/6.78 MHz	13.56 MHz	6.78 MHz	**6.78 MHz/85–500 kHz**
Input voltage range (V)	4–8	1.5–4	7–20	**3–20**
Efficiency of rectifier (%)	81 @ 3.23 MHz	90.1	91.5	91.7 @ 6.78 MHz
	74 @ 6.78 MHz	(Rectifier only)		/92.7 @ 150 kHz
Efficiency of dc–dc converter (%)	92.5	–	88	**92.3**
System efficiency (%)	75	82.2–90.1	80.86	**84.5 @ 6.78 MHz**
				85.5 @ 150 kHz
Max. output power (W)	3	0.024	5	**9**
Die area (mm^2)	18.3	0.186	12.25	**17.5**

function is used, the maximum efficiency of the dc–dc converter is 92.3% at a load current of 500 mA.

Table III compares the reported related TWPRUs and this paper [14]–[16]. The proposed TWPRU shows the highest overall efficiency.

In this paper, the efficiency of the proposed triple-mode active rectifier is higher than those of prior works in the A4WP mode [14]–[16]. Also, it can support WPC, PMA, and A4WP standards with an efficiency of 92.7% in contrast to previous work, which can support just A4WP. The die size of the proposed triple-mode active rectifier is 17.5 mm^2, which is smaller than that of [14]. The efficiency of the dc–dc converter is higher than that of the previous dc–dc converter for the A4WP mode [16]. And as compared with limited output power levels (3 W, 5 W) of previous works, the proposed dc–dc converter can support up to 9 W [14]–[16].

V. CONCLUSION

This paper presents the design of a TWPRU with high efficiency for A4WP, WPC, and PMA applications. In the triple-mode active rectifier, the AAGC technique is proposed to block the reverse leakage current and improve the PCE. The PC circuit is adopted to minimize the dead time between the gate driving signals for high-side driver and low-side driver in the proposed dc–dc converter.

This chip is implemented in 0.18-μm BCD technology with an active area of 5.0 mm $\times$ 3.5 mm. The maximum PCEs of the triple-mode active rectifier are 91.7% in the A4WP mode, and 92.7% in the WPC mode or PMA mode, respectively. The maximum PCE of the dc–dc converter is 92.3% at a load current of 500 mA, while the system efficiencies of TWPRU at A4WP and WPC, PMA modes are about 84.5% and 85.5%, respectively.

REFERENCES

[1] K. A. Kalwar, M. Aamir, and S. Mekhilef, "Inductively coupled power transfer (ICPT) for electric vehicle charging a review," *Renewable Sustain. Energy Rev.*, vol. 47, pp. 462–475, Mar. 2015.
[2] Wireless Power Consortium, "System description, wireless power transfer, Vol. I: Low power, Part 1: Interface definition," Version 1.0, Jul. 2010.
[3] J. J. Casanova *et al.*, "Design and test of a high-power high-efficiency loosely coupled planar wireless power transfer system," *IEEE Trans. Ind. Electron.*, vol. 56, no. 5, pp. 1801–1812, May 2009.
[4] "Introduction to wireless power," Texas Instruments, Dallas, TX, USA, 2012, pp. 1–49
[5] S. Bastami, "Magnetic induction or magnetic resonance for wireless charging?," *Bodo's Power Syst.*, pp. 22–26, Jan. 2013.
[6] Y.-K. Moon *et al.*, "Wide input range, high-efficiency magnetic resonant wireless power receiver," *Int. J. Electron.*, vol. 102, no. 2, pp. 326–334, 2015.
[7] R. Shinoda *et al.*, "Voltage-boosting wireless power delivery system with fast load tracker by $\Delta\Sigma$-modulated sub-harmonic resonant switching," in *Proc. Solid-State Circuits Conf. Dig. Tech. Papers*, Feb. 2012, pp. 288–290.
[8] Jun-Han Choi *et al.*, "A resonant regulating rectifier (3R) operating at 6.78MHz for a 6W wireless charger with 86% efficiency," in *Proc. Solid-State Circuits Conf. Dig. Tech. Papers*, Feb. 2013, pp. 64–65.
[9] P. S. Riehl *et al.*, "Wireless power receiver for mobile devices supporting inductive and resonant operating modes," *IEEE Trans. Microw. Theory Techn.*, vol. 63, no. 3, pp. 780–790, Mar. 2015.
[10] Y.-J. Park *et al.*, "A design of a 92.4% efficiency triple mode control DC–DC buck converter with low power retention mode and adaptive zero current detector for IoT/Wearable applications," *IEEE Trans. Power Electron..*, vol. 32, no. 9, pp. 6946–6960, Sep. 2017, doi: 10.1109/TPEL.2016.2623812.
[11] A. Berzoy, O. A Mohammed, and A. A. S. Mohamed, "Optimizing power converter PCB magnetic design for lower EMI levels," *COMPEL Int. J. Comput. Math. Elect.*, vol. 34, no. 5, p. 1, Aug. 2015
[12] S. Kong *et al.*, "An investigation of electromagnetic radiated emission and interference from multi-coil wireless power transfer systems using resonant magnetic field coupling," *IEEE Trans. Microw. Theory Techn.*, vol. 63, no. 3, pp. 833–846, Mar. 2015.
[13] S. Kim *et al.*, "High-efficiency PCB- and package-level wireless power transfer interconnection scheme using magnetic field resonance coupling," *IEEE Trans. Compon., Packag. Manuf. Technol.*, vol. 5, no. 7, pp. 863–878, Jul. 2015.
[14] Y.-J. Moon *et al.*, "A 3.0-W wireless power receiver circuit with 75-% overall efficiency," in *IEEE Asian Solid State Circuits Conf.*, Nov. 2012, pp. 97–100.
[15] Y. Lu *et al.*, "A 13.56 MHz CMOS active rectifier with switched-offset and compensated biasing for biomedical wireless power transfer systems," *IEEE Trans. Biomed. Circuits Syst.*, , vol. 8, no. 3, pp. 334–344, Jul. 2013.
[16] H._Gu Park *et al.*, "A design of a wireless power receiving unit with high efficiency 6.78 MHz active rectifier using shared DLLs for magnetic resonant A4WP applications," *IEEE Trans. Power Electron.,* vol. 31, no. 6, pp. 4484–4498, Jun. 2016.

[17] J.-H. Kang *et al.*, "A design of wide input range, high efficiency rectifier for mobile wireless charging receiver," in *Proc. Wireless Power Transfer Conf.*, 2014, pp. 154–157.
[18] K. Sujan *et al.*, "94.6% peak efficiency DCM buck converter with fast adaptive dead-time control," in *Proc. ESSCIRC*, Sep. 2013, pp. 2–3.
[19] Mi Zhou *et al.*, "A high efficiency synchronous buck converter with adaptive dead-time control," in *Proc. Int. Conf. VLSI Syst.–Chip*, Oct. 2011, pp. 1–2.
[20] L. Mei *et al.*, "A synchronous buck converter using a new predictive analog dead-time control circuit to improve efficiency," *Can. J. Elect. Comput. Eng.*, vol. 36, no. 4, pp. 1–2 Mar. 2014.
[21] SangYun Kim *et al.*, "A design of a high efficiency DC-DC buck converter with two-step digital PWM and low power self tracking zero current detector for IoT applications," *IEEE Trans. Power Electron.*, to be published, doi: 10.1109/TPEL.2017.2688387.
[22] I. Cortes *et al.*, "Analysis of the C-V characteristic in SiO2/GaN MOS capacitors," in *Proc. 2009 Spanish Conf. Electron. Devices*, 2009, pp. 254–257.
[23] K. Hong Jin *et al.*, "High power efficiency, 8 V∼20 V input range DC-DC buck converter with phase-locked loop," in *Proc. 9th Int. Conf. Power Electron./ECCE Asia*, 2015, pp. 1772–1777.
[24] S. W. Hong *et al.*, "Secondary-side LLC resonant controller IC with dynamic PWM dimming and dual-slope clock generator for LED backlight units," *IEEE Trans. Power Electron.*, vol. 26, no. 11, pp. 3410–3422, Nov. 2011.
[25] Y. Yuan *et al.*, "A CMOS bandgap reference with wide input voltage range," in *Proc. 2009 WRI World Congr. Comput. Sci. Inf. Eng.*, Mar. 2009, vol. 3, pp. 364–368.
[26] M. El-Nozahi *et al.*, "High PSR low drop-out regulator with feed-forward ripple cancellation technique," *IEEE J. Solid-State Circuits,* , vol. 45, no. 3, pp. 565–577, Mar. 2010.
[27] NX1A4WP, NXP Semiconductor Products Inc., Eindhoven, The Netherlands, 2006

Young-Jun Park received the B.S. degree in electronics engineering from the Kumoh National Institute of Technology, Gumi, South Korea, in 2013. Since then he has been working toward the M.S. degree in electronics and computer engineering at Sungkyunkwan University, Suwon, South Korea.

His research interest mainly focuses on the design of power management integrated circuits for high-efficiency and wireless power transfer system.

ByeongGi Jang received the B.S. degree in electronics engineering from the Department of Electronic Engineering, Chonbuk National University, Jeonju, South Korea, in 2015, where he is currently working toward the M.S. degree in School of Information and Communication Engineering, Sungkyunkwan University, Seoul, South Korea.

His research interests include power management IC.

Seong-Mun Park received the B.S. degree in electronics engineering from the Department of Electronic Engineering, Sungkyunkwan University, Suwon, South Korea, in 2016, where he is currently working toward the M.S. degree in School of Information and Communication Engineering, Sungkyunkwan University, Seoul, South Korea.

His research interests include power management IC and CMOS RF transceiver.

Ho-Cheol Ryu received the B.S. degree in electronics engineering from the Department of Electronic Engineering, Sungkyunkwan University, Suwon, South Korea, in 2015, where he is currently working toward the Combined Ph.D. and M.S. degree in the School of Information and Communication Engineering.

His research interests include CMOS RF transceiver, phase-locked loop.

Seong-Jin Oh received the B.S. degree in electronics engineering from the Department of Electronic Engineering, Sungkyunkwan University, Suwon, South Korea, in 2014, where he is currently working toward the Combined Ph.D. and M.S degree in the School of Information and Communication Engineering.

His research interests include CMOS RF transceiver, phase-locked loop, push–push voltage controlled oscillator.

Sang-Yun Kim (S'13) received the B.S. degree in electronics engineering from the Department of Electronic Engineering, Konkuk University, Seoul, South Korea, in 2013. He is currently working toward the Combined Ph.D. and M.S. degree in the School of Information and Communication Engineering, Sungkyunkwan University, Suwon, South Korea.

His research interests include high-speed interface IC and CMOS RF transceiver.

YoungGun Pu received the B.S., M.S., and Ph.D. degrees in electronics engineering from the Department of Electronic Engineering, Konkuk University, Seoul, South Korea, in 2006, 2008, and 2012, respectively.

His research interest focuses on CMOS fully integrated frequency synthesizers and oscillators and on transceivers for low-power mobile communication.

Sang-Sun Yoo received the B.S. degree in electronics engineering from Dongguk University, Seoul, South Korea, in 2004, and the M.S./Ph.D. degree in electronics engineering received from the Korea Advanced Institute of Science and Technology (KAIST), Daejeon, South Korea, in 2012.

From 2012 to 2015, he was with the System LSI Division, Samsung Electronics, , where his research was focused on ADPLL for 3/4G mobile applications as a Senior Design Engineer. From 2015 to 2016, he was a Research Assistant Professor in KAIST and Sungkyunkwan University. Since 2017, he has been with Department of Smart Automobile, Pyeongtaek University, Pyeongtaek, South Korea, where he is currently an Assistant Professor. His research interests include RF systems for mobile communications, reconfigurable RFICs, automotive ICs, ADPLL, RFID, and sensor communications.

Dr. Yoo received of the Best Paper Award of the IEEE TRANSACTIONS ON INDUSTRIAL ELECTRONICS in 2011.

Keum Cheol Hwang (SM'13) received the B.S. degree in electronics engineering from Pusan National University, Busan, South Korea, in 2001, and the M.S. and Ph.D. degrees in electrical and electronic engineering from the Korea Advanced Institute of Science and Technology, Daejeon, South Korea, in 2003 and 2006, respectively.

From 2006 to 2008, he was a Senior Research Engineer with the Samsung Thales, Yongin, South Korea, where he was involved with the development of various antennas including multiband fractal antennas for communication systems and Cassegrain reflector antenna and slotted waveguide arrays for tracking radars. From 2008 to 2014, he was an Associate Professor in the Division of Electronics and Electrical Engineering, Dongguk University, Seoul, South Korea. In 2015, he joined the Department of Electronic and Electrical Engineering, Sungkyunkwan University, Suwon, South Korea, where he is currently an Associate Professor. His research interests include advanced electromagnetic scattering and radiation theory and applications, design of multiband/broadband antennas and radar antennas, and optimization algorithms for electromagnetic applications.

Prof. Hwang is a life member of KIEES and a member of IEICE.

Youngoo Yang (S'99–M'02) was born in Hamyang, South Korea, in 1969. He received the Ph.D. degree in electrical and electronic engineering from the Pohang University of Science and Technology, Pohang, South Korea, in 2002.

From 2002 to 2005, he was with Skyworks Solutions Inc., Newbury Park, CA, USA, where he designed power amplifiers for various cellular handsets. Since March 2005, he has been with the School of Information and Communication Engineering, Sungkyunkwan University, Suwon, South Korea, where he is currently an Associate Professor. His research interests include power amplifier design, RF transmitters, RFIC design, integrated circuit design for RFID/USN systems, and modeling of high-power amplifiers or devices.

Minjae Lee (M'08) received the B.Sc. and M.S. degrees in electrical engineering from Seoul National University, Seoul, South Korea, in 1998 and 2000, respectively, and the Ph.D. degree in electrical engineering from the University of California, Los Angeles, Los Angeles, CA, USA, in 2008.

In 2000, he was a Consultant with GCT semiconductor, Inc., and Silicon Image Inc., designing analog circuits for wireless communication and digital signal processing blocks for Gigabit Ethernet. He joined Silicon Image Inc., Sunnyvale, CA, USA, in 2001, developing Serial ATA products. In August 2008, he joined Agilent Technologies, Santa Clara, CA, where he was involved with the development of next-generation high-speed ADCs and DACs. Since 2012, he has been with the School of Information and Communications, Gwangju Institute of Science and Technology, Gwangju, South Korea, where he is currently an Assistant Professor.

Dr. Lee received the 2007 Best Student Paper Award at the VLSI Circuits Symposium in Kyoto, Japan and the GIST Distinguished Lecture Award in 2015.

Kang-Yoon Lee (SM'10) received the B.S., M.S., and Ph.D. degrees in the School of Electrical Engineering from the School of Electrical Engineering, Seoul National University, Seoul, South Korea, in 1996, 1998, and 2003, respectively.

From 2003 to 2005, he was with the GCT Semiconductor Inc., San Jose, CA, USA, where he was a Manager of the Analog Division and worked on the design of CMOS frequency synthesizer for CDMA/PCS/PDC and single-chip CMOS RF chip sets for W-CDMA, WLAN, and PHS. From 2005 to 2011, he was with the Department of Electronics Engineering, Konkuk University, as an Associate Professor. Since 2012, he has been with the College of Information and Communication Engineering, Sungkyunkwan University, Suwon, South Korea, where he is currently an Associate Professor. His research interests include implementation of power integrated circuits, CMOS RF transceiver, analog integrated circuits, and analog/digital mixed-mode VLSI system design.