A Single Phase AC/DC/AC Converter With Unified Ripple Power Decoupling

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***Abstract*—In single phase ac/dc/ac converters, the low frequency ripple powers exist both at the source and load sides. Usually, large dc-link filter components are used to buffer the ripple powers, which increases volume and weight. To overcome the drawback, this paper presents a single phase ac/dc/ac current source converter with unified ripple power decoupling. The converter only consists of three bridge arms and a decoupling circuit. The three bridge arms play the role of rectification and inversion with sharing a bridge arm. And the decoupling circuit is in series with the dc-link energy storage unit to buffer the ripple powers. The circuit configuration and operation principles are introduced first. Then, a modulation strategy based on Cartesian space is developed to achieve sinusoidal input and output currents. The control idea that the dc-link current is regulated by the decoupling circuit and the averaged decoupling capacitor voltage is maintained by the rectifier is adopted. The ripple power buffer is automatically achieved. Finally, the theoretical analysis is favorably verified by the simulations and experimental results.**

***Index Terms*—Asymmetrical half-bridge circuit (AHC), current source converter (CSC), controlled voltage source, power decoupling.**

NOMENCLATURE

C_d	Decoupling capacitor.
u_d	Voltage of decoupling capacitor.
L_{dc}	Dc-link inductor.
u_g	Grid voltage.
V_i	Amplitude of the grid voltage.
ω_i	Angular frequency of the grid voltage.
i_g	Grid current.
I_i	Amplitude of the grid current.
φ_i	Displacement angle between the grid voltage and current.
u_o	Load voltage.
V_o	Amplitude of the load voltage.
ω_o	Angular frequency of the load voltage.
i_o	Load current.
I_o	Amplitude of the grid current.
φ_o	Displacement angle between the load voltage and current.
φ_{io}	Initial displacement angle between the source voltage and load voltage.
L_g	Input filter inductor.
C_g	Input filter capacitor.
u_i	Voltage of the input filter capacitor.
i_{fi}	Averaged current before the rectifier.
i_{fo}	Averaged current after the inverter.
$\bar{p}_i$	Average power at the source side.
$\bar{p}_o$	Average power at the load side.
$\tilde{p}_i$	Ripple power at the source side.
$\tilde{p}_o$	Ripple power at the load side.
p_d	Power difference between the load side and source side.
p_{total}	Sum of the absolute values of ripple powers at the source and load sides.
$\bar{u}_o$	Dc component of the decoupling capacitor voltage.
$u_{d\max}$	Allowable maximum voltage across the decoupling capacitor.
$C_{d\min}$	Minimum value of the decoupling capacitor.
$\boldsymbol{I}_{ref}$	Reference current vector.
I_{ref}	Amplitude of $\boldsymbol{I}_{ref}$.
i_{dc}	Dc-link current.
d_m	Duty cycle of the former active vector.
d_m	Duty cycle of the latter active vector.
d_0	Duty cycle of the zero vector.
θ	Absolute angle between $\boldsymbol{I}_{ref}$ and the related vector.
u_{ab}	Equivalent voltage provided by the decoupling circuit.
d_d	Ratio between u_{ab} and u_d.
R	Load resistance.
L_o	Load inductance.
C_o	Output filter capacitor.
f_s	Switching frequency.

I. INTRODUCTION

SINGLE-PHASE ac/dc/ac converters, which provide variable output voltage and frequency, have been widely applied in line voltage regulators [1], universal active power filters [2], [3], uninterruptible power supplies [4], [5], active power compensator [6], [7], cascade converter cells for medium voltage systems [8], [9], and so on. However, the inherent low frequency ripple power in the single phase system will cause a noticeable fluctuation on the dc-link voltage/current, especially when the instantaneous powers of the source and

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load are seriously out of synchronization. Consequently, a large capacitor or inductor is required to limit the dc-link voltage/current ripple in an accepted range. That is, however, adverse to the power density or (and) lifetime [10], [11].

To reduce the volume of dc-link components, from the perspective of the control technique a possible solution is to synchronize the source power with the load power as much as possible [12]–[18]. The concept has been carried out in various circuit topologies, such as single-phase ac power supply configured with a front diode rectifier [12], single-phase to single-phase half-bridge converter [13], single-phase to single-phase full-bridge converter [14], six switches ac/dc/ac voltage source converter (VSC) [15], six switches ac/ac current source converter (CSC) [16], [17], and single-phase multistage solid state transformers system [18]. The required dc-link filter capacitance is minimized by power synchronization control. However, the same source/load frequencies and phases are mandatory, which restricts widespread applications of the converters. Since the required output voltage frequency and phase are dependent on the loads in most cases, such as speed control of a fan, induction motor drive, and induction heating.

Another solution is the active-power decoupling method (APDM), which has been widely investigated in single-phase rectifiers/inverters [19]–[37]. Its basic idea is to divert the power difference between input and output into additional passive component(s) with long lifetime and small volume. Then the adverse effects caused by the power mismatch are avoided. At first, simple bidirectional dc/dc circuits, such as buck [19], boost [20], [21], buck–boost [22], H-bridge [20], [23]–[27] circuits, are taken as the ripple ports to buffer the low frequency ripple power. They are in parallel [19]–[22] or series [23]–[27] with the dc-link and work independently with the original converters, which make the control realization easy. In the series decoupling concept, H-bridge circuit can be in series with the dc-link line [23]–[26] or with the dc-link capacitor [27]. Besides, in [26], another switching arm and an inductor are added to the H-bridge circuit to further reduce the decoupling capacitance. Thereafter, to reduce the usage of the semiconductor devices, switching-multiplexing decoupling circuits, which share the active switches with the original circuit, are proposed [28]–[31]. Their drawbacks are the increased control complexity and voltage/current stresses. As research continues, other functions begin to be merged into the decoupling circuits [32]–[35]. In [32] the decoupling capacitor voltage is exploited to achieve the three-level conversion, and then, improve the efficiency. In [33] and [34], the decoupling circuit is cascaded with a diode rectifier and plays the role of power decoupling and power factor correction (PFC) functions. However, in both of them the output voltage is limited to half peak value of the grid voltage. Then, a single-stage two-switch PFC rectifier with wide output voltage range and ripple power decoupling is proposed [35]. However, the voltage of the decoupling capacitor has to be more than the sum of the grid voltage and the output voltage, which increases the voltage stress significantly. More decoupling circuits and the pros and cons of them can be found in [36] and [37].

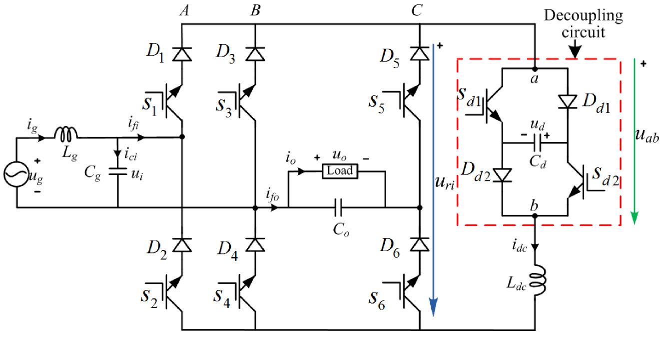
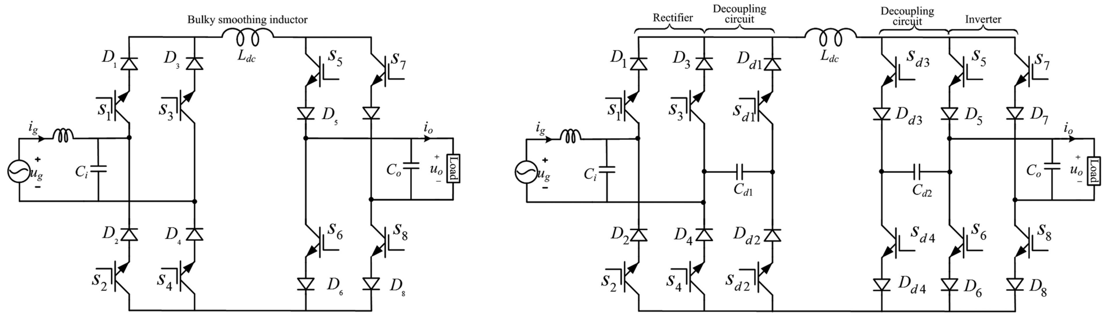


Fig. 1. Proposed single-phase ac/dc/ac CSC.

Literature [38] first introduced APDM to single-phase ac/dc/ac VSC and CSC under a preliminary condition that the source and load operate at the same frequency. Two sets of decoupling circuit are employed to respectively buffer the double ripple powers at the source and load sides. It can be viewed as a separate buffering method (SBM). However, this method may be not cost-effective and significant power losses are also introduced. This paper attempts to investigate the unified buffering method (UBM). It is carried out by employing a single decoupling circuit to buffer the power difference between the source and load. Compared with SBM, the proposed method costs less as a less decoupling circuit is required. In addition, it is more efficient because the power processed by the decoupling circuit in UBM is less than that in SBM.

With adopting UBM, the proposed single-phase ac/dc/ac converter is shown in Fig. 1. Three bridge arms are employed to achieve rectification and inversion. Therefore, it can be implemented by a three-phase inverter module, which reduces cost and size. The decoupling circuit is configured by inserting an asymmetrical half-bridge circuit (AHC) into the dc-link. It emulates the behavior of a large-size passive inductor to smooth the dc-link current. Compared with the conventional single-phase ac/dc/ac CSC, shown in Fig. 2(a), the count of the semiconductor devices is the same and one more film capacitor is increased to buffer the power difference. But the dc-link inductor in the proposed converter is much smaller. In addition, two less semiconductor devices are involved in the current path. Compared with the SBM proposed in [38] shown in Fig. 2(b), the proposed method costs less as four active switches, four diodes, and a decoupling capacitor are saved. Additionally, the proposed converter can achieve higher conversion efficiency because the dc-link current flows two less semiconductor devices and the power processed by the decoupling circuit is also smaller.

This paper first introduces the proposed circuit structure and its operation principles. Then the power difference between the source and load are analyzed under different operation conditions. It reveals that the decoupling capacitor voltage can be much different under various operation conditions, which brings a challenge for controller design. In this paper the decoupling circuit is taken as a controlled voltage source to keep the voltage-second balance of the dc-link inductor. Then, the dc-link current can be smooth and the ripple power buffer is automatically achieved. Finally, the simulations and experimental tests were conducted to verify the effectiveness of the proposed converter and control method.



(a) (b)

Fig. 2. Single-phase ac/dc/ac CSCs. (a) Conditional circuit structure with a bulky dc-link inductor. (b) Proposed circuit in [38] with two sets of decoupling circuits.

II. CIRCUIT CONFIGURATION AND OPERATION PRINCIPLES

A. Circuit Configuration

Fig. 1 shows the configuration of the proposed single-phase ac/dc/ac CSC. It consists of three switching bridge arms and a decoupling circuit. The bridge arms A and B form the rectifier, and the bridge arms B and C form the inverter. The decoupling circuit is composed of two active switches (S_{d1}, S_{d2}), two diodes (D_{d1}, D_{d2}), and a film capacitor C_d. The film capacitor is used to buffer the power difference between the source and load, and the decoupling capacitor voltage u_d is always positive. Then a small dc-link inductor $L_{\rm dc}$ is enough to filter high frequency switching harmonics.

B. Operation States

To avoid open-circuit of the dc-link inductor current, for the three bridge arms there are nine feasible switching states, as shown in Fig. 3. They can be classified to four groups. The first group consists of states 1 and 2, in which the input current is synthesized and the load is bypassed. The second group is composed of states 3 and 4, in which the output current is synthesized and the grid is disconnected. The third group includes states 5 and 6, in which the input current and output current are synthesized simultaneously. The last group contains states 7, 8, and 9, which are used for free-wheeling. The effects of different switching states on currents i_{fi} and i_{fo} are summarized in Table I.

As for the decoupling circuit, it has three operation states, i.e., charging C_d (S_{d1} and S_{d2} are turned OFF), discharging C_d (S_{d1} and S_{d2} are turned ON), and bypassing C_d (S_{d1} (S_{d2}) is turned ON and S_{d2} (S_{d1}) is turned OFF).

III. POWER DIFFERENCE AND DECOUPLING CAPACITOR VOLTAGE

A. Power Difference

In this paper, a linear resistance–inductance load is employed. The voltage and current in rectifier and inverter are given by

$$u_g = V_i \cos(\omega_i t) \tag{1-1}$$

$$i_g = I_i \cos(\omega_i t + \varphi_i) \tag{1-2}$$

$$u_o = V_o \cos(\omega_o t + \varphi_{io}) \tag{2-1}$$

$$i_o = I_o \cos(\omega_o t + \varphi_{io} + \varphi_o) \tag{2-2}$$

where V_i and I_i (V_o and I_o) are respectively the amplitudes of source (load) ac voltage and current, ω_i and ω_o are the source and load angular frequencies, φ_i and φ_o are the displacement angles, and φ_{io} is the initial displacement angle between the source voltage and load voltage.

As the filter inductor L_g is small, the filter capacitor voltage u_i is approximatively equals to the source ac voltage u_g, then the averaged current before the rectifier i_{fi} is

$$i_{fi} = i_g - i_{ci} \ = I_i \cos(\omega_i t + \varphi_i) + V_i C_g \omega_i \sin(\omega_i t) . \tag{3}$$

Then the power processed by the rectifier can be obtained

$$p_i = u_i i_{fi} = \underbrace{V_i I_i \cos(\varphi_i)/2}_{\bar{P}_i} + \underbrace{V_i I_i \cos(2\omega_i t + \varphi_i)/2 + \omega_i C_g V_i{}^2 \sin(2\omega_i t)/2}_{\tilde{p}_i} . \tag{4}$$

Similarly, the power processed by the inverter is expressed as

$$p_o = u_o i_{fo} = \underbrace{V_o I_o \cos(\varphi_o)/2}_{\bar{P}_o} + \underbrace{V_o I_o \cos(2\omega_o t + 2\varphi_{io} + \varphi_o)/2 - \omega_o C_o V_o{}^2 \sin(2\omega_o t + 2\varphi_{io})/2}_{\tilde{p}_o} . \tag{5}$$

In (4) and (5), $\bar{p}_i$ (over the line period) and $\bar{p}_o$ (over the load period) are average powers; and $\tilde{p}_i$ and $\tilde{p}_o$ are ripple powers.

Assuming that the power converter is lossless and the power difference P_d is completely absorbed by the decoupling capacitor C_d. Then, according to power balance and (4) and (5), the

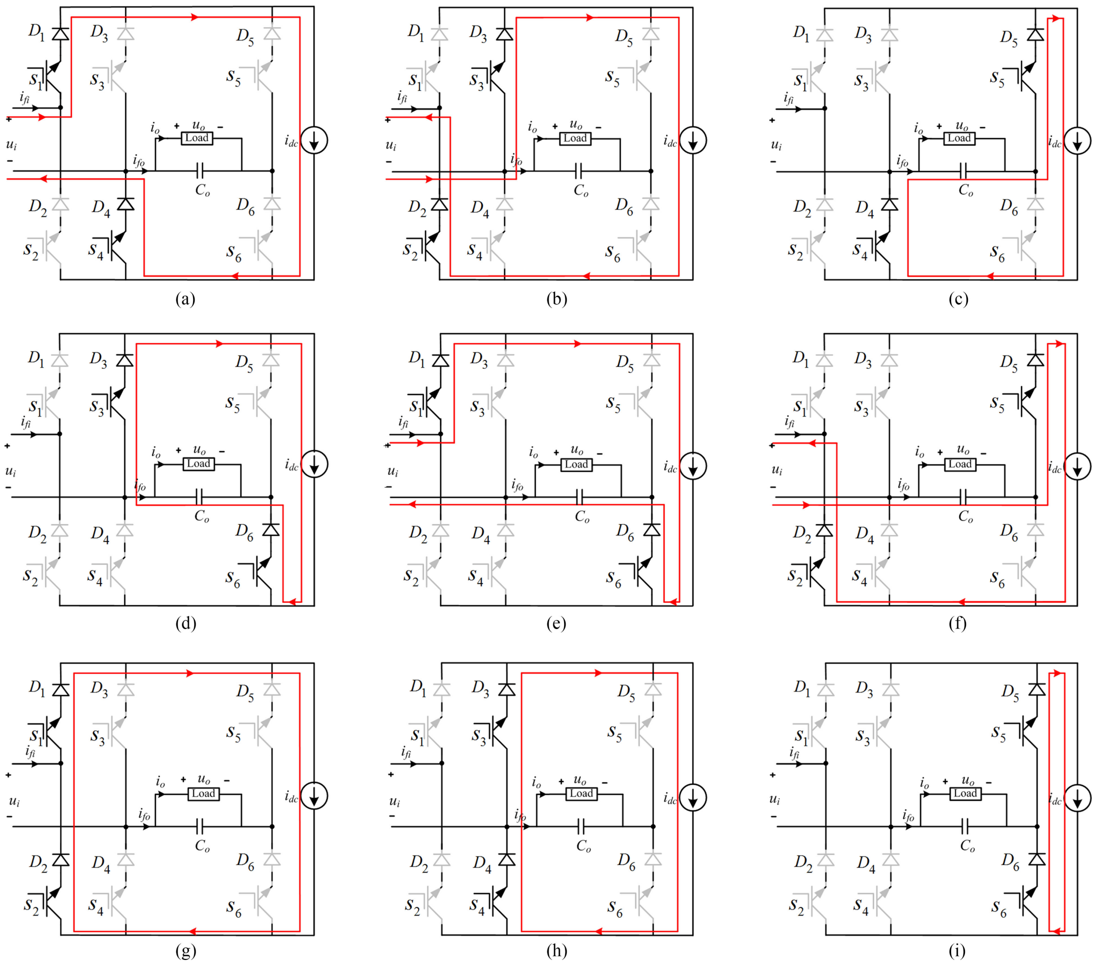


Fig. 3. Switching states for the three switching arms. (a) State 1. (b) State 2. (c) State 3. (d) State 4. (e) State 5. (f) State 6. (g) State 7. (h) State 8. (i) State 9.

TABLE I
SWITCHING STATES AND CURRENTS

Switching states		i_{fi}	i_{fo}
Group 1	1	i_{dc}	0
	2	$-i_{dc}$	0
Group 2	3	0	i_{dc}
	4	0	$-i_{dc}$
Group 3	5	i_{dc}	$-i_{dc}$
	6	$-i_{dc}$	i_{dc}
Group 4	7, 8, 9	0	0

average power and ripple power can be separately expressed as

$$\bar{P}_i = \bar{P}_o \tag{6}$$

$$\begin{aligned} p_d &= \tilde{p}_o - \tilde{p}_i \\ &= \frac{V_o I_o \cos\left(2\omega_o t + 2\varphi_{io} + \varphi_o\right) - V_i I_i \cos\left(2\omega_i t + \varphi_i\right)}{2} \\ &\quad - \frac{\omega_o C_o {V_o}^2 \sin\left(2\omega_o t + 2\varphi_{io}\right) + \omega_i C_g {V_i}^2 \sin\left(2\omega_i t\right)}{2}. \end{aligned} \tag{7}$$

From (7), if the source/load frequencies are the same, the power difference P_d can be minimized by choosing a proper value of φ_{io}. This is the basic principle of reducing dc-link capacitor in [12]–[18]. However, if the initial displacement angle φ_{io} is not a free degree [7], [8] or the source/load frequencies are different [39], [40], this method fails. Then, APDM may be more appropriate.

On the other hand, by using SBM [38], the total ripple power processed by the two sets of decoupling circuits is

$$p_{\text{total}} = |\tilde{p}_i| + |\tilde{p}_o| \tag{8}$$

where "||"denotes the absolute value sign. According to triangle inequality theorem, p_{total} is always more than $|p_d|$. That means the power proceed by SBM is always larger than that proceed by UBM and more power losses are introduced.

B. Decoupling Capacitor Voltage

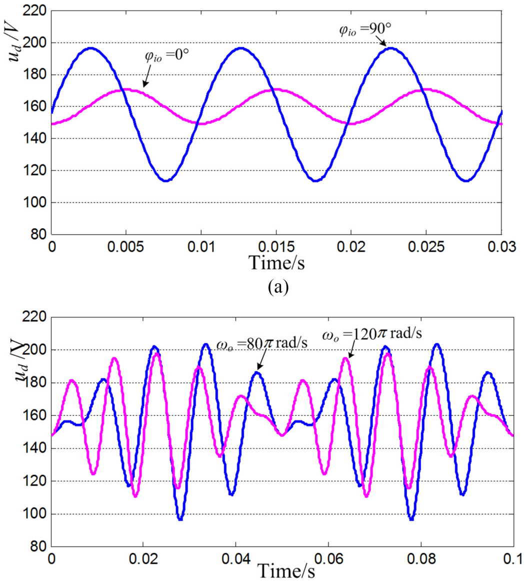
The dynamic differential equation for C_d is

$$C_d \frac{du_d}{dt} u_d = -p_d. \tag{9}$$

By integrating both sides of (8) with respect to time, u_d is expressed as (10) shown at the bottom of the next page.

The derivation is given in Appendix A.

Waveforms of u_d are illustrated in Fig. 4 under various operation conditions with the parameters in Table IV. As can be seen, even if the power level is identical, the waveforms of the decoupling capacitor voltage are quite different. That brings a



(a)

(b)

Fig. 4. Waveforms of u_d under different operation conditions: (a) $\omega_i = \omega_o = 100\,\pi$rad/s with $\varphi_{io} = 0$ and $\varphi_{io} = 90°$. (b) $\omega_i = 100\,\pi$rad/s with $\omega_o = 80\,\pi$ and 120 πrad/s.

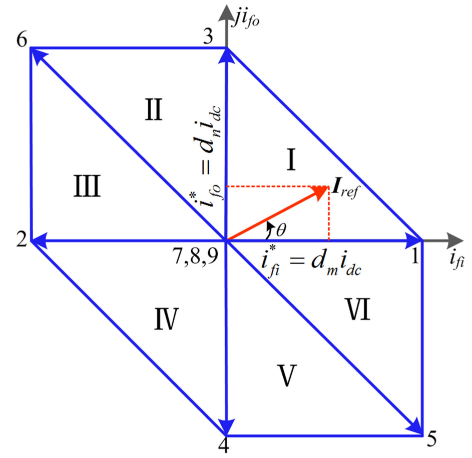


Fig. 5. Vectors for the three bridge arms.

challenge when designing the controller of the decoupling capacitor voltage.

On the other hand, once the allowable maximum voltage $u_{d\max}$ is given, the minimum value of C_d is

$$C_{d\min} = \frac{2}{u_{d\max}^2}\left(\sqrt{\left(\frac{V_iI_i}{2\omega_i}\right)^2 + \left(\frac{C_gV_i{}^2}{2}\right)^2 - \frac{C_gV_i{}^3I_i}{2\omega_i}\sin(\varphi_i)} + \sqrt{\left(\frac{V_oI_o}{2\omega_o}\right)^2 + \left(\frac{C_oV_o{}^2}{2}\right)^2 + \frac{C_oV_o{}^3I_o}{2\omega_o}\sin(\varphi_o)}\right). \tag{11}$$

The derivation is given in Appendix B. It can be found that there is a tradeoff between the voltage stress and size of the capacitor. A comprehensive consideration should be taken into account when selecting the value of the capacitor.

IV. MODULATION

A. Modulation Strategy for Three Bridge Arms

Nine vectors by using Cartesian space (i_{fi}, ji_{fo}), shown in Fig. 5, are obtained according to the nine switching states listed in Table I. The expected reference current (i^*_{fi}, ji^*_{fo}) is synthesized by its two adjacent vectors and a zero vector. The principle of selecting the zero vectors is to minimize the switching count. For example, if the reference current $I_{\text{ref}} = i^*_{fi} + ji^*_{fo}$ is located in the sector I, vectors (states) 1, 3, and 8 will be used. The corresponding duty cycles can be expressed as follows:

$$\begin{cases} d_m = i^*_{fi}/i_{\text{dc}} \\ d_n = i^*_{fo}/i_{\text{dc}} \\ d_0 = 1 - d_m - d_n \end{cases} \tag{12}$$

where d_m, d_n, and d_0 are the duty cycles of the vectors 1, 2, and 8, respectively. Similarly, if $\boldsymbol{I}_{ref}$ is located in the other sectors, the corresponding duty cycles could also be obtained in the same way. The duty ration in each sector is summarized in Table II. θ is the absolute angle between $\boldsymbol{I}_{ref}$ and the related vector and calculated by

$$\theta = \begin{cases} \text{atan2}(i^*_{fi}/i^*_{fo}), & \text{sector I} \\ \text{atan2}(i^*_{fi}/i^*_{fo}) - \dfrac{\pi}{2}, & \text{sector II} \\ \text{atan2}(i^*_{fi}/i^*_{fo}) - \dfrac{3\pi}{4}, & \text{sector III} \\ \text{atan2}(i^*_{fi}/i^*_{fo}) + \pi, & \text{sector IV} \\ \text{atan2}(i^*_{fi}/i^*_{fo}) + \dfrac{\pi}{2}, & \text{sector V} \\ \text{atan2}(i^*_{fi}/i^*_{fo}) + \dfrac{\pi}{4}, & \text{sector VI} \end{cases} \tag{13}$$

where atan2() is the arctangent function with two arguments and varies from $-\pi$ to π. And I_{ref} is the amplitude of $\boldsymbol{I}_{ref}$ and expressed as

$$I_{\text{ref}} = \sqrt{i^{*2}_{fi} + i^{*2}_{fo}}. \tag{14}$$

$$\begin{cases} u_d = \sqrt{\bar{u}_0^2 + \sqrt{A^2+B^2-2AB\sin(\varphi_i)}\sin(2\omega_i t+\gamma_1) - \sqrt{C^2+D^2+2CD\sin(\varphi_o)}\sin(2\omega_o t+2\varphi_{io}+\gamma_2)} \\ A = \frac{V_iI_i}{2\omega_iC_d}, B = \frac{C_gV_i{}^2}{2C_d}, C = \frac{V_oI_o}{2\omega_oC_d}, D = \frac{C_oV_o{}^2}{2C_d} \\ \gamma_1 = \arctan\frac{V_iI_i\sin(\varphi_i) - \omega_iC_gV_i{}^2}{V_iI_i\cos(\varphi_i)}, \gamma_2 = \arctan\frac{V_oI_o\sin(\varphi_o) + \omega_oC_oV_o{}^2}{V_oI_o\cos(\varphi_o)} \end{cases} \tag{10}$$

TABLE II
DUTY RATIOS IN EACH SECTOR

Sector	Conditions	d_m	d_n	Selected zero sector	Constraints
I $(0 \sim \pi/2)$	$i^*_{fi} \geq 0, i^*_{fo} > 0$	$\frac{i^*_{fi}}{i_{dc}}$	$\frac{i^*_{fo}}{i_{dc}}$	8	$i^*_{fi} + i^*_{fo} \leq i_{dc}$
II $(\pi/2 \sim 3\pi/4)$	$i^*_{fi} < 0, i^*_{fo} > 0, i^*_{fo} > \lvert i^*_{fi} \rvert$	$\frac{\sqrt{2} I_{ref} \sin(\frac{\pi}{4} - \theta)}{i_{dc}}$	$\frac{I_{ref} \sin \theta}{i_{dc}}$	9	$i^*_{fo} \leq i_{dc}$
III $(3\pi/4 \sim \pi)$	$i^*_{fi} < 0, i^*_{fo} > 0, i^*_{fo} < \lvert i^*_{fi} \rvert$	$\frac{I_{ref} \sin(\frac{\pi}{4} - \theta)}{i_{dc}}$	$\frac{\sqrt{2} I_{ref} \sin \theta}{i_{dc}}$	7	$-i^*_{fi} \leq i_{dc}$
IV $(\pi \sim 3\pi/2)$	$i^*_{fi} \leq 0, i^*_{fo} \leq 0$	$\frac{i^*_{fi}}{i_{dc}}$	$\frac{i^*_{fo}}{i_{dc}}$	8	$-(i^*_{fi} + i^*_{fo}) \leq i_{dc}$
V $(3\pi/2 \sim 7\pi/4)$	$i^*_{fi} > 0, i^*_{fo} \leq 0, \lvert i^*_{fo} \rvert > i^*_{fi}$	$\frac{\sqrt{2} I_{ref} \sin(\frac{\pi}{4} - \theta)}{i_{dc}}$	$\frac{I_{ref} \sin \theta}{i_{dc}}$	9	$-i^*_{fo} \leq i_{dc}$
VI $(7\pi/4 \sim 2\pi)$	$i^*_{fi} > 0, i^*_{fo} \leq 0, \lvert i^*_{fo} \rvert < i^*_{fi}$	$\frac{I_{ref} \sin(\frac{\pi}{4} - \theta)}{i_{dc}}$	$\frac{\sqrt{2} I_{ref} \sin \theta}{i_{dc}}$	7	$i^*_{fi} \leq i_{dc}$

Note that I_{ref} is time-varying.

From Fig. 5, nine vectors form a hexagon. The loci (i^*_{fi}, ji^*_{fo}) should not be beyond the hexagon to work in linear modulation region. When the loci lies in sector I, the following operation constraint should be satisfied:

$$i_{\text{dc}} \geq i^*_{fi} + i^*_{fo} = I^*_i \cos(\omega_i t) + I^*_o \cos(\omega_o t + \varphi_{12}) \tag{15}$$

where I^*_i and I^*_o are the amplitude references, and φ_{12} is the initial displacement angle between i^*_{fi} and i^*_{fo}. The detailed derivation can be seen in Appendix C. For other sectors, the operation constrains can be similarly analyzed and the results are summarized in Table II.

Then, a uniform expression for the operation constraints is obtained as follows:

$$\begin{cases} i_{\text{dc}} \geq \left| i^*_{fi} + i^*_{fo} \right| = \left| I^*_i \cos(\omega_i t) + I^*_o \cos(\omega_o t + \varphi_{12}) \right| \\ i_{\text{dc}} \geq I^*_i, I^*_o \end{cases}. \tag{16}$$

After further simplification, we have

$$\begin{cases} i_{\text{dc}} \geq I^*_i + I^*_o, & \omega_i \neq \omega_o \\ \begin{cases} i_{\text{dc}} \geq \sqrt{I^{*2}_i + I^{*2}_o + 2\cos(\varphi_{12}) I^*_i I^*_o} \\ i_{\text{dc}} \geq I^*_i, I^*_o \end{cases}, & \omega_i = \omega_o \end{cases}. \tag{17}$$

The derivation is given in Appendix D. To reduce power losses and switching stress, i_{dc} should be minimized. In practice it is selected according to (17) with a proper margin.

B. Modulation Strategy for Decoupling Circuit

Regarding to the decoupling circuit, the required operation states are determined by u_{ab}. u_{ab} is an equivalent voltage provided by the decoupling circuit to keep the voltage-second balance of the dc-link inductor. When $u_{ab} > 0$, charging and bypassing states will be selected and when $u_{ab} \leq 0$, discharging and bypassing states will be selected. The duty ratios d_{d1} and d_{d2} of switching S_{d1} and S_{d2} are summarized in Table III. $d_d = u_{ab}/u_d$ is a variable that can be positive or negative. Fig. 6 shows a specific switching pattern of S_{d1} and S_{d2} when the source and load frequencies are 50 and 60 Hz, respectively.

TABLE III
DUTY RATIOS OF THE DECOUPLING CIRCUIT

Cases	d_{d1}	d_{d2}
$d_d = u_{ab}/u_d > 0$	$1 - d_d$	0
$d_d = u_{ab}/u_d < 0$	1	$-d_d$

TABLE IV
PARAMETERS USED IN ANALYSIS, SIMULATION, AND EXPERIMENT

Parameters	Symbol	Value
Input phase voltage	V_i	110 $\sqrt{2}$ V
Output phase voltage	V_o	63 $\sqrt{2}$~122 $\sqrt{2}$ V
Source angular frequency	ω_i	314 rad/s
Input filters	L_i/C_i	0.6 mH/10 uF
DC-link filter inductor	L_{dc}	5 mH
Output filters	C_o	10 uF
Active buffer capacitor	C_d	100 μF
Load	R/L_o	50 Ω/0.6 mH
Switching frequency	f_s	20 kHz

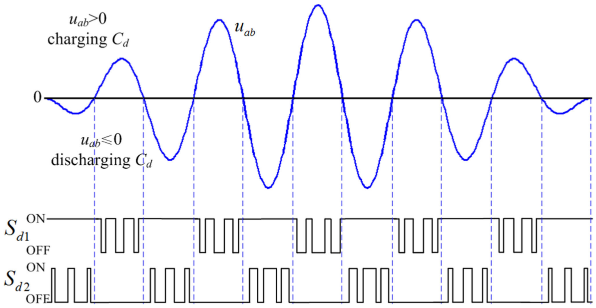


Fig. 6. Switching operations of S_{d1} and S_{d2}.

V. MODEL AND CONTROL

A. System Model

According to Fig. 1, the average model of the rectifier over one switching period is formulated as follows:

$$L_g \frac{di_g}{dt} = u_g - u_i \tag{18}$$

$$C_g \frac{du_i}{dt} = i_g - i_{fi}. \tag{19}$$

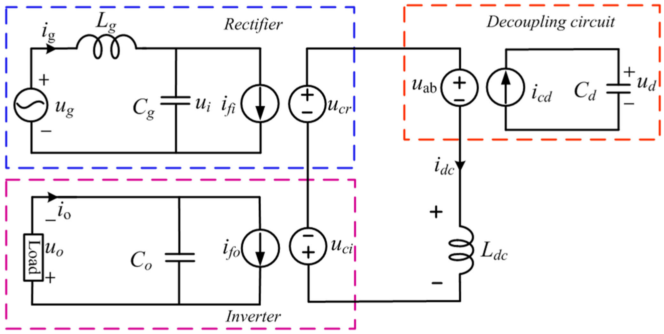


Fig. 7. Equivalent circuit model of the proposed converter.

For the inverter, we obtain

$$C_o \frac{du_o}{dt} = i_{fo} - i_o. \tag{20}$$

And for the decoupling circuit, the average differential equation of the capacitor voltage is rewritten as

$$C_d \frac{du_d}{dt} = d_d i_{\mathrm{dc}}. \tag{21}$$

Then according to the basic Kirchhoff's voltage law (KVL), the dc-link dynamics can be described by the following differential equation:

$$\begin{cases} L_{\mathrm{dc}} \dfrac{di_{\mathrm{dc}}}{dt} = u_{ri} - u_{ab} \\ u_{ri} = \underbrace{u_i i_{fi}/i_{\mathrm{dc}}}_{u_{cr}} - \underbrace{u_o i_{fo}/i_{\mathrm{dc}}}_{u_{ci}} \end{cases}. \tag{22}$$

According to (18)–(22), the equivalent circuit of the proposed converter is shown in Fig. 7.

B. Controller Design

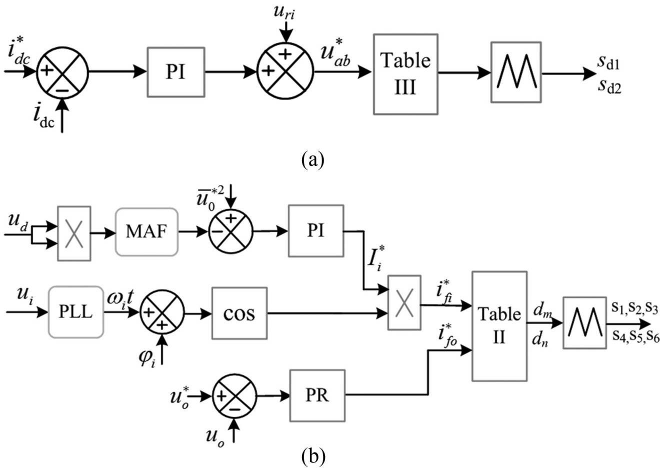
1) DC-Link Current Regulation: The dc-link current presents low frequency oscillation if the power difference is not completely absorbed by the decoupling circuit. From (22) and Fig. 7, voltages u_{cr}, u_{ci}, and u_{ab} can be used to regulate the dc-link current i_{dc}. If u_{cr} or u_{ci} is taken as the control input, the dynamic response of the dc-link regulation loop cannot be very fast to avoid deteriorating the grid current or load current. Therefore, u_{ab} is taken as the control input and u_{cr} and u_{ci} are viewed as the disturbances.

Here, the control idea of combining a proportional-integral (PI) controller with a feedforward is adopted. The PI compensator is employed to track the dc-link current reference and the feedforward is used to compensate the distortion u_{ri}. Then, according to the internal model principle, zero error tracking can be achieved. Then, the control input u_{ab} is designed as

$$u_{ab}^* = \left(k_p + \frac{k_i}{s}\right) e + u_{ri} \tag{23}$$

where $e = i_{\mathrm{dc}}^* - i_{\mathrm{dc}}$. u_{ri} is the feedforward and obtained according to (22). Submitting (23) into (22) leads to

$$L_{\mathrm{dc}} \frac{de}{dt} = \left(k_p + \frac{k_i}{s}\right) e. \tag{24}$$



(a)

(b)

Fig. 8. Block diagram of the control scheme. (a) Dc-link current regulation. (b) Decoupling capacitor voltage and output voltage regulation.

Apparently, k_p and k_i should be less than zero to ensure stability. Then, according to Table III the duty ratios of the switches in the decoupling circuit can be obtained. The control block is shown in Fig. 8(a). Note that once the dc-link current is well regulated the ripple power will be automatically buffered by the decoupling circuit. That is because the residual ripple power will be imposed on the dc-link inductor L_{dc} and cause a dc-link current distortion. Therefore, the dc-link current error can be taken as an indicator to reflect the decoupling effect, which has been well stated in [31], [32], [35], and [41].

2) Decoupling Capacitor Voltage Regulation: The decoupling circuit is taken as a controlled voltage source to provide expected u_{ab}. As a result, the decoupling capacitor voltage swings to absorb and release the low frequency ripple power periodically. It works like an active power filter and consumes no power in theory. However, the power losses will decay decoupling capacitor voltage. Therefore, the dc component of the decoupling capacitor voltage is maintained at a given voltage by controlling the input active power [31], [32], [35], and [41].

According to (9), one has

$$C_d \frac{dx}{dt} = 2\left(p_i - p_o\right) \tag{25}$$

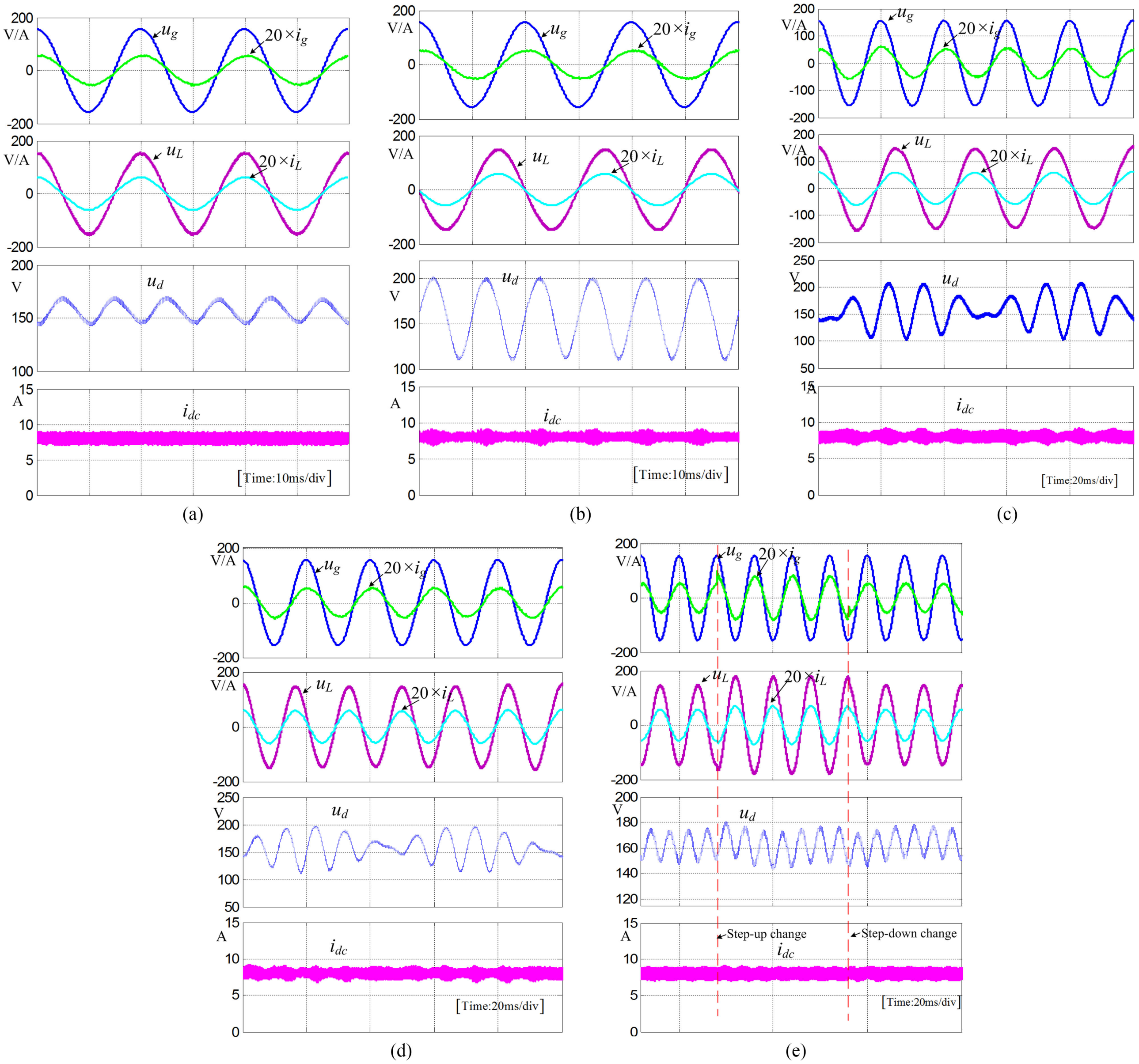
where $x = u_d^2$. The right side of (25) is a periodic function. The periodic averaging method is used to facilitate the control design. The average differential equation is written as

$$C_d \frac{d\bar{x}}{dt} = V_i I_i \cos\left(\varphi_i\right) - \bar{P}_o \tag{26}$$

where $\bar{x}$ is obtained by a moving average filter and can be described in continuous-time domain by

$$\bar{x} = \frac{1}{T_\omega} \int_{t-T_\omega}^{t} x(t)dt \tag{27}$$

where T_ω is referred to as the window length. In practice, it is selected to be the period of u_d. Form (26), I_i is selected to be the control variable to maintain the dc component of the decoupling capacitor voltage. As (26) is a linear first-order differential equation, a PI controller is adopted. The input current



(a) (b) (c)

(d) (e)

Fig. 9. Simulation results. (a) $\omega_i = \omega_o = 100\ \pi$rad/s, $\varphi_{io} = 0$. (b) $\omega_i = \omega_o = 100\ \pi$rad/s, $\varphi_{io} = 90°$. (c) $\omega_i = 100\ \pi$rad/s and $\omega_o = 80\ \pi$rad/s. (d) $\omega_i = 100\ \pi$rad/s and $\omega_o = 120\ \pi$rad/s. (e) Dynamic simulation results.

reference is obtained by multiplying I_i^* with the phase information $(\omega_i t + \varphi_i)$, which is obtained though a phase-locked loop. The control block is shown in Fig. 8(b).

Note that when the system starts up the decoupling capacitor voltage is first charged to its dc component to ensure normal operation. When the system shuts down the open-circuit of the dc-link current must be avoided.

3) Output Voltage Regulation: As for the inverter, the periodic controller (such as proportional resonant (PR) controller, repetitive control, or learning control) should be used to track the sinusoidal output voltage [42], [43]. Here, the PR controller is adopted. It is described by

$$G(s) = k_{p1} + \frac{2k_{i1}\omega_c s}{s + 2\omega_c s + \omega_o^2} \tag{28}$$

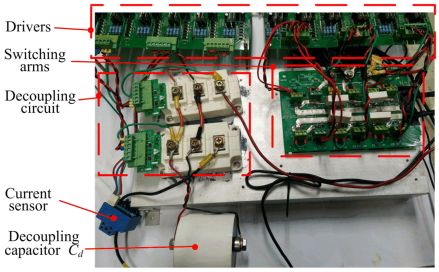
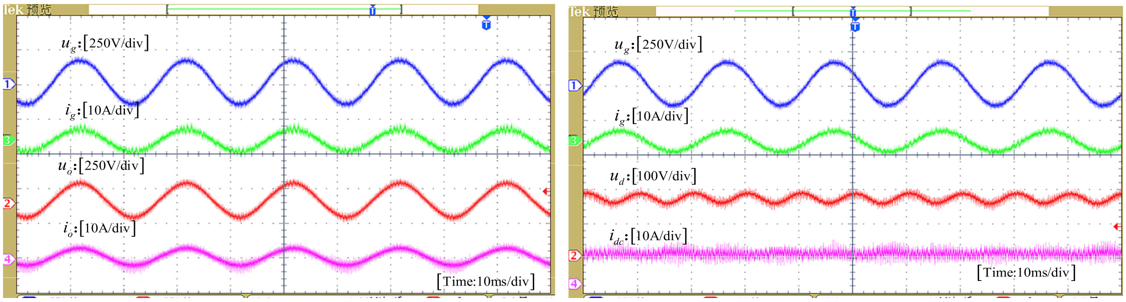


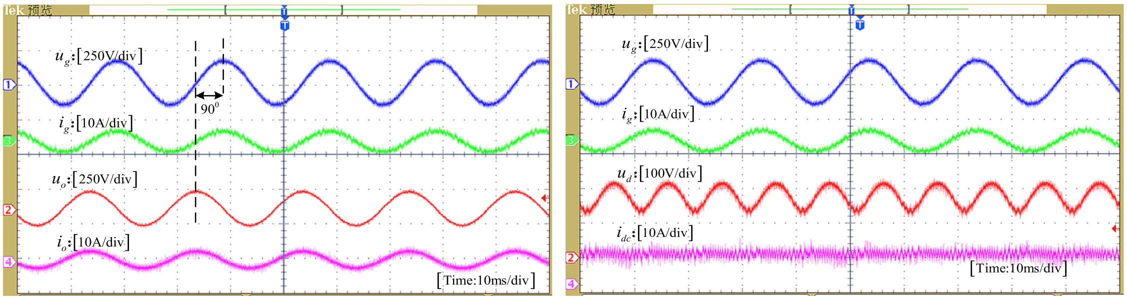
Fig. 10. Experimental prototype.

where ω_c is -3-dB cut-off frequency. The output of the PR regulator is taken as the current reference i_o^*. Then, according to Table II the duty ratios of the three bridge arms are obtained.



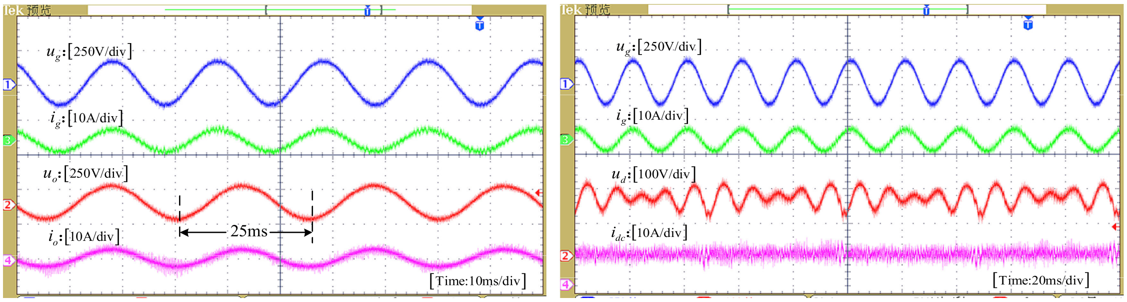
(a) (b)

Fig. 11. Experimental results with the same source and load frequencies (50 Hz) and $\varphi_{io} = 0$. (a) Input and output voltages and currents. (b) Decoupling capacitor voltage and dc-link current.



(a) (b)

Fig. 12. Experimental results with the same source and load frequencies (50 Hz) and $\varphi_{io} = 90°$. (a) Input and output voltages and currents. (b) Decoupling capacitor voltage and dc-link current.



(a) (b)

Fig. 13. Experimental results with 50-Hz source frequency and 40 Hz load frequency. (a) Input and output voltages and currents. (b) Decoupling capacitor voltage and dc-link current.

Note that the designed controller is based on the linear load. For the nonlinear load, other nonlinear control methods such as repetitive control and sliding mode control could be considered.

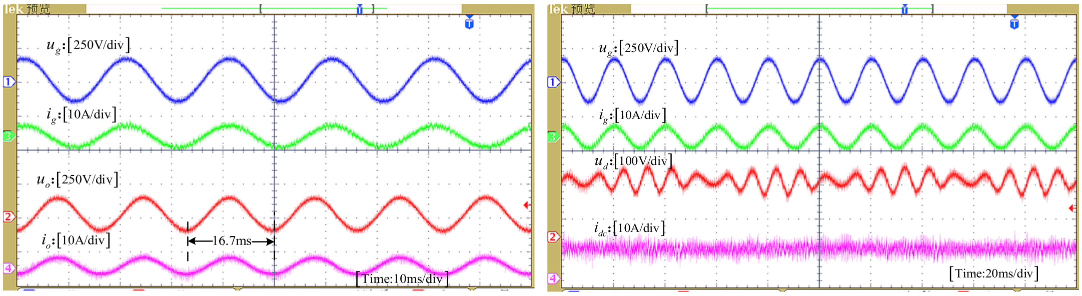
VI. SIMULATIONS AND EXPERIMENTAL RESULTS

A. *Simulations Results*

Numerical simulations were carried out in MATLAB/Simulink environment with the circuit parameters listed in Table IV. When selecting the value of L_{dc} maintaining the dc-link current ripple inside an acceptable range is the main consideration. However, the analytical expression of the maximum current ripple is hard to solve. So the inductor value is determined based on the simulation results. The average value of the decoupling capacitor voltage is selected to be 160 V. And the dc-link current reference is set to be 8 A. The simulation results under different conditions are shown in Fig. 9.

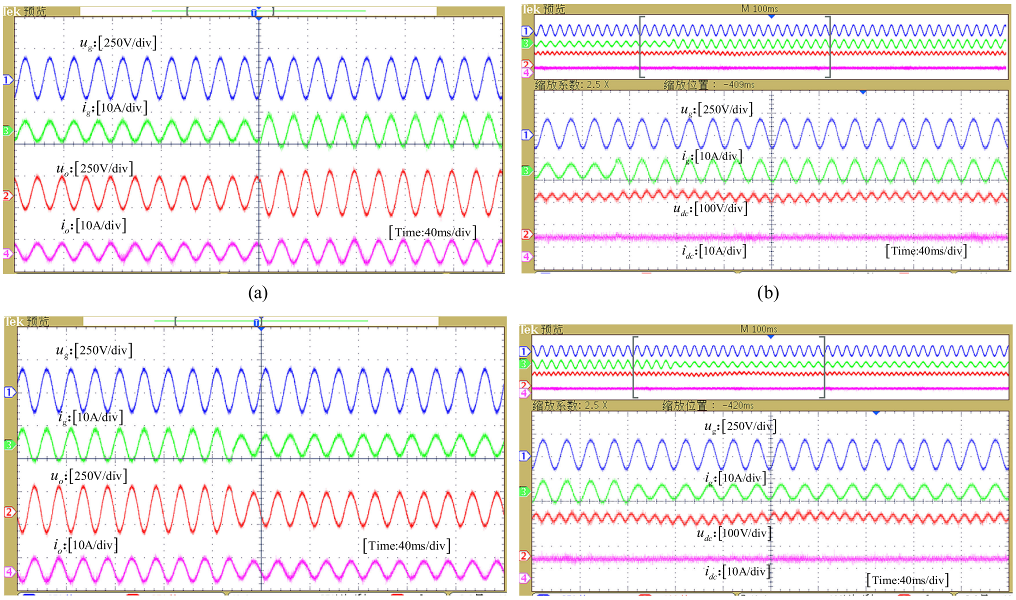
Fig. 9(a) and (b) show the steady-state results with the same source and load frequencies (50 Hz). The difference is that in Fig. 9(a) the initial displacement angle φ_{io} is 0 and in Fig. 9(b) it is 90°. As seen, the dc-link current i_{dc} is always constant with only switching frequency ripple. And the source and load currents are sinusoidal. The decoupling capacitor voltage in Fig. 9(b) has a larger swing than that in Fig. 9(a), which is in accordance with the theoretical analysis in Fig. 4(a).

Fig. 9(c) and (d) illustrate the simulation results when the source frequency is 50 Hz, and the load frequencies are 40 and 60 Hz, respectively. As can be seen, the dc-link current is



(a) (b)

Fig. 14. Experimental results with 50-Hz source frequency and 60-Hz load frequency. (a) Input and output voltages and currents. (b) Decoupling capacitor voltage and dc-link current.



(a) (b) (c) (d)

Fig. 15. Dynamic experimental waveforms. (a) Input and output waveforms when the load power is changed from 200 to 300 W. (b) Waveforms of decoupling capacitor voltage and dc-link current when the load power is changed from 200 to 300 W. (c) Input and output waveforms when the load power is changed from 300 to 200 W. (d) Waveforms of decoupling capacitor voltage and dc-link current when the load power is changed from 300 to 200 W.

still constant due to the adopted control method. In both cases the frequencies of the decoupling capacitor voltage are 10 Hz. And the waveforms are in good agreement with the theoretical analysis in Fig. 4(b). The result in Fig. 9(a)–(d) proves that even with the same power level, the decoupling capacitor voltage can be very different under different operation conditions. That is totally different from that in the single phase ac/dc rectifier or dc/ac inverter. Fig. 9(e) shows the dynamic response of the system when the load power is changed from 200 to 300 W and then back to 200 W. As seen, the transient process is smooth and no obvious distortions happen to the input current, the load current, and the dc-link current.

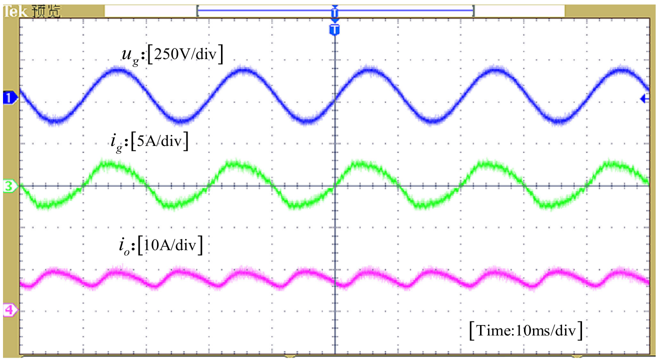
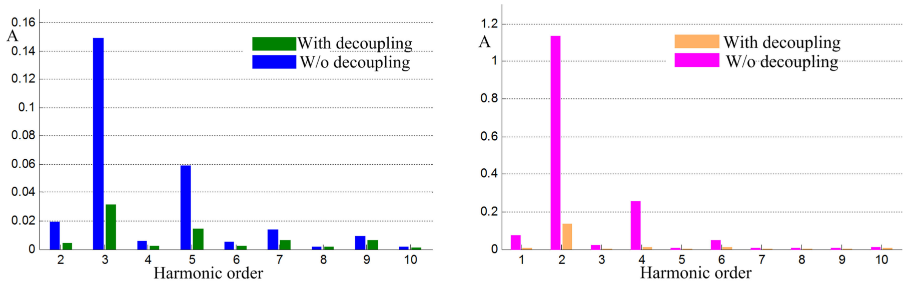


Fig. 16. Experimental results with removing the decoupling circuit.

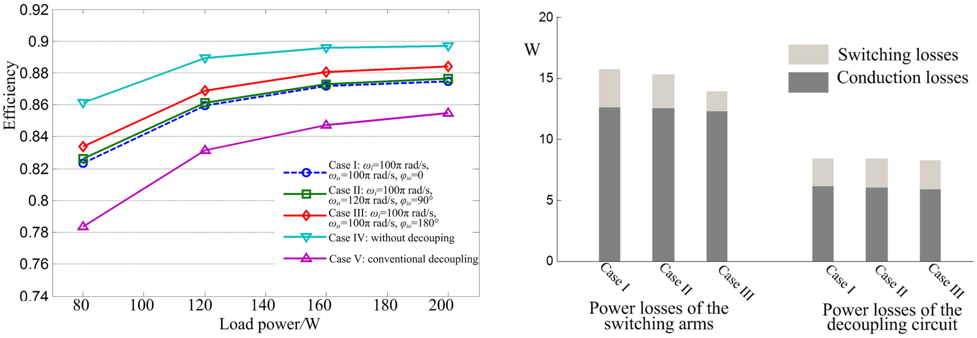
B. *Experimental Results*

A prototype for proposed converter was built in lab for experimental verification, as shown in Fig. 10. It is fabricated by using the components available in laboratory. The experimental parameters are the same as those in the simulation. The control of the converter was realized by a combination of digital signal processor TMS320F28335 and field programmable gate array FPGA EP2C8T144C8N.



(a) (b)

Fig. 17. Spectral analysis for (a) the grid current and (b) the dc-link current.



(a) (b)

Fig. 18. System efficiency and losses distribution. (a) Efficiency carves under different cases. (b) Loss distribution of the proposed circuit under different conditions when the load power is 200 W.

Figs. 11 and 12 show the experimental waveforms when the source and load frequency are the same. In Fig. 11, $\varphi_{io} = 0$. As seen, the dc-link current is constant and the load current is sinusoidal. The source current i_g is in phase with the source voltage u_g. Fig. 12 shows the waveforms when the source voltage leads the load voltage 90°. Under such case the power processed by the decoupling circuit is increased and the decoupling capacitor voltage has a larger swing. The experimental results are consistent with those simulation results in Fig. 9(a) and (b). With 40- and 60-Hz load frequencies the experiment waveforms are shown in Figs. 13 and 14. The waveforms are the same as those in Fig. 9(c) and (d). Fig. 15 shows the dynamic response of the system. The experimental results are in accordance with those in the simulation.

Fig. 16 shows the experimental waveforms with removing the decoupling circuit. The test was carried out based on the same source and load frequencies. And the dc-link current is regulated by controlling the rectifier. As seen, the dc-link current fluctuates at twice the grid frequency and its peak–peak value is up to about 4 A. Moreover, the grid current is distorted.

Fig. 17(a) shows the spectrum of the grid current with/without the decoupling circuit. And the harmonic currents with the decoupling circuit are much smaller than those without the decoupling circuit. Fig. 17(b) shows the spectrum of the dc-link current with/without the decoupling circuit. It is clear that there is a dramatic reduction of the rms of the second harmonic current when adopting the decoupling circuit (ratio to the dc component is 1.72%). To realize the same current ripple level with a large inductor, the required inductance is 109.2 mH.

Fig. 18(a) shows the efficiencies as a function of the load power. For the proposed circuit, the efficiencies under three conditions (case I: $\omega_i = 100\,\pi$rad/s, $\omega_o = 100\,\pi$rad/s, $\varphi_{io} = 0$; case II: $\omega_i = 100\,\pi$rad/s, $\omega_o = 120\,\pi$rad/s, $\varphi_{io} = 90^\circ$; and case III: $\omega_i = 100\,\pi$rad/s, $\omega_o = 100\,\pi$rad/s, $\varphi_{io} = 180^\circ$) were measured. Besides, the efficiencies without the decoupling circuit (case IV) and with the decoupling circuit proposed in [38] (case V) are given. It can be found that the efficiencies under cases I, II, and III increase successively. To reveal the reason, the loss distributions at rated power are evaluated by using piecewise linear electrical circuit simulation. The result is shown in Fig. 18(b). As seen, the power losses caused by the decoupling circuit (including switching losses and conduction losses) and the conduction losses caused by the switching arms are nearly the same for those three cases. But the switching losses of the switching arms decrease successively. That is mainly because the voltage stress between switching arms A and C $(|u_i + u_o|)$ is always enhanced in case I due to that the input voltage and load voltage are in phase. For case II, the voltage stress is enhanced when the polarities of u_i and u_o are the same and weakened when they are opposite. And, for case III, the voltage stress is always weakened due to that the input voltage and load voltage are out of phase. High voltage stresses lead to high switching losses and hence, the switching losses under those three cases decrease successively. When the decoupling circuit in the proposed circuit is removed (case IV), the efficiency is higher as the power losses caused by the decoupling circuit is saved. However, the dc-link current cannot be constant as the power difference between the source and load is imposed on the dc-link inductor.

On the other hand, the system efficiency in the proposed circuit is higher than that in [38] (case V) as two less semiconductor devices are involved in the current paths and two less switches operates at high frequency.

VII. CONCLUSION

This paper proposed a UBM to buffer the ripple powers in single-phase ac/dc/ac CSC. It is cost-effective and efficient. Only three bridge arms are used to achieve rectification and inversion and only a decoupling circuit is used to achieve ripple power decoupling. The operation principles of the proposed circuit are introduced in detail. A modulation method based on Cartesian space is developed to reduce the switching count and then the switching power losses. The power difference between the source and load is analyzed. And it is found that power difference varies with operation conditions, which is different from that in the single phase ac/dc rectifier or dc/ac inverter. The control concept that the decoupling circuit is directly used to regulate the dc-link current is adopted. The simulations and experimental results showed that the source and load currents are always sinusoidal and the dc-link current is well regulated to be constant under different operation conditions. The proposed method is suitable for applications where the grid and the load operate at the same frequency or not. Besides, the proposed method can also be extended to single-phase ac/dc/ac VSC with adopting suitable decoupling circuits. When a nonlinear load is connected, the controller should be redesigned carefully. The disadvantage is the higher dc-link current, which could be the sum of the peak values of the grid and load currents in the worst case.

APPENDIX

A. Derivation of (10)

Substituting (7) into (9) leads to

$$\begin{aligned}C_d\frac{du_d}{dt}u_d &= -p_d\\ &= \frac{\omega_o C_o {V_o}^2\sin(2\omega_o t+2\varphi_{io})+\omega_i C_g {V_i}^2\sin(2\omega_i t)}{2}\\ &\quad-\frac{V_o I_o\cos(2\omega_o t+2\varphi_{io}+\varphi_o)-V_i I_i\cos(2\omega_i t+\varphi_i)}{2}.\end{aligned}\tag{A1}$$

By integrating both sides of (A1) with respect to time, we have

$$\begin{aligned}u_d^2 = {}&\frac{-C_o {V_o}^2\cos(2\omega_o t+2\varphi_{io})}{2C_d}+\frac{-C_g {V_i}^2\cos(2\omega_i t)}{2C_d}\\ &+\frac{-V_o I_o\sin(2\omega_o t+2\varphi_{io}+\varphi_o)}{2\omega_o C_d}\\ &+\frac{V_i I_i\sin(2\omega_i t+\varphi_i)}{2\omega_i C_d}+\bar{u}_0^2\end{aligned}\tag{A2}$$

where $\bar{u}_0$ is the dc component of u_d. Then, u_d is expressed as (A3) shown at the bottom of this page.

To guarantee u_d is always positive $\bar{u}_0$ can be selected by (A4) shown at the bottom of this page.

B. Derivation of (11)

With considering the lower limit of $\bar{u}_0$ in (A4), the maximum u_d is expressed as

$$u_{d\max} = \sqrt{2\sqrt{A^2+B^2-2AB\sin(\varphi_i)}+2\sqrt{C^2+D^2+2CD\sin(\varphi_o)}}.\tag{A5}$$

In turn, if $u_{d\max}$ is given, according to (A3) shown at the bottom of this page, and (A5) the minimum value of C_d can be solved out

$$\begin{aligned}C_{d\min} &= \frac{2}{u_{d\max}^2}\left(\sqrt{\left(\frac{V_i I_i}{2\omega_i}\right)^2+\left(\frac{C_g {V_i}^2}{2}\right)^2-\frac{C_g {V_i}^3 I_i}{2\omega_i}\sin(\varphi_i)}\right.\\ &\quad\left.+\sqrt{\left(\frac{V_o I_o}{2\omega_o}\right)^2+\left(\frac{C_o {V_o}^2}{2}\right)^2+\frac{C_o {V_o}^3 I_o}{2\omega_o}\sin(\varphi_o)}\right).\end{aligned}\tag{A6}$$

C. Derivation of (15)

In sector I, according to the sine law, we have

$$\frac{I_{\text{ref\_max}}}{\sin(\pi/4)} = \frac{i_{\text{dc}}}{\sin(3\pi/4-\theta)}\tag{A7}$$

where $I_{\text{ref\_max}}$ is the maximum I_{ref} and obtained when the loci (i_{fi}^*, ji_{fo}^*) is located at the bound. To ensure the system works in linear modulation region, I_{ref} should be no more than $I_{\text{ref\_max}}$.

$$\begin{cases}u_d = \sqrt{\bar{u}_0^2+\sqrt{A^2+B^2-2AB\sin(\varphi_i)}\sin(2\omega_i t+\gamma_1)-\sqrt{C^2+D^2+2CD\sin(\varphi_o)}\sin(2\omega_o t+2\varphi_{io}+\gamma_2)}\\ A=\frac{V_i I_i}{2\omega_i C_d}, B=\frac{C_g {V_i}^2}{2C_d}, C=\frac{V_o I_o}{2\omega_o C_d}, D=\frac{C_o {V_o}^2}{2C_d}\\ \gamma_1=\arctan\frac{V_i I_i\sin(\varphi_i)-\omega_i C_g {V_i}^2}{V_i I_i\cos(\varphi_i)}, \gamma_2=\arctan\frac{V_o I_o\sin(\varphi_o)+\omega_o C_o {V_o}^2}{V_o I_o\cos(\varphi_o)}\end{cases}\tag{A3}$$

$$\sqrt{\sqrt{A^2+B^2-2AB\sin(\varphi_i)}+\sqrt{C^2+D^2+2CD\sin(\varphi_o)})}\le\bar{u}_0\tag{A4}$$

That yields

$$I_{\mathrm{ref}} = \sqrt{i_{fi}^{*2} + i_{fo}^{*2}} \le \frac{i_{\mathrm{dc}}}{\sqrt{2}\sin(3\pi/4 - \theta)}. \tag{A8}$$

As the absolute angle $\theta = \operatorname{atan2}(i_{fi}^{*}/i_{fo}^{*})$, its sine and cosine are expressed as

$$\sin(\theta) = \frac{i_{fo}^{*}}{\sqrt{i_{fi}^{*2} + i_{fo}^{*2}}}, \cos(\theta) = \frac{i_{fi}^{*}}{\sqrt{i_{fi}^{*2} + i_{fo}^{*2}}}. \tag{A9}$$

Substituting (A9) into (A8) leads to

$$i_{fi}^{*} + i_{fo}^{*} \le i_{\mathrm{dc}}. \tag{A10}$$

D. Derivation of (17)

Suppose

$$i_{\mathrm{dc}} \ge f(t) = \left| I_i^{*}\cos(\omega_i t) + I_o^{*}\cos(\omega_o t + \varphi_{12}) \right|. \tag{A11}$$

When $\omega_i \ne \omega_o$, the maximum value of *f*(*t*) is $I_i^{*} + I_o^{*}$. Then, (16) can be rewritten as

$$i_{\mathrm{dc}} \ge I_i^{*} + I_o^{*}. \tag{A12}$$

When $\omega_i = \omega_o$, $f(t)$ is rewritten as

$$\begin{cases} f(t) = \left| \sqrt{I_o^{*2} + I_i^{*2} + 2\cos(\varphi_{12}) I_o^{*} I_i^{*}} \cos(\omega_i t + \gamma) \right| \\ \gamma = \arctan \frac{I_o^{*}\sin(\varphi_{12})}{I_o^{*}\cos(\varphi_{12}) + I_i^{*}} \end{cases}. \tag{A13}$$

Then, (16) can be rewritten as

$$\begin{cases} i_{\mathrm{dc}} \ge \sqrt{I_i^{*2} + I_o^{*2} + 2\cos(\varphi_{12}) I_i^{*} I_o^{*}} \\ i_{\mathrm{dc}} \ge I_i^{*}, I_o^{*} \end{cases}. \tag{A14}$$

Finally, the relation between the dc-link current and the amplitudes of input and output currents can be expressed as

$$\begin{cases} i_{\mathrm{dc}} \ge I_i^{*} + I_o^{*}, & \omega_i \ne \omega_o \\ \begin{cases} i_{\mathrm{dc}} \ge \sqrt{I_i^{*2} + I_o^{*2} + 2\cos(\varphi_{12}) I_i^{*} I_o^{*}} \\ i_{\mathrm{dc}} \ge I_i^{*}, I_o^{*} \end{cases}, & \omega_i = \omega_o \end{cases}. \tag{A15}$$

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