A High Step-Up Ratio Soft-Switching DC–DC Converter for Interconnection of MVDC and HVDC Grids

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***Abstract*—DC grid technology is regarded as a promising solution for future electric networks integrating a great amount of renewable energies. It calls for high-efficiency dc–dc converters with high voltage step-up ratio to interconnect medium-voltage (MV) dc distribution grids and high-voltage (HV) dc transmission grids. This paper presents an isolated bidirectional soft-switching dc–dc converter combining two-level converters in parallel on the MV side and a modular multilevel converter (MMC) on the HV side. A dedicated control method of the proposed converter is presented. By the proposed method, a certain reactive current is injected into the MV side by the MMC to ensure soft-switching on the MV side. The proposed converter presents low power-semiconductor total device rating and low semiconductor losses over a wide power range at variable input and output voltages. Simulation of a 50 kV/400 kV, 400 MW converter is conducted to evaluate semiconductor losses and verify the validity of this work.**

***Index Terms*—DC–DC converter, high-voltage dc (HVDC), medium-voltage dc (MVDC), modular multilevel converter (MMC), soft switching.**

NOMENCLATURE

${}^1\hat{V}_p$	Magnitude of the fundamental-frequency component of the primary-side phase voltage.
i_{pq}	Magnitude of the reactive current on the primary side.
$\hat{I}_p$	Magnitude of the rated primary-side phase current.
$I_{F(\mathrm{AV})}$	Average ON-state current of the power-semiconductor device on the MV side in full-load situation.
$I_{F(\mathrm{AV})M}$	Maximum average ON-state current of the power-semiconductor device on the MV side.
$\hat{V}_{\mathrm{sa}}$	Peak value of the secondary-side phase voltage of "a" phase.
$\hat{V}_{\mathrm{sa,MMC}}$	Peak value of the phase voltage of "a" phase synthesized by submodules of the MMC.

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I. INTRODUCTION

COMPARED to the existing ac grids, the dc grids present several significant advantages such as high efficiency, high power density, flexibility, high controllability, no reactive power, free of bulky line-frequency transformer, etc. The dc grid technology is a promising solution to integrate a great amount of renewable energies and energy storage systems, which calls for more flexible and more controllable smart grids [1].

On transmission level, the voltage-source converter high-voltage direct-current (HVDC) transmission is an emerging technology to integrate large renewable power plants such as offshore wind farms. The world's first multiterminal HVDC grid has been built to integrate wind farms in [2]. On distribution level, medium-voltage dc (MVDC) grids are promising for the efficient connection of distributed renewable generations and storage [3]. To build up such dc grids, the MVDC–HVDC converter is one of the key components to interconnect MVDC distribution grids and HVDC transmission grids. The possible applications of such a converter are the interconnection of an MVDC collector grid of an offshore wind farm with an HVDC transmission line, and the interconnection of MVDC urban distribution grids with the HVDC transmission grids [4]. For the MVDC–HVDC converter, following characteristics are of concern:

1) high voltage step-up ratio;
2) variable input and output voltages in a certain range;
3) high power rating ranging from tens to hundreds of MW;
4) high efficiency;
5) high reliability which means component fault-tolerant capability [5].

In some applications, such as offshore wind farms, high power density is a crucial factor as well.

In the past years, numerous topologies of high power dc–dc converters including both nonisolated [6]–[17] and isolated [18]–[29] types have been proposed and discussed. For MVDC–HVDC power conversion where the voltage step-up ratio is high ($V_{\mathrm{dc,HV}}/V_{\mathrm{dc,MV}} > 5$), galvanic isolation is preferred not

only for safety but also to reduce power-semiconductor total device ratings and losses [18]. The existing isolated types can be classified into the input-series output-parallel (ISOP) converters based on isolated dc–dc building blocks [18]–[23] and the modular-multilevel-converter-based [30] front-to-front (MMC-FTF) converters [24]–[29].

For ISOP converters, the series resonant converter (SRC) [23] and the dual-active bridge (DAB) [18], [19] are most popular isolated dc–dc building blocks. The SRC presents the advantage of the very high efficiency due to the zero-current switching (ZCS). However, it lacks of dynamic controllability and presents very poor dynamic performance. Moreover, it calls for high-current HV resonant capacitors. On the other hand, the DAB presents the high efficiency due to the zero-voltage switching (ZVS) and the excellent dynamic performance. In addition, it does not require a resonant capacitor and only utilizes the transformer leakage inductance for power transfer. Hence, the DAB is one of the most promising candidates as the ISOP-converter building block for MVDC–HVDC power conversion.

In high-power applications, the DAB presents several advantages such as higher operation frequency of the transformer, small dc-link capacitor, and ZVS capability to reduce semiconductor switching losses. To increase the converter voltage rating, a series connection of power-semiconductor devices might be considered. In [20], an integrated gate-commutated thyristor (IGCT)-based 5 kV/5 kV, 7.5 MW DAB converter has been investigated where two 4.5 kV IGCTs are connected in series to withstand 5 kV dc-link voltage. It is shown that the turn-OFF losses of the IGCTs can be significantly reduced by connecting snubber capacitors in parallel with IGCTs. Moreover, employing snubber capacitors results in more effective voltage sharing of series-connected IGCTs. However, the main drawback of the DAB is that it requires a certain amount of lagging reactive current to ensure the soft switching and to charge and discharge the snubber capacitors completely [19], [20]. Thus, a so-called auxiliary resonant commutation pole (ARCP) [32] has to be employed and activated to always ensure the soft switching and the charging and discharging of the snubber capacitors in case of part-load conditions or unbalanced input/output voltages. The employment and activation of the ARCP cause penalties of additional costs and non-negligible losses which lead to a poor efficiency in part-load situations [20], [33].

While the DAB is employed to build up an MVDC–HVDC converter, a series connection of power-semiconductor devices would be another concern. An imperfect voltage sharing occurs among the series-connected devices during turn-OFF transients due to unavoidable deviations in gate impedances, gate signal delays, and semiconductor storage times [34]. The maximum turn-OFF current of the devices in the DAB is as high as two-third of the peak phase current, and such a high turn-OFF current makes it more challenging to connect a higher number of devices in series [34], [35]. Therefore, DAB building blocks with lower voltage and power ratings must be stacked in series on the HVDC side, and be stacked in both series and parallel on the MVDC side as shown in [18]. However, the transformer in each DAB building block is subjected to an HV stress despite the fact that it only shares a limited power portion of the MVDC–HVDC converter, which would lead to a considerable penalty of increased costs and engineering efforts.

On the contrary, the MMC presents a simple scaling of voltage and power ratings and no necessity of series connection of power-semiconductor devices. Moreover, the efficiency of the MMC-FTF converter is not sensitive to the operating power or variation of the input/output voltage ratio. However, the operating frequency of the transformer connecting the MMCs on both sides is limited due to the hard-switching characteristic of the MMC. Moreover, compared to a two-level converter (TLC) of an identical power rating, the number of required power-semiconductor devices is almost doubled and it leads to higher device costs and conduction losses. Another drawback of the MMC-FTF converter is that the MMC combines three single-phase legs and a large amount of submodule (SM) capacitors are required due to the second-order power fluctuation in the SM capacitors. Typically, the capacitance of the SM capacitors is selected giving average SM-capacitor voltage ripple in the range of 10% in full-load situation [53]. In the case of a $\pm$200 kV, 400 MW MMC (60 Hz ac to dc) where the rated SM-capacitor voltage is 2.2 kV, an SM capacitor of around 4.5 mF capacitance (220 SMs per arm and six arms per MMC) is necessary to limit average SM-capacitor voltage ripple within $\pm$10% range [36].

For MMC-FTF converters, the sine-waveform operation scheme generating sinusoidal voltage and current to the transformer [24], [25] is popular. In [26]–[28], the square-waveform (or quasi-square-waveform) operation scheme and the triangular waveform operation scheme are proposed to increase power capacity by exploiting the power associated with harmonic voltages and currents. However, for HVDC applications where the transformer winding current is very high, leakage fluxes induced by the harmonic winding currents can lead to a serious thermal problem [42], and even the transformer failure caused by the harmonic winding currents has been reported [31]. Thus, the sine-waveform operation scheme is advantageous and preferred for MVDC–HVDC power conversion. The MMC-FTF converters based on other derivative topologies of the MMC such as controlled transition bridge and alternate arm converter are discussed in [29].

In summary, for MVDC–HVDC applications, the MMC presents advantages of simple voltage scaling and insensitivity of efficiency to the power condition and input/output voltage variation. On the contrary, the TLC used in the DAB presents advantages of a less amount of power-semiconductor devices, lower device conduction losses, and a less amount of dc-link capacitors. In this paper, a novel high step-up ratio isolated bidirectional soft-switching dc–dc converter is proposed to interconnect MVDC and HVDC grids. The proposed converter combines TLCs on the MV side and an MMC on the HV side, and it is named as the TLC–MMC hybrid dc–dc converter. Moreover, a dedicated operation strategy is developed for the proposed converter to significantly reduce the total device rating and turn-OFF currents in TLCs where power-semiconductor devices are connected in series. The proposed converter compromises the advantages and disadvantages of the DAB-based ISOP converter and the MMC-FTF converter [49]. Different

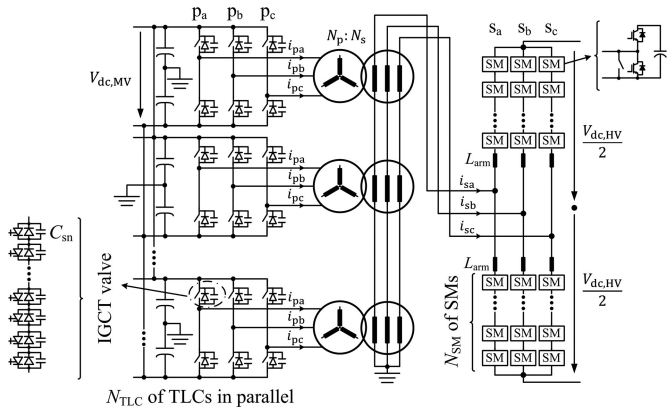

Fig. 1. Configuration of the proposed MVDC–HVDC converter.

from the DAB-based ISOP topology presented in [18], the proposed converter presents low semiconductor losses over a wide power range at variable input/output voltages. In addition, the power density and efficiency can be drastically improved compared to the MMC-FTF converter presented in [24].

The subsequent parts of this paper are organized as follows. In Section II, the configuration of the proposed converter is introduced and its operation principles are discussed in Section III. In Section IV, simulation results of a $\pm$25 kV/$\pm$200 kV 400-MW dc–dc converter system are presented. In Section V, the semiconductor-loss calculation results are presented and the highly efficient characteristic of the proposed converter is demonstrated. In Section VI, the proposed converter is compared with the MMC-FTF converter in terms of the number of required power-semiconductor devices, transformer winding current, size of passive components, and power-semiconductor losses, whereby the superiority of the proposed converter is demonstrated. Finally in Section VII, a further discussion on the proposed converter is presented in practical implementation point of view.

II. Configuration of the Proposed Converter

The configuration of the proposed MVDC–HVDC converter is depicted in Fig. 1. It includes a number of $N_{\rm TLC}$ of TLCs in parallel on the MV side. They are connected via the same number of open-end winding transformers to an MMC on the HV side. The number $N_{\rm TLC}$ is determined by the converter current rating on the MV side. Each TLC on the MV side is based on series-connected IGCTs with snubber capacitors, and the number of the series-connected IGCTs is determined by both the device voltage rating and the MV-side operation voltage. The IGCT is considered as the most suitable device on the MV side of the proposed converter for the following reasons:

1) the press-pack packaging simplifies the series connection of devices and offers double-side cooling;
2) compared to the insulated-gate bipolar transistor (IGBT), the IGCT offers higher current ratings which reduces $N_{\rm TLC}$;
3) the IGCT achieves lower conduction loss which is revealed more critical than the switching loss on the MV side of the proposed converter as presented in Section V.

Due to the series connection of IGCTs, the snubber capacitors are not optional but mandatory since it has already been well proven that it is virtually impossible to balance turn-OFF voltages of series-connected IGCTs without snubber capacitors [34]. Moreover, the snubber capacitors significantly contribute to a reduction of turn-OFF loss and $\mathrm{d}v/\mathrm{d}t$ across the IGCT valves. The ac outputs of the TLCs are connected to the primary sides of the open-end winding transformers, and the secondary sides of the transformers are connected in series. This has been proven in the first generation of two/three-level converter based static synchronous compensators [37]. Finally, the transformer cascade is linked to the ac side of the MMC. There are six arms included in the MMC, and each arm contains $N_{\rm SM}$ half-bridge SMs. The rated SM-capacitor voltage is $V_{\rm SM,cap}$. It should be noted that the cascaded connection of the transformers ensures equal phase currents of the TLCs and prevents the circulating power among the TLCs inherently. The MV side of the proposed converter is grounded at the dc-link midpoints in a symmetrical monopole configuration to reduce the voltage stresses on the components with respect to the ground, and the HV side is grounded at the neutral point of the transformer's secondary side.

Different from the DAB-based ISOP topology, the ARCPs are not necessary because ZVS of the IGCTs and the charging and discharging of the snubber capacitors are always ensured by the dedicated operation strategy introduced in the next section. Moreover, the turn-OFF currents of the IGCTs in the TLCs can be controlled constantly at a very low value regardless of operation conditions. In the case of a $\pm$25 kV/$\pm$200 kV 400 MW system investigated in the simulation study, the turn-OFF currents of the IGCTs are constantly regulated to 100 A while the peak of the TLC's phase current in full-load situation is 4.25 kA. In parallel to each IGCT device, a 1 μF snubber capacitor is connected. The IGCT operation with a very low turn-OFF current brings benefits in the following aspects:

1) The turn-OFF voltage balancing is highly dependent on the turn-OFF current. The smaller the turn-OFF current, the better the voltage sharing [34], [35]. If deviations of gate signal times are 200 ns, which are almost two times of the feasible value by standard means [38], the voltage differences caused by the gate signal delay are only 20 V. By this means, a higher number of devices can be directly connected in series with moderate efforts. Consequently a lower number of transformers withstanding HV stress are required.
2) Another practical issue of stacking IGCTs in series is the increasing cost to supply gate-drive units by isolated power supplies. The power demand of the gate-drive units for the IGCT is relatively high due to its gate current commutation principle, and it depends on the turn-OFF current. In a typical case when the switching frequency is 250 Hz, the maximum gate-drive unit's input power can be reduced from 66 W at 2 kA turn-OFF current by 60% to 26 W at 100 A turn-OFF current [35]. Hence, thanks to the very low turn-OFF current on the MV side, the efforts to supply gate-drive units can be significantly reduced.

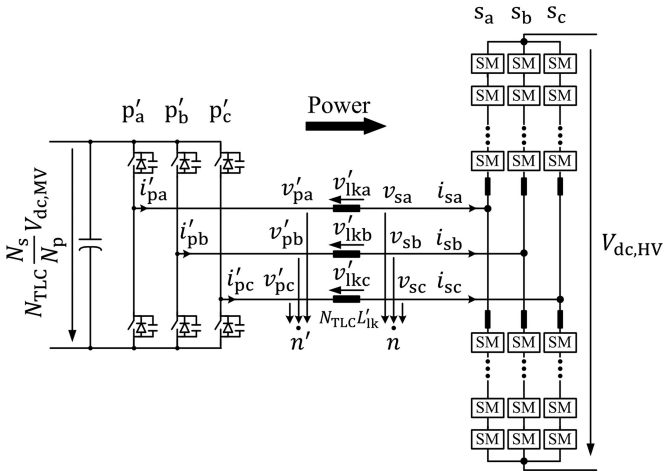

Fig. 2. Equivalent circuit diagram of the proposed MVDC–HVDC converter referred to the secondary side.

3) In practice, it can be approximated that the turn-OFF loss increases linearly with the turn-OFF current [35]. At a very low turn-OFF current, an extremely low switching loss can be expected.
4) In the IGCT-based MV drive inverters, the power capacity is restricted by the switching losses due to the thermal dissipation limit [44], [48]. In a typical IGCT-based 3.3 kV, 10 MW three-level neutral-point-clamped (NPC) inverter [39], [40], the phase current can reach 1.75 kA. Since the switching losses are significantly minimized in the proposed converter by the snubber capacitors and the extremely low turn-OFF current, the power capacity of the TLCs on the MV side can be maximized and consequently N_{TLC} can be reduced.
5) In a snubber-capacitor equipped device, the $\mathrm{d}v/\mathrm{d}t$ rate is related to the turn-OFF current. In the case investigated in this study, a turn-OFF current of 100 A results in a $\mathrm{d}v/\mathrm{d}t$ rate of 100 V/μs over a single IGCT and 2 kV/μs over an IGCT valve, which is already much lower than that of a single hard-switched MV IGBT.

Compared to the MMC-FTF converter, a number of power-semiconductor devices and SM capacitors on the MV side can be saved and only small dc-link capacitors are needed. Moreover, the devices on the MV side are turned ON in a ZVS manner and are turned OFF with snubber capacitors at a very low current. As a result, the conduction and switching losses of the power-semiconductor devices can be conspicuously reduced.

III. Operation Principles

The equivalent circuit diagram of the proposed dc–dc converter referred to the secondary side is depicted in Fig. 2. All TLCs on the MV side operate synchronously in the six-step mode and open-loop manner, and they can be modeled as a single TLC referred to the secondary side. The operation principles of the proposed dc–dc converter are illustrated in Fig. 3. While the phase angle θ increases from 0 to 2π, the primary-side phase voltage of the "a" phase varies in the following sequence: $\frac{N_{\mathrm{TLC}}}{3}\frac{N_s}{N_p}V_{\mathrm{dc,MV}}$, $\frac{2N_{\mathrm{TLC}}}{3}\frac{N_s}{N_p}V_{\mathrm{dc,MV}}$, $\frac{N_{\mathrm{TLC}}}{3}\frac{N_s}{N_p}V_{\mathrm{dc,MV}}$,

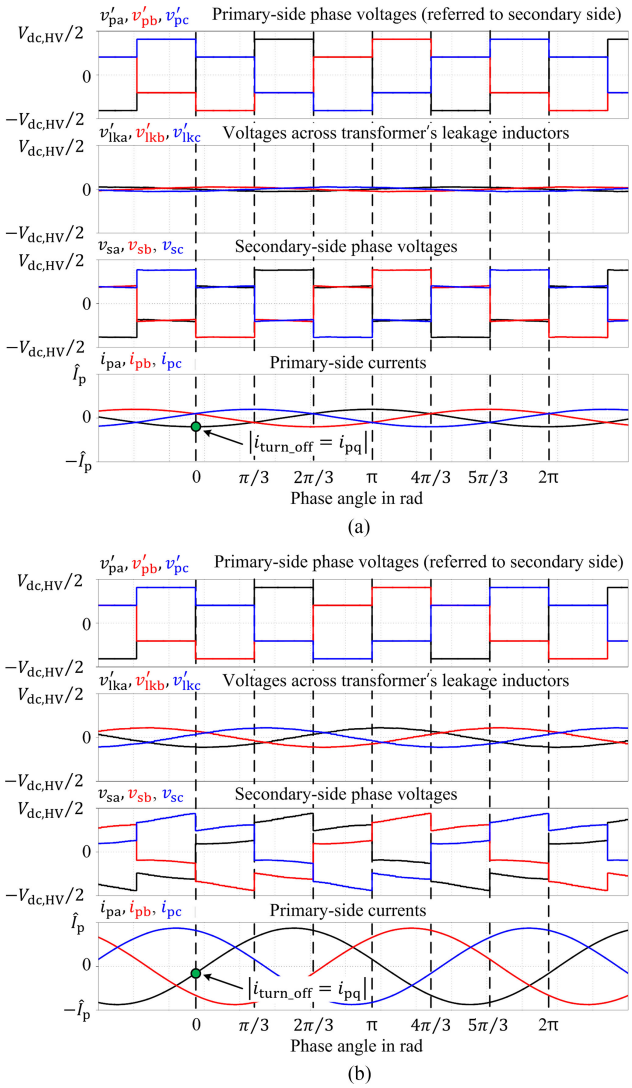

Fig. 3. Operation principles of the proposed dc–dc converter, (a) no-load situation and (b) loaded situation.

$\frac{-N_{\mathrm{TLC}}}{3}\frac{N_s}{N_p}V_{\mathrm{dc,MV}}$, $\frac{-2N_{\mathrm{TLC}}}{3}\frac{N_s}{N_p}V_{\mathrm{dc,MV}}$, $\frac{-N_{\mathrm{TLC}}}{3}\frac{N_s}{N_p}V_{\mathrm{dc,MV}}$. The MMC on the HV side controls the transformer's secondary-side current to a sinusoidal form in a closed-loop manner. The transformer-current model and the block diagram of the transformer-current controller are depicted in Fig. 4. The transformer-current model shown in Fig. 4 is derived from the equivalent circuit depicted in Fig. 2 by introducing the ac-side current model of the MMC [43]. More details of the control scheme of the proposed converter will be presented in future publications. Consequently, the primary-side currents are driven by the ac currents of the MMC uniformly. The harmonics of HVDC-transformer currents cause non-negligible stray losses since the leakage flux creates eddy currents in all exposed metallic parts [41]. Moreover, the stray losses contributed by each harmonic component are approximately proportional to the square of the current magnitude and the square of the harmonic order [42]. Hence, generating the transformer current in a form of sinusoidal greatly reduces stray losses and efforts on thermal management.

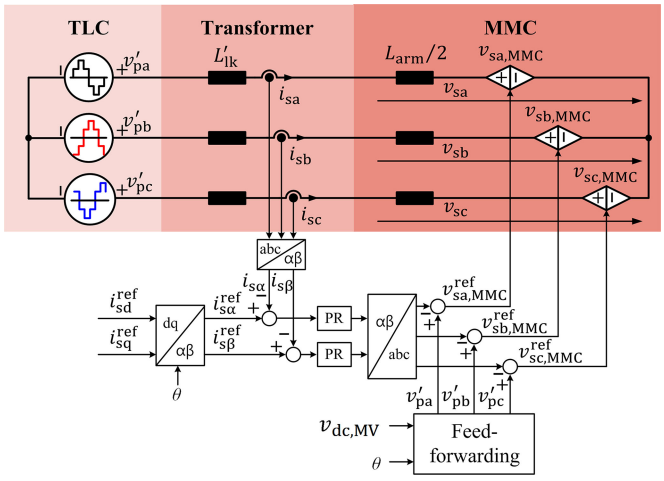

Fig. 4. Transformer-current model of the proposed converter and the block diagram of the transformer-current controller.

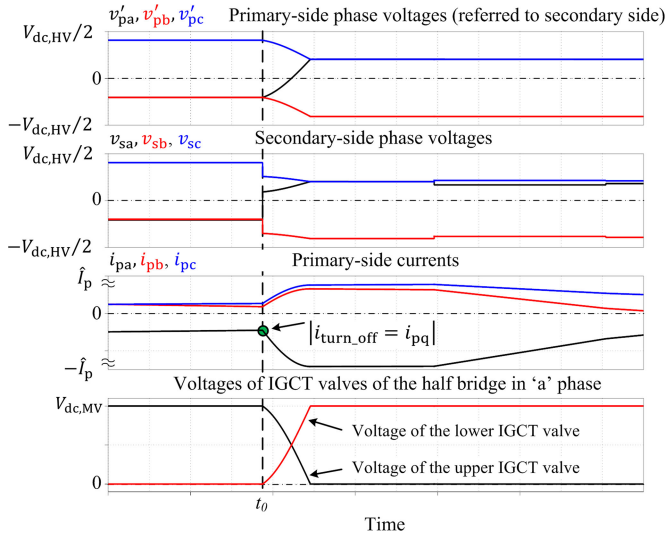

Fig. 5. Voltage and current transients during the charging and discharging process of the snubber capacitors of the half-bridge in "a" phase on the MV side in no-load situation.

Fig. 3(a) shows the operation principles of the proposed converter in no-load situation. Since there is no active power flowing between the primary and the secondary sides, the MMC only draws inductive reactive current from the transformer side intentionally. Consequently, the TLCs supply the inductive reactive currents into the transformers. The reactive currents ensure ZVS of the IGCTs in the TLCs and the complete charging and discharging of the snubber capacitors in the dead time. It should be mentioned that, neglecting the magnetizing inductance of the transformer, the turn-OFF current of the IGCT is always identical to the magnitude of the reactive current. At the same time, the transformer current is in sinusoidal as shown in Fig. 3(a). Since the reactive current does not contribute to the active power and is fully controllable, the IGCT turn-OFF current can be constantly controlled as the magnitude of the reactive current intentionally drawn by the MMC. Different from the DAB, the reactive current is not affected by the operation power or the input/output voltages. In no-load situation, since the voltages across the transformer leakage inductors are negligible compared to the TLC's phase voltages, the phase voltages of the secondary side are almost identical to those of the TLC in the steady state as shown in Fig. 3(a).

In a DAB, a sufficient initial current (namely, the turn-OFF current of the IGCT) is required to fully complete the charging and discharging of the snubber capacitors on the primary side while the secondary side is lagging referred to the primary side [20]. In a 5 kV, 7.5 MW DAB investigated in [20], an initial current of 500 A is required while each IGCT device is equipped with a 1 μF snubber capacitor. In part-load situation, the ARCP circuit has to be activated to assist the charging and discharging processes and it leads to extra losses. On the contrary, when the secondary side is leading referred to the primary side, the charging and discharging of the snubber capacitors on the primary side can be fully completed as long as the initial phase current lies in the proper direction [20].

Compared to the DAB, another crucial advantage of the proposed dc–dc converter is the inherent capability of the unassisted charging and discharging of the snubber capacitors in the TLCs. In the proposed converter, the primary-side phase voltages are utilized as a feed-forward term in the transformer-current control as shown in Fig. 4 not only to improve the dynamic performance but also to support the charging and discharging of the snubber capacitors on the primary side. The charging and discharging process of the half-bridge in "a" phase in the TLC in no-load situation is illustrated in Fig. 5. Before $t = t_0$, the lower switch of the half-bridge in "a" phase is conducting the phase current while the upper switch is in OFF-state. At $t = t_0$, the lower switch is turned OFF, and in the meantime the secondary-side phase voltages change correspondingly due to the feed-forwarding of the primary-side phase voltage. Afterwards, the commutation starts and the resonance of the snubber capacitors and the transformer leakage inductor is initiated since the initial phase current is negative. The charging and discharging process of the snubber capacitors on the primary side is equivalent to the case of the DAB when the secondary side is leading referred to the primary side. Hence, similar to the case of the DAB, the charging and discharging process of the snubber capacitors can be fully completed as long as the initial phase current is negative.

If an active power transfer occurs from the MV side to the HV side, an active current flows between the TLCs and the MMC as shown in Fig. 3(b). Concurrently the inductive reactive current is drawn as well to ensure soft switching of the TLCs. It should be noted that the switching losses (namely, the turn-OFF losses) of the TLCs are determined by the reactive current. Since the magnitude of the reactive current is constantly controlled to a rather small value (compared to the rated active current), the switching losses on the MV side can be maintained very low over the whole power range. In full-load situation, magnitude of the primary-side phase current can be calculated as follows neglecting the reactive component:

$$P_{\text{rated}} = \frac{3}{2} N_{\text{TLC}}{}^{1}\hat{V}_p \hat{I}_p = \frac{3}{2}\frac{2}{\pi} N_{\text{TLC}} V_{\text{dc,MV}} \hat{I}_p. \quad (1)$$

In the proposed converter, the IGCTs on the MV side conduct the phase currents in the so-called "half-sine wave" mode with negligible switching currents when the power flows from the MV side to the HV side. On the contrary, the free-wheeling diodes (FWDs) on the MV side conduct phase currents in the "half-sine wave" mode when the power flows in the opposite direction. The average ON-state current in full-load situation is calculated as follows and should not exceed the maximum value of the device's average ON-state current $I_{F(\mathrm{AV})M}$:

$$I_{F(\mathrm{AV})} = \frac{1}{2\pi}\int_0^{\pi} \hat{I}_p \sin\,\theta \mathrm{d}\theta = \frac{\hat{I}_p}{\pi}. \tag{2}$$

In full-load situation, there are considerable voltages across the leakage inductors. In steady state, the phase voltages of the secondary side are equal to the superposition of the primary-side six-step phase voltages and the sinusoidal voltages across the leakage inductors as shown in Fig. 3(b). The peak value of the secondary-side phase voltage v_{sa} ("a" phase as an example) occurs while the phase angle θ is $\frac{2}{3}\pi$ as illustrated in Fig. 3(b), which can be calculated using

$$\hat{V}_{\mathrm{sa}} = \frac{2}{3}\frac{N_{\mathrm{TLC}}N_s V_{\mathrm{dc,MV}}}{N_p} + \frac{1}{2}\omega L'_{\mathrm{lk}}\left(\frac{N_p}{N_s}\hat{I}_p\right). \tag{3}$$

Thus, the peak value of the phase voltage synthesized by SMs of the MMC can be derived using

$$\hat{V}_{\mathrm{sa,MMC}} = \frac{2}{3}\frac{N_{\mathrm{TLC}}N_s V_{\mathrm{dc,MV}}}{N_p} + \frac{1}{2}\omega\left(L'_{\mathrm{lk}} + \frac{1}{2}L_{\mathrm{arm}}\right)\left(\frac{N_p}{N_s}\hat{I}_p\right) \tag{4}$$

taking the voltage across the arm inductor into account [43]. Hence, the following equations should be satisfied on the HV side to avoid over-modulation of the MMC:

$$\hat{V}_{\mathrm{sa,MMC}} < \frac{V_{\mathrm{dc,HV}}}{2} \tag{5}$$

$$\hat{V}_{\mathrm{sa,MMC}} + \frac{V_{\mathrm{dc,HV}}}{2} < N_{\mathrm{SM}}V_{\mathrm{SM,cap}}. \tag{6}$$

IV. Simulation Results

To evaluate the conversion losses of the proposed dc–dc converter and validate the proposed operation method, a proposed ±25 kV/±200 kV, 400 MW MVDC–HVDC converter system is investigated. A steady-state voltage variation of 5% on the input and output sides is considered.

Detailed parameters of the simulated converter are shown in Table I. On the MV side, two ±25 kV, 200 MW TLCs are connected in parallel, and the TLCs are linked to the HV side via two 200 Hz, 200 MVA transformers. In each TLC on the MV side, twenty 4.5 kV IGCTs are connected in series to withstand 50 kV dc-link voltage, and each IGCT is connected with a 1 μF snubber capacitor in parallel. For $V_{\mathrm{dc,MV}} = 1.05$ p.u., each IGCT must block a voltage of 2.63 kV which is still lower than the 100-FIT voltage of the selected devices (the 100-FIT voltage of the IGCTs is 2.8 kV). On the MMC side, 4.5 kV IGBTs are employed. The capacitance of the SM capacitors is designed to keep the average SM-capacitor voltage ripples under full-load condition within ±10% [53].

TABLE I
Parameters of the Simulated Proposed Converter

MV-side TLCs	
Converter quantity (N_{TLC})	2
Rated dc voltage ($V_{\mathrm{dc,MV}}$)	50 kV
Rated power	200 MW
Switch	4.5 kV device × 20 per valve
Snubber capacitor (C_{sn})	1 μF
Transformers	
Transformer quantity	2
Turns ratio ($N_p : N_s$)	9:22
Leakage inductance (L'_{lk})	10 mH
Fundamental frequency	200 Hz
HV-side MMC	
Rated dc voltage ($V_{\mathrm{dc,HV}}$)	400 kV
Rated power	400 MW
Number of SMs (N_{SM})	216 per arm (8% redundancy)
Rated SM voltage ($V_{\mathrm{SM,cap}}$)	2.2 kV
SM capacitor	1.13 mF
Arm inductor (L_{arm})	15 mH
Control	
Sampling frequency	12 kHz
Controller delay	83.3 μs
Induced reactive current (peak)	100 A

In the first test case MV- and HV-side voltages are 1.00 p.u. Fig. 6 shows the simulation results while the converter operates under no-load condition. As shown in Fig. 6(a), the reactive current of 100 A is induced successfully which equals the IGCT turn-OFF current. Judging from the voltages across the IGCTs and the corresponding gate signals shown in Fig. 6(b), the IGCTs are turned ON in a ZVS manner even though no assisting circuit such as the ARCP is employed.

In the second test case, the converter operates under full-load condition. Fig. 7(a) indicates that the transformer current is dominated by the active current while the overlaying reactive current of 100 A is negligible. However, the IGCTs are still turned OFF at 100 A. Judging from the voltages across the IGCTs and the corresponding gate signals shown in Fig. 7(b), the IGCTs on the MV side are turned ON in a ZVS manner as before. The total harmonic distortion (THD) of the transformer current is below 2.0% which could effectively suppress stray losses caused by the winding harmonic currents.

The results of voltages and currents of the MMC under full-load condition are shown in Fig. 8. The closed-loop indirect-modulation based control strategy of the MMC proposed in [43] is employed and hence the second-order circulating current is inherently avoided. With the designed SM capacitance of 1.13 mF, the average SM-capacitor voltage fluctuations are limited to ±10%. As a comparison, in an MMC for ac–dc conversion at line-frequency with the same voltage and power ratings, SM capacitors with capacitance of 4.5 mF are required. Even though the transformer frequency of the proposed converter cannot be increased further due to the hard-switching nature of the MMC, the size of the transformers and

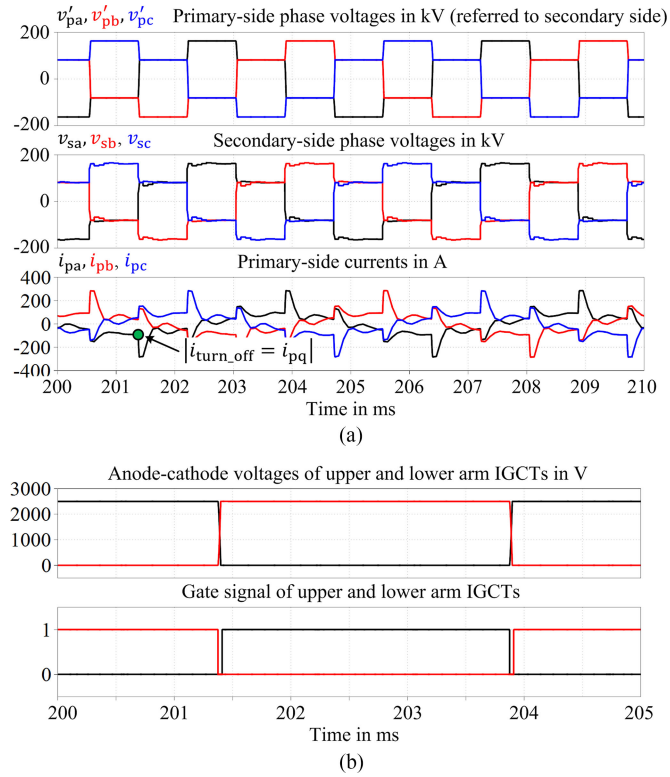

Fig. 6. Simulation results under no-load condition while MV- and HV-side voltages are both 1.00 p.u., (a) transformer's phase voltages and currents, and (b) voltages across IGCTs and the corresponding gate signals.

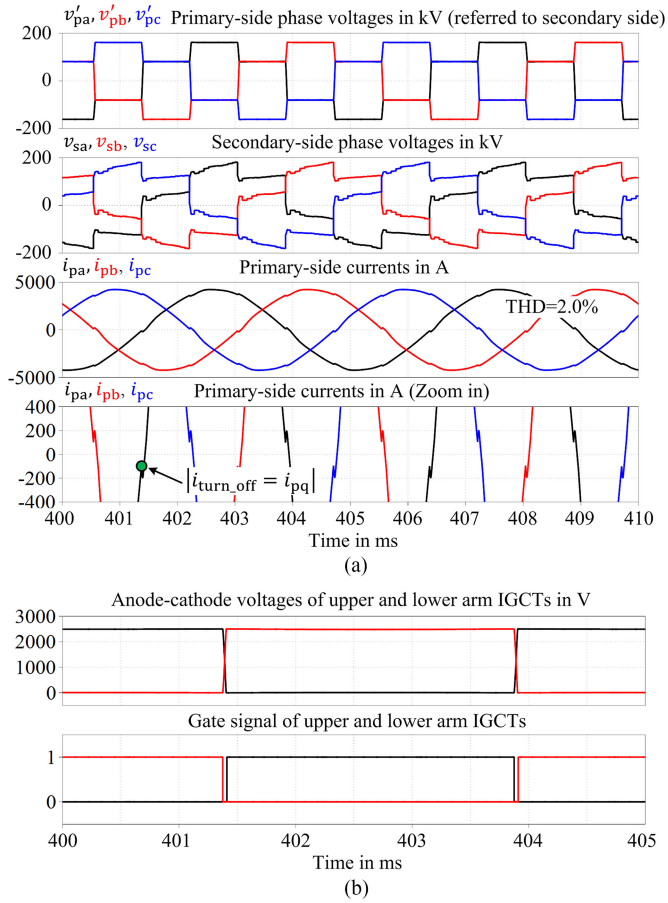

Fig. 7. Simulation results under full-load condition while MV- and HV-side voltages are both 1.00 p.u., (a) transformer's phase voltages and currents, and (b) voltages across IGCTs and corresponding gate signals.

SM capacitors can be conspicuously reduced compared to the MMC–HVDC converters used in ac–dc conversions. This can be an attractive characteristic especially for the platforms of offshore wind farms where the high power density is highly desired.

In this study, the sorting-based modulation method with virtual SM-capacitor voltages presented in [36] is employed to reduce the switching frequency in the MMC. The parameters of the modulation scheme are tuned so that the individual SM-capacitor voltages do not exceed 2.75 kV (IGBT 100-FIT voltage of 3 kV) under full-load condition as shown in Fig. 9. The individual SM-capacitor voltages of only ten randomly selected SMs of each arm are displayed in Fig. 9 for better visibility. In accordance with the simulation results, the average switching frequency of the IGBT modules is 260 Hz under full-load condition.

The dynamic performance of the transformer-current control when the load is changed from 0.5 to 1.0 p.u. at $t = 0.604$ s is shown in Fig. 10. Thanks to the high feasible bandwidth of the MMC-current controller, the transformer-current control presents good tracking. In the dynamic process, the reactive current is kept constant and the IGCTs on the MV side are still turned OFF at 100 A.

The grounding technique is another important issue in HV applications. As shown in Fig. 1, the MV side of the proposed converter is grounded at the midpoint of the split capacitors in the dc-link. The voltages at the ac terminals of the TLC with respect

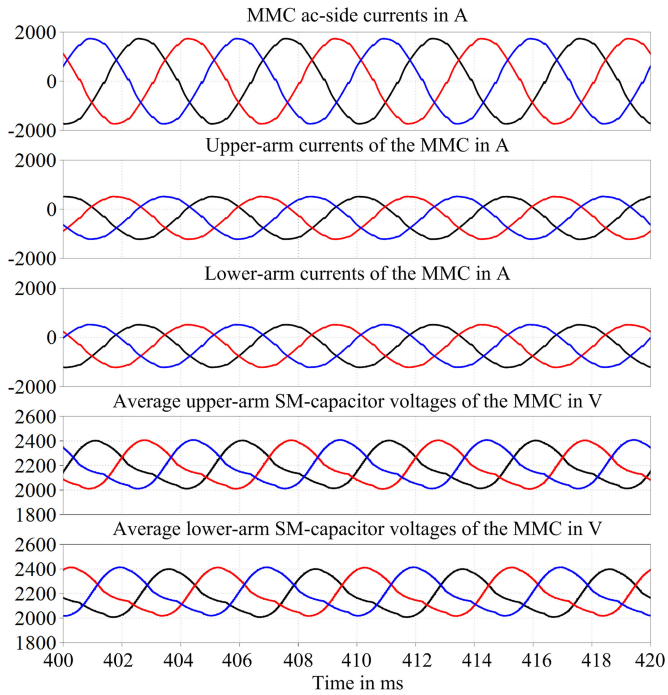

Fig. 8. Simulation results of voltages and currents of the MMC under full-load condition.

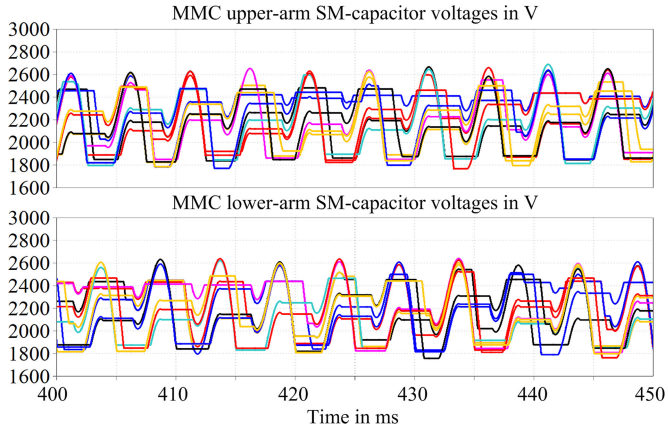

Fig. 9. Individual SM-capacitor voltages in upper and lower arms of "a" phase of the MMC under full-load condition.

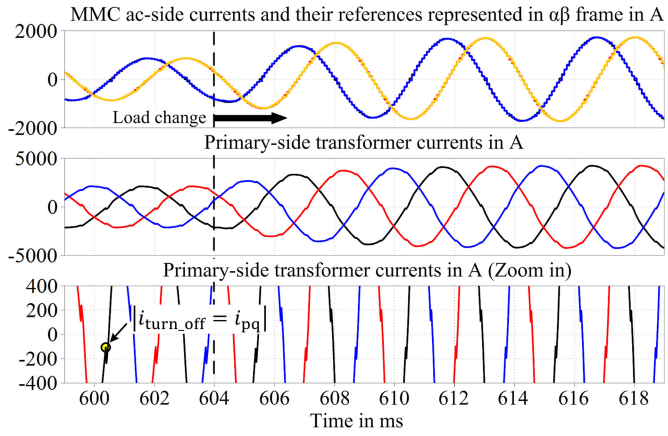

Fig. 10. Dynamic performance of the transformer-current controller.

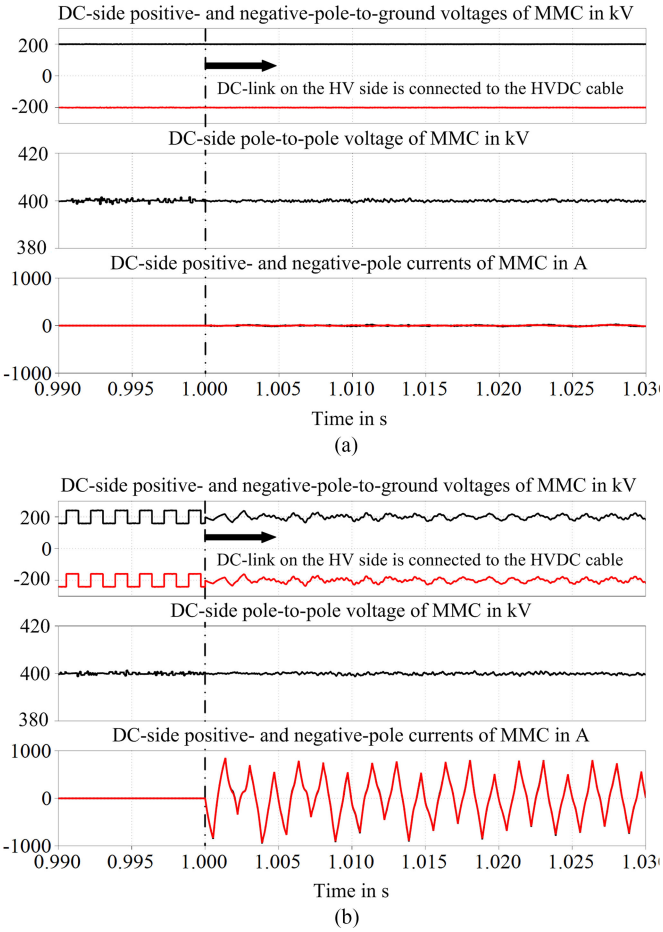

Fig. 11. DC-side voltage and current of the MMC when the dc-side is connected to a precharged open-end HVDC cable, (a) when the MMC generates a six-step ac-terminal voltage, and (b) when the MMC generates a square-wave ac-terminal voltage.

to the ground (defined as the ac-terminal voltages in this paper) are square waves. This leads to the third-order zero-sequence component included in the ac-terminal voltages. However, since the MV side is grounded via the dc side instead of the ac side, the zero-sequence ac-terminal voltage would not be imposed on the dc-side pole-to-ground voltages. On the contrary, the HV side of the proposed converter is grounded at the neutral point of the transformer's secondary side. The MMC generates a six-step ac-terminal voltage (with respect to the virtual midpoint of the dc side) instead of a square-wave ac-terminal voltage on the transformer's secondary side, hence there is no zero-sequence voltage generated on the transformer's secondary side.

Consequently there is no ac component imposed on the pole-to-ground voltages on the dc side. The dc-side voltage and current of the MMC are shown in Fig. 11 when the dc-side is connected to an end of a 100 km precharged HVDC cable at $t = 1.0$ s and the other end of the cable is open. Parameters of the simulated cable are shown in the Appendix, and the distributed parameter line model [52] is employed in the simulation. The positive- and negative-pole-to-ground voltages on the dc side of the MMC are purely in a form of dc as shown in Fig. 11(a), and the dc-side pole currents are zero since there is no active power flowing via the open-end HVDC cable. On the contrary, if the MMC generates a square-wave ac-terminal voltage on the transformer's secondary side, then a significant third-order ac component will be imposed on the pole-to-ground voltages. Consequently, it induces a great amount of charging current through the parasitic capacitors between the cable and the ground as shown in Fig. 11(b) even if there is no active power flowing via the cable.

In the third test case, the MV- and HV-side voltages are, respectively, 0.95 and 1.05 p.u. Under no-load condition, Fig. 12(a) shows that the reactive current of 100 A is induced successfully and the IGCT valves are turned OFF at 100 A. Judging from the voltages across the IGCTs and the corresponding gate signals shown in Fig. 12(b), the IGCTs are turned ON in a ZVS manner. Different from the DAB, the ac and dc sides of the proposed converter are fully decoupled. Consequently, ZVS in the TLCs is always guaranteed in spite of power or voltage variations.

V. Loss Evaluation

To evaluate the proposed dc–dc converter in terms of efficiency, power-semiconductor loss estimation has been performed by simulation. For the ZVS soft-switched IGCTs on the

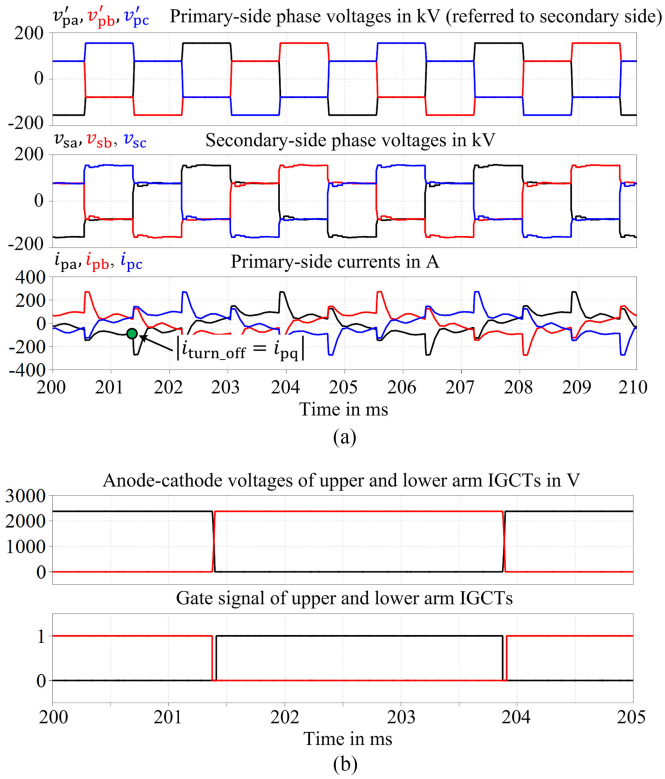

Fig. 12. Simulation results under no-load condition while MV- and HV-side voltages are, respectively, 0.95 and 1.05 p.u., (a) transformer's voltages and currents, and (b) voltages across IGCTs and the corresponding gate signals.

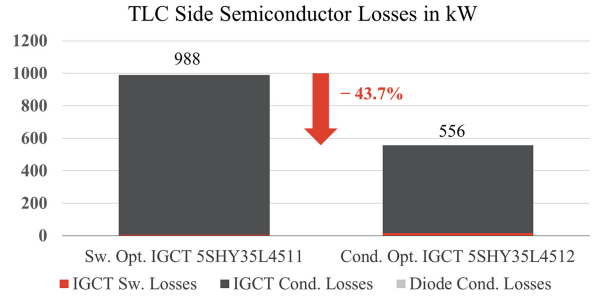

Fig. 13. Loss comparison of switching and conduction optimized IGCTs on the MV side under full-load condition.

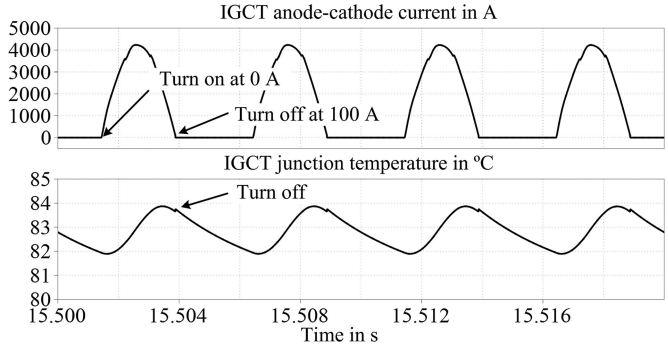

Fig. 14. Current and junction temperature of a double-sided water-cooled IGCT at full load.

MV side, the calculation of the reduced turn-OFF losses by the snubber capacitors is based on the measurement results of [20].

A. Device Selection on the MV side

A proper selection of power-semiconductor devices has been conducted on the MV side to optimize the efficiency of the converter. Considering that the TLCs on the MV side operate in ZVS mode and the device switching frequency is relatively low compared to the hard-switched MV inverters, the grid-commutated rectifier diode seems attractive for the FWD rather than the fast-recovery diode. However, the forward recovery of the slow rectifier diode after current commutation would impose additional reverse voltage stresses to the asymmetric IGCTs and the specification limits would be exceeded (17 V for asymmetrical IGCTs) [20]. Thus, in this paper a fast-recovery diode of type ABB 5SDF28L4520 is selected as FWD.

According to [20], switching optimized IGCTs with shorter carrier lifetime are preferred for multimegawatt MV high-power DAB rather than the conduction optimized IGCTs with longer carrier lifetime since the switching loss is more critical than the conduction loss due to the relatively high transformer operation frequency (up to 1.5 kHz). While in the proposed dc–dc converter, the transformer operation frequency is relatively low compared to the DAB. Moreover, the IGCTs are always turned-OFF at very low currents. It could be expected that on the MV side of the proposed dc–dc converter, conduction loss is more critical than the switching loss. Fig. 13 depicts the semiconductor-device losses of the MV side under full-load condition while switching optimized IGCT (ABB 5SHY35L4511) and conduction optimized IGCT (ABB 5SHY35L4512) are employed. It is clearly shown that on the MV side the conduction loss is dominant and that the overall semiconductor losses can be reduced by 43.7% if conduction optimized IGCTs are used. Simulation results of the current and the junction temperature of the IGCT at full load are shown in Fig. 14 while the IGCTs are double-sided water cooled. In the simulation, the water temperature of 40 °C and heatsink-to-water thermal resistance of 5 K/kW are assumed. The IGCT conducts current in "half-sine wave" mode and the junction temperature is well below the maximum operating junction temperature even though the rms phase current of the TLC is as high as 3 kA. An interesting phenomena observed in Fig. 14 is that, different from the hard-switched MV inverter [44], the junction-temperature spike in switching transient is negligible because of the very low switching loss. Compared to the 3.3 kV, 10-MW, hard-switched NPC inverter [39], [40], the phase-current capacity could be increased by more than 70% thanks to the significantly reduced switching losses.

B. Converter Power Semiconductor Losses

Power-semiconductor losses of the proposed dc–dc converter at various voltages and operating powers are shown in Figs. 15 and 16. The 4.5 kV IGBTs are considered on the HV side and the conduction-optimized IGCTs are considered on the MV side. On the HV side, the 4.5 kV IGBT module of type Infineon FA1200R45HL3 is used for loss calculation. Since the ac and dc

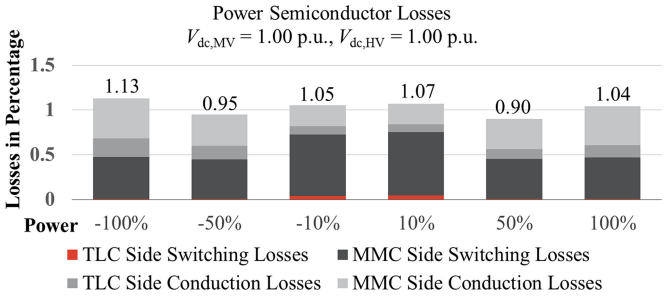

Fig. 15. Losses of the proposed dc–dc converter while the MV- and HV-side voltages are both 1.0 p.u.

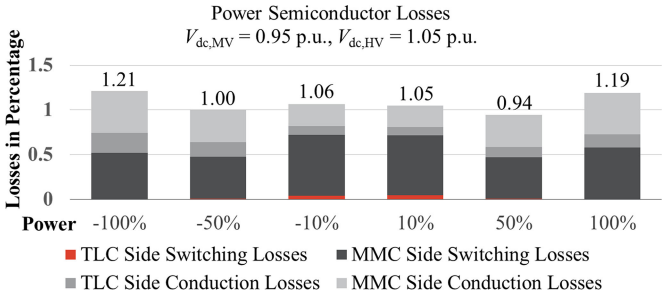

Fig. 16. Losses of the proposed dc–dc converter while the MV- and HV-side voltages are 0.95 and 1.05 p.u., respectively.

sides of the MMC are fully decoupled, the semiconductor losses do not vary significantly in accordance with variations of power or input/output voltage. Since the ZVS on the MV side is always guaranteed by the reactive-current injection instead of activating auxiliary circuits, it does not lead to a significant efficiency reduction in part-load situations. Under the rated condition, the overall semiconductor losses in percentage are 1.04% under full-load condition and 1.07% at load of 0.1 p.u. When the power flows from the HV side to the MV side, the overall semiconductor losses are slightly higher than those while the power flows in the opposite direction. The main reason is that the ON-state voltage of the MV-side diodes is slightly higher than that of the conduction optimized IGCTs.

From Figs. 15 and 16, it can be concluded that the conduction losses of the MV side are much lower than those of the HV side. The reasons are that the MMC employs almost twice number of power-semiconductor devices compared to an equivalent TLC. Moreover, the IGBT employed on the HV side has a higher ON-state voltage than the IGCT employed on the MV side. It is also shown in Figs. 15 and 16 that switching losses on the MV side are extremely low. The reasons are attributed as follows:

1) ZVS soft-switching is always realized and consequently the turn-ON losses are saved;
2) the turn-OFF losses are reduced due to the presence of the snubber capacitors;
3) the IGCTs on the MV side are always turned OFF at very low currents.

Compared to the HV side where an MMC is employed, the switching losses on the MV side are negligible and the conduction losses are lower than one-third of those on the HV side. Consequently, the overall semiconductor losses can be

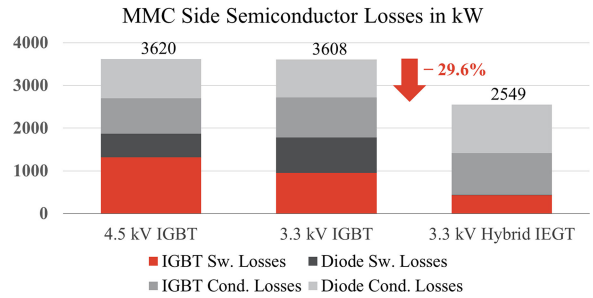

Fig. 17. Loss comparison of the MMCs under full-power condition employing 4.5 kV IGBTs, 3.3 kV IGBTs, and 3.3 kV hybrid IEGTs.

conspicuously reduced compared to those of the MMC-FTF converters [24].

C. Future Potentials

In the multilevel converters for transmission level applications, a lower number of levels based on higher blocking-voltage devices are preferred in terms of overall semiconductor-loss reduction [45]. Since the current rating of today's 6.5 kV IGBTs is not high enough to build up such high current converter, the 4.5 kV IGBTs are the most suitable devices. When a higher efficiency is demanded, the Si/SiC hybrid module is a promising option. The newly launched 3.3 kV hybrid injection-enhanced gate transistor (IEGT)/SiC Schottky barrier diode (SBD) module (MG1500FXF1US71 from Toshiba) is an attractive alternative. Even though higher number of levels leads to higher conduction loss, more advantages could be expected due to the reduced switching loss offered by the SiC SBDs.

The 400 MW proposed dc–dc converter employing 3.3 kV devices in the MMC is simulated. In each arm of the MMC, 270 (250 SMs for normal operation) SMs are included and the rated SM-capacitor voltage $V_{\mathrm{SM,cap}}$ is 1.6 kV. The parameters of the modulation strategy of [36] are tuned so that the individual SM-capacitor voltages do not exceed 2.05 kV and the average switching frequency of the hybrid modules is the same as the case of 4.5 kV IGBTs in Sections IV and V, namely 260 Hz.

The loss comparison of the MMCs under full-load conditions is shown in Fig. 17 where the 4.5 kV IGBT of type Infineon FA1200R45HL3, the 3.3 kV IGBT of type Infineon FA1200R45HL3, and the 3.3 kV hybrid module of type Toshiba MG1500FXF1US71 are employed. The 3.3 kV IGBT presents reduced switching loss; however, the saved switching loss is offset by the increased conduction loss due to the increased number of SMs. Therefore, the 3.3 kV IGBT does not introduce favorable benefit of total semiconductor-loss reduction. While the hybrid module is employed, the total semiconductor losses are reduced by 29.6% in spite of penalty of increased conduction losses. This is attributed to the fact that the SiC SBD significantly reduces not only the diode reverse-recovery loss but also the turn-ON loss of the IEGT as shown in Fig. 17. By replacing the 4.5-kV IGBTs by the 3.3 kV hybrid IEGT modules, the converter overall semiconductor losses can be reduced from 1.04% to 0.77%. It is reasonable to expect that in the near future, the converter overall semiconductor losses could be further

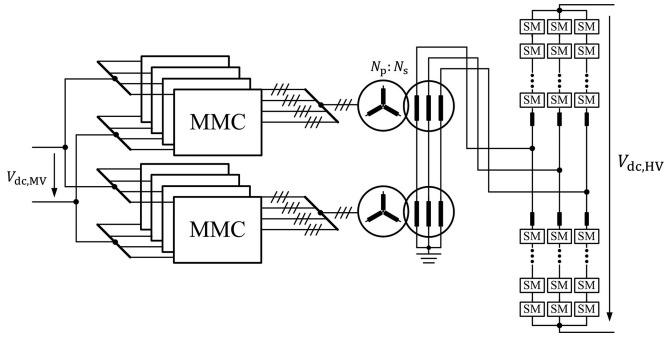

Fig. 18. Schematic of the investigated MMC-FTF system.

TABLE II
PARAMETERS OF THE SIMULATED MMC-FTF CONVERTER

Transformers	
Transformer quantity	2
Turns ratio ($N_p : N_s$)	1:4
Leakage inductance (L'_{1k})	10 mH
Fundamental frequency	200 Hz
MV-side MMCs	
MMC quantity	8
Rated dc voltage ($V_{dc,MV}$)	50 kV
Rated power	50 MW
Number of SMs ($N_{SM(MV)}$)	25
Rated SM voltage ($V_{SM(MV),cap}$)	2.2 kV
SM capacitor	1.13 mF
Arm inductor ($L_{arm(MV)}$)	5 mH
Control	
Sampling frequency	12 kHz
Controller delay	83.3 μs

reduced with the availability of high current 10 kV/15 kV full SiC modules [46].

VI. COMPARISON WITH THE MMC-FTF CONVERTER

The proposed converter is compared with the MMC-FTF converter which is a popular and suitable candidate in implementation point of view for MVDC–HVDC power conversion. A $\pm$25 kV/$\pm$200 kV, 400 MW MMC-FTF converter is designed and compared with the proposed converter investigated in Sections IV and V. The schematic of the designed MMC-FTF converter is depicted in Fig. 18. The MMC-FTF converter operates in the sine-waveform scheme due to its superiority against the square-waveform and triangular-waveform schemes as discussed in Section I. Similar to the proposed converter, there are two 200 Hz, 200 MVA open-end winding transformers employed to connect the MV side and the HV side. On the primary side of each transformer, there are four identical MMCs connected in parallel, and the power rating of each MMC is 50 MW. The MMC on the HV side is identically designed as in the proposed converter investigated in Sections IV and V. The detailed parameters of the designed MMC-FTF converter are shown in Table II. For a fair comparison with the proposed converter which employs 4.5 kV IGCTs on the MV side, 4.5 kV IGBTs are employed in eight MMCs on the MV side of the

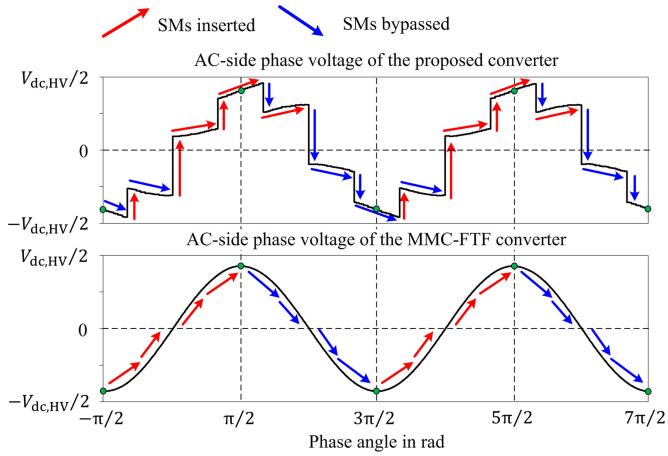

Fig. 19. AC-side phase voltages generated by the MMCs in the proposed converter and the MMC-FTF converter.

MMC-FTF converter. In the MMC-FTF converter, the same as in the MMC on the HV side, the 4.5 kV IGBT module of type Infineon FA1200R45HL3 is used for loss calculation on the MV side. Typically, the capacitance of the SM capacitors in the MMC is selected giving average SM-capacitor voltage ripple in the range of 10% in full-load situation [53]. Thus, the capacitances of the SM capacitors on both the HV side and the MV side are designed to keep the average SM-capacitor voltage ripples in full-load situation within $\pm$10%.

The same modulation technique and modulation parameters used in the MMC of the proposed converter are employed in the MMCs on both sides of the MMC-FTF converter, so that the individual SM-capacitor voltages do not exceed 2.75 kV. In accordance with the simulation results, the average switching frequency of the MMC IGBT modules in the full-load situation is 210 Hz in the MMC-FTF converter which is lower than that of the proposed converter. The waveform of the ac-side voltage generated by the MMC in the proposed converter is a superposition of a six-step waveform and a sinusoidal waveform, and the waveform of the ac-side voltage generated by the MMC in the MMC-FTF converter is purely sinusoidal as shown in Fig. 19. Over each half-cycle ($[\frac{-\pi}{2}, \frac{\pi}{2}]or[\frac{\pi}{2}, \frac{3\pi}{2}]$), the waveform of the MMC-FTF converter is monotonic but that of the proposed converter is nonmonotonic. Thus, the proposed converter results in a higher number of SM-insertion/bypass actions over each half-cycle than the MMC-FTF converter. Consequently, the proposed converter results in a higher average switching frequency than the MMC-FTF converter.

Simulation results of the MMC-FTF converter in full-load situation are shown in Fig. 20. The transformer current is controlled in a sinusoidal form as shown in Fig. 20(a), and the THD of the transformer current in full-load situation is 0.3% which is lower than that of the proposed converter. It is because in the proposed converter there is always a disturbance term included in the transformer current as shown in Figs. 6 and 7 which is induced by the resonance of snubber capacitors on the MV side and the transformer leakage inductor during commutation. However, the transformer-current THD of the proposed

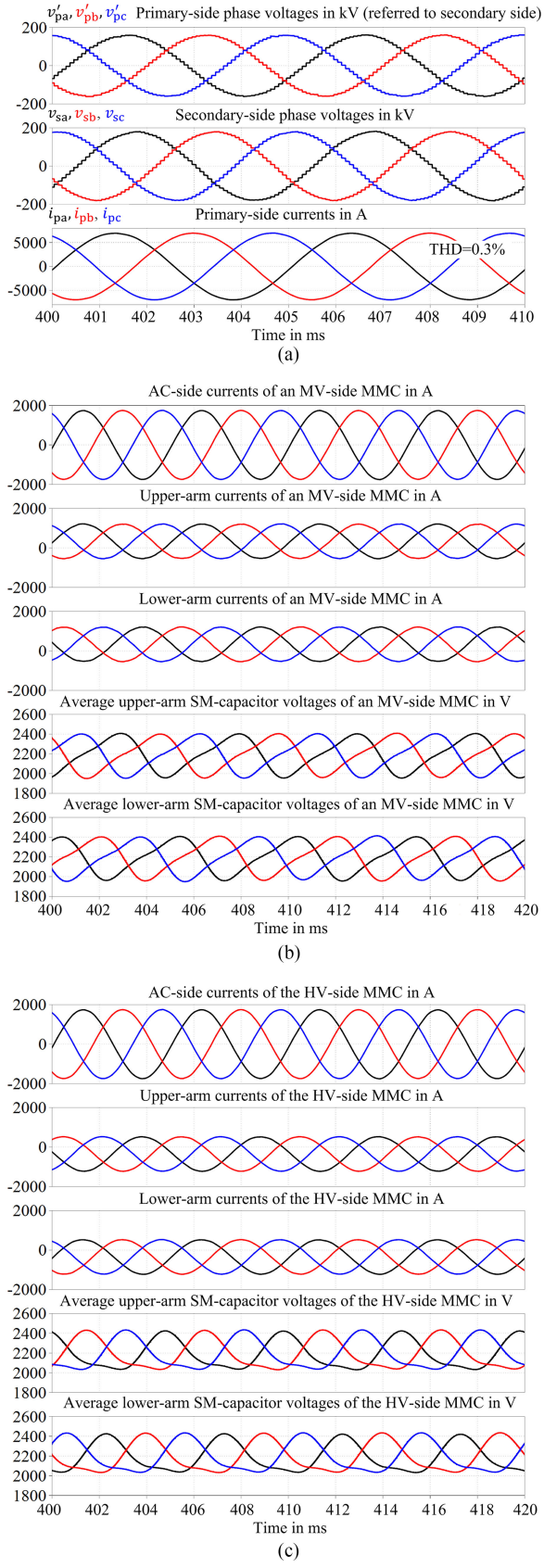

Fig. 20. Simulation results of the MMC-FTF converter in full-load situation while MV- and HV-side voltages are both 1.00 p.u. (a) Transformer's phase voltages and currents, (b) voltages and currents of an MV-side MMC, and (c) voltages and currents of the HV-side MMC.

converter is already as low as 2.0% in full-load situation which is low enough to suppress stray losses caused by the harmonic-current leakage flux [31], [41]. The rms value of the primary-side transformer-current of the MMC-FTF converter in full-load situation is 4.83 kA. However, that of the proposed converter is just 3 kA. It is attributed to the fact that with the same dc-link voltage the fundamental component of the phase voltage generated by a TLC operating in the six-step mode is much higher than that generated by an MMC in the sine-waveform operation. Thus, for the same transferred power, the proposed converter results in lower rms value of the transformer winding current and consequently in lower winding losses. Simulation results of voltages and currents of the MMCs on both MV and HV sides of the MMC-FTF converter are shown in Fig. 20(b) and (c), respectively. With the designed SM capacitance, the average SM-capacitor voltage ripples are limited within $\pm 10\%$.

Since the HV sides of the MMC-FTF converter and the proposed converter are identical, detailed comparison should be focused on the MV side. In the MMC-FTF converter, there are eight 50 MW MMCs required on the MV side. However, in the proposed converter, there are only two 200 MW TLCs required on the MV side. Reduction of the number of converters on the MV side in the proposed converter is attributed to following two reasons: 1) the current rating of the commercial 4.5 kV IGBT modules is much lower than that of the 4.5 kV IGCTs; and 2) the switching loss of the IGCTs in the proposed converter is greatly reduced by the dedicated operation method, and consequently the power capacity is significantly enhanced. In practical HVDC projects, the dc-link current rating of the 4.5 kV IGBT-based MMC is up to 1 kA [50], and the dc-link current rating of the 3.3 kV IGBT-based MMC is increased up to 1.6 kA [51] since the current rating of the commercial 3.3 kV IGBT modules is higher than that of the 4.5-kV IGBT modules. However, the significant disadvantage of utilizing 3.3 kV IGBTs is the increased number of SMs which results in higher conduction losses and increased complexity of the control system.

Regarding power-semiconductor devices in the MMC-FTF converter, 300 IGBT modules are required in each MV-side MMC, and 2400 IGBT modules are required on the MV side in total. In the proposed converter, 150 IGCTs are required in each TLC, and only 300 IGCTs are required on the MV side in total.

Regarding passive components in the MMC-FTF converter, the total SM-capacitor stored energy of the MMC on the MV side is 3.28 MJ. In the proposed converter, specifying the MV-side dc-link voltage ripple within $\pm 0.5\%$, a dc-link capacitor of 273.7 μF is required for the MV side corresponding to the stored energy of 0.34 MJ, which is 10.3% of that of the MMC-FTF converter. In addition, the dc-link capacitor on the MV side of the proposed converter can be reduced by 85% by the capacitor ripple-current cancellation technique via a modification of the transformer connection as shown in Section VII. Consequently, the capacitor energy on the MV side can be reduced to 49 kJ (only 1.5% of that of the MMC-FTF converter). Unfortunately, this ripple-current cancellation technique is not applicable for the MMC-FTF converter.

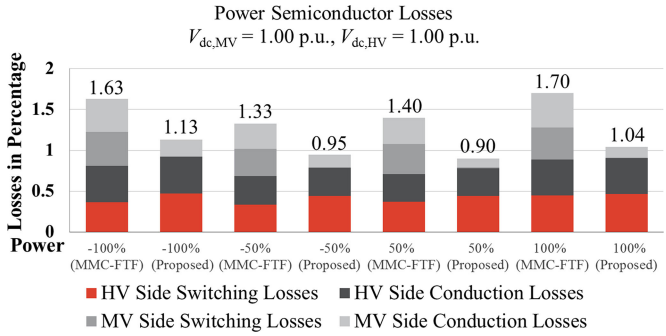

Fig. 21. Power-semiconductor loss comparison of the MMC-FTF converter and the proposed converter in various load conditions.

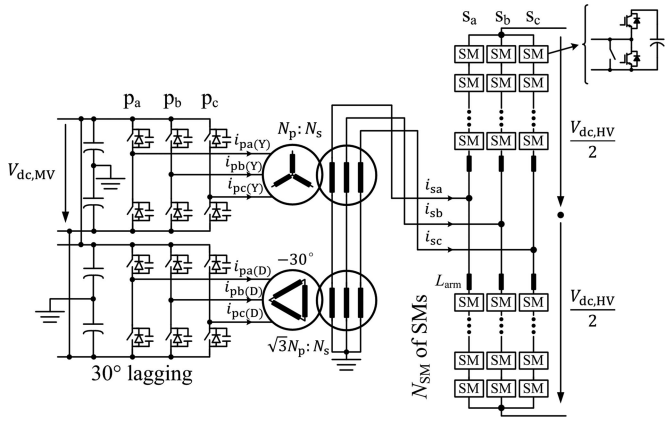

Fig. 22. Configuration of the proposed MVDC–HVDC converter employing the modified YD/Y transformer connection.

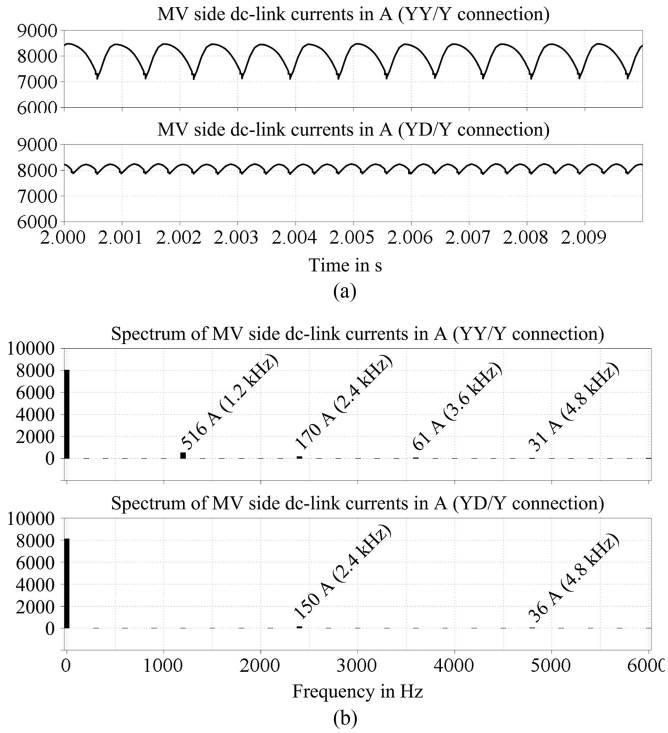

Fig. 23. DC-link currents on the MV side with different configurations of the transformer connection, (a) time domain results and (b) frequency domain results.

Power-semiconductor losses of the MMC-FTF converter and the proposed converter are compared under various load conditions as shown in Fig. 21. On the HV side, the conduction losses are almost identical. However, the switching loss of the proposed converter is higher than that of the MMC-FTF converter due to the higher average switching frequency in the proposed converter. On the MV side, the conduction loss of the MMC-FTF converter is much higher than that of the proposed converter due to the significantly larger number of power-semiconductor devices in the MMC-FTF converter and the higher ON-state voltage of the IGBT compared to the IGCT. The MMC-FTF converter generates a considerable switching loss on the MV side due to hard-switching. On the contrary, the switching loss on the MV side of the proposed converter is almost negligible. In full-load situation, the overall power-semiconductor loss of the MMC-FTF converter is 63% higher than that of the proposed converter.

In summary, compared to the MMC-FTF converter, the proposed converter presents various significant advantages such as reduced transformer winding current, reduced power-semiconductor devices and passive components, and reduced power-semiconductor losses under various load conditions.

VII. Discussion on Practical Implementation

This section discusses the practical implementation of the proposed converter. In the following, a practical structure of the transformer connection is introduced to reduce the size of the MV-side dc-link capacitor and $\mathrm{d}v/\mathrm{d}t$ rate on the HV side. Afterwards, the necessity of the reactive current even in no-load situation is introduced.

A. Configuration of Transformer Connection

When the MV and HV sides of the proposed converter are connected simply via Y/Y transformers as shown in Fig. 1, the dominant ripple current in the dc link of the MV side is the sixth-order harmonic current. In the case investigated in Section IV, the dominant ripple current is at 1.2 kHz with a magnitude of 516 A. Specifying the dc-link voltage ripple within $\pm 0.5\%$ and neglecting other higher frequency ripple currents, a dc-link capacitor of 273.7 μF is required for the MV side which corresponds to the stored energy of 0.34 MJ. The total SM-capacitor stored energy of the MMC on the HV side is 3.54 MJ, which is larger than ten times of that on the MV side. It should be noted that in the MMC-FTF converter, it requires such a large amount of total SM-capacitor stored energy not only on the HV side but also on the MV side as shown in Section VI. Thus, the proposed converter saves a great amount of capacitors compared to the MMC-FTF converter.

The size of the dc-link capacitor on the MV side can be further reduced by modifying of the transformer connection as shown in Fig. 22. In the modified structure, the primary side includes both Y- and D-winding connections, and the TLC connected to the D-winding transformer lags 30° with respect to the other one connected to the Y-winding transformer. By this means, the

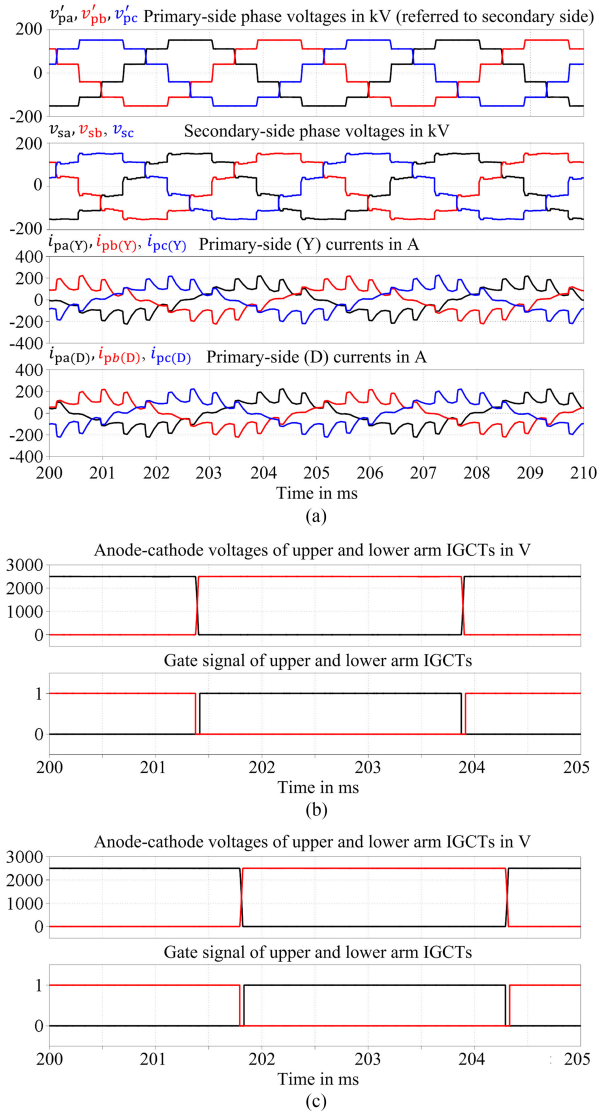

Fig. 24. Simulation results under no-load condition while the modified transformer connection is employed, (a) transformer's phase voltages and currents, (b) voltages across IGCTs and corresponding gate signals in the TLC connected to the Y-winding transformer, and (c) voltages across IGCTs and corresponding gate signals in the TLC connected to the D-winding transformer.

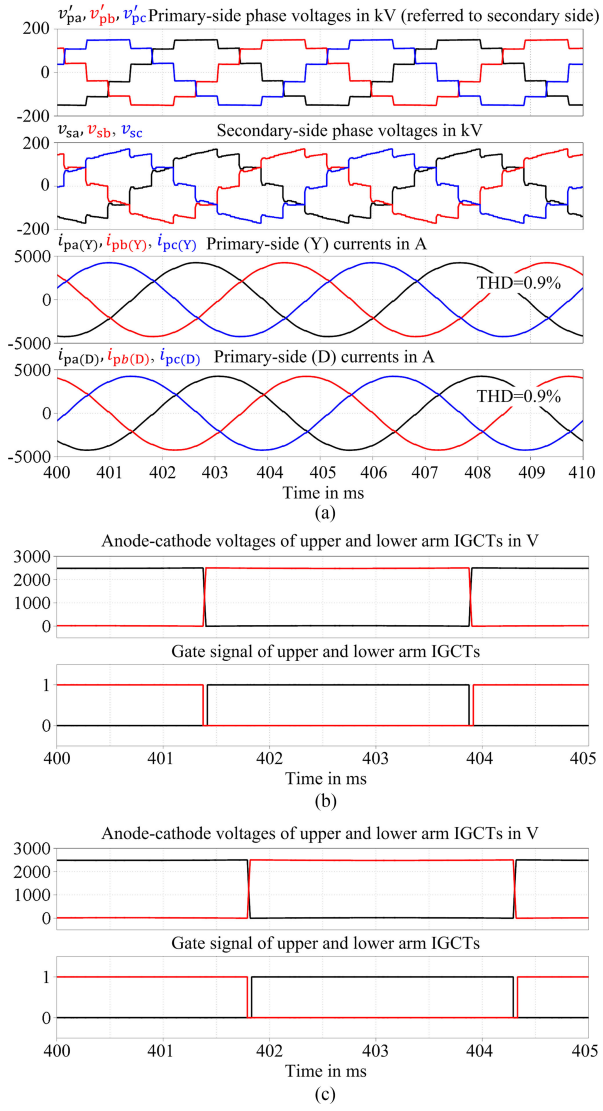

Fig. 25. Simulation results under full-load condition while the modified transformer connection is employed, (a) transformer's phase voltages and currents, (b) voltages across IGCTs and corresponding gate signals in the TLC connected to the Y-winding transformer, and (c) voltages across IGCTs and corresponding gate signals in the TLC connected to the D-winding transformer.

6th- and 18th-order ripple components included in the dc-link current of the MV side can be canceled out.

The simulation results of dc-link currents on the MV side with different structures of transformer connection are shown in Fig. 23 in time and frequency domains. By the modified transformer connection, the frequency of the dominant ripple current is doubled and the magnitude is reduced to lower than one-third. Consequently, the dc-link capacitor on the MV side can be reduced from 273.7 to 39.8 μF which corresponds to the stored energy of 0.049 MJ.

The simulation results of the proposed converter with the modified transformer connection under no-load and full-load conditions are shown in Figs. 24 and 25, respectively, while both input and output voltages are 1.0 p.u. The phase current of the TLC connected to the D-winding transformer is 30° lagging with respect to that of the TLC connected to the Y-winding transformer. The IGCTs in both TLCs are turned ON in a ZVS manner under both no-load and full-load conditions. An additional benefit that can be gained by the modified structure is that the transformer's secondary-side phase voltage is changed from the six-step mode to the twelve-step mode as shown in Figs. 24 and 25 which decreases the $\mathrm{d}v/\mathrm{d}t$ rate to half.

B. Necessity of Reactive Current

Considering the operation principle of the proposed converter, one might argue that since the transformer current is fully controllable, it would make sense to remove the reactive current and turn ON and turn OFF the IGCTs in a ZCS manner so that the switching loss could be further saved. Actually the reactive current is strictly required to complete the charging and discharging processes of the snubber capacitors during the dead

time. Otherwise the IGCTs will be turned ON at an uncontrolled $\mathrm{d}i/\mathrm{d}t$ rate while the connected snubber capacitors are not fully discharged and the energies stored in the snubber capacitors would be dissipated into the IGCTs resulting in the damage of the IGCTs.

In the meantime, it should be kept in mind that the IGCT is a bipolar device. If a bipolar device such as the IGBT or IGCT is turned OFF as soon as the current reaches zero, the remaining charge carriers stored in the device cannot be swept out since there is no current flowing through the device any more. Consequently it results in current spike to sweep out the charge carriers and leads to considerable losses [1], [47]. This dramatic effect is more significant in conduction-optimized IGCT due to the longer charge-carrier lifetime. In accordance with the measurement result accomplished in [1], the minimum turn-OFF loss is obtained not at zero current but at 100 A. This is one of the reasons that a constant turn-OFF current of 100 A is designed in this study.

VIII. Conclusion

A novel high voltage step-up ratio isolated bidirectional soft-switching dc–dc converter is proposed in this paper for interconnection of MVDC and HVDC grids. The proposed converter combines TLCs connected in parallel on the MV side and the MMC on the HV side. Thanks to the dedicated control strategy, the efforts of semiconductor-device series connection can be significantly reduced on the MV side. Consequently the employment of a massive amount of HV insulated transformers is avoided. Compared to the existing solutions, the proposed converter presents low semiconductor losses over a wide power range at variable input/output voltages. Validity of this work is verified by computer simulation and loss calculation.

Appendix A

Parameters of the simulated HVDC cable

Resistance	0.0178 Ω/km
Capacitance	0.275 μF/km
Inductance	0.158 mH/km

References

[1] C. Meyer, "Key components for future offshore dc grids," Ph.D. dissertation, Inst. Power Electron. Electr. Drives, RWTH Aachen Univ., Aachen, Germany, 2007.

[2] H. Rao, "Architecture of Nan'ao multi-terminal VSC-HVDC system and its multi-functional control," *CSEE J. Power Energy Syst.*, vol. 1, pp. 9–18, 2015.

[3] R. W. De Doncker, "Power electronic technologies for flexible dc distribution grids," in *Proc. IEEE Int. Power Electron. Conf.*, 2014, pp. 736–743.

[4] S. Kenzelmann, "Modular dc/dc converter for dc distribution and collection networks," Ph.D. dissertation, Swiss Federal Inst. Technol., Lausanne, Switzerland, 2012.

[5] C. D. Barker, C. C. Davidson, D. R. Trainer, and R. S. Whitehouse, "Requirements of dc-dc converters to facilitate large dc grids," CIGRE Session, 2012.

[6] J. Ferreira, "The multilevel modular dc converter," *IEEE Trans. Power Electron.*, vol. 28, no. 10, pp. 4460–4465, Oct. 2013.

[7] J. Yang, Z. He, H. Pang, and G. Tang, "The hybrid-cascaded dc-dc converters suitable for HVDC applications," *IEEE Trans. Power Electron.*, vol. 30, no. 10, pp. 5358–5363, Oct. 2015.

[8] K. Filsoof and P. Lehn, "A bidirectional modular multilevel dc-dc converter of triangular structure," *IEEE Trans. Power Electron.*, vol. 30, no. 1, pp. 54–65, Jan. 2015.

[9] S. Norrga, L. Ängquist, and A. Antonopoulos, "The polyphase cascaded-cell dc-dc converter," in *Proc. IEEE Energy Convers. Congr. Expo.*, 2013, pp. 4082–4088.

[10] A. Parastar, Y. C. Kang, and J. K. Seok, "Multilevel modular dc/dc converter for high-voltage dc-connected offshore wind energy applications," *IEEE Trans. Ind. Electron.*, vol. 62, no. 5, pp. 2879–2890, May 2015.

[11] Y. Hu, R. Zeng, W. Cao, J. Zhang, and S. J. Finney, "Design of a modular, high step-up ratio dc-dc converter for HVDC applications integrating offshore wind power," *IEEE Trans. Ind. Electron.*, vol. 63, no. 4, pp. 2190–2202, Apr. 2016.

[12] X. Zhang, T. Green, and A. Junyent-Ferré, "A new resonant modular multilevel step-down dc-dc converter with inherent-balancing," *IEEE Trans. Power Electron.*, vol. 30, no. 1, pp. 78–88, Jan. 2015.

[13] W. Lin, J. Wen, and S. Cheng, "Multiport dc-dc autotransformer for interconnecting multiple high-voltage dc systems at low cost," *IEEE Trans. Power Electron.*, vol. 30, no. 12, pp. 6648–6660, Dec. 2015.

[14] G. Kish, M. Ranjram, and P. Lehn, "A modular multilevel dc/dc converter with fault blocking capability for HVDC interconnects," *IEEE Trans. Power Electron.*, vol. 30, no. 1, pp. 148–162, Jan. 2015.

[15] A. Schön and M. M. Bakran, "A new HVDC-dc converter with inherent fault clearing capability," in *Proc. Eur. Conf. Power Electron. Appl.*, 2013, pp. 1–10.

[16] W. Chen, X. Wu, L. Yao, W. Jiang, and R. Hu, "A step-up resonant converter for grid-connected renewable energy sources," *IEEE Trans. Power Electron.*, vol. 30, no. 6, pp. 3017–3029, Jun. 2015.

[17] D. Jovcic, "Bidirectional, high power dc transformer," *IEEE Trans. Power Del.*, vol. 24, no. 4, pp. 2276–2283, Oct. 2009.

[18] S. P. Engel, M. Steineker, N. Soltau, S. Rabiee, H. Stagge, and R. W. De Doncker, "Comparison of the modular multilevel dc converter and the dual-active bridge converter for power conversion in HVDC and MVDC grids," *IEEE Trans. Power Electron.*, vol. 30, no. 1, pp. 124–137, Jan. 2015.

[19] R. W. De Doncker, D. M. Divan, and M. H. Kheraluwala, "A three-phase soft-switched high-power-density dc/dc converter for high-power applications," *IEEE Trans. Ind. Appl.*, vol. 27, no. 1, pp. 63–73, Jan./Feb. 1991.

[20] R. Lenke, "A contribution to the design of isolated dc-dc converters for utility applications," Ph.D. dissertation, E. ON Energy Res. Center, RWTH Aachen Univ., Aachen, Germany, 2012.

[21] W. Li, Q. Jiang, Y. Mei, C. Li, Y. Deng, and X. He, "Modular multilevel dc/dc converters with phase-shift control scheme for high-voltage dc-based systems," *IEEE Trans. Power Electron.*, vol. 30, no. 1, pp. 99–107, Jan. 2015.

[22] A. Mohammadpour, L. Parsa, M. H. Todorovic, R. Lai, R. Datta, and L. Garces, "Series-input parallel-output modular-phase dc-dc converter with soft-switching and high-frequency isolation," *IEEE Trans. Power Electron.*, vol. 31, no. 1, pp. 111–119, Jan. 2016.

[23] G. Ortiz, "High-power dc-dc converter technologies for smart grid and traction applications," Ph.D. dissertation, Swiss Federal Inst. Technol., Zurich, Switzerland, 2014.

[24] T. Lüth, M. M. C. Merlin, T. C. Green, F. Hassan, and C. D. Barker, "High-frequency operation of a dc/ac/dc system for HVDC applications," *IEEE Trans. Power Electron.*, vol. 29, no. 8, pp. 4107–4115, Aug. 2014.

[25] F. Sasongko, M. Hagiwara, and H. Akagi, "A front-to-front (FTF) system consisting of multiple modular multilevel cascade converters for offshore wind farms," in *Proc. IEEE Int. Power Electron. Conf.*, 2014, pp. 1761–1768.

[26] I. A. Gowaid, G. P. Adam, A. M. Massoud, S. Ahmed, and D. Holliday, "Quasi two-level operation of modular multilevel converter for use in a high-power dc transformer with dc fault isolation capability," *IEEE Trans. Power Electron.*, vol. 30, no. 1, pp. 108–123, Jan. 2015.

[27] Z. Xing, X. Ruan, H. You, X. Yang, D. Yao, and C. Yuan, "Soft-switching operation of isolated modular dc/dc converters for application in HVDC grids," *IEEE Trans. Power Electron.*, vol. 31, no. 4, pp. 2753–2765, Apr. 2016.

[28] B. Zhao, Q. Song, J. Li, Y. Wang, and W. Liu, "High-frequency-link modulation methodology of dc-dc transformer based on modular multilevel converter for HVDC application: Comprehensive analysis and experimental verification," *IEEE Trans. Power Electron.*, vol. 32, no. 5, pp. 3413–3424, May 2017.

[29] G. P. Adam, I. A. Gowaid, S. J. Finney, D. Holliday, and B. W. Williams, "Reivew of dc-dc converters for multi-terminal HVDC transmission networks," *IET Power Electron.*, vol. 9, pp. 281–296, 2016.
[30] A. Lesnicar and R. Marquardt, "An innovative modular multilevel converter topology suitable for a wide power range," in *Proc. IEEE Power Tech Conf.*, vol. 3, 2003, 6 p.
[31] J. Forrest and B. Allard, "Thermal problems caused by harmonic frequency leakage fluxes in three-phase, three-winding converter transformers," *IEEE Trans. Power Del.*, vol. 19, no. 1, pp. 208–213, Jan. 2004.
[32] R. W. De Doncker and J. P. Lyons, "The auxiliary resonant commutated pole converter," in *Proc. IEEE Ind. Appl. Soc. Annu. Meeting*, 1990, pp. 1228–1235.
[33] N. Soltau, J. Lange, M. Stieneker, H. Stagge, and R. W. De Doncker, "Ensuring soft-switching operation of a three-phase dual-active bridge dc-dc converter applying an auxiliary resonant-commutated pole," in *Proc. Eur. Conf. Power Electron. Appl.*, 2014, pp. 1–10.
[34] H. Kuhn, "Physikalische Modellbildung von IGCTs für die Schaltungssimulation, " *Ph.D. dissertation*, Technische Universität München, Munich, Germany, 2002 (in German).
[35] T. Setz and M. Lüscher, "Applying IGCTs," *Integrated Gate Commutated Thyristors Application Note*, ABB Switzerland Ltd Semiconductors, Lenzburg, Switzerland, 2007.
[36] H. Lee, J. J. Jung, and S. K. Sul, "A switching frequency reduction and a mitigation of voltage fluctuation of modular multilevel converter for HVDC," in *Proc. IEEE Energy Convers. Congr. Expo.*, 2014, pp. 483–490.
[37] N. Hingorani and L. Gyugi, *Understanding FACTS: Concepts and Technology of Flexible AC Transmission Systems*. Piscataway, NJ, USA: Wiley-IEEE Press, 2000.
[38] B. Oedegard, T. Stiasny, E. Carroll, and M. Rossinelli, "An application-specific asymmetric IGCT," in *Proc. Power Control Intell. Motion Conf.*, 2001.
[39] "The reliable medium-voltage drive with IGCTs," *Sinamics GM150 and SM150 medium-voltage drives*, Siemens AG, Munich, Germany, 2008.
[40] R. Zhang, "Advanced high power industrial drives," in *Proc. IEEE Energy Convers. Congr. Expo.*, Tutorial Session, 2016.
[41] C. Kim, V. Sood, G. Jang, S. Lim, and S. Lee, *HVDC Transmission: Power Conversion Applications in Power Systems*. Hoboken, NJ, USA: Wiley, 2009.
[42] A. Carlson, "Specific requirements on HVDC converter transformers," ABB Transformers AB, Valhallavägen, Sweden, 1996.
[43] S. Cui, S. Kim, J. J. Jung, and S. K. Sul, "A comprehensive cell capacitor energy control strategy of a modular multilevel converter (MMC) without a stiff dc bus voltage source," in *Proc. IEEE Appl. Power Electron. Conf. Expo.*, 2014, pp. 602–609.
[44] J. Shen et al., "Modulation schemes for a 30-MVA IGCT converter using NPC H-bridges," *IEEE Trans. Ind. Appl.*, vol. 51, no. 5, pp. 4028–4040, Sep./Oct. 2015.
[45] J. W. Kolar and J. Huber, "Solid-state transformers: Key design challenges, applicability, and future concepts," in *Proc. IEEE Appl. Power Electron. Conf.*, Tutorial Session, 2016.
[46] M. Das, C. Capell, D. Grider, R. Raju, M. Schutten, and J. Nasadoski, "10 kV, 120 A SiC half H-bridge power MOSFET modules suitable for high frequency, medium voltage applications," in *Proc. IEEE Energy Convers. Congr. Expo.*, 2011, pp. 2689–2692.
[47] G. Ortiz, H. Uemura, D. Bortis, J. Kolar, and O. Apeldoorn, "Modeling of soft-switching losses of IGBTs in high-power high-efficiency dual-active-bridge dc/dc converters," *IEEE Trans. Electron Devices*, vol. 60, no. 2, pp. 587–597, Feb. 2013.
[48] J. Shen, S. Schröder, H. Stagge, and R. W. De Doncker, "Impact of modulation schemes on the power capability of high-power converters with low pulse ratios," *IEEE Trans. Power Electron.*, vol. 29, no. 11, pp. 5696–5705, Nov. 2014.
[49] S. Cui, N. Soltau, and R. W. De Doncker, "A high step-up ratio soft-switching dc-dc converter for interconnection of MVDC and HVDC grids," in *Proc. IEEE Energy Convers. Congr. Expo.*, 2016, pp. 1–8.
[50] J. Dorn, H. Gambach, J. Strauss, and J. Alligan, "HVDC and power electronic system for overhead line and insulated cable applications," Cigre Colloquium, San Francisco, CA, USA, Paper B1-9, 2012.
[51] J. Peralta, H. Saad, S. Dennetière, J. Mahseredjian, and S. Nguefeu, "Detailed and averaged models for a 401-level MMC-HVDC system," *IEEE Trans. Power Del.*, vol. 27, no. 3, pp. 1501–1508, Jul. 2012.
[52] H. W. Dommel, "Digital computer solution of electromagnetic transients in single- and multiphase networks," *IEEE Trans. Power App. Syst.*, vol. PAS-88, no. 4, pp. 388–399, Apr. 1969.
[53] B. Jacobson, P. Karlsson, G. Asplund, L. Harnefors, and T. Jonsson, "VSC-HVDC transmission with cascaded two-level converters," in *Proc. CIGRÉ 2010*, Paris, France, vol. B4–110, 2010.

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