A Dual Half-Bridge Phase-Shifted Converter With Wide ZVZCS Switching Range

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***Abstract*—This paper presents a phase-shifted dual-half-bridge converter, which achieves zero-voltage switching (ZVS) for the leading-leg switches and zero-current switching (ZCS) for the lagging-leg switches. The proposed converter contains two paralleled half-bridge inverters in the primary side. The rectifier stage is composed of six diodes connected with the form of full-bridge rectification. The ZVS condition is created by the output filter inductor and leakage inductor, while the ZCS condition is created by the blocking capacitors. A wide range of soft-switching operation can be achieved with small leakage inductors. Compared with the traditional phase-shifted full-bridge converter, the proposed converter can obtain a three-level output rectified voltage, and the power is transferred from the primary side to the secondary side during the whole period, which can significantly reduce the current ripple of the output filter inductor. In this paper, the operation principle and relevant analysis are presented. A laboratory prototype is built to verify the performance of the proposed converter.**

***Index Terms*—Current ripple, dual half-bridge converter, full-bridge converter, zero-voltage and zero-current switching (ZVZCS).**

NOMENCLATURE

n	Turns ratio of transformer.
C_1	Blocking capacitance of Lagging-leg (in farads).
C_2	Blocking capacitance of Leading-leg (in farads).
$C_{\rm oss}$	junction capacitance of MOSFET (in farads).
T_1	Transformer of lagging half-bridge inverter.
T_2	Transformer of leading half-bridge inverter.
$L_{\rm lk1}$	Leakage inductance of T_1 (in henrys).
$L_{\rm lk2}$	Leakage inductance of T_2 (in henrys).
L_m	Magnetizing inductance of T_2 (in henrys).
L_o	Output filter inductor (in henrys).
D	Duty cycle.
T_s	Switching period (in second).
f_s	Switching frequency (in hertz).
ΔI_m	Current ripple of L_m (in amperes).
ΔV_{C1}	Voltage ripple of C_1 (in volts).
ΔV_{C2}	Voltage ripple of C_2 (in volts).
$V_{\rm in}$	Input voltage (in volts).
V_o	Output voltage (in volts).
I_o	Current of the output filter inductor (in amperes).
$i_{\rm lag}(t)$	Current of lagging-leg (in amperes).
$i_{\rm lea}(t)$	Current of leading-leg (in amperes).
$i_{\rm Lm}(t)$	Magnetizing current (in amperes).
$v_{\rm lea}(t)$	Voltage of leading-leg (in volts).
$v_{\rm lag}(t)$	Voltage of lagging-leg (in volts).
$v_{p1}(t)$	Primary voltage of T_1 (in volts).
$v_{p2}(t)$	Primary voltage of T_2 (in volts).
$v_{C1}(t)$	Voltage of C_1 (in volts).
$v_{C2}(t)$	Voltage of C_2 (in volts).
$v_{\rm rec}(t)$	Rectifier voltage (in volts).
$v_{s1}(t)$	Secondary voltage of T_1 (in volts).
$v_{s2}(t)$	Secondary voltage of T_2 (in volts).
G	Voltage gain.
$t_{\rm ZCS}$	Resetting time (in second).

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I. INTRODUCTION

A FULL-BRIDGE converter with a phase-shifted method can achieve zero-voltage switching (ZVS) without any additional devices, which makes the phase-shifted full-bridge (PSFB) converter well suited for medium- and high-power applications [1]–[3]. However, the traditional PSFB converter has several well-known serious problems. First, the ZVS characteristic is lost under light-load conditions, which leads to low efficiency and high electromagnetic interference [4]. Second, parasitic oscillation across the rectifier increases the voltage stress of devices and output voltage noise [5], [6]. At last, the existence of circulating current during the freewheeling interval significantly increases conduction loss [7].

Several methods [8]–[25] have been proposed to overcome the aforementioned drawbacks. With a wide range of soft-switching operation and a reduction of circulating current, the zero-voltage and zero-current switching (ZVZCS) converters are very attractive solutions [13]–[25]. In the ZVZCS converters, MOSFETs are used in the leading-leg and insulated-gate bipolar transistors (IGBTs) are used as the lagging-leg switches. Compared with MOSFETs, IGBTs have higher voltage rating and power density. However, the maximum switching frequency of an IGBT is limited since the IGBT has high turn-off switching losses due to the tail current characteristic. The zero-current switching (ZCS) technique can significantly reduce the tail current, which is benefit to reduce turn-off losses and to increase switching frequency. The ZCS condition is created by introducing some auxiliary circuits into the secondary or primary side. In [15]–[20], the secondary auxiliary circuits are added to bypass load current

and to absorb the energy stored in the leakage inductance during the freewheeling period, which makes the primary current decay to zero. These converters can obtain higher effective duty cycle of the secondary side than that of the primary side, which is benefit to improve the conversion efficiency. However, the secondary auxiliary circuits increase the voltage rating of rectifier diodes and the output voltage ripple. In the primary-side-assisted converters [21]–[25], a voltage source is introduced into the primary side to reset the current in every half cycle. The primary-side-assisted converters have better performance over the secondary-side-assisted converters in terms of current stresses and the output voltage ripple. However, the power from the primary side cannot be transferred to the output side during the freewheeling interval, which results in large current ripple and low efficiency in variable input voltage applications.

In order to reduce the current ripple or the required output filter inductor, some hybrid-type converters with three-level output rectified voltages have been proposed in [26]–[31]. By integrating two kinds of converters, the energy can be transferred from the primary side to the secondary side during the whole switching period. The hybrid-type converters have many advantages, such as wide ZVS range, reduced circulating current, and lower voltage stress of rectified diodes, which results in high conversion efficiency. However, the hybrid converters need some auxiliary components.

This paper presents a novel ZVZCS converter with phase-shifted control. The proposed converter has the benefits of the hybrid converters presented in [26]–[29], but with fewer auxiliary components. The primary side of the proposed converter consists of a leading half-bridge-inverter (leading-HBI) and a lagging half-bridge-inverter (lagging-HBI). Each HBI contains a blocking capacitor, a transformer, and two switches. In the secondary side, the rectifier stage is composed of six diodes connected with the form of full-bridge rectification. With this structure, the ZCS condition of lagging-HBI and the ZVS condition of leading-HBI can be created. The voltage ripple of the blocking capacitor is used to reset the lagging-HBI current. For the leading-HBI, the ZVS operation can be achieved with a low leakage inductance. Thus, the secondary-voltage oscillation is reduced and the problem of duty-cycle loss is also eliminated.

This paper is organized as follows. In Section II, the operation principle of the proposed converter is described. The relevant analysis and main features are presented in Section III. The design considerations are given in Section IV. The performance of the proposed converter is verified by an experimental prototype with 350–400-V input voltage and 260-V/4-A output in Section V. Finally, the conclusion is given in Section VI.

II. Operation Principle

The circuit diagram of the proposed ZVZCS converter is shown in Fig. 1. The converter is composed of two half-bridge inverters (HBIs) in parallel. Q_1, Q_3, C_1, and T_1 form the lagging-HBI. Q_2, Q_4, C_2 and T_2 form the leading-HBI. The lagging-leg switches are IGBTs and the leading-leg switches are MOSFETs. Two full-bridge rectifiers are employed at the

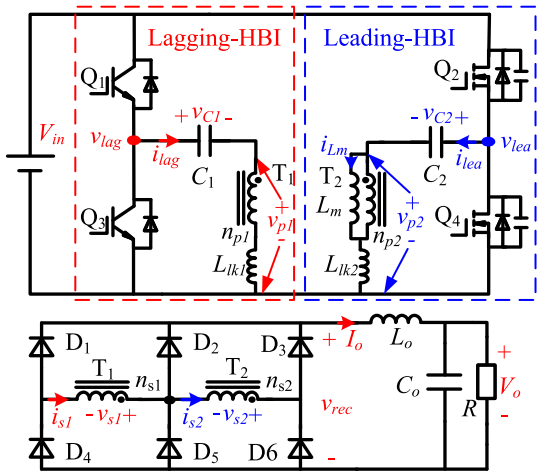

Fig. 1. Proposed ZVZCS dual-half-bridge converter.

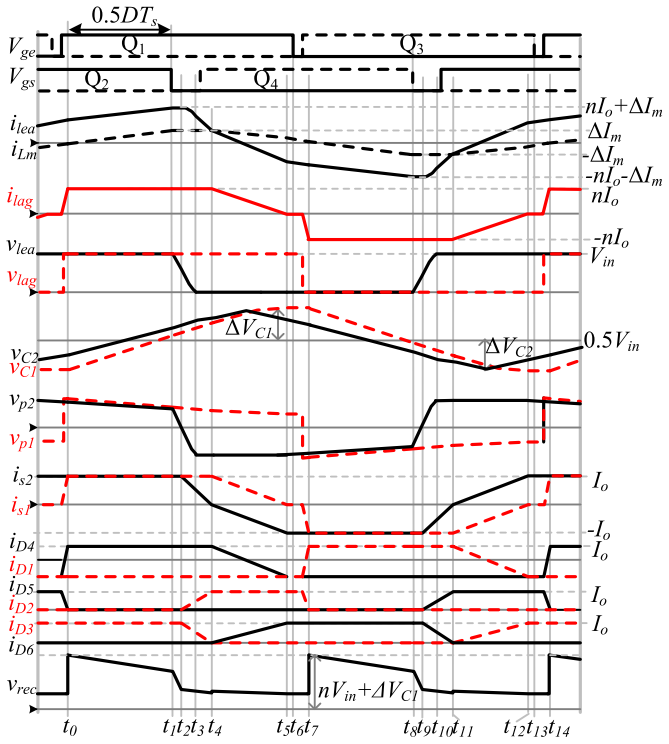

Fig. 2. Key waveforms of the proposed converter.

rectifier stage. The turns ratios $n_p : n_s$ of transformers T_1 and T_2, are 1:n.

In order to simplify analysis, the following assumptions are made:

1) all components are ideal;
2) the junction capacitance of MOSFET is $C_{\rm oss}$;
3) the magnetizing inductance of T_1 is neglected and the leakage inductance is $L_{\rm lk1}$;
4) the magnetizing inductance of T_2 is L_m and the leakage inductance is $L_{\rm lk2}$;
5) the output filter inductor L_o is treated as a constant current source.

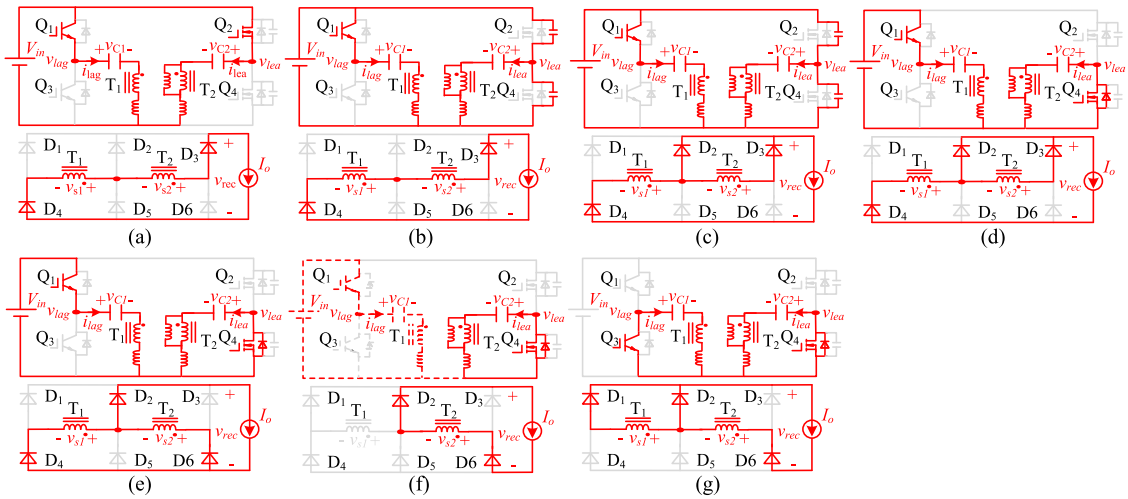

Fig. 3. Topological stages in the half-operation cycle. (a) Mode 1 $[t_0 - t_1]$. (b) Mode 2 $[t_1 - t_2]$. (c) Mode 3 $[t_2 - t_3]$. (d) Mode 4 $[t_3 - t_4]$. (e) Mode 5 $[t_4 - t_5]$. (f) Mode 6 $[t_5 - t_6]$. (g) Mode 7 $[t_6 - t_7]$.

Fig. 2 shows the detailed operating waveforms of the proposed converter in the steady state. D means duty cycle and T_s is the switching period. ΔI_m is the current ripple of L_m. ΔV_{C1} and ΔV_{C2} are the voltage ripple of C_1 and C_2, respectively. The converter is controlled with the phase-shifted method. The duty cycle of primary switches keeps constant (50%) if the dead time is ignored. Based on the voltage-second of the transformer, the average voltages of blocking capacitors v_{C1} and v_{C2} are 0.5 $\mathrm{V_{in}}$. The output voltage is regulated by adjusting the phase-shift time $0.5DT_\mathrm{s}$ between leading-HBI and lagging-HBI. The operating sequence during one switching period can be divided into two half periods, which are $t_0 - t_7$ and $t_7 - t_{14}$. Due to the symmetrical structure, only the first half period is given. Fig. 3 shows the equivalent circuits during the first half period.

Mode 1 $[t_0 - t_1]$: Q_1, Q_2, D_3, and D_4 are in the on-state during this interval. The output filter inductor is reflected to the primary side. The lagging current $i_\mathrm{lag}(t)$ is equal to nI_o. The voltages of blocking capacitors and the magnetizing current $i_{Lm}(t)$ rise from the initial values. The power is transferred to the output side through leading-HBI and lagging-HBI. The voltages in this mode are expressed as

$$v_{C1}(t) = \frac{V_\mathrm{in}}{2} - \Delta V_{C1} + \frac{nI_o}{C_1}(t - t_0) \tag{1}$$

$$v_{C2}(t) = v_{C2}(t_0) + \frac{nI_o + i_{Lm}(t)}{C_2}(t - t_0) \tag{2}$$

$$v_{p1}(t) = \frac{V_\mathrm{in}}{2} + \Delta V_{C1} - \frac{nI_o}{C_1}(t - t_0) \tag{3}$$

$$v_{p2}(t) = V_\mathrm{in} - v_{C2}(t_0) - \frac{nI_o + i_{Lm}(t)}{C_2}(t - t_0) \tag{4}$$

$$v_\mathrm{rec}(t) = nv_{p1}(t) + nv_{p2}(t) \tag{5}$$

$$i_{Lm}(t) = i_{Lm}(t_0) + \frac{v_{p2}(t)}{L_m}(t - t_0). \tag{6}$$

Mode 2 $[t_1 - t_2]$: At time t_1, Q_2 is turned OFF. To simplify analysis, the voltages of blocking capacitors and the magnetizing current are considered to reach the maximum values, respectively. The junction capacitances of Q_2 and Q_4 are discharged linearly by a constant current source $nI_\mathrm{o} + \Delta I_m$. The voltage of leading-leg $v_\mathrm{lea}(t)$, the primary voltage of T_2 $v_{p2}(t)$, and the rectifier voltage $v_\mathrm{rec}(t)$ start to decrease linearly. The voltages and currents of lagging-leg are maintained constant. The voltages in this mode are expressed as

$$v_{C1}(t) = \frac{V_\mathrm{in}}{2} + \Delta V_{C1} \tag{7}$$

$$v_{C2}(t) = \frac{V_\mathrm{in}}{2} + \Delta V_{C2} \tag{8}$$

$$v_{p1}(t) = \frac{V_\mathrm{in}}{2} - \Delta V_{C1} \tag{9}$$

$$v_{p2}(t) = \frac{V_\mathrm{in}}{2} - \Delta V_{C2} - \frac{nI_o + \Delta I_m}{2C_\mathrm{oss}}(t - t_1). \tag{10}$$

Mode 3 $[t_2 - t_3]$: When $v_{p2}(t)$ falls to zero at t_2, the middle voltage of leading-leg $v_\mathrm{lea}(t)$ is $0.5V_\mathrm{in} + \Delta V_{C2}$. At the same time, D_2 starts to conduct and the secondary winding of T_2 is shorted. The resonance between junction capacitances and leakage inductance of T_2 occurs in the primary side. The key currents and voltages are calculated as follows:

$$i_\mathrm{lea}(t) = (nI_o + \Delta I_m)\cos\omega(t - t_2) \tag{11}$$

$$v_\mathrm{lea}(t) = \frac{V_\mathrm{in}}{2} + \Delta V_{C2} - \sqrt{\frac{L_{lk2}}{2C_\mathrm{oss}}}(nI_o + \Delta I_m)\sin\omega(t - t_2) \tag{12}$$

where $\omega = \frac{1}{\sqrt{2L_{lk2}C_\mathrm{oss}}}$

Mode 4 $[t_3 - t_4]$: *Mode 4* begins when $v_\mathrm{lea}(t)$ falls to zero. The body diode of Q_4 starts to conduct and Q_4 can be turned ON with zero voltage. The voltages and currents of lagging-leg are continuously maintained constant. The voltage across L_lk2 is $-(0.5V_\mathrm{in} + \Delta V_{C2})$, which leads to $i_\mathrm{lea}(t)$ decreasing linearly. *Mode 4* ends when $i_\mathrm{lea}(t)$ reaches the maximum current of

magnetizing inductor at t_4. $i_{\rm lea}(t)$ is given by

$$i_{\rm lea}(t) = i_{\rm lea}(t_3) - \frac{0.5V_{\rm in} + \Delta V_{C2}}{L_{\rm lk2}}(t - t_3). \tag{13}$$

Mode 5 $[t_4 - t_5]$: The secondary winding current of T_2 falls to zero at time t_4; thus, diode D_3 is turned OFF and T_2 comes out from the shorted status. The secondary voltage of T_2 $v_{s2}(t)$ is $-n(0.5V_{\rm in} + \Delta V_{C2})$ and the secondary voltage of T_1 $v_{s1}(t)$ is $n(0.5V_{\rm in} - \Delta V_{C1})$. Since the sum of $v_{s1}(t)$ and $v_{s2}(t)$ is less than zero, D_6 starts to conduct. The secondary windings of T_1 and T_2 are connected in parallel. The leading-HBI current rises in the negative direction while the lagging-HBI current falls. The voltages and currents of leakage inductances are given by

$$v_{\rm lk1}(t) = -\frac{L_{\rm lk1}}{L_{\rm lk1} + L_{\rm lk2}}(\Delta V_{C1} + \Delta V_{C2}) \tag{14}$$

$$v_{\rm lk2}(t) = -\frac{L_{\rm lk2}}{L_{\rm lk1} + L_{\rm lk2}}(\Delta V_{C1} + \Delta V_{C2}) \tag{15}$$

$$i_{\rm lag}(t) = nI_o + \frac{v_{\rm lk1}(t)}{L_{\rm lk1}}(t - t_4) \tag{16}$$

$$i_{\rm lea}(t) = \Delta I_m + \frac{v_{\rm lk2}(t)}{L_{\rm lk2}}(t - t_4). \tag{17}$$

At t_5, $i_{\rm lag}$(t) falls to zero, $i_{\rm lea}(t)$ reaches $-nI_{\rm o} + \Delta I_m$ and D_4 is naturally turned OFF.

Mode 6 $[t_5 - t_6]$: During this mode, the lagging-leg current is zero. Thus, the power is only transferred to the output side through the leading-HBI. $v_{C2}(t)$ and $v_{\rm rec}(t)$ decreases since $i_{\rm lea}(t)$ discharges C_2. The magnetizing current decreases from the maximum value. The currents and voltages are expressed as follows:

$$v_{C2}(t) = -v_{p2}(t) = \frac{V_{\rm in}}{2} + \Delta V_{C2} + \frac{-nI_o + i_{Lm}(t)}{C_2}(t - t_5) \tag{18}$$

$$i_{Lm}(t) = \Delta I_m + \frac{v_{p2}(t)}{L_m}(t - t_5). \tag{19}$$

Mode 7 $[t_6 - t_7]$: Q_1 is turned OFF at t_6. As the lagging-leg current is zero, Q_1 is turned OFF with zero current. After a short time, Q_3 is turned ON with zero current since $L_{\rm lk1}$ limits the rise rate of current. D_1 starts to conduct at the same time. The secondary winding of T_1 is shorted. Thus, the voltage of C_1 appears on $L_{\rm lk1}$, $i_{\rm lag}(t)$ starts to rise in the negative direction. The voltages and currents of leading-leg are nearly constant. The lagging-leg current is given by

$$i_{\rm lag}(t) = -\frac{0.5V_{\rm in} + \Delta V_{C1}}{L_{\rm lk1}}(t - t_6). \tag{20}$$

At t_7, $i_{\rm lag}(t)$ rises to the reflected output current. At the same time, the commutation between D_1 and D_2 is completed. D_2 is naturally turned OFF. Both the leading-HBI and the lagging-HBI can transfer the power to the output side. The operations during $[t_7 - t_{14}]$ are similar to the previous analysis.

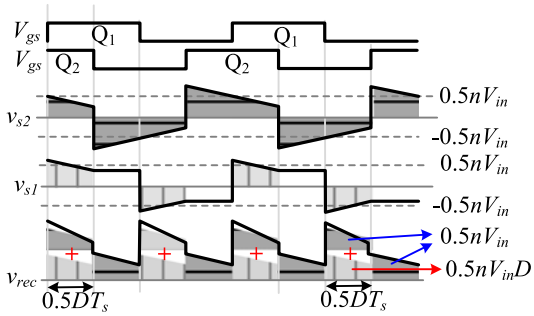

Fig. 4. Simplified waveforms of secondary voltages.

III. Analysis of the Converter

A. Voltage Ripples of the Blocking Capacitors

Since the durations of leading-HBI and lagging-HBI transitions are very narrow, they can be ignored to simplify analysis. When Q_2 is turned ON, C_2 is charged, and it is discharged when Q_2 is turned OFF. The average magnetizing current of T_2 is zero during charging C_2, so the effect of magnetizing current on the voltage ripple can be ignored. The voltage ripple of C_2 is calculated as follows:

$$\Delta V_{C2} = \frac{nI_oT_s}{4C_2}. \tag{21}$$

C_1 is charged during the first duty-cycle interval and is discharged during the next duty-cycle interval. The voltage of C_1 remains unchanged during the freewheeling interval since the lagging-HBI current is zero. The voltage ripple of C_1 is

$$\Delta V_{C1} = \frac{nI_oDT_s}{4C_1}. \tag{22}$$

B. Voltage Gain Analysis

Only *Mode 1* and *Mode 6* are investigated once the durations of leg's transition are ignored. The simplified waveforms of secondary voltage can be shown as in Fig. 4.

The output voltage is equal to the average voltage of rectifier. Thus, the output voltage can be calculated as

$$V_o{=}0.5nV_{\rm in} + 0.5nV_{\rm in}D. \tag{23}$$

The voltage gain is given by

$$G(D) = \frac{V_o}{nV_{\rm in}} = \frac{1 + D}{2}. \tag{24}$$

For the traditional PSFB converter, duty-cycle loss is one of the main drawbacks, which significantly affects the voltage gain [32]. In this paper, duty-cycle loss is ignored to simplify analysis. The voltage gain of the traditional PSFB converter can be simplified as follows:

$$G(D) = \frac{V_o}{nV_{\rm in}} = D. \tag{25}$$

Fig. 5 shows the curves of voltage gain. Compared with the traditional PSFB converter, the proposed converter can obtain higher gain. Therefore, the turns of secondary winding in the proposed converter can be reduced, which is benefit to improve

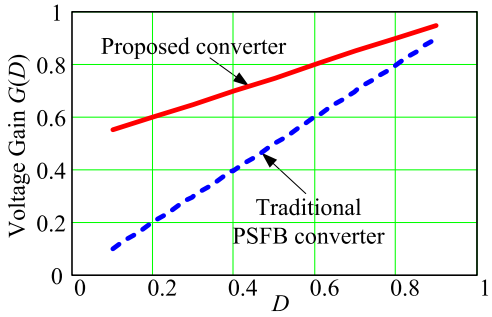

Fig. 5. Voltage gain versus duty cycle.

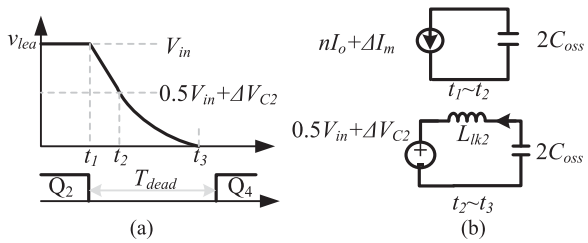

Fig. 6. ZVS operation of leading-leg. (a) Key waveforms. (b) Simplified equivalent circuit.

the efficiency especially for the applications with high output current and low output voltage.

The rectifier voltage of the traditional PSFB converter is zero in the freewheeling interval and the power from the primary side cannot be transferred to the output side. However, for the proposed converter, the rectifier voltage is nonzero, as shown in Fig. 4, and the power can be transferred to the output side in the whole switching period. Therefore, the current ripple can be reduced, which is benefit for the reduction of conduction and magnetic core losses.

C. ZVS Condition for the Leading-Leg

For the leading-leg switches, the ZVS operation is achieved in $[t_1, t_3]$, which is divided into two phases, as shown in Fig. 6. In the first phase, the middle voltage of leading-leg $v_{\rm lea}(t)$ is decreased linearly by the energies stored in L_m and L_o. The transition time of the first phase is given by

$$T_{12} = \frac{2C_{\rm oss}(0.5V_{\rm in} - \Delta V_{C2})}{\Delta I_m + nI_o}. \tag{26}$$

When $v_{\rm lea}(t)$ reaches $0.5V_{\rm in} + \Delta V_{C2}$ at t_2, the secondary winding of T_2 is shorted. Then, $v_{\rm lea}(t)$ is decreased with a sinusoidal waveform, which is caused by the resonance between the junction capacitances and the leakage inductance of T_2. The resonance voltage reaches a minimum at one-fourth of the resonant period

$$\delta_{23} = \frac{\pi}{2}\sqrt{2L_{\rm lk2}C_{\rm oss}}. \tag{27}$$

In order to ensure that all the energy stored in $L_{\rm lk2}$ is available to discharge the junction capacitances, the dead time between the gate signals of Q_2 and Q_4 should satisfy the following inequality:

$$T_{\rm dead} > T_{12} + \delta_{23}. \tag{28}$$

The ZVS condition for leading-leg switches is obtained from (12) as follows:

$$\frac{1}{2}L_{\rm lk2}(nI_o + \Delta I_m)^2 > C_{\rm oss}\left(\frac{V_{\rm in}}{2} + \Delta V_{C2}\right)^2. \tag{29}$$

Ignoring the voltage ripple of C_2, ΔI_m can be derived as

$$\Delta I_m = \frac{V_{\rm in}}{8L_m f_s}. \tag{30}$$

As seen in (29), the energy stored in the junction capacitances, which should be discharged completely by $L_{\rm lk2}$, is smaller than the total energy. Moreover, the current of magnetizing inductor is benefit to realize the ZVS operation, and it is independent of load current. Therefore, the leading-leg switches can achieve ZVS operation over a wide load range.

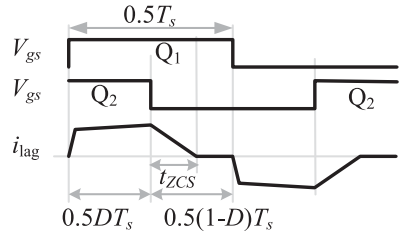

Fig. 7. ZCS condition for the lagging-leg.

D. ZCS Condition for the Lagging-Leg

During *Mode 5*, the lagging-leg current is reset by the voltage ripples of blocking capacitors. The resetting time is derived from (16)

$$t_{\rm ZCS} = \frac{4C_1C_2(L_{\rm lk1} + L_{\rm lk2})f_s}{C_1 + DC_2}. \tag{31}$$

In order to achieve ZCS operation, the gate pulses of lagging-leg switches should be maintained until the current decays to zero. According to Fig. 7, the ZCS condition is given by

$$t_{\rm ZCS} < 0.5T_s(1 - D). \tag{32}$$

To simplify the analysis, C_1 is equal to C_2. According to (31) and (32), the following inequality can be obtained:

$$\frac{4C_1(L_{\rm lk1} + L_{\rm lk2})f_s}{1 + D} < 0.5T_s(1 - D). \tag{33}$$

Equation (33) can be represented as

$$D < \sqrt{1 - 8C_1(L_{\rm lk1} + L_{\rm lk2})f^2}. \tag{34}$$

Therefore, $D = D_{\rm max}$ is the global worst case. If $D_{\rm max}$ satisfies the condition (34), the lagging-leg can achieve ZCS over the entire line and load range.

E. Voltage Stress of the Semiconductors

The voltages of primary switches are clamped to the input voltage. The maximum voltages of rectifier diodes can be

TABLE I
PARAMETERS OF THE PROTOTYPE

Item	Symbol	Value/Part
Input Voltage	$V_{\rm in}$	350–400 V
Output Voltage	V_o	260 V
Output Current	I_o	4 A
Switching Frequency	f_s	100 kHz
Primary Switches	$Q_1\ Q_3$	IGW20N60H3
	$Q_2\ Q_4$	SPW20N60C3
Rectifier Diodes	$D_1 - D_6$	IDH08SG60C

obtained based on Fig. 4. The voltage stress of D_1, D_3, D_4, and D_6 is equal to $nV_{\rm in} + n\Delta V_{C1}$, and the voltage stress of D_2 and D_5 is $0.5nV_{\rm in} + n\Delta V_{C2}$. The voltage stress of D_2 and D_5 is lower than that of others. Therefore, D_2 and D_5 can employ the lower voltage-rated diodes to improve efficiency and to save cost.

F. Blocking Capacitors

Based on the aforementioned analysis, the values of blocking capacitors have an important influence on the performance of the proposed converter. In order to extend the ZVS range of leading-leg and to reduce the voltage stress of rectifier diodes, the values of blocking capacitors should be as large as possible. Conversely, the values should be minimized to reduce the resetting time. Therefore, a tradeoff should be made in selecting the values of blocking capacitors. In general, the voltage ripple of blocking capacitor is set around 5% of V_{in}.

IV. DESIGN CONSIDERATIONS

The design considerations of the converter are illustrated in this section. The parameters are listed as in Table I.

A. Magnetics Design

The converter should be able to regulate output voltage when input voltage is the minimum. Considering the resetting and transition times, the maximum duty cycle $D_{\max}$ is 0.75 at the lowest input voltage. The turns ratio is determined from (24) as

$$n=\frac{2V_o}{(1+D_{\max})V_{\text{in\_min}}}=\frac{2\times 260}{(1+0.75)\times 350}=0.85. \quad (35)$$

The voltage across the primary windings of transformer is about $0.5V_{\rm in}$. The number of primary turns is calculated as follows:

$$n_p=\frac{V_{\rm in}}{8f_sB_mA_e} \quad (36)$$

where B_m means maximum magnetic flux density, and A_e means effective cross-sectional area.

The transformers are made using PC47P*Q*35/35Z-12 from TDK company, and $B_m = 0.15\,\text{T}, A_e = 196\,\text{mm}^2$. The number of primary turns is 20 and the number of secondary turns is 17. The specifications of the lagging-HBI transformer are measured as follows: $L_{\rm m1} = 2\,\text{mH}$ and $L_{\rm lk1} = 1.5\,\mu\text{H}$. The leakage inductance is measured by electrically shorting the secondary winding. This measured value corresponds to the sum of the primary winding leakage inductance and the reflected leakage inductance of the secondary winding on the primary side [34]. The maximum magnetizing current of the leading-HBI transformer is selected as 1.2 A. The value of L_m is determined from (30) as

$$L_m=\frac{V_{\rm in}}{8\Delta I_m f_s}=416\,\mu\text{H}. \quad (37)$$

To obtain the specified L_m, the gap of T_2 is set as about 0.5 mm. The specifications of T_2 are measured as follows: $L_m = 390\,\mu\text{H}$ and $L_{\rm lk2} = 5\,\mu\text{H}$. The current ripple of L_m is 1.3 A.

A reduction in magnetizing inductance is an effective way to achieve a wide ZVS range. However, this approach increases the current stress of primary components and leads to more conduction losses. Ignoring the transition time, the simplified primary currents are shown in Fig. 8. As shown in Fig. 8, the magnetizing current never flows through the lagging-leg switches Q_1, Q_3, and the current stress of lagging-leg is not increased.

For the proposed converter, the RMS currents flow through switches are expressed as

$$i_{Q1Q3}=nI_o\sqrt{\frac{D}{2}} \quad (38)$$

$$i_{Q2Q4}=\frac{\sqrt{2}}{2}nI_o\sqrt{1+\frac{1}{3}\left(\frac{\Delta I_m}{nI_o}\right)^2}. \quad (39)$$

Fig. 9 shows the RMS currents versus load current at $D = 0.5$. It clearly shows that the contribution of magnetizing current to the total RMS current can be negligible, especially at heavy loads. Consequently, a reduction in magnetizing inductance has a little impact on the conduction losses in the proposed converter.

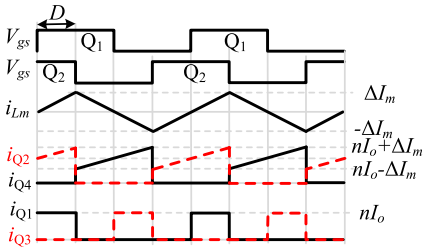

Fig. 8. Simplified currents through the primary switches.

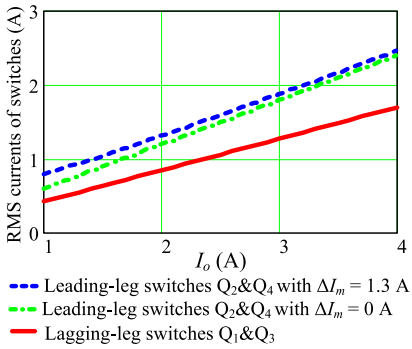

Fig. 9. RMS currents versus load current.

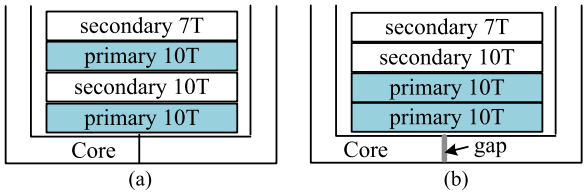

Fig. 10. (a) Winding position of T_1. (b) Winding position of T_2.

Fig. 10 shows the winding position of T_1 and T_2. To reduce the leakage inductance of T_1, interleaving windings with two primary layers and two secondary layers are adopted. For the windings of T_2, the primary and secondary layers are separated. This structure provides a relatively high leakage inductance and there is no need to use an extra inductor. However, it is difficult to design a transformer with a precisely specified leakage inductance, and an extra inductor can be adopted to reach the specified value in practice.

B. Selection of Blocking Capacitors

In order to realize $\Delta V_{C1} = \Delta V_{C2} = 0.05V_{\rm in}$, the values of blocking capacitors are calculated according to (21) and (22)

$$C_2 = \frac{nI_oT_s}{4\Delta V_{C2}} = 425\,\text{nF} \tag{40}$$

$$C_1 = \frac{nI_oDT_s}{4\Delta V_{C1}} = 212\,\text{nF}. \tag{41}$$

We choose $C_1 = C_2 = 390\,\text{nF}$, The maximum voltage ripples of C_1 and C_2 are calculated as follows:

$$\Delta V_{C1} = \frac{nI_oDT_s}{4\Delta C_1} = \frac{0.85\times 4\,\text{A}\times 0.75\times 10\,\mu\text{s}}{4\times 390\,\text{nF}} = 16\,\text{V} \tag{42}$$

$$\Delta V_{C2} = \frac{nI_oT_s}{4C_2} = \frac{0.85\times 4\,\text{A}\times 10\,\mu\text{s}}{4\times 390\,\text{nF}} = 22\ \text{V}. \tag{43}$$

C. Verification of the ZVS Condition

At 20% of the full load, the available energy stored in the leakage inductance is

$$E_{\rm avi} = \frac{1}{2}L_{\rm lk2}(nI_O + \Delta I_{\rm m})^2 = 9.8\,\mu\text{J}. \tag{44}$$

The required energy for ZVS operation is

$$E_{\rm req} = C_{\rm oss}\left(\frac{V_{\rm in}}{2} + \Delta V_{C2}\right)^2. \tag{45}$$

$E_{\rm req}$ can be directly obtained from the datasheet of MOSFET [33]. The maximum stored energy of junction capacitances, which should be discharged by $L_{\rm lk2}$, is about 6 μJ. Therefore, the ZVS condition is satisfied and the leading-leg switches can achieve ZVS operation over a wide range of load current. When $L_m = 390\,\mu\text{H}$, $L_{\rm lk2} = 5\,\mu\text{H}$, and $C_{\rm oss} = 160\,\text{pF}$, δ_{23} is 63 ns and the value of T_{12} is between 13 and 50 ns. Considering the design margin for the real implementation, the dead time of leading-leg switches is set as 140 ns.

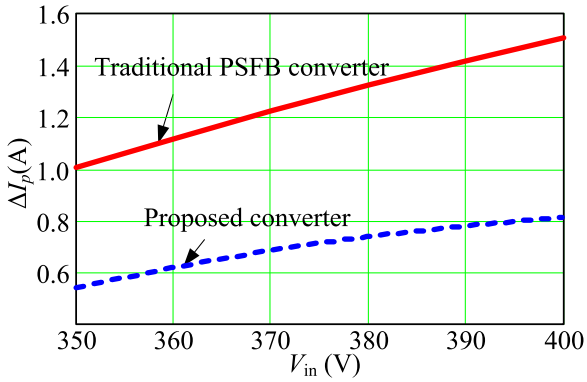

Fig. 11. Current ripple versus input voltage.

D. Verification of the ZCS Condition

The resetting time is determined from (31) as

$$t_{\rm ZCS} = \frac{4C_1C_2(L_{\rm lk1}+L_{\rm lk2})f_s}{C_1 + D_{\max}C_2} = 0.55\,\mu\text{s}. \tag{46}$$

The maximum duty cycle $D_{\max}$ is 0.75 and the allowable resetting time is 1.25 μs according to (32). Thus, the ZCS condition is satisfied and the lagging-leg switches can achieve ZCS operation.

E. Current Ripple

The rectifier voltage of the traditional PSFB converter is zero in the freewheeling interval, and the power from the primary side cannot be transferred to the output side. However, for the proposed converter, the rectifier voltage is nonzero, as shown in Fig. 4, and the power from the primary side is transferred to the output side in the whole switching period. Therefore, the current ripple can be significantly reduced.

In the traditional PSFB converter, the voltage across output filter inductor is $nV_{\rm in} - V_o$ in the duty-cycle interval, while the value is $-V_{\rm o}$ in the freewheeling interval. The current ripple of output filter inductor in the traditional PSFB converter is given by

$$\Delta I_{\rm tra} = \frac{V_o}{4f_sL_{\rm o}}(1-D). \tag{47}$$

In the proposed converter, the voltage ripple of the blocking capacitor is neglected to simplify analysis. The voltage applied on L_o is $0.5nV_{\rm in} - V_o$ in the freewheeling interval. The current ripple of L_o is calculated as

$$\Delta I_{\rm pro} = \frac{V_o}{4f_sL_o}\frac{D(1-D)}{1+D}. \tag{48}$$

Fig. 11 shows the relationship between the current ripple of the output filter inductor and the input voltage at $L_o = 130\,\mu\text{H}$. Compared with the traditional PSFB converter, the reduction of current ripple in the proposed converter is about 50% under the input voltage range.

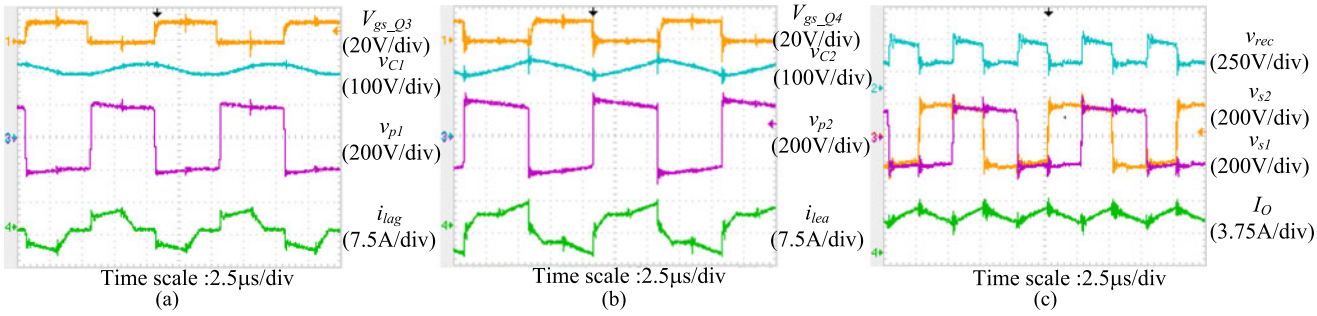

Fig. 12. Experimental waveforms at $V_{\rm in} = 400\,{\rm V}$ and $I_o = 4\,{\rm A}$. (a) Lagging-HBI. (b) leading-HBI. (c) Secondary waveforms.

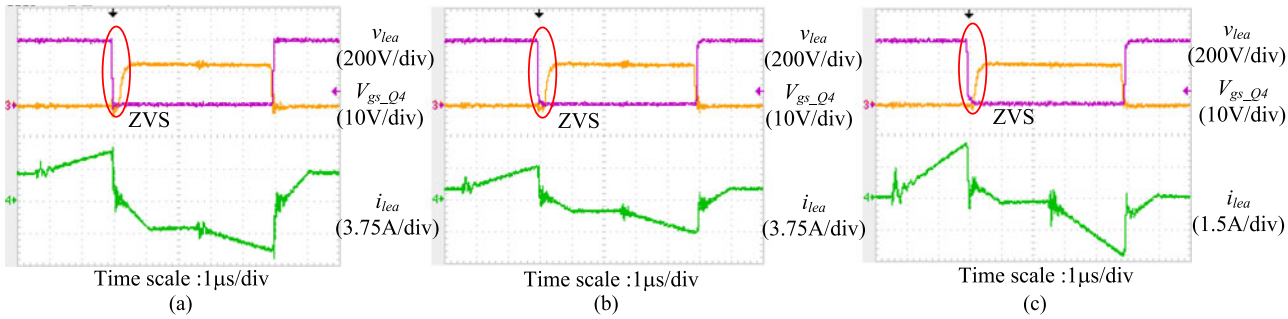

Fig. 13. ZVS waveforms of leading-HBI at $V_{\rm in} = 400$ V. (a) Full load. (b) 50% of full load. (c) 20% of full load.

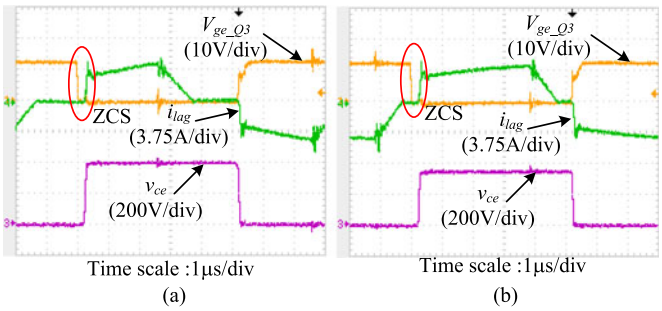

Fig. 14. ZCS waveforms at full load. (a) $V_{\rm in} = 400\,{\rm V}$. (b) $V_{\rm in} = 350\,{\rm V}$.

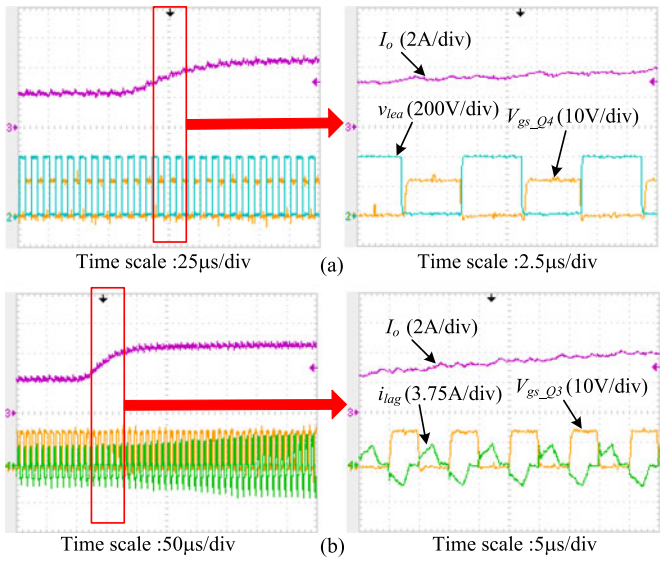

Fig. 15. Soft-switching waveforms during load change. (a) ZVS waveforms. (b) ZCS waveforms.

V. Experimental Results

An experimental prototype was built to demonstrate the performance of the proposed converter. In order to alleviate the secondary voltage oscillation caused by the leakage inductances and junction capacitances of rectifier diodes, the RCD-snubber circuit ($R = 5\,{\rm k}\Omega/2{\rm W}$, $C = 220\,{\rm nF}/630\,{\rm V}$, $D =$ UF4007) introduced in [35] is employed. Fig. 12 shows the experimental waveforms at $V_{\rm in} = 400\,{\rm V}$ and $I_o = 4\,{\rm A}$. The experimental waveforms coincide well with the theoretical waveforms described in Fig. 2. Fig. 12(a) shows the key waveforms of lagging-HBI. The lagging-HBI current falls to zero during the freewheeling interval. Fig. 12(b) shows the key waveforms of leading-HBI. The leading-HBI can transfer power to the secondary side during the whole switching period. Fig. 12(c) shows the key secondary waveforms. The rectifier voltage is nonzero, which makes the current ripple of filter inductor reduced. Due to the low leakage inductances, the secondary-voltage oscillation is weakened. Moreover, the problem of duty-cycle loss is eliminated.

Fig. 13 shows the ZVS experimental waveforms of leading-HBI at different output currents. It can be noted that the leading-HBI switches can be turned ON with zero voltage under a wide range of load conditions. Fig. 14 shows the ZCS experimental waveforms of lagging-HBI at different input voltages.

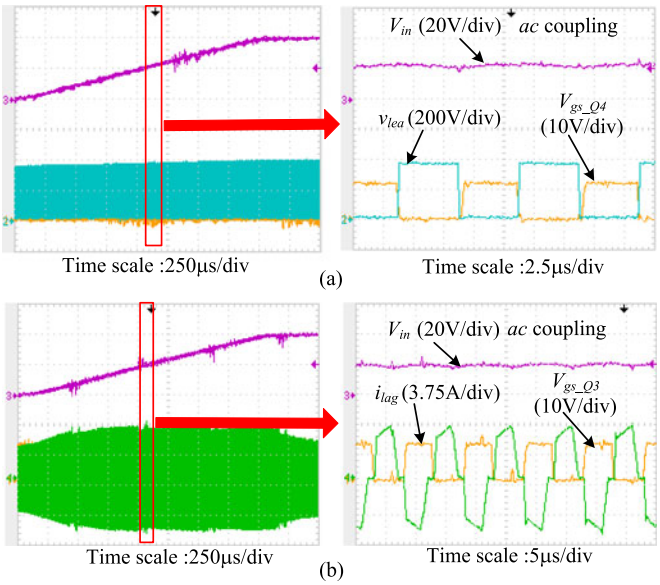

Fig. 16. Soft-switching waveforms during input voltage change. (a) ZVS waveforms. (b) ZCS waveforms.

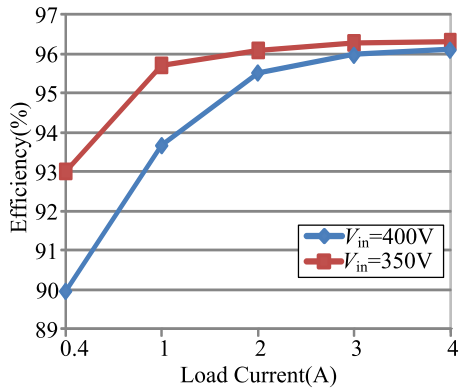

Fig. 17. Measured efficiency at different input voltages.

The lagging-HBI switches are turned OFF with zero current. Figs. 15 and 16 show the key soft-switching waveforms during load current and input voltage changes. The load current is changed from 50% load to 100% load (2–4 A), and the input voltage is increased from 350 to 400 V. The experimental results confirm that the primary switches are operated with soft-switching characteristic under the dynamic input and load conditions. Fig. 17 shows the measured efficiency curves at different input voltages. The maximum efficiency is 96.3% at $V_{\rm in} = 350\,{\rm V}$ and $I_o = 4\,{\rm A}$.

VI. Conclusion

This paper proposed a novel ZVZCS dual-half-bridge converter. The ZCS condition is determined by the voltage ripple of the blocking capacitor, while the ZVS condition is created by the output filter inductor and leakage inductor. An experimental prototype was built to demonstrate the performance of the proposed converter. Compared with the traditional PSFB converter, the proposed converter has the following advantages.

1) The lagging-HBI switches are turned OFF with ZCS over the entire load and line ranges. Although the leakage inductance is set as a small value, the leading-HBI switches can achieve a wide range of ZVS operation. Due to the low leakage inductance, the secondary-voltage oscillation is weakened.
2) For the proposed converter, the output rectified voltage is a three-level waveform and the power is transferred from the primary side to the secondary side during the whole period. The current ripple of the output filter inductor is significantly reduced.

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