A Dead-Time-Controlled Gate Driver Using Current-Sense FET Integrated in SiC MOSFET

Akimasa Niwa, *Member, IEEE*, Takanori Imazawa, Ryota Kojima, Masahiro Yamamoto, Takanari Sasaya, Takanori Isobe, *Member, IEEE*, and Hiroshi Tadano, *Member, IEEE*

***Abstract*—In comparison with silicon IGBT, silicon carbide (SiC) MOSFET is expected to reduce the switching loss and the conduction loss and to remove external freewheeling diodes (FWDs). However, its body diode has comparatively high forward voltage; therefore, the diode conduction loss generated during dead time increases. As a result, the loss reduction by the use of the SiC MOSFET can be weakened. This paper proposes a simple dead-time controller integrated in an isolated gate driver in order to reduce the diode conduction loss during the dead time. The proposed method has high speed and high robustness against switching noise by using of a current-sense FET with small parasitic capacitance. As a result, the diode conduction time can be shortened within 0.1 μs. In addition, the proposed dead-time control method can be achieved by existing components, including the current-sense FET, which is currently used for short-circuit current detection in hybrid vehicle applications. The proposed method was applied to a 10 kW boost converter with SiC MOSFET. The experimental results showed 1% higher efficiency of the converter with the proposed dead-time-controlled gate driver compared to that without dead-time control circuit, and the efficiency was the similar level as when a SiC Schottky barrier diode (SBD) was used as FWDs.**

***Index Terms*—Body diode conduction loss, dead-time control, gate driver, MOSFET, silicon carbide (SiC).**

I. Introduction

SILICON(Si) IGBT is currently used for in-vehicle inverter systems as a power semiconductor device. However, its electrical performance approaches are theoretically limited. Therefore, silicon carbide (SiC) devices or gallium nitride (GaN) devices are expected as the next-generation power semiconductor devices [1]. In comparison with Si IGBT, SiC MOSFET is expected to reduce the switching loss and the conduction loss. It is also expected to remove external freewheeling diodes (FWD) by using its body diode.

In comparison with Si IGBT, SiC MOSFET is expected to reduce the switching loss and the conduction loss and to remove external freewheeling diodes (FWD) by using its body diode. However, SiC MOSFET body diode has a high forward voltage; therefore, the diode conduction loss during dead time increases. As a result, the loss reduction effect by the use of SiC MOSFET can be weakened.

For such problems, some approaches from both circuit and device technologies have been reported [4]–[24]. For example, connecting SiC SBD in antiparallel to the MOSFET have been reported in [4]–[6], integrating low forward voltage drop diode with MOSFET have been reported in [7], and gate drive circuit approaches shortening dead time have been reported in [8]–[24]. The circuit approaches are the most effective for cost down of SiC MOSFET. However, they still have some problems such as the possible remaining body diode conduction and need for extra components, which increase the difficulty to achieve integrated circuit board and intelligent power module.

In contrast to high-voltage applications, many dead-time shortening methods have been proposed for the low-voltage converter [8]–[15]. These methods are referred as dynamic dead-time control methods, which monitor gate-source voltage of the opposite-side device or drain-source voltage of the target-side device in order to shorten the dead time. However, these methods require high withstanding voltage elements of voltage detection circuits for the high-voltage applications such as a hybrid electric vehicle (HEV) inverter system. Therefore, isolated gate drivers must be fabricated with high-voltage IC technology or external components such as isolators need to be added to the driver; this is a significant issue for HEV inverter system that requires high integration of circuit elements.

On the other hand, some improved methods for high-voltage applications have been proposed [16]–[19]. One method to detect the switching time by utilizing the parasitic capacitance of power devices has been proposed, and it has been reported that the dead time of 15 ns was able to be achieved [19]. However, those methods have been applied to only the voltage-source converter with a constant dc voltage, which is constructed of one-leg half-bridge. The reason for that is difficulty in detecting the switching time accurately over the noise current affected by other leg switching and dc-link voltage change. Therefore, it is difficult to implement these methods to the variable input inverter such as the HEV inverter system.

In addition to aforementioned concepts, dead-time control methods based on the measured load current [20], [21], diode conduction detecting techniques for a three-phase inverter [22], [23], and a sensor-less technique [24] have been proposed. How-

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A. Niwa, T. Imazawa, R. Kojima, M. Yamamoto, and T. Sasaya are with the Research Division 3, DENSO Corporation, Kariya 448-8661, Japan (e-mail: akimasa_niwa@denso.co.jp; takanori_imazawa@denso.co.jp; ryota_kojima@denso.co.jp; masahiro_b_yamamoto@denso.co.jp; takanari_sasaya@denso.co.jp).

T. Isobe and H. Tadano are with the Institute of Applied Physics, University of Tsukuba, Tsukuba 305-8573, Japan (e-mail: isobe.takanori.gf@u.tsukuba.ac.jp; tadano.hiroshi.fn@u.tsukuba.ac.jp).

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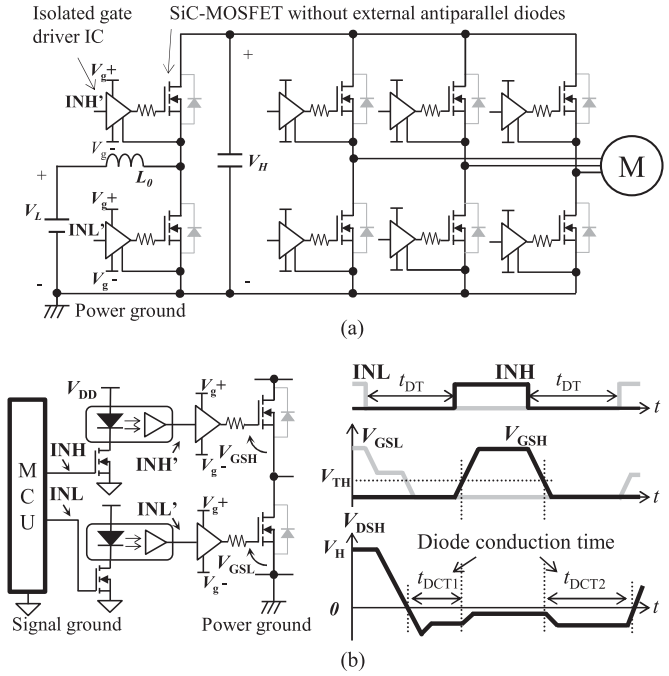

Fig. 1. Schematic of HEV inverter system. (a) SiC MOSFET based HEV inverter system. (b) Isolated gate drive circuit and timing diagram indicating dead time t_{DT} and diode conduction time t_{DCT1} and t_{DCT2}.

ever, it can be said that it is difficult to shorten the dead time in HEV inverter system by the existing solutions since accurate current sensing in the wide load range is difficult. In addition, the number of isolators and the dead-time calculation time are increased.

This paper proposes a simple dead-time shortening technique for the HEV inverter system. The proposed technique is based on the premise of using SiC MOSFET body diode as FWD and aiming to reduce power losses at the same level as when using SiC SBD. It shortens dead time by utilizing the current-sense FET integrated in SiC MOSFET, and the dead-time control circuit is integrated in each isolated gate driver. This paper concludes that the proposed technique enables shortening dead time within 0.1 μs and designing the power module compactly.

First, the characteristics of SiC MOSFET body diode and the dead-time issue are discussed. Second, the basic structure and detailed operation principles of the new dead-time-controlled gate driver are presented. Third, its operating stability is analyzed and the diode conduction time is estimated. Finally, experimental results by using the prototyped power module integrated with SiC MOSFET and the proposed gate driver IC are explained.

II. Dead-Time Issue

A. HEV Inverter System

The typical HEV inverter system with SiC MOSFET is shown in Fig. 1. It is constructed in a boost converter and a three-phase inverter. The gate drivers for each SiC MOSFET are isolated from each other and connected to the microcontroller unit (MCU) through signal isolators such as photocouplers. Each

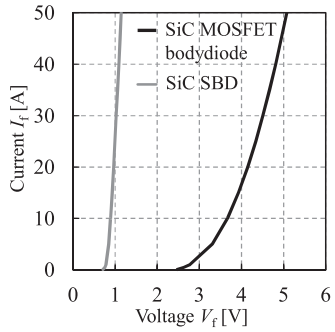

Fig. 2. $I_F - V_F$ characteristics of SiC MOSFET body diode and SiC SBD ($T_j = 25\,^{\circ}$C).

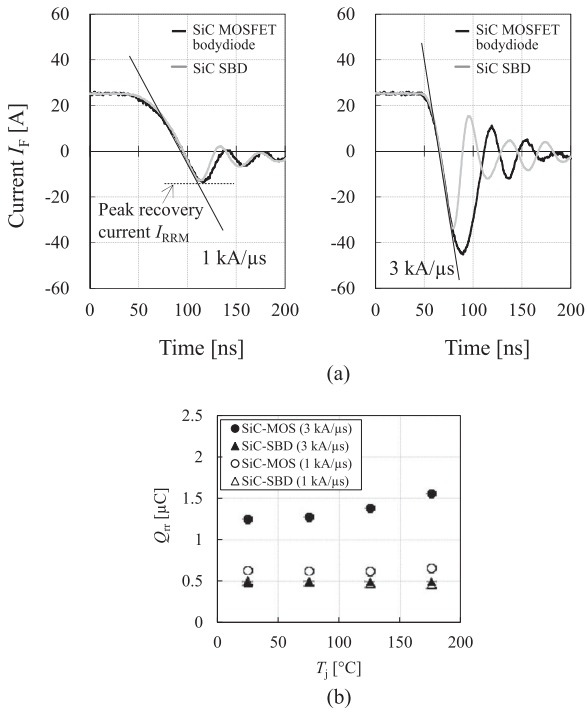

Fig. 3. Reverse recovery characteristics of SiC MOSFET body diode. (a) Reverse recovery current in the condition of $di/dt = 1$ kA/μs and 3 kA/μs ($T_j = 25\,^{\circ}$C). (b) Reverse recovery charge Q_{rr} – junction temperature T_j ($I_F = 25$ A).

gate driver receives a pulsewidth-modulated (PWM) signal with dead time t_{DT} from MCU as its input INH' or INL' and controls the gate-source voltage, depending on the input signal level. In the case of both converter and inverter, while the high-side device and the low-side device are in off state, either of the body diodes becomes on. As a result, during t_{DCT1} and t_{DCT2} in Fig. 1(b), diode conduction losses are generated.

B. Body Diode Conduction Loss During Dead Time

Figs. 2 and 3 show typical characteristics of SiC MOSFET body diode. The specifications of SiC MOSFET used in these experiments are given in Table I. The forward voltage V_F of the body diode is higher than that of the SiC SBD as shown in Fig. 2. This feature is caused by higher built-in voltage of the SiC pin diode. The reverse recovery charge Q_{rr} of the body

TABLE I
SPECIFICATIONS OF SiC MOSFET USED IN THE EXPERIMENTS

Item	Symbol	Value	Condition
Die size	–	6.0 mm × 5.5 mm	–
Breakdown voltage	$V_{\rm BR}$	1200 V	–
On-state resistance	$R_{\rm DS}$	20 mΩ	T_j 25 °C, V_{GS} 20 V, I_D 20 A
Gate threshold voltage	$V_{\rm GS}$ (th)	4.6 V	T_j 25 °C, $V_{\rm DS}$ 10 V, $I_{\rm D}$ 10 mA
Diode forward voltage	V_F	2.8 V	T_j 25 °C, $V_{\rm GS}$ 0 V, $I_{\rm F}$ 10 A
Input capacitance	$C_{\rm iss}$	4150 pF	T_j 25 °C, $V_{\rm GS}$ 0 V, $V_{\rm DS}$ 800 V, f = 1 MHz
Output capacitance	$C_{\rm oss}$	310 pF	
Reverse trans capacitance	$C_{\rm rss}$	45 pF	

TABLE II
POWER LOSS ESTIMATION CONDITIONS OF BOOST CONVERTER

Item	Symbol	Value
Input voltage	V_L	250 V
Output voltage	V_H	500 V
Output current	$I_{\rm OUT}$	30 A
Boost inductance	L_0	25 μH
Carrier frequency	F_C	100 kHz
Dead time	$t_{\rm DT}$	1.5 μs
SiC MOSFET junction temperature	T_j	125 °C

diode in case of di/dt = 1 kA/μs is as low as that of SiC SBD, as shown in Fig. 3. Under the condition of fast switching speed at di/dt = 3 kA/μs, the peak recovery current $I_{\rm RRM}$ of the body diode was larger than that of SiC SBD, and $Q_{\rm rr}$ was larger as the junction temperature increased. Under the condition of di/dt = 1 kA/μs, however, $Q_{\rm rr}$ hardly changed even by the increase of the junction temperature. These body diode losses have a significant influence on the high-frequency converters in HEV inverter system. Thus, the diode conduction losses of 15 kW boost converter were estimated.

The diode conduction loss $P_{\rm Di}$ can be calculated with (1). And the diode conduction times $t_{\rm DCT1}$ and $t_{\rm DCT2}$ are given by (2) and (3). In consideration of on-delay and off-delay variabilities, dead time $t_{\rm DT}$ was set to 1.5 μs, and we used experimentally measured values for switching periods $t_{\rm on}$ and $t_{\rm off}$. F_C is the carrier frequency and $t_{\rm on-del}$ and $t_{\rm off-del}$ are the total values of on-delay and off-delay from MCU to the gate driver output. The parameters used for loss estimation of boost converter are given in Table II. $t_{\rm DCT1}$ and $t_{\rm DCT2}$ were measured by operating SiC MOSFET under the condition of Table II, and then $P_{\rm Di}$ was calculated by using the measured I_F–V_F characteristic of SiC MOSFET.

$$P_{\rm Di} = (V_F \cdot I_F \cdot t_{\rm DCT1} + V_F \cdot I_F \cdot t_{\rm DCT2}) \cdot F_C \quad (1)$$

$$t_{\rm DCT1} = t_{\rm DT} + t_{\rm on-del} - t_{\rm off-del} - t_{\rm off} \quad (2)$$

$$t_{\rm DCT2} = t_{\rm DT} + t_{\rm on-del} - t_{\rm off-del} + t_{\rm on}. \quad (3)$$

Fig. 4 shows the diode conduction loss at $t_{\rm DCT1}$ and $t_{\rm DCT2}$. The total conduction loss without SiC SBD was 73.8 W, which

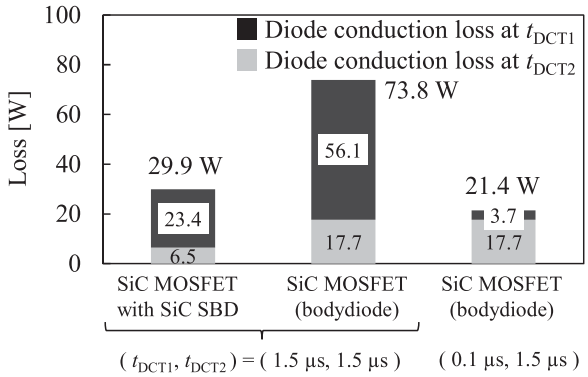

Fig. 4. Diode conduction losses of 15 kW boost converter (F_c = 100 kHz).

was larger than that of 29.9 W in case of using SiC SBD. The loss of the section $t_{\rm DCT1}$ was much larger than that of the section $t_{\rm DCT2}$. It is caused by the fact that the inductor current ripple is large because HEV inverter system requires small-sized boost inductor [25].

As shown in the previous works [16]–[24], it is very difficult to shorten the diode conduction time $t_{\rm DCT2}$ without isolators in HEV inverter system. For example in [16], it can shorten dead time to 40 ns calculated using the microcontroller, by taking note that turn-off operation of diode conduction side is decided by the parameters of the gate source loop. This method is effective for applications such as the voltage-source converter. However, it is difficult to determine which dead time is shortened in the HEV inverter system, because the current flow changes frequently. In addition, it is necessary to tune the dead time appropriately, considering the delay-time variations of isolators, gate drivers and power devices. Thus, in order to reduce body diode losses at the same level as SiC SBD system, the target diode conduction time $t_{\rm DCT1}$ had to be set at 0.1 μs.

III. PROPOSED DEAD-TIME-CONTROLLED GATE DRIVER

A. Dead-Time Shortening Technique

Fig. 5 shows the circuit schematic of the proposed gate driver. The proposed gate driver detects the commutation to the body diode on the target-side device by using the current-sense FET integrated in SiC MOSFET. Then, it turns on automatically to shorten dead time without any isolator as diode commutating detection elements. Therefore, it can downsize the power module integrated with the gate driver because no additional components are needed.

Fig. 6 is the photograph of SiC MOSFET prototyped for HEV inverter system. A dotted line frame shows an active area of the current-sense FET. The current-sense FET is originally used for detecting short-circuit current for HEV inverter systems [26], [27]. The current-sense FET is the same cell structure with main FET and the size is about 1/10 000 of the main FET. Therefore, the current-sense FET hardly affects electrical characteristics of SiC MOSFET and the production cost hardly increases.

The source electrode of the current-sense FET $M_{\rm SH}$ is connected to the node CMPH of gate driver. It is also fixed to the power supply voltage $V_{\rm DDH}$ when the target-side device is in off

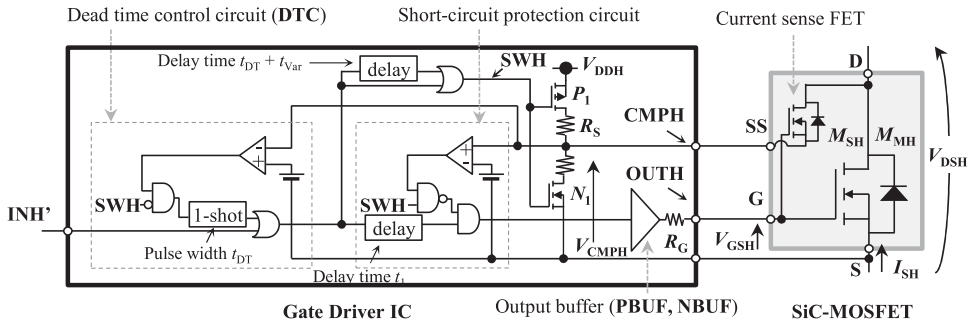

Fig. 5. Circuit schematic of the proposed gate driver integrated with the dead-time controller (an example for a high-side MOSFET).

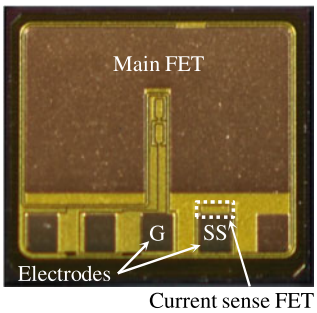

Fig. 6. SiC MOSFET for the HEV inverter system.

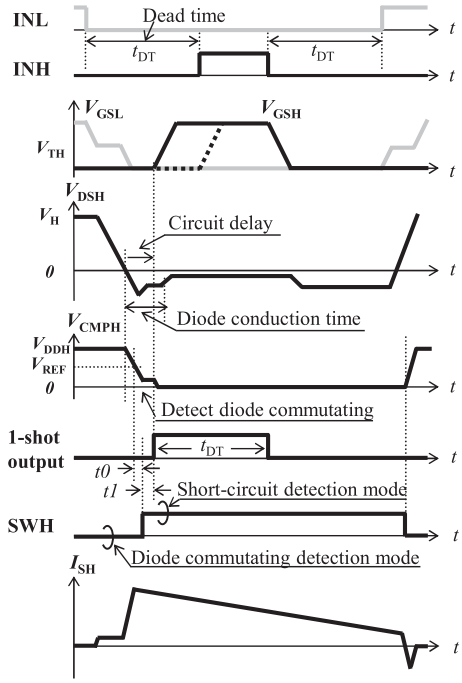

Fig. 7. Timing diagram of the proposed dead-time shortening technique.

state and is configured to detect the voltage change of high side comparator input (CMPH) to turn on automatically when load current commutates to body diode during dead time. Therefore, it can make a transition from the body diode conduction mode to the channel conduction mode even if INH' is in off state.

Fig. 7 shows the timing diagram of the proposed dead-time shortening technique. When the low-side device is turned off, the high side voltage V_{DSH} decreases. Before long, the body diode of the high-side device turns on, and the potential of the node D becomes lower than that of the node S. Then, the body diode of the current-sense FET M_{SH} also turns on because the potential difference between V_{DDH} and node D becomes larger than the built-in voltage of SiC MOSFET body diode. When the body diode of M_{SH} turns on, voltage V_{CMPH} decreases lower than the threshold voltage V_{REF}, because current flows from the power supply V_{DDH} through the body diode of M_{SH}. Then the comparator output becomes high, so the body diode commutation can be detected.

V_{REF} is the threshold voltage to detect the body diode commutation. Because the resistance R_s is higher than 1 kΩ, V_{CMPH} becomes negative regardless of the load current when the body diode of M_{SH} is in on state. Therefore, V_{REF} has a large design margin from 0 V to V_{DDH}. However, it is recommended to set it to about 1 V to prevent false operation. This false operation is explained in Section IV.

After detecting the body diode commutation, it is necessary to prevent from short-circuit faults. Then, the gate driver IC changes SWH to high-level to detect the short-circuit current. In order to certainly detect the short-circuit current, it changes gate-source voltage V_{GSH} to high-level after a small delay t_1 from the start of short-circuit current detection mode. In order to complete mode change, the period t_1 can be designed at about 3 ns in consideration of signal propagation delay.

When the target-side device is gate-off, the body diode is commutated again. If SWH is changed to low level in this period, the target-side device is in on state again and the short-circuit operation occurs at the turn-on timing of the opposite-side device. Therefore, in order to prevent the short-circuit operation, SWH keeps high level until the complete turn on of the opposite-side device. In Fig. 5, the delay time, which is longer than variability of dead time $t_{\mathrm{DT}} + t_{\mathrm{Var}}$, is added by the "delay" part. After this delay, SWH is changed to low level and the gate driver returns into the diode commutating detection mode again.

As mentioned earlier, the proposed technique makes it possible to realize a robust and safe switching operation for the wide current range. And the dead-time controller can be integrated in each isolated gate driver without fabrication overhead. Moreover, the proposed technique does not require any external components.

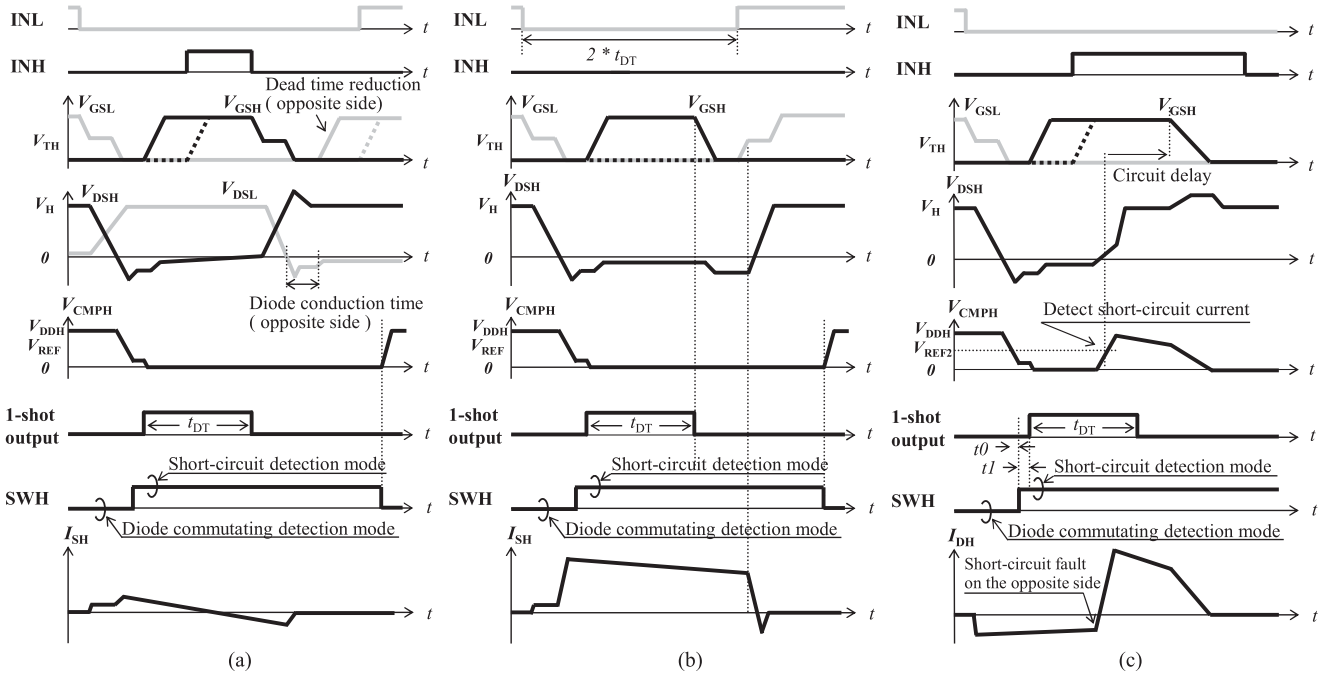

Fig. 8. Timing diagrams of the gate drive operations in HEV inverter system. (a) The case that the load current reverses while FET is in on state. (b) The case that the gate driver input continues to be low at high modulation index. (c) The case that the short-circuit fault occurs on the opposite side.

B. Gate Drive Operation in the HEV Inverter System

In the previous section, the typical operation of the dead-time shortening technique was explained. However, there are various operation conditions in the HEV inverter system. In this section, some special operations in the HEV inverter system are considered in order to guarantee behavioral safety of the dead-time-controlled gate driver.

Fig. 8 shows three timing diagrams of the special conditions in HEV inverter system. Fig. 8(a) shows the case that inductor current reverses while SiC MOSFET is in on state. Because the current I_{SH} reverses while high-side device is in on state, the inductor current commutates to the body diode of the low side at the turn-off timing of the high-side MOSFET M_{MH}. In this case, the high-side drive operation is the same as the typical operation shown in Fig. 7. In addition, the low-side gate driver detects diode commutation and turns on the low-side MOSFET to reduce diode losses.

Fig. 8(b) shows one of the inverter operations at the high modulation index. In this case, INH does not switch to on state while INL is in off state. The off-state period of the low-side device is twice that of the dead time t_{DT} in this case. In the proposed gate driver, the pulse width of the one-shot circuit is designed to t_{DT} so that V_{GSH} turns off before INL becomes high again. Because t_{DT} is set to be longer than the switching time, short-circuit operation can be avoided.

Fig. 8(c) shows the case of short-circuit fault. In HEV inverter system, it is necessary for gate drivers to detect the short-circuit current when the target-side device is in on state. The proposed gate driver sets SWH to high level just after detecting diode commutation and resets SWH to low level after voltage V_{GSH} turns off again. In this way, it enables realization of the dead-time control and the short-circuit protection operations. As mentioned earlier, under various conditions in the HEV inverter system, the proposed gate driver can shorten dead time safely.

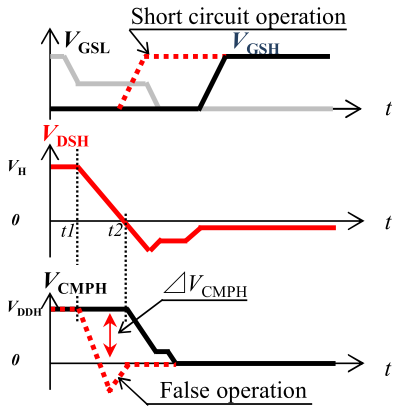

Fig. 9. Timing diagram of the unstable operation due to the parasitic current.

IV. Diode Conduction Time Estimation

A. Unstable Operation Mechanism by Parasitic Current

As shown in Fig. 7, when V_{DSH} varies due to the switching of the opposite-side device, the noise current flows thorough the parasitic capacitance of M_{SH}. As a result, the gate controllability may be unstable due to this noise current. The unstable operation mechanism caused by the parasitic current is analyzed.

Fig. 9 shows the timing diagram of the unstable operation in comparison with the correct operation. When the target-side device is in off state, the comparator input voltage V_{CMPH} equals to the power supply voltage V_{DDH} of the gate driver. When the opposite-side device turns off and V_{DSH} drops, V_{CMPH} starts

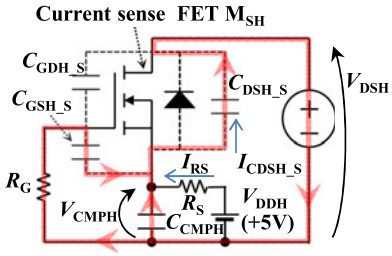

Fig. 10. Equivalent circuit around the current-sense FET. Red line indicates parasitic current in the period from t_1 to t_2.

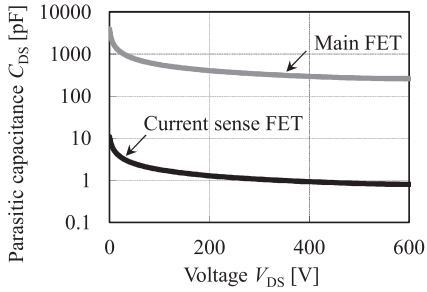

Fig. 11. $C_{\rm DS} - V_{\rm DS}$ characteristics of the main FET and the current-sense FET.

decreasing from t_2 at the correct operation. However, when the parasitic current through the current-sense FET becomes large, $V_{\rm CMPH}$ starts decreasing from t_1. Then, $V_{\rm CMPH}$ drops under the comparator threshold voltage $V_{\rm REF}$, so $V_{\rm GSH}$ switches to high. Therefore, if the false operation is caused by the parasitic current while the opposite-side device is still in on state, it results in short-circuit operation.

B. Gate Drive Operation in the HEV Inverter System

In order to prevent unstable operation caused by the parasitic current, the transient characteristic of the current-sense FET was analyzed and a design policy for stable operation was derived.

The current-sense FET of the power device is generally suggested for use with lower voltage than the isolation breakdown voltage, because when the voltage between the current-sense FET and the main FET source electrodes exceeds the isolation breakdown voltage, leak current increases [27]. The power supply voltage $V_{\rm DDH}$ was set at less than the isolation breakdown voltage (+5 V in this paper) in order to narrow down the parasitic current propagation paths.

Fig. 10 shows an equivalent circuit around the current-sense FET. Under this condition, it can be explained with the equivalent circuit, which is electrically isolated between the source electrode and the main MOSFET source electrode. In Fig. 10, $C_{\rm GSH_S}$, $C_{\rm DSH_S}$, and $C_{\rm GDH_S}$ indicate the parasitic capacitances of the current-sense FET, and $C_{\rm CMPH}$ indicates the total capacitance of comparator input node CMPH. In addition, R_G stands for the gate resistance of SiC MOSFET while R_S stands for the current adjusting resistance between $M_{\rm SH}$ source electrode and $V_{\rm DDH}$. CMPH voltage fluctuation $\Delta V_{\rm CMPH}$ is derived due to parasitic current, which bases on the equivalent circuit, as shown in Fig. 10.

When the opposite-side device turns off and $V_{\rm DSH}$ decreases, the current $I_{\rm CDSH_S}$ flows also through the parasitic capacitance $C_{\rm DSH_S}$. This current also flows through $C_{\rm CMPH}$ and $C_{\rm GSH_S}$ until the commutation to the body diode is completed. Therefore, the voltage fluctuation $\Delta V_{\rm CMPH}$ during this period can be determined as

$$\Delta V_{\rm CMPH} = \frac{1}{C_{\rm CMPH} + C_{\rm GSH\_S}} \int_{t_1}^{t_2} (I_{\rm CDSH\_S} - I_{\rm RS}) dt \quad (4)$$

$$= \frac{C_{\rm DSH_S}}{C_{\rm CMPH} + C_{\rm GSH_S}} \cdot \Delta V_{\rm DSH} \quad (5)$$

where $C_{\rm DSH_S}$ is very small in general, which is only a few picofarads. Fig. 11 shows the measured $C_{\rm DS} - V_{\rm DS}$ characteristics of the main and the current-sense FETs. The parasitic current $I_{\rm CDSH_S}$ due to $C_{\rm DSH_S}$ is quite small; then the influence of parasitic inductance between the source electrode SS and the comparator input node CMPH is small enough. For this reason, the term about the parasitic inductance is omitted. $I_{\rm RS}$ is the current caused by voltage fluctuation $\Delta V_{\rm CMPH}$ and depends on the switching period $t_2 - t_1$. In order to make the circuit design parameter for stable operation, which was unaffected by the switching period, $I_{\rm RS}$ was simplified and set at 0 A. From (4), $\Delta V_{\rm CMPH}$ during the switching period is determined by the balance between the parasitic capacitance of the current-sense FET $M_{\rm SH}$ and the capacitance of CMPH. Then, the following designs are required in order to realize its stability:

1) small-sized parasitic capacitance of the current-sense FET;
2) large-sized comparator input capacitance.

Some experiments were performed to confirm these requirements.

C. Experimental Validation

SiC MOSFET integrated with the current-sense FET was used in the experiment. $V_{\rm CMPH}$ during the switching period was observed, by connecting extra capacitor at the node of CMPH to adjust the total capacitance of CMPH. In order to measure $\Delta V_{\rm CMPH}$ caused only by parasitic current, the power supply voltage $V_{\rm DDH}$ was lowered to 0 V. Moreover, $V_{\rm DSH}$ was set at 500 V, which was the control upper limit, in order to maximize the parasitic current.

Fig. 12 shows the experimental waveforms of $V_{\rm DSH}$ and $V_{\rm CMPH}$. Voltage fluctuation $\Delta V_{\rm CMPH}$ depending on the total capacitance of $C_{\rm CMPH}$ occurs while $V_{\rm DSH}$ is from 0 to 500 V. Fig. 13 shows the relation between $\Delta V_{\rm CMPH}$ and $C_{\rm CMPH}$. $\Delta V_{\rm CMPH}$ was calculated based on (4) when the conditions of $C_{\rm DSH_S} = 1$, 2.5, and 5 pF. From Fig. 13, it was confirmed that the measured values were almost similar with the calculated values in case of $C_{\rm DSH_S} = 2.5$ pF, and $\Delta V_{\rm CMPH}$ was approximately 3.0 V at $C_{\rm CMPH} = 390$ pF. The experimental result shows that (4) has a good agreement and that it is effective to use the current-sense FET as a diode commutating detector for the safety operation.

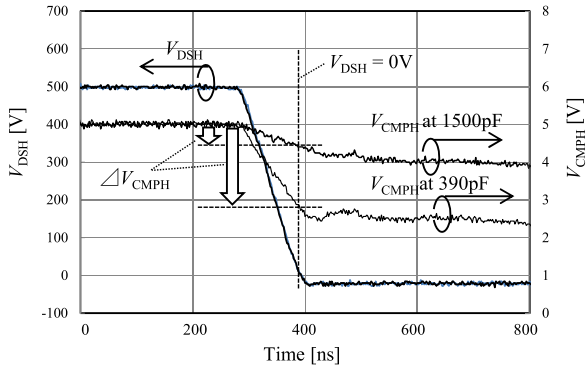

Fig. 12. Measured waveforms of V_{DSH} and V_{CMPH} ($dV_{\mathrm{DSH}}/dt = 5\,\mathrm{kV}/\mu\mathrm{s}$).

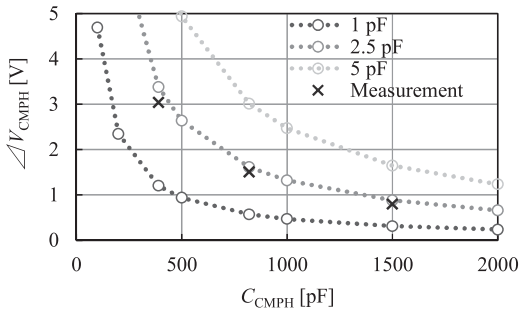

Fig. 13. Comparison between the calculated value and the experimental result of $\Delta V_{\mathrm{CMPH}} - C_{\mathrm{CMPH}}$ ($dV_{\mathrm{DSH}}/dt = 20\,\mathrm{kV}/\mu\mathrm{s}$).

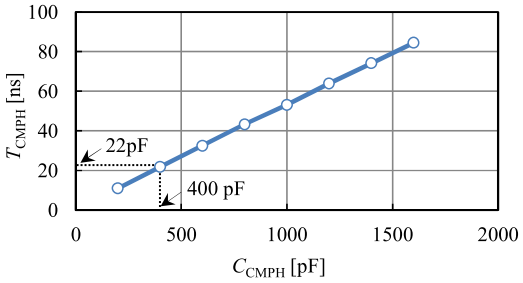

Fig. 14. Comparator response time $T_{\mathrm{CMPH}} - C_{\mathrm{CMPH}}$.

D. Diode Conduction Time Estimation and Driver Design

In the proposed gate driver, the response time of the comparator after detecting ΔV_{CMPH} has the major influence on the diode conduction time. While it is effective to make C_{CMPH} large for its stabilized operation, it lengthens the comparator response time T_{CMPH}. Therefore, T_{CMPH} was estimated in the view point of C_{CMPH} dependence.

As shown in Fig. 13, when the limit of ΔV_{CMPH} caused by parasitic current is 3.5 V, C_{CMPH} requires 400 pF. Fig. 14 shows the C_{CMPH} dependence of response time. In the condition of $C_{\mathrm{CMPH}} = 400\,\mathrm{pF}$, the comparator response time became 22 ns. It is clear from (4) that this depends on the small parasitic capacitance $C_{\mathrm{DSH_S}}$. If the current-sense FET is designed smaller, the diode conduction time can be shortened more. Fig. 15 shows the diode conduction time estimated using circuit simulation.

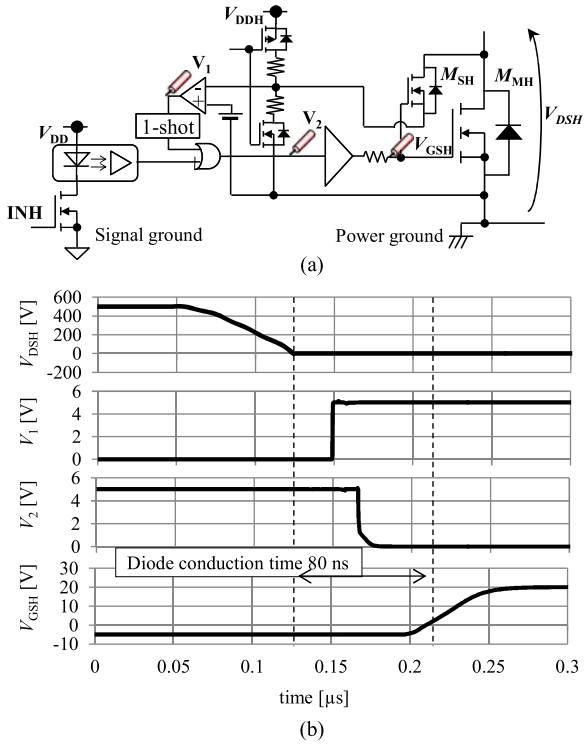

Fig. 15. Estimation result of the diode conduction time of the proposed gate driver implimented in 0.5 μm LVIC technology. (a) Schematic of the circuit model. (b) Simulated waveforms.

The simulated diode conduction time was 80 ns, which was from V_{DSH} of 0 V to V_{GSH} higher than the gate-source threshold voltage V_{th}.

V. Experimental Results

A. Proposed Gate Driver IC and Power Module

Fig. 16 shows the prototyped intelligent half-bridge power module with 1.2 kV SiC MOSFETs and the gate driver ICs with the proposed dead-time controller. The maximum current of the power module was 50 A. This intelligent power module was constructed in two 1.2 kV SiC MOSFETs and two gate driver ICs only and was able to be designed very compactly.

The gate driver IC was fabricated in 0.35-μm BiCDMOS LVIC technology, and the die size was 7 mm $\times$ 4 mm (28 mm^2). It had a serial communication circuit for debug as the prototype one. The final gate driver IC was estimated to be designed smaller, since the main circuit parts were able to be designed small die size 4.1 mm^2, including the dead-time controller DTC of 0.8 mm^2. Fig. 17 shows the experimental circuit of the boost converter used in the HEV inverter system.

B. Verification of Diode Conduction Time Stability

To make clear the control stability, it was verified that the diode conduction time was kept at the same period even if output current was changed. The experimental conditions are listed in Table III. Fig. 18 shows the experimental waveforms of V_{DSH}, V_{GSL}, and V_{GSH} with the dead-time control. When the output

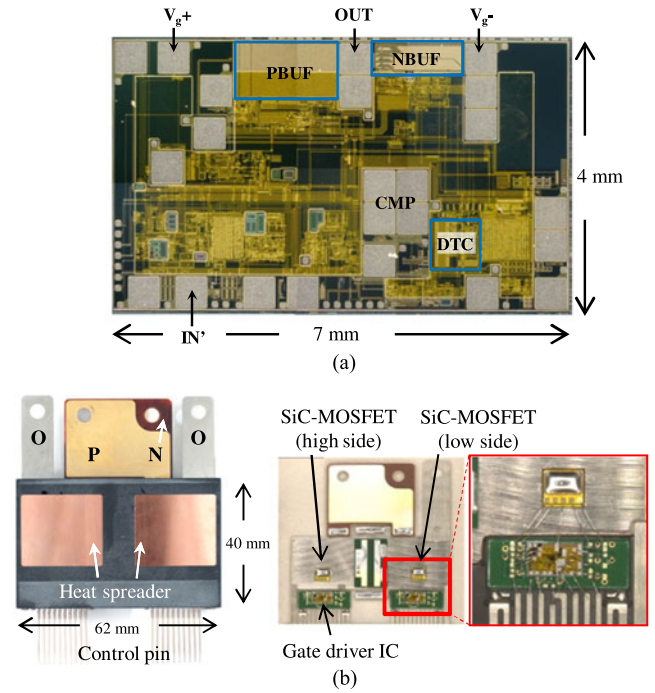

Fig. 16. Prototype photographs. (a) Gate driver IC integrated with dead-time controller. (b) Compact half-bridge module of SiC MOSFET.

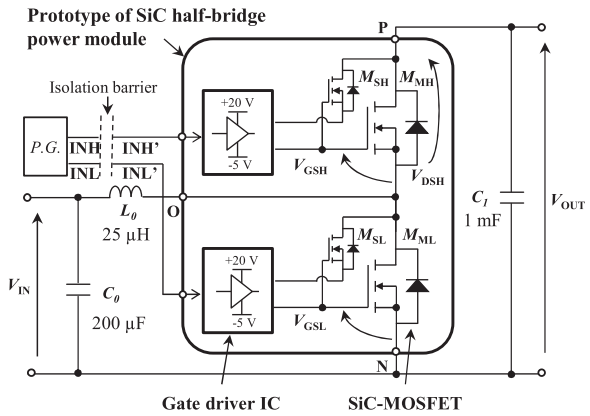

Fig. 17. Experimental environment.

current was changed to 10, 20, and 30 A, V_{GSL} off time varied, depending on the output current. However, the diode conduction time, which is from when $V_{\mathrm{DSH}} = 0\,\mathrm{V}$ to when $V_{\mathrm{GSH}} = V_{\mathrm{th}}$, was stable with 80–84 ns. In addition, even in the maximum switching speed of 20 kV/μs, no fault operation occurred and it was confirmed that the proposed gate driver can robustly work against the parasitic current.

C. Validation of Power Conversion Efficiency

The boost converter power conversion efficiency was measured with prototyped intelligent power module in each case of "dead-time control on" and "dead-time control off" and "with SiC SBD in antiparallel." The measurements were conducted under the condition of $di/dt = 1\,\mathrm{kA}/\mu\mathrm{s}$. The input power and

TABLE III
EXPERIMENTAL CONDITIONS

Item	Symbol	Value
Input voltage	V_{IN}	250 V
Output voltage	V_{OUT}	500 V
Output current	I_{OUT}	30 A maximum
Boost Inductance	L_0	25 μH
Carrier frequency	F_C	100 kHz
Dead time	t_{DT}	1.5 μs

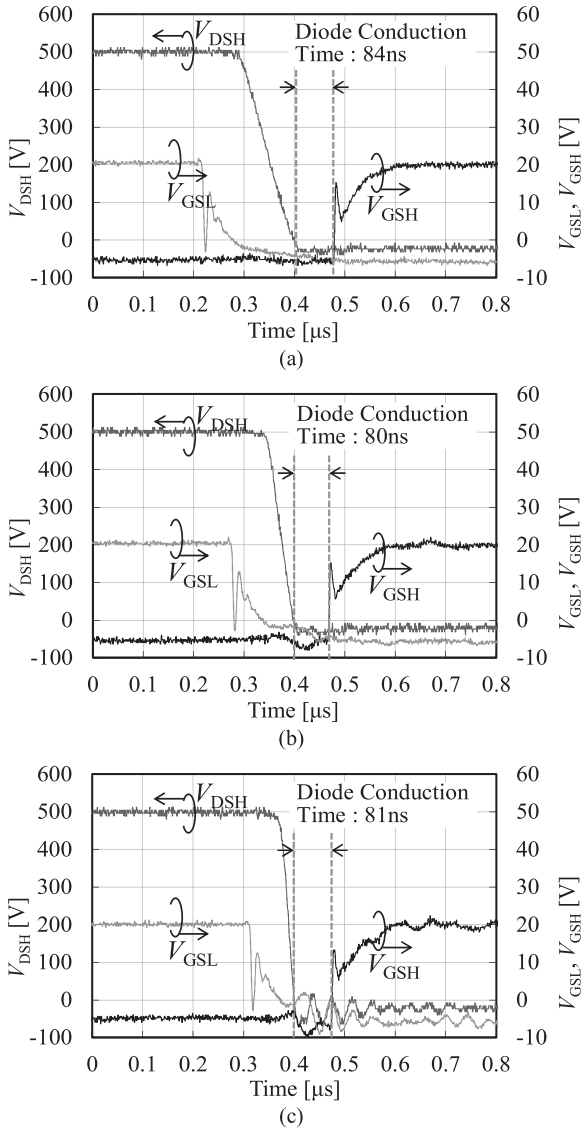

Fig. 18. Experimental waveforms of the diode conduction time with dead-time control. I_{OUT} = (a) 10 A, (b) 20 A, and (c) 30 A.

the output power of the boost converter were measured by using power meter under the condition that cooling water is adjusted to be 20 °C. Besides, the gate driver ICs are connected to a separate power source. Then, the power conversion efficiency was calculated from the difference between the measured input and the output power. In addition, the calculated junction

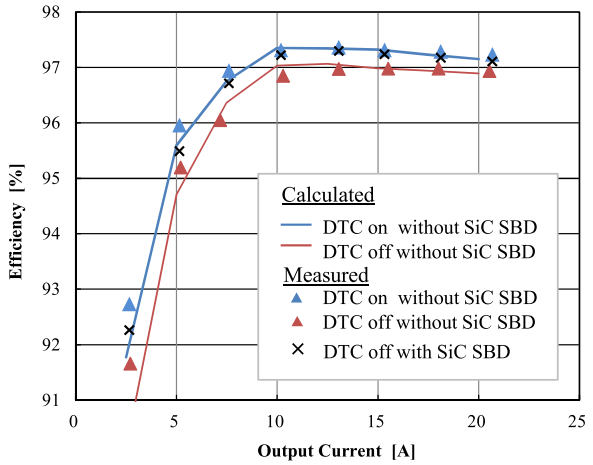

Fig. 19. Power conversion efficiency of 10 kW boost converter with SiC MOSFET.

temperature T_j at $I_{\mathrm{OUT}} = 2.5$ A was 57 °C and T_j at $I_{\mathrm{OUT}} = 20$ A was 126 °C in case of "dead-time control off."

Fig. 19 shows the power conversion efficiencies of boost converter. In all the range of measurement, the efficiency of boost converter under the condition of "dead-time control on" was higher by 1% than that under the condition of "dead-time control off." In addition, these experimental results indicate that the power conversion efficiency could be achieved equivalently to the condition of using SiC SBD as FWD.

VI. Conclusion

In this paper, the simple dead-time-controlled gate driver using the current-sense FET of SiC MOSFET was proposed. It was experimentally demonstrated that the proposed gate driver was able to integrate the proposed dead-time control circuit in it and does not require external components. This controller shortens the diode conduction time within 0.1 μs. When SiC MOSFET body diode, which has high forward voltage, is used as FWD, the proposed gate driver improves the power conversion efficiency of 10 kW boost converter by 1% and reduces the loss of boost converter at almost the same level as that using SiC SBD as FWD.

By incorporating the dead-time-controlled gate driver together with SiC MOSFET into HEV inverter system, the efficiency of the system and the vehicle driving range would be increased.

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Akimasa Niwa (M'16) received the B.E. and M.E. degrees in information systems engineering from Osaka University, Suita, Japan, in 1998 and 2000, respectively.

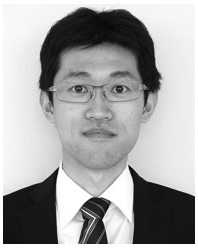
Since 2000, he has been with DENSO Corporation, Kariya, Japan. His current research interests include semiconductor integrated circuit in power electronics for vehicular applications.

Mr. Niwa is a Member of the Institute of Electrical Engineers of Japan and the Society of Automotive Engineers of Japan.

Takanori Imazawa received the M.E. degree in materials science from Nara Institute of Science and Technology, Ikoma, Japan, in 2011.

Since 2011, he has been with DENSO Corporation, Kariya, Japan. His current research interests include gate drive circuit and power module for SiC transistors.

Mr. Imazawa is a member of the Institute of Electrical Engineers of Japan.



Ryota Kojima received the B.E., M.E., and Ph.D. degrees in electronic engineering from Tohoku University, Sendai, Japan, in 2009, 2011, and 2014, respectively.

Since 2014, he has been with DENSO Corporation, Kariya, Japan. His current research interests include gate drive circuit for SiC and GaN transistors and pulse power applications.

Dr. Kojima is a member of the Institute of Electrical Engineers of Japan, the Society of Automotive Engineers of Japan, and the Japan Society of Applied Physics.

Masahiro Yamamoto received the B.E. degree in electronic engineering from Doshisha University, Kyotanabe, Japan, in 2001.

Since 2008, he has been with DENSO Corporation, Kariya, Japan. His current research interests include semiconductor integrated circuit in power electronics.

Mr. Yamamoto is a member of the Society of Automotive Engineers of Japan.

Takanari Sasaya received the B.E. and M.E. degrees in electrical and electronic engineering from Shizuoka University, Hamamatsu, Japan, in 1985 and 1987, respectively.

Since 1987, he has been with DENSO Corporation, Kariya, Japan, where he is engaged in the research and development of gate drive circuit for power devices and power conversion systems for vehicular applications.

Mr. Sasaya is a member of the Institute of Electrical Engineers of Japan, the Society of Automotive Engineers of Japan and the Japan Institute of Electronics Packaging.

Takanori Isobe (M'07) was born in Hamamatsu, Japan, in 1978. He received the B.Eng. degree in physical electronics, the M.Eng. degree in nuclear engineering, and the D.Eng. degree in energy sciences from the Tokyo Institute of Technology, Tokyo, Japan, in 2003, 2005, and 2008, respectively.

From 2008 to 2010 and from 2012 to 2013, he was a Researcher with the Tokyo Institute of Technology, where from 2010 to 2012, he was an Assistant Professor. From 2013 to 2014, he was with MERSTech, Tokyo. In 2013, he joined the University of Tsukuba, Tsukuba, Japan, where he is currently an Associate Professor at the Faculty of Pure and Applied Sciences. His current research interests include static reactive power compensators and soft-switching power converters.

Dr. Isobe is a Member of the Institute of Electrical Engineers of Japan and the Japan Institute of Power Electronics.

Hiroshi Tadano (M'80) received the Ph.D. degree in semiconductor technology from Tohoku University, Sendai, Japan, in 1980.

In 1980, he joined Toyota Central R&D Labs, Inc., where he was involved in the research and development of power devices such as SIT, IGBT, diodes, and power MOSFETs. Since 2013, he has been a Professor at the Graduate School of Pure and Applied Science, University of Tsukuba, Tsukuba, Japan. His current research interests include high-efficiency power conversion circuits for electric vehicles using advanced power devices.

Dr. Tadano is a member of the Institute of Electrical Engineering of Japan, the Institute of Electronics, Information and Communication Engineers, and the Japan Institute of Power Electronics.