AC–DC–AC Single-Phase Multilevel Six-Leg Converter With a Reduced Number of Controlled Switches

Nayara Brandão de Freitas, *Student Member, IEEE*, Cursino Brandão Jacobina, *Fellow, IEEE*, Nustenil Segundo de Moraes Lima Marinus, *Member, IEEE*, and Nady Rocha, *Member, IEEE*

***Abstract*—This paper proposes two unidirectional single-phase ac–dc–ac converters with a reduced number of controlled switches composed of two three-leg converters connected in series. The proposed converters allow us to feed the load voltage with sinusoidal voltages with constant amplitude and frequency and to operate with sinusoidal grid current with a high power factor. The converters can then be used as uninterruptible power supplies and unified power quality conditioners for nonregenerative applications. The system model, space-vector pulse width modulation technique, and a complete control system are given. A method to regulate the dc-link voltages using the voltage vector redundancies is presented. The proposed topologies are compared with the conventional one in terms of operation range, capability to operate with a unity grid power factor, voltage harmonic distortions, semiconductor losses, and others characteristics. Simulation and experimental results in many operating conditions are provided to validate the feasibility of the system.**

***Index Terms*—DC-link control, single-phase converter, space-vector pulse width modulation (PWM), unidirectional ac–dc–ac converter.**

I. Introduction

GIVEN the wide use of electronic equipment connected to the power grid, the implementation of ac–dc–ac systems is important as it enables the load to be fed from an ac electric system with the desired output voltage over all loading conditions and transients. The uninterruptible power supply (UPS) is an example of the system that supplies clean and uninterrupted power to critical loads under normal or abnormal grid conditions. In addition, UPS devices can also function as active power filters (APFs), compensating for load current power-quality issues, when the utility is in the normal condition [1]–[5]. In relation to the configuration, UPSs can be classified as line preferred (also known as offline), inverter preferred (also known as online), or line interactive [6].

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N. B. de Freitas is with the Post-Graduate Program in Electrical Engineering, PPgEE, COPELE, Federal University of Campina Grande, Campina Grande 58429-900, Brazil (e-mail: nayara.freitas@ee.ufcg.edu.br).

C. B. Jacobina is with the Federal University of Campina Grande, Campina Grande 58429-900, Brazil (e-mail: jacobina@dee.ufcg.edu.br).

N. S. M. L. Marinus is with the Federal Institute of Ceará, Cedro 63400-000, Brazil (e-mail: nustenilsegundo@gmail.com).

N. Rocha is with the Federal University of Paraíba, João Pessoa 58051-900, Brazil (e-mail: nadyrocha@gmail.com).

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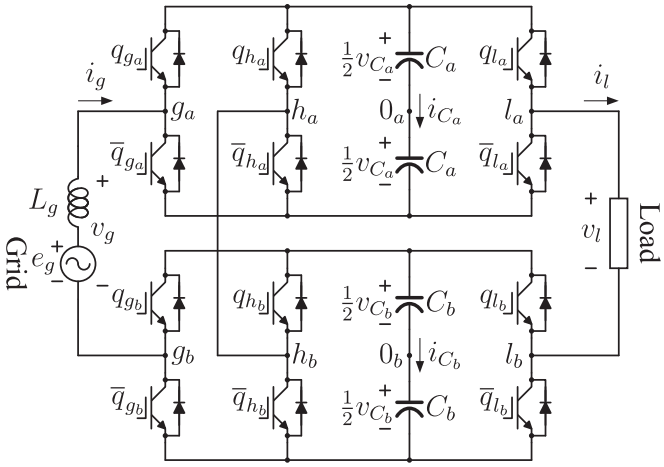

Fig. 1. 6L topology (conventional topology).

Considering that regulating the output voltage, keeping the grid current with low harmonic distortion, and guaranteeing high grid power factor are desirable functionalities, unified power quality conditioners (UPQCs) have been developed. UPQCs are part of the APF family members and, in addition to compensate for supply voltage power-quality issues (sags, swells, unbalance, flicker, harmonics, etc.) using series compensation, are utilized to handle load current power-quality issues (harmonics, unbalance, reactive current, etc.) using shunt compensation [7], [8]. Javadi *et al.* [9] proposed a hybrid series active filter that aims to address the same issues as the UPQC using less reactive and semiconductor components. Considering single-phase UPQCs, the three-leg topology is usually a preferable choice for low-cost low-power applications [10]–[12]. A single-phase UPQC based on the modular multilevel matrix converter is introduced in [13].

In some applications, even though regulated input currents and output voltages are required, the regenerative operation is not required or allowed. In this case, diodes can be used to avoid the driving circuits. This makes the systems simpler and less expensive. Wang *et al.* [14] proposed an open-winding power conversion system using half-controlled converters, while Nian and Zhou [15] introduced an open-winding permanent-

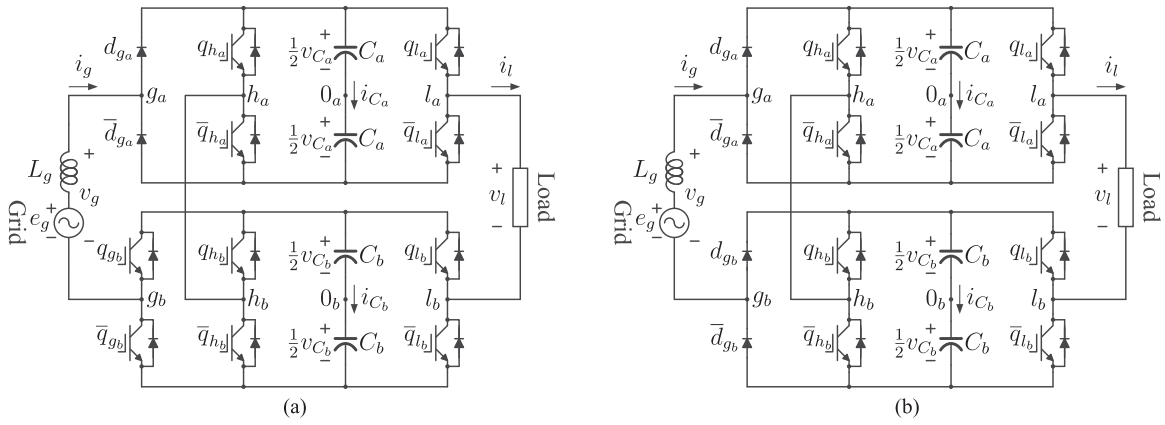

Fig. 2. Proposed topologies. (a) 6L1D topology. (b) 6L2D topology.

magnet synchronous generator that uses a fully controlled and an uncontrolled converter. Although the utilization of diodes introduces issues related to the current zero-crossing distortion, some synchronization techniques can be utilized to address this problem.

AC–DC–AC single-phase conversion usually employs the three-leg configuration [5] for applications, in which the grid and load frequencies are equal (e.g., UPS and UPQC). Jacobina *et al.* [16] proposed a single-phase ac–dc–ac converter for unidirectional power flux applications that is based on the three-leg configuration and has a reduced number of controlled switches. This paper utilizes a synchronization method that minimizes the current zero-crossing distortion.

Chang *et al.* [17] proposed a six-leg topology that allows regenerative operation and is composed of six controlled legs (see Fig. 1). This topology is named here as 6L configuration. Compared with the three-leg topology, the 6L system has some advantages, such as lower: 1) voltages and power processed by the converter switches; 2) voltages harmonic distortions; and 3) semiconductor losses [18].

Given the interest for systems that operate as output voltage and input current compensators and that some applications do not require or permit regenerative operation, this paper proposes two unidirectional ac–dc–ac single-phase converters based on the 6L topology. The 6L1D converter [see Fig. 2(a)] is composed of an uncontrolled leg (composed only of diodes) and five controlled legs. On the other hand, the 6L2D converter [see Fig. 2(b)] is composed of two uncontrolled legs and four controlled legs. Consequently, compared with the 6L converter, the proposed topologies reduce the total cost of the systems, as there is a decrease in the number of drivers.

The proposed converters allow us to feed the load with sinusoidal voltage (assuming that there is an *RLC* filter in the load side) with constant amplitude and frequency and also to operate with sinusoidal grid current with a high power factor. Thus, the converters can be used as UPS and UPQC for nonregenerative operations without zero-crossing distortion, even though the topologies utilize diodes. In addition, a method to regulate the dc-link voltages using the voltage vector redundancies is presented in this paper.

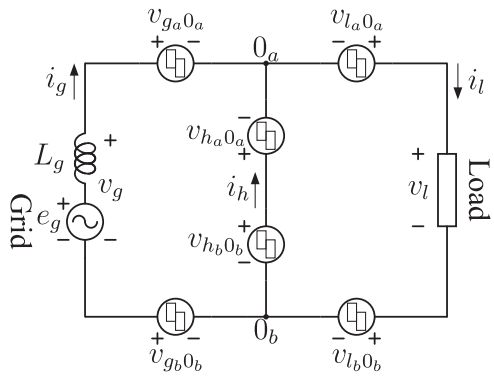

Fig. 3. Equivalent circuit of the system (the model is similar for 6L, 6L1D, and 6L2D configurations).

The proposed topologies are compared with the conventional 6L converter in terms of operation range, capability to operate with a unity grid power factor, and the need to utilize or not a line transformer. The systems are also compared in terms of voltages harmonic distortions and semiconductor losses. By these means, it was possible to compare the performances of conventional and proposed systems. Simulation and experimental results in many operating conditions (for example, with grid overvoltage, linear and nonlinear loads, and load variations) are provided to support the theoretical considerations.

II. System Model

The 6L1D and 6L2D topologies are composed of two converters employing the three-leg rectifier–inverter topology. These converters utilize an electrical grid (voltage and current given by e_g and i_g, respectively) to supply a load (voltage and current given by v_l and i_l, respectively). The 6L, 6L1D, and 6L2D configurations have the same equivalent circuit, as shown in Fig. 3.

Consider that q_{s_k}/d_{s_k} represents the state of the upper switch/diode of the leg s_k, such that $q_{s_k}/d_{s_k} = 1$ indicates that the switch is ON, while $q_{s_k}/d_{s_k} = 0$ indicates that the switch is OFF, where $k = a, b$ and $s = g, h, l$. Thus, when the leg utilizes

TABLE I
REGIONS OF OPERATION

Topology	Unity grid power factor?	Regenerative operation?	f_g/f_l	V_g^m/V_l^m	v_{C_t}	α
6L	yes	yes	$f_g = f_l$	$V_g^m = V_l^m = 1$ p.u.	1 p.u.	$-60^\circ \leq \alpha \leq 60^\circ$
				$V_g^m = 2V_l^m = 1$ p.u.	1 p.u.	$-75^\circ \leq \alpha \leq 75^\circ$
				$V_g^m = 0.5V_l^m = 0.5$ p.u.	1 p.u.	$-75^\circ \leq \alpha \leq 75^\circ$
			$f_g \neq f_l$	$V_g^m = V_l^m = 1$ p.u.	2 p.u.	any
				$V_g^m = 2V_l^m = 1$ p.u.	1.5 p.u.	any
				$V_g^m = 0.5V_l^m = 0.5$ p.u.	1.5 p.u.	any
6L1D	yes	no	$f_g = f_l$	$V_g^m = V_l^m = 1$ p.u.	1 p.u.	$-28.95^\circ \leq \alpha \leq 28.95^\circ$
				$V_g^m = 2V_l^m = 1$ p.u.	1 p.u.	$-28.95^\circ \leq \alpha \leq 28.95^\circ$
				$V_g^m = 0.5V_l^m = 0.5$ p.u. *	1.225 p.u.	$-28.95^\circ \leq \alpha \leq 28.95^\circ$
			$f_g \neq f_l$ *	$V_g^m = V_l^m = 1$ p.u.	2 p.u.	any
				$V_g^m = 2V_l^m = 1$ p.u.	1.5 p.u.	any
				$V_g^m = 0.5V_l^m = 0.5$ p.u.	2 p.u.	any
6L2D	no	no	$f_g = f_l$	$V_g^m = V_l^m = 1$ p.u.	1 p.u.	0°
				$V_g^m = 2V_l^m = 1$ p.u.	1 p.u.	0°
				$V_g^m = 0.5V_l^m = 0.5$ p.u.		cannot operate
			$f_g \neq f_l$			cannot operate

* The load may impose further operation restrictions. More details are provided in the text.

switches, the pole voltages can be calculated by

$$v_{s_k 0_k} = (2q_{s_k} - 1)\frac{v_{C_k}}{2} \tag{1}$$

where the converter pole voltage $v_{s_k 0_k}$ is the voltage between the point s_k and the dc-link midpoint (point 0_k) and v_{C_k} is the voltage of the dc-link k.

For the legs composed of diodes, the pole voltages depend on the polarity of current i_g. When $i_g \geq 0$, d_{g_a} conducts, and consequently, $v_{g_a 0_a} = \frac{v_{C_a}}{2}$ for both topologies, while, for the 6L2D converter, $\bar{d}_{g_b}$ conducts, and consequently, $v_{g_b 0_b} = -\frac{v_{C_b}}{2}$. Otherwise, $\bar{d}_{g_a}$ conducts, and consequently, $v_{g_a 0_a} = -\frac{v_{C_a}}{2}$ for both topologies, while, for the 6L2D converter, d_{g_b} conducts, and consequently, $v_{g_b 0_b} = \frac{v_{C_b}}{2}$. Therefore, these diodes switch at the fundamental frequency of i_g.

Converter grid voltage v_g and converter load voltage v_l are written as functions of the pole voltages as follows:

$$v_g = v_{g_a 0_a} - v_{g_b 0_b} - v_{h_a 0_a} + v_{h_b 0_b} \tag{2}$$

$$v_l = v_{l_a 0_a} - v_{l_b 0_b} - v_{h_a 0_a} + v_{h_b 0_b}. \tag{3}$$

III. REGIONS OF OPERATION

The maximum amplitudes of v_g and v_l are represented as V_g^m and V_l^m, respectively, and the total dc-link voltage is given as $v_{C_t} = v_{C_a} + v_{C_b}$. The amplitudes of v_g and v_l are represented as V_g and V_l, respectively. The fundamental frequencies of v_g and v_l are represented by f_g and f_l, respectively, and the angle between v_g and v_l is represented by α. Considering an *RL* load, the load power factor is represented by $\cos\varphi$. Table I shows the operational limitations, degrees of freedom, and dc-link voltage specifications of conventional and proposed topologies considering six modes of operation.

Considering the 6L topology, the angle between v_g and i_g can be any value. Consequently, this topology can operate with a unity grid power factor and is suitable for regenerative applications. Using the information provided in Table I, it can be seen that this topology is more interesting when $f_g = f_l$ and $V_g^m = V_l^m = 1$ p.u., because the generated voltages have a high modulation index and the dc-link voltages values are minimum. In this case, V_g can drop to zero and V_l can still be equal to 1 p.u. Due the shared leg, the dc-link voltages need to be increased when $f_g \neq f_l$. Consequently, this type of topology is not interesting for motor drive applications because the generated voltages should have amplitude and frequency variable.

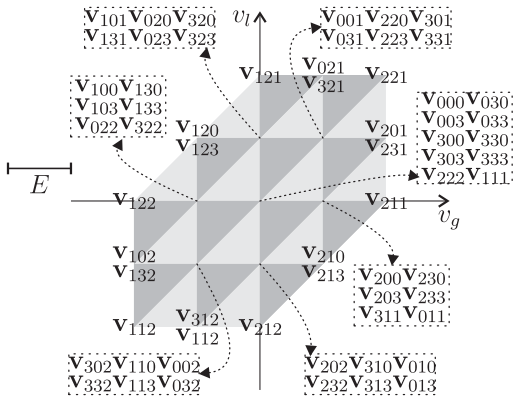

Fig. 4. Space-vector plane generated by the 6L configuration.

As can be seen in Table I, the 6L1D topology is more suitable when $f_g = f_l$ and $V_g^m = V_l^m = 1$ p.u. or $V_g^m = 2V_l^m = 1$ p.u. The displacement angle between v_g and i_g is up to 30° when $V_g^m = 1$ p.u. and $v_{C_t} = 1$ p.u. As the angle between v_g and e_g is usually lower than that, the topology can operate with a unity grid power factor. However, for a regenerative operation, the angle between v_g and i_g should be able to be larger than 90°. Consequently, this configuration is only suitable for nonregenerative applications. When $f_g = f_l$, $V_g^m = V_l^m = 1$ p.u., $v_{C_t} = 1$ p.u., and $\alpha = 0^\circ$, V_g can drop to 0.5 p.u., if the load is *RL* with

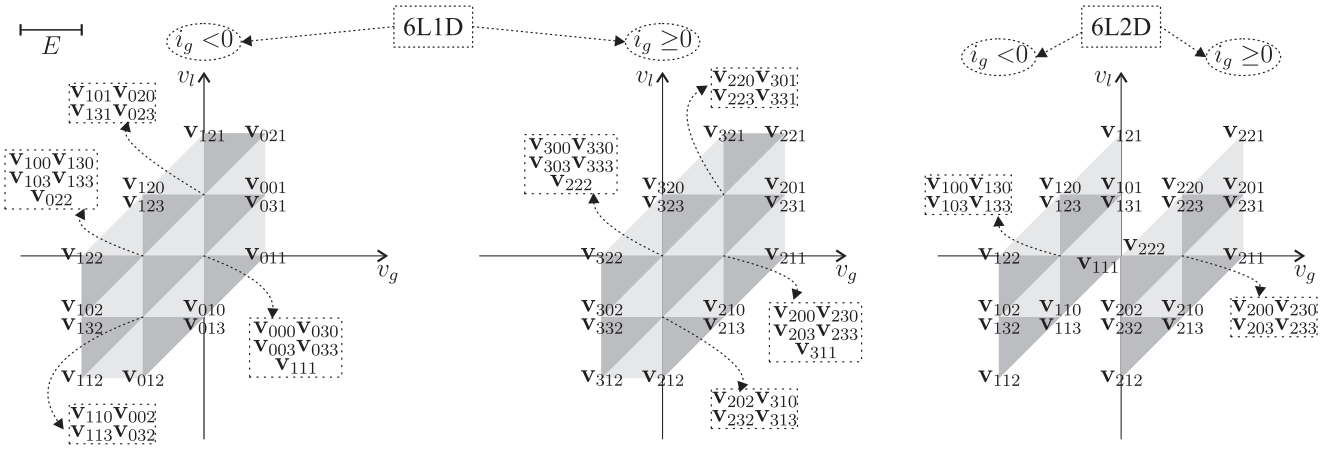

Fig. 5. Space-vector planes generated by the 6L1D and 6L2D configurations.

$\cos\varphi \leq 0.43$. Under the same condition and with $\alpha = -28.95°$, V_g can drop to 0.75 p.u., if the load is *RL* with $\cos\varphi \leq 0.93$. When $\alpha = -28.95°$ and the load is *RL* with $\cos\varphi = 1$, V_g can drop to 0.85 p.u. The dc-link regulation of the converter with $f_g = f_l$ and $V_g^m = 0.5V_l^m = 0.5$ p.u. cannot be accomplished when $\cos\varphi$ is high. Although the topology can operate with $f_g \neq f_l$, the load may impose restrictions in the dc-link control.

In the case of the 6L2D topology, v_g, v_l, and i_g should be synchronized and $V_g \geq V_l$. Consequently, this topology cannot accomplish a unity grid power factor or be suitable for regenerative applications. Given $f_g = f_l$, $V_g^m = 2V_l^m = 1$ p.u., and $v_{C_t} = 1$ p.u., V_g can drop to 0.5 p.u. In order to operate with $f_g = f_l$, $V_g^m = V_l^m = 1$ p.u., and allow V_g to drop to 0.8 p.u., a grid-side step-up transformer with turn-ratio equal to 1.25 should be used and $v_{C_t} = 1.25$ p.u. (this guarantees that $V_g \geq V_l$). This topology cannot operate when $f_g \neq f_l$. Having this information in mind, the configuration is more suitable for applications in which $f_g = f_l$ and $V_g \geq V_l$ p.u. As an example is the system in which $E_g = 220$ V(rms) and $V_l = 110$ V(rms), very common in Brazil.

For all analyses presented in this paper, grid and load frequencies are considered the same. The dc-link voltages of studied and proposed configurations need to be increased to operate with grid voltage swells. For example, if $f_g = f_l$ and $V_g = V_l = 1$ p.u., a 20% increase in v_{C_t} allows all the systems to operate with 20% grid voltage swells. This increase in the dc-link voltages also affects the maximum grid voltage sag.

IV. Space-Vector Pulse Width Modulation (PWM) Technique

Henceforth, it is assumed that $v_{C_a} = v_{C_b} = E$. Fig. 4 shows the space-vector plane generated by the 6L configuration. The space-vector planes generated by the 6L1D and 6L2D topologies are represented in Fig. 5. Each triangle is a sector and each vertex represents a voltage vector.

$\mathbf{v}_{n_g n_l n_h}$ represents the vector generated by a given switching combination, where n_s is the binary number $q_{s_a} q_{s_b}$ (with the exception of n_g for 6L1D and 6L2D topologies, where it represents $d_{g_a} q_{g_b}$ and $d_{g_a} d_{g_b}$, respectively) converted to decimal. For example, if $q_{h_a} = 1$ and $q_{h_b} = 0$, $n_h = 2$. The voltage in each point of the space-vector plane is represented by

$$\mathbf{v} = v_g + jv_l \tag{4}$$

where $v_g = \text{Re}(\mathbf{v})$ and $v_l = Im(\mathbf{v})$.

An asterisk $*$ in the superscript indicates a reference variable. Given that $\mathbf{v}^* = v_g^* + jv_l^*$ represents the voltages to be generated by the converter, the reference vector located inside a sector should be synthesized by the vectors $\mathbf{v}_1$, $\mathbf{v}_2$, and $\mathbf{v}_3$ that are located at the vertices of the triangle. Then, for each sector, it can be written

$$\mathbf{v}^* = \frac{t_1}{T}\mathbf{v}_1 + \frac{t_2}{T}\mathbf{v}_2 + \frac{t_3}{T}\mathbf{v}_3 \tag{5}$$

$$T = t_1 + t_2 + t_3 \tag{6}$$

where T is the sampling period and t_1, t_2, and t_3 are the application times of the vectors $\mathbf{v}_1$, $\mathbf{v}_2$, and $\mathbf{v}_3$, respectively. These time lengths are calculated as follows:

$$\begin{bmatrix} t_1 \\ t_2 \\ t_3 \end{bmatrix} = \begin{bmatrix} \frac{\text{Re}(\mathbf{v}_1)}{T} & \frac{\text{Re}(\mathbf{v}_2)}{T} & \frac{\text{Re}(\mathbf{v}_3)}{T} \\ \frac{\text{Im}(\mathbf{v}_1)}{T} & \frac{\text{Im}(\mathbf{v}_2)}{T} & \frac{\text{Im}(\mathbf{v}_3)}{T} \\ 1 & 1 & 1 \end{bmatrix}^{-1} \begin{bmatrix} v_g^* \\ v_l^* \\ T \end{bmatrix}. \tag{7}$$

In many cases, a voltage vector can be generated by more than one switching state. These redundancies and the application sequence of the voltage vectors are selected to reduce the switching frequency of the converter and, consequently, the switching losses. The studied configurations can operate changing the states of only two switches over a sampling period.

Considering the 6L1D and 6L2D converters, some controlled switches are replaced by diodes, and consequently, part of the voltage vectors and redundancies are lost. For example, as can be seen in Fig. 5, the voltage vectors that can be generated and the redundancies that can be utilized depend on the direction of i_g. This explains why these converters have a more restricted region of operation. As can be observed from the space-vector planes, the generated voltages can have up to five voltage levels.

TABLE II
VALUES OF i_{C_a} FOR THE VECTOR $\mathbf{v} = E + jE$ (6L TOPOLOGY)

Voltage vector	Switching combination						i_{C_a}
	q_{g_a}	q_{g_b}	q_{l_a}	q_{l_b}	q_{h_a}	q_{h_b}	
$\mathbf{v}_{001}$	0	0	0	0	0	1	0
$\mathbf{v}_{031}$	0	0	1	1	0	1	i_l
$\mathbf{v}_{220}$	1	0	1	0	0	0	$-i_h$
$\mathbf{v}_{223}$	1	0	1	0	1	1	0
$\mathbf{v}_{301}$	1	1	0	0	0	1	i_g
$\mathbf{v}_{331}$	1	1	1	1	0	1	$-i_h$

V. TECHNIQUES FOR BALANCING DC-LINK VOLTAGES

Given that some equivalent voltage vectors are generated by more than one switching combination and many of these combinations can have different effects in the capacitor's voltages, the dc-link voltages can be regulated using these redundancies.

The instantaneous value of dc-link A current (i_{C_a}) depends on the switching combination that is being utilized to generate a given voltage vector. Consequently, the value of i_{C_a} can be calculated by

$$i_{C_a} = q_{g_a} i_g - q_{l_a} i_l + q_{h_a} i_h \tag{8}$$

for the 6L topology, and

$$i_{C_a} = d_{g_a} i_g - q_{l_a} i_l + q_{h_a} i_h \tag{9}$$

for 6L1D and 6L2D topologies, where $i_h = i_l - i_g$.

The redundancies can be used to impose instantaneous values of i_{C_a} that contribute to increase or decrease the voltage of dc-link A (v_{C_a}). For example, as can be seen in Fig. 4, the voltage vector $E + jE$ can be generated by six different switching combinations when the 6L topology is implemented. Table II shows the value of i_{C_a} for each of these redundancies. The instantaneous values of i_{C_a} can be ranked, so the combinations that generate the highest values can be used when to increase v_{C_a} is desired, while the ones that generate the lowest values can be used when to decrease v_{C_a} is desired. Additionally, the redundancies that generate i_{C_a} equal to zero can be used when there is no need to increase or decrease v_{C_a}. When two or more redundancies impose the same i_{C_a}, the one that reduces the switching frequency of the converter is chosen.

Three PWM operation modes are developed to balance the dc-link voltages.

1) *PWM mode I:* This mode is utilized when v_{C_a} is within the tolerable balancing range. The redundancies are selected so i_{C_a} is equal to zero, when this is possible, or has the minimum amplitude.
2) *PWM mode II:* This mode is utilized when v_{C_a} should be increased. The redundancies are selected so i_{C_a} has one of its highest possible values.
3) *PWM mode III:* This mode is utilized when v_{C_a} should be decreased. The redundancies are selected so i_{C_a} has one of its lowest possible values.

Fig. 6 shows how to choose the PWM operating mode. In the beginning of the sampling period, v_{C_a} is compared with $v^*_{C_a}$. If the voltage is within the tolerable balancing range, the converter uses PWM mode I. Otherwise, it uses PWM modes II or III. If dc-link A voltage needs to be increased, PWM mode II is utilized. If dc-link A voltage needs to be decreased, PWM mode III is utilized. This procedure can be done for the proposed and conventional topologies, since i_{C_a} can be calculated for all switching states using (8) and (9).

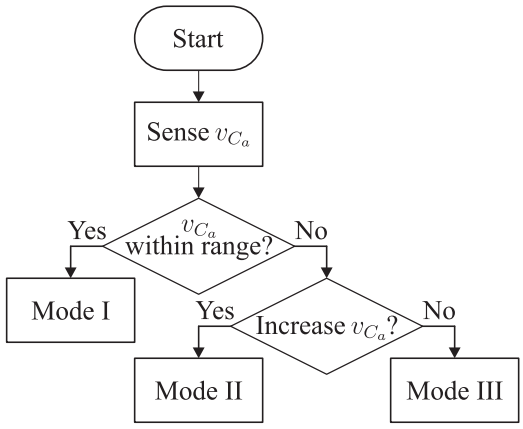

Fig. 6. Operation mode selection.

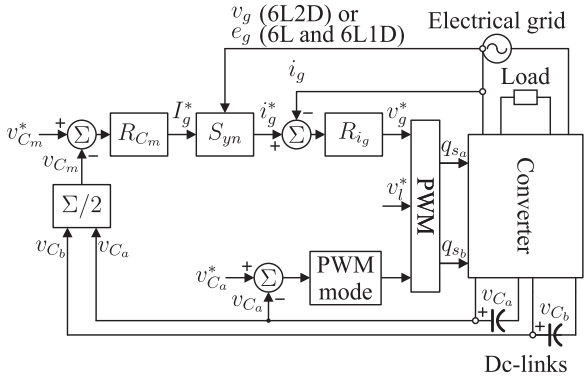

Fig. 7. Control diagram.

Many voltage vectors have redundancies. However, the dc-link voltages can be regulated using only part of these redundancies. This reduces the processing time of the technique. The 6L2D topology is the one with the lowest number of redundancies. However, its redundancies are sufficient to regulate the dc-link voltages in most of the cases. It is worthwhile to mention that the control can be implemented using more distant voltage levels in a load condition in which the use of redundancies is not sufficient to balance the dc-link voltages.

VI. CONTROL SYSTEM

The control block diagram of the proposed systems is presented in Fig. 7. R_{C_m} is a PI controller that receives the error $v^*_{C_m} - v_{C_m}$, where $v_{C_m} = \frac{v_{C_a} + v_{C_b}}{2}$, and generates the reference amplitude of i^*_g (I^*_g). The reference current is calculated by block S_{yn}, which synchronizes i^*_g to e_g or v_g, depending on the configuration utilized. In the case of 6L and 6L1D topologies, i^*_g and e_g are synchronized and this guarantees a unity grid power factor. On the other hand, in the case of the 6L2D

TABLE III
PARAMETERS USED IN THE ANALYSIS

Parameter		Value
Reference grid-side voltage	V_g^*	122.1 V(rms)
Reference load voltage	V_l^*	120 V(rms)
Dc-link voltages	v_{C_a}/v_{C_b}	90 V
Angle between v_g and v_l	α	0°
Load power	P_l	500 W
Load power factor	$\cos\varphi$	0.9
Grid and load frequencies	f_g/f_l	60/60 Hz
Sampling frequency	f_s	10.02 kHz

TABLE IV
VOLTAGE WTHD VALUES (%)

Converter	WTHD_{v_g}	WTHD_{v_l}
6L	0.1423	0.1346
6L1D	0.1423	0.1346
6L2D	0.1423	0.1347

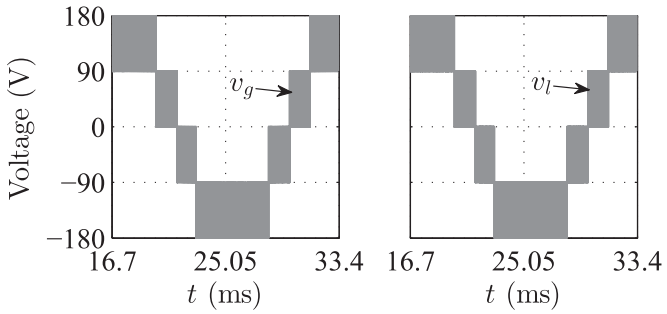

Fig. 8. Voltages generated (the waveforms are similar for 6L, 6L1D, and 6L2D converters).

converter, i_g^* and v_g need to be synchronized, so the topology can generate the reference voltages correctly and operate without zero-crossing grid current distortion. In this case, the topology cannot operate with the unity grid power factor. However, the grid inductor filter is projected, so the phase angle between e_g and v_g is small, and consequently, the grid can operate with the high power factor.

The controller R_{i_g} receives the error $i_g^* - i_g$ and generates the reference voltage v_g^* using a double-sequence controller [19]. In addition to the control of v_{C_m}, v_{C_a} and v_{C_b} should be balanced. As explained previously, the voltage vectors applied impact on the capacitors voltages. As a solution, the technique presented in Section V should be utilized (the block PWM mode in Fig. 7 operates as described in Fig. 6). This technique selects the operation mode according to the value of v_{C_a}.

The possible values of α for each configuration and operation condition are provided in Section III. This angle can be utilized to reduce the common leg current (i_h). This is not discussed in this paper because the 6L2D converter can only operate with $\alpha = 0^\circ$. Besides, the common leg current technique is not interesting for some applications. More information about this technique is provided in [18].

TABLE V
POWER LOSSES AND EFFICIENCY OF THE TOPOLOGIES

Converter	P_{cd} (W)	P_{sw} (W)	P_{to} (W)	E_f (%)
6L	23.36	9.11	32.47	93.90
6L1D	23.36	9.11	32.47	93.90
6L2D	21.48	8.36	29.84	94.37

TABLE VI
SWITCHING FREQUENCY VALUES (KHZ)

Converter	$f_{q_{g_a}}$	$f_{q_{h_a}}$	$f_{q_{l_a}}$	$f_{q_{g_b}}$	$f_{q_{h_b}}$	$f_{q_{l_b}}$
6L	0.06	6.54	0.06	0.06	3.72	10.08
6L1D	x	6.54	0.06	0.06	3.72	10.08
6L2D	x	6.54	0.06	x	3.72	10.08

TABLE VII
PARAMETERS USED IN SIMULATIONS AND EXPERIMENTAL TESTS

Parameter		Value
Grid voltage	E_g	110 and 126 V(rms)
Reference load voltage	V_l^*	110 V(rms)
DC-link voltages	v_{C_a}/v_{C_b}	90 V
Hysteresis voltage band	2% of v_{C_a}	1.8 V
DC-link capacitancies	C_a/C_b	2200 μF
Grid and load frequencies	f_g/f_l	60/60 Hz
Sampling frequency	f_s	10 kHz

VII. COMPARISON OF CONFIGURATIONS

In this section, a comparative analysis of the investigated topologies in terms of harmonic distortion and semiconductor losses is performed. The simulations were done in open loop, and Table III shows the parameters used in the analysis.

Given that 6L1D and 6L2D topologies are basically the 6L converter with a lower number of controlled switches, all considered topologies have redundancies in common. Considering an operation point that is part of the operation range of all the converters, they may use the same redundancies, and consequently, they will generate voltages with similar harmonic distortions. To generate the results presented in this section, all the converters were simulated using their redundancies in common.

The voltage vectors are always applied symmetrically with respect to half of the sampling interval and the redundancies are selected so the switching frequency is minimized. Besides, whenever possible, the switching combinations that generate $i_{C_a} = 0$ are utilized, so the power flux between the two dc-links is minimized.

The voltage supplied by the grid was $E_g = 120$ V(rms) (6L and 6L1D configurations) and $E_g = 124.8$ V(rms) (6L2D configuration). These values of E_g generate a reference voltage $V_g^* = 122.1$ V(rms). As the 6L2D configuration synchronizes v_g and i_g (in the case simulated, the grid power factor is 0.98), V_g will be lower than E_g, and to guarantee that $V_g \geq V_l$ so this topology will operate properly, E_g needs to be higher than 1 p.u. [in this case, 1 p.u. corresponds to 120 V(rms)]. The others con-

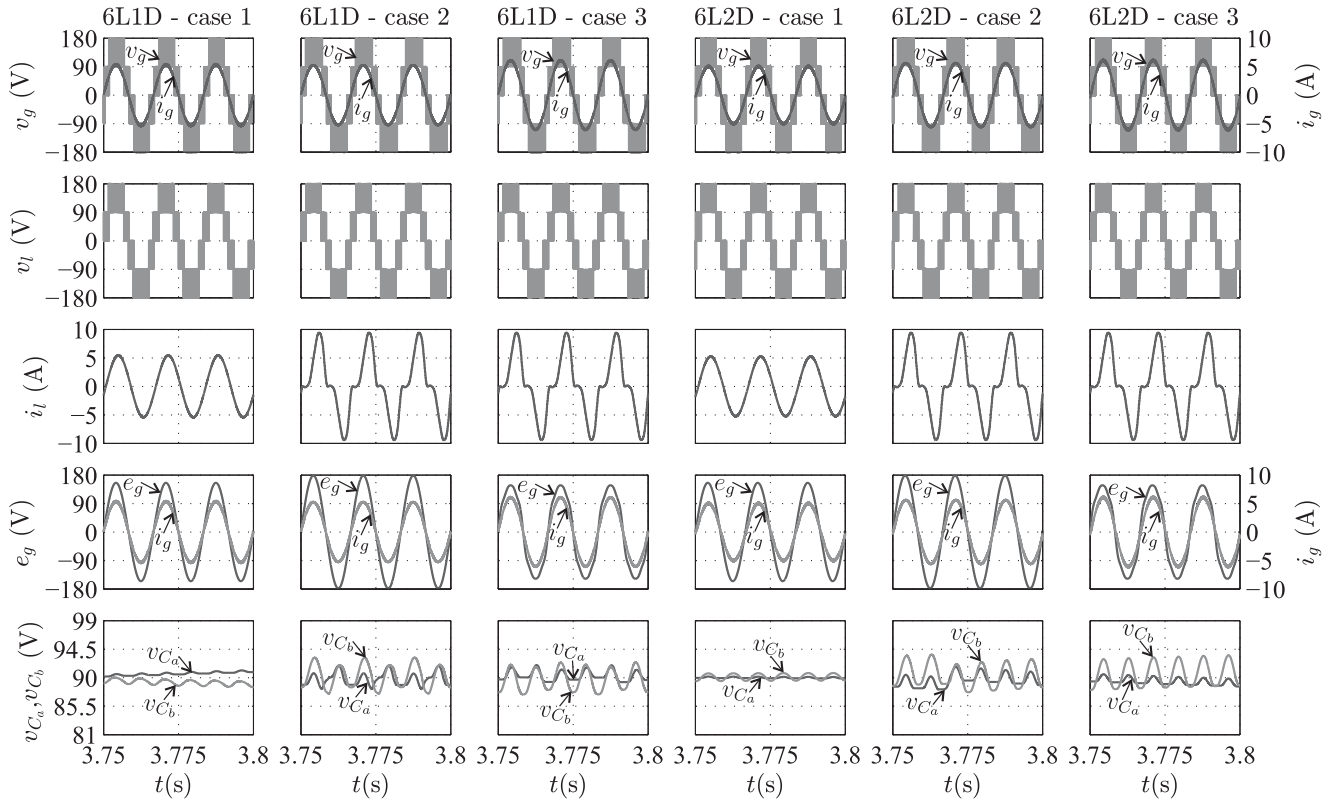

Fig. 9. Simulation of the control (the results of the 6L1D configuration are left, while the results of the 6L2D configuration are right).

verters synchronize e_g and i_g (the grid has a unity power factor) and can operate with E_g equal to 1 p.u. Considering this information, in order to operate with grid and load voltages equal to 1 p.u. and under voltage sags, the 6L2D system needs to utilize a grid-side step-up transform and to increase the dc-link voltages. If this topology operates with $E_g = 220$ V(rms) and $V_l = 110$ V(rms), there is no need to use a transformer because V_g will always be greater than V_l.

A. Harmonic Distortion

The weighted total harmonic distortion (WTHD) of the voltages generated by the converter is given by

$$\text{WTHD}(\%) = \frac{100}{\gamma_1}\sqrt{\sum_{h=2}^{N_h}\left(\frac{\gamma_h}{h}\right)^2} \tag{10}$$

where γ_1 is the fundamental voltage amplitude, γ_h is the corresponding harmonic component amplitude of the hth order, and N_h is the number of considered harmonics ($N_h = 1000$).

Table IV shows the WTHDs of the voltages generated by each configuration. As can be seen, all the topologies have the same results because they utilize the same redundancies to generate the voltages. It is important to point out that, even though the proposed topologies have less redundant voltage vectors, all the converters can operate changing only two switching states over a sampling period. Fig. 8 shows the voltages generated by the converters (the waveforms are similar for all the topologies).

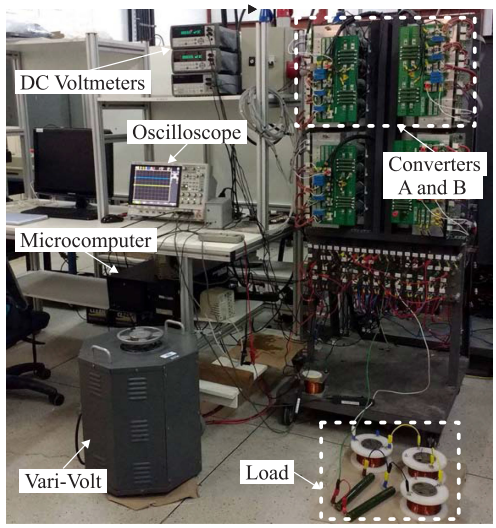

Fig. 10. Experimental setup.

B. Semiconductor Losses

Table V shows the conduction, switching, and total losses (P_{cd}, P_{sw}, and P_{to}, respectively) of the investigated configurations. These results were obtained under the same conditions presented in the previous subsection. The efficiency of the conversion systems [$E_f(\%)$], also shown Table V, is defined by

$$E_f(\%) = 100\left(\frac{P_l}{P_l + P_{to}}\right). \tag{11}$$

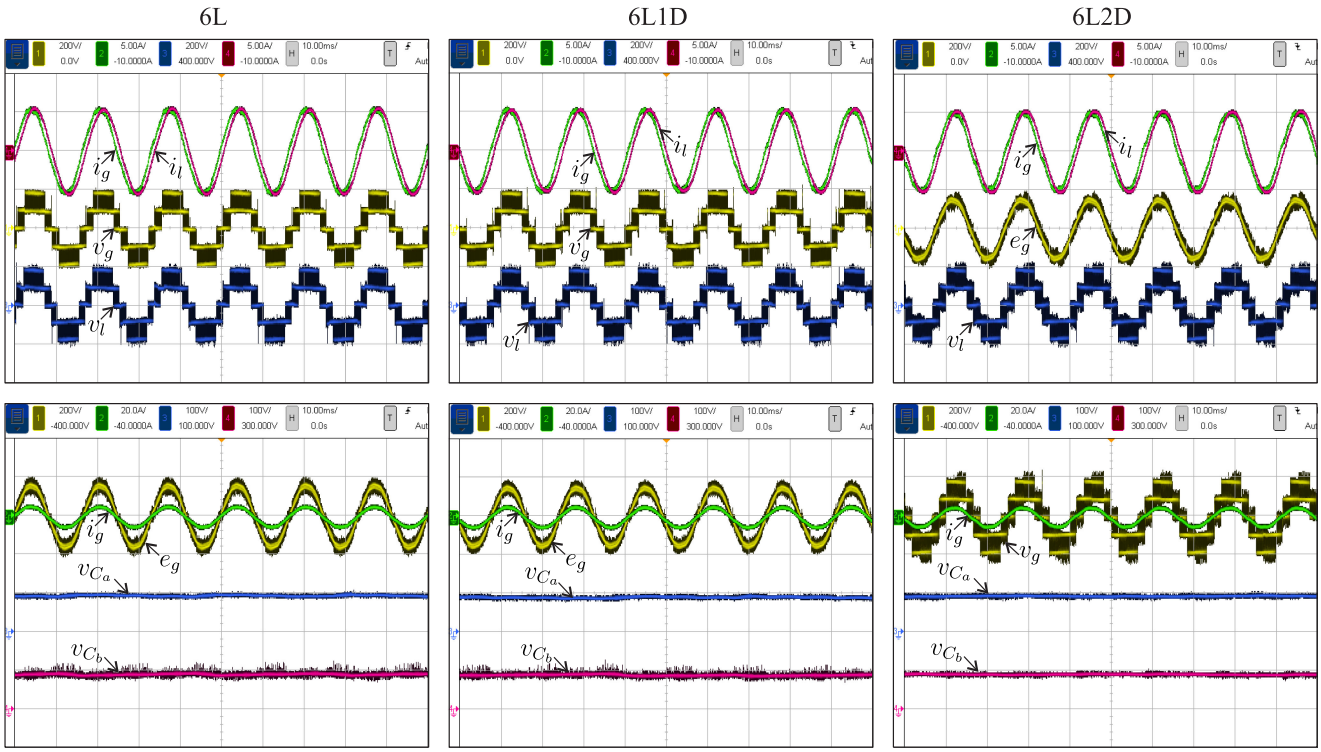

Fig. 11. Experimental results with an *RL* load.

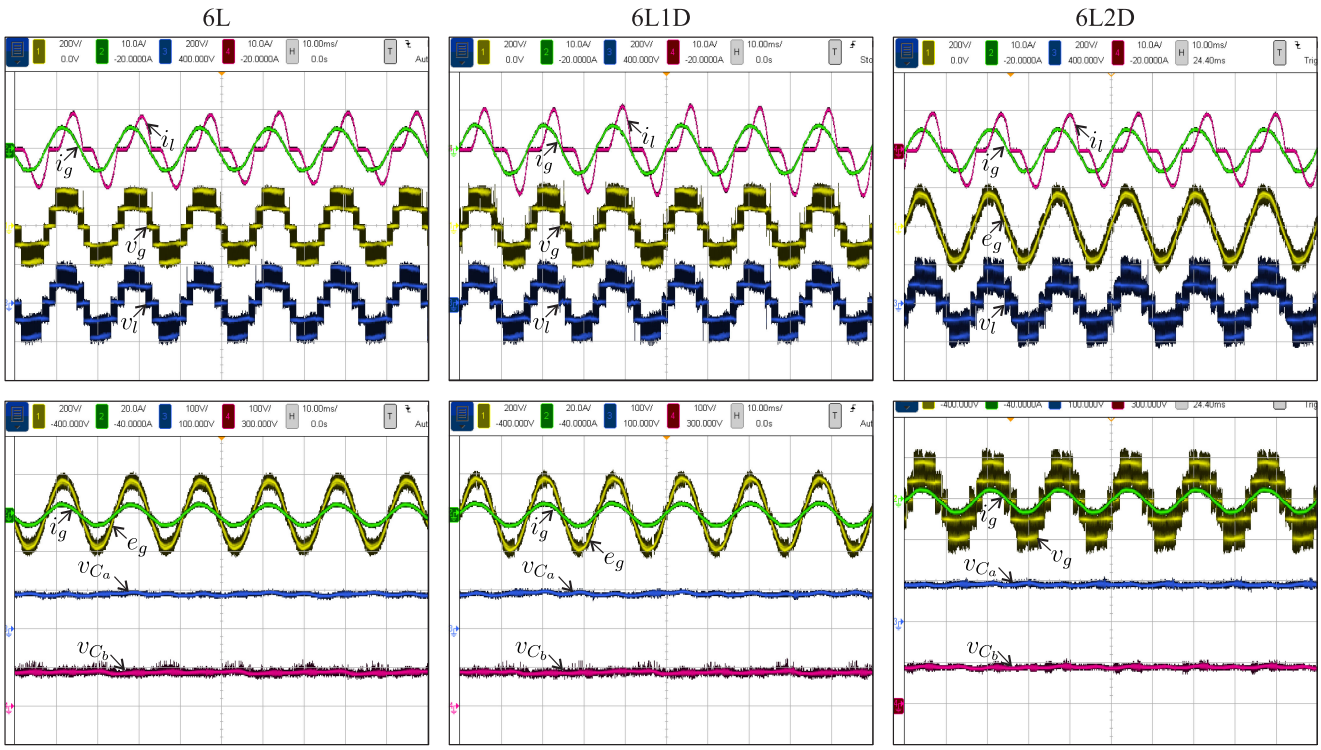

Fig. 12. Experimental results with a nonlinear load and grid overvoltage.

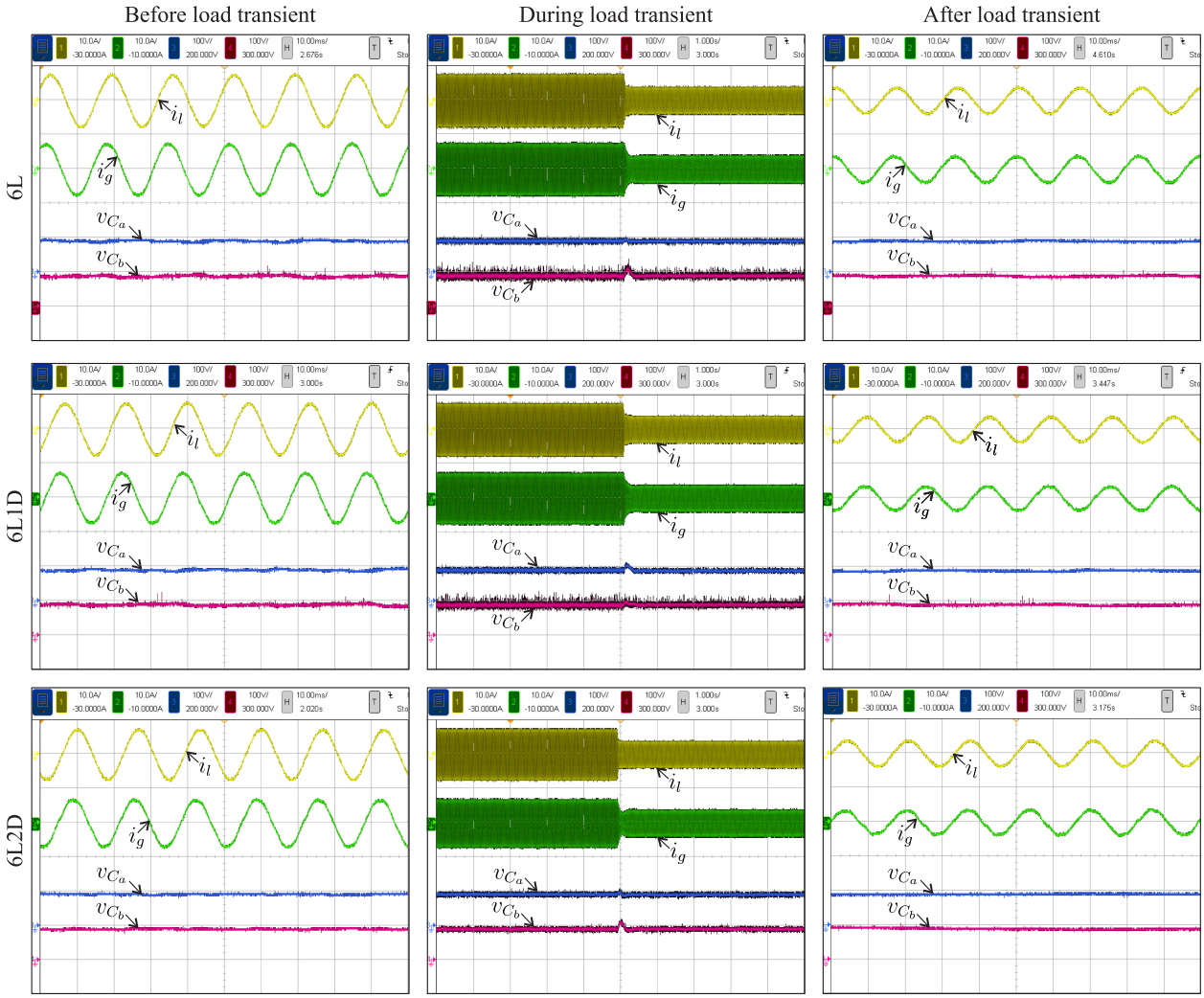

Fig. 13. Experimental results with load transient.

The switch loss model used was presented in [20] and takes into account insulated-gate bipolar transistor (IGBT) and diode conduction losses, IGBT turn-on losses, IGBT turn-off losses, and diode turn-off energy.

The 6L and 6L1D topologies have the same semiconductor losses because they both operate with e_g and i_g synchronized, and consequently, the values of i_g, i_l, and i_h are the same for both converters. As should be noticed, the 6L2D topology has the lowest total losses (8% lower than the ones from 6L and 6L1D converters) and, consequently, the highest efficiency. This happens because this configuration operates with v_g and i_g synchronized. This reduces the displacement angle between i_g and i_l and, consequently, reduces the amplitude of the common leg current i_h. It is important to notice that, if the other topologies operate with v_g and i_g synchronized, they will have the same efficiency of the 6L2D converter.

Table VI shows the frequency of each switch with all the topologies operating with the same sampling frequency. The diodes of 6L1D and 6L2D configurations operate with the switching frequency equal to the fundamental frequency of the grid current (in this case, 60 Hz).

VIII. Simulation and Experimental Results

Computer simulations and experimental results have been carried in the same operation conditions to verify the validity of the theoretical considerations. The parameters utilized in the tests are provided in Table VII.

A. Simulation Results

The simulation was carried out using the software MATLAB. Three cases were simulated.

1) *Case 1:* $E_g = 110$ V(rms) and an *RL* load (load resistance and inductance $R_l = 27\,\Omega$ and $L_l = 21$ mH, respectively).
2) *Case 2:* $E_g = 126$ V(rms) and a nonlinear load.
3) *Case 3:* Fundamental grid voltage $E_{g_1} = 110$ V(rms) with harmonics (8% of the third harmonic, 5% of the fifth harmonic, and 2% of the seventh harmonic) and a nonlinear load.

Fig. 9 shows the simulation results of the configurations 6L1D and 6L2D in all the cases. As expected, 6L1D operates with the

unity grid power factor. On the other hand, 6L2D operates with v_g and i_g synchronized. The dc links are adequately controlled, and grid and load voltages have five levels, which is consistent with the theoretical analysis.

B. Experimental Results

The setup used in the experimental tests has been built employing power devices from SEMIKRON, with the switches being IGBTs with dedicated drives (SKHI23). A digital signal processor TMS320F28335 with plug-in boards and sensors are used to gating signals generation and to measure variables. Fig. 10 shows a general view of the experimental setup highlighting some devices.

The experimental results showing operation of the systems with $E_g = 110$ V(rms) and an *RL* load are presented in Fig. 11. The parameters utilized are equal to the ones in case 1 of the simulation results. When the converters 6L and 6L1D are utilized, it can be seen that i_g and e_g are synchronized, so the grid unity power factor is guaranteed. It also shows that the dc-link voltages are adequately controlled and that the generated voltages have five levels. When the converter 6L2D is utilized, it can be seen that i_g and v_g are synchronized, as expected, the dc-link voltages are adequately controlled, and the generated voltages have five levels. The experimental results showing the operation of the systems with $E_g = 126$ V(rms) (grid overvoltage) and a nonlinear load (the parameters utilized are equal to the ones in case 2 of the simulation results) are presented in Fig. 12. Similarly to the results with an *RL* load and without grid overvoltage, the systems worked adequately.

In the last set of experimental results, a variation in load was performed to evaluate the dynamical performance of the systems, as shown in Fig. 13. A step reduction in the load was made, so the amplitude of the load current was decreased by 50% in relation to its initial value. Notice that all control requirements have been established.

IX. Conclusion

Single-phase ac–dc–ac topologies for nonregenerative applications composed of two three-leg converters with equal dc-link voltages connected in series are proposed and discussed in this paper. Compared to the conventional configuration, the proposed systems permit to reduce the number of drivers and controlled switches, reducing the total cost of the systems. The system model, the region of operation, the space-vector PWM technique, and a method to regulate the dc-link voltages using the voltage vector redundancies are presented, and a complete control system is given. Under some conditions, 6L and 6L1D converters can operate with similar voltage harmonic distortions and semiconductor losses. Besides, the angle between the grid voltage and current can be synchronized, so both topologies can operate with a unity grid power factor. The 6L2D topology should operate with v_g, v_l, and i_g synchronized to avoid zero-crossover distortion in the grid current. Consequently, it cannot operate with the unity grid power factor. Additionally, the amplitude of the load-side voltage should be lower than or equal to the amplitude of the grid-side voltage. Therefore, in applications in which the amplitudes of grid and load voltages are equal to 1 p.u., a step-up transformer should be utilized to increase E_g above 1 p.u. and guarantee that $V_g \geq V_l$. Simulation and experimental results are provided to support the theoretical considerations. The 6L1D topology was verified as the more interesting option because, compared to the conventional 6L topology, it has approximate performance and lower total cost. Summarizing, it is shown that the converter can supply a load (including a nonlinear load) with sinusoidal regulated voltage consuming sinusoidal grid current with a high input power factor (even if the grid voltage is distorted). Consequently, the proposed converters can be used as UPSs and UPQCs for nonregenerative applications.

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Nayara Brandão de Freitas (S'12) was born in Campina Grande, Brazil, in 1991. She received the B.S. and M.S. degrees in electrical engineering in 2015 and 2016, respectively, from the Federal University of Campina Grande, Campina Grande, where she is currently working toward the Ph.D. degree in electrical engineering.

Her current research interests include power electronics and electrical drives.

Cursino Brandão Jacobina (S'78–M'78–SM'98–F'14) was born in Correntes, Brazil, in 1955. He received the B.S. degree in electrical engineering from the Federal University of Paraíba, Campina Grande, Brazil, in 1978, and the Diplôme d'Etudes Approfondies and the Ph.D. degrees in electrical engineering from the Institut National Polytechnique de Toulouse, Toulouse, France, in 1980 and 1983, respectively.

From 1978 to March 2002, he was with the Department of Electrical Engineering, Federal University of Paraíba, João Pessoa, Brazil. Since April 2002, he has been with the Department of Electrical Engineering, Federal University of Campina Grande, Campina Grande, where he is currently a Professor. His research interests include electrical drives, power electronics, and energy systems.

Nustenil Segundo de Moraes Lima Marinus (S'11–M'17) was born in Castanhal, Pará, Brazil, in 1989. He received the B.S., M.S., and Ph.D. degrees in electrical engineering from the Federal University of Campina Grande, Campina Grande, Brazil, in 2011, 2012, and 2016, respectively.

From 2011 to April 2013, he was with the Federal Institute of Alagoas, Arapiraca, Brazil. Since May 2013, he has been with the Federal Institute of Ceará, Cedro, Brazil, where he is currently a Professor. His research interests include electrical drives, power electronics, and energy systems.

Nady Rocha (M'10) was born in São Gabriel, Bahia, Brazil, in 1982. He received the B.S., M.S., and Ph.D. degrees in electrical engineering from the Federal University of Campina Grande, Campina Grande, Brazil, in 2006, 2008, and 2010, respectively.

Since 2011, he has been with the Department of Electrical Engineering, Federal University of Paraíba, João Pessoa, where he is currently a Professor of electrical engineering. From 2013 to March 2015, he was a tutor of the PET Education Program Tutorial undergraduate degree in electrical engineering. His research interests include power electronics, renewable energy sources, and electrical drives.