Letters

2-Phase 3-Level ETSM With Mismatch-Free Duty Cycles Achieving 88.6% Peak Efficiency for a 20-MHz LTE RF Power Amplifier

Hui-Dong Gwon, Jun-Suk Bang, Kye-Seok Yoon, Se-Hong Park, Sang-Hui Park, Min-Yong Jung, Sang-Han Lee, Min-Woo Kim, Sung-Wan Hong, and Gyu-Hyeong Cho, *Fellow, IEEE*

***Abstract*—This letter presents a 2-phase 3-level (2P3L) envelope tracking supply modulator (ETSM) for a long-term evolution 20 MHz (LTE20) radio frequency power amplifier as a solution for the ET system. This 2P3L ETSM that is composed of only switching converters achieves high efficiency, fast transient response, and a small output current ripple. To properly operate the proposed 2P3L ETSM, 4 pulse width modulatiop (PWM) signals with a 90° phase shift from each PWM signal are required without any mismatch between duty cycles. To remove the mismatch, a time-division multiplexing comparator and a duty-cycle calibrator are proposed. Thanks to the proposed techniques, the proposed ETSM fabricated in 0.18-μm CMOS achieved the highest peak dynamic efficiency of 88.6% with an LTE20 signal, which is superior to the state-of-the-art systems.**

***Index Terms*—2-phase 3-level (2P3L) architecture, duty-cycle calibrator (DCC), envelope tracking supply modulator (ETSM), mismatch-free duty cycles, time-division multiplexing comparator (TDMC).**

I. Introduction

RECENT long-term evolution 20 MHz (LTE20) wireless communication system demands advanced modulation techniques and high transmitting speeds to improve spectral efficiency and provide high data rates. An orthogonal frequency division multiplex (OFDM) system is suitable for LTE20 system. However, this OFDM system results in a signal with a high peak-to-average ratio (PAPR) [1].

Efficient radio frequency (RF) power amplifiers (PAs) are required in battery-operated LTE20 wireless systems. Unfortunately, conventional RF PAs having a fixed supply voltage ($V_{\rm DD}$) suffer from a low efficiency, which decreases the battery life time of mobile devices, especially when the signal has a higher PAPR [2]. An envelope tracking (ET) technique is an attractive solution for improving the efficiency of the RF PA. The envelope tracking supply modulator (ETSM) provides a dynamically modulated $V_{\rm DD}$ to the RF PA to increase the efficiency dramatically.

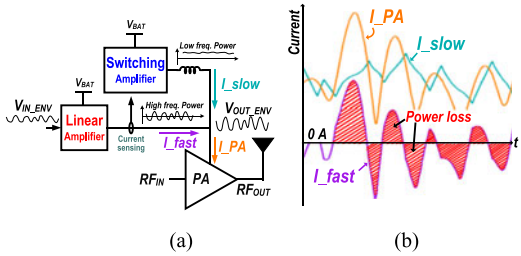

Fig. 1. Conventional hybrid ETSM. (a) Structure. (b) Current flow.

Previously, a hybrid amplifier (HA), which combines a switching converter (SC) and a linear amplifier (LA) in parallel, has been researched as the ETSM [3]–[8], as shown in Fig. 1(a). In the HA, the SC provides the lower frequency power for the RF PA, and the LA provides higher frequency power for the RF PA. However, the HA suffers from the low efficiency because the LA, which consumes large power, takes a large portion of the whole signal especially in LTE20, as shown in Fig. 1(b).

To increase the efficiency, ETSMs mainly composed of two SCs were introduced [9]–[11]. However, these ETSMs have mismatch problems between inductor currents of 2-phase interleaved SCs [10] and duty cycles of 3-level (3L) SC [9], [11]. Because of these mismatches, the ETSMs could also suffer from low efficiency, a low transient response, and a large output current ripple [13]–[15]. If there is no mismatch problem, both the 2-phase interleaved SCs and the 3L SC can achieve better performance. The inductor current sensing scheme could be used to remove the mismatch problems by error-integral feedback [14]. However, it is almost impossible to match the inductor currents of a time-varying ac, such as envelope signal, by the error-integral feedback.

This letter proposes a 2-phase 3-level (2P3L) ETSM that achieves high efficiency and solves the mismatch problems. The proposed ETSM is composed of only two interleaved SCs

Manuscript received July 6, 2017; revised August 12, 2017; accepted September 5, 2017. Date of publication September 20, 2017; date of current version January 3, 2018. This work was supported in part by the SAMSUNG ELECTRO-MECHANICS-KAIST MRFC center, and in part by the Sookmyung Women's University Research under Grant 1-1703-2037. *(Corresponding author: Sung-Wan Hong.)*

H.-D. Gwon, J.-S. Bang, K.-S. Yoon, S.-H. Park, S.-H. Park, M.-Y. Jung, S.-H. Lee, M.-W. Kim, and G.-H. Cho are with the School of Electrical Engineering, Korea Advanced Institute of Science and Technology, Daejeon 34141, South Korea (e-mail: wings@kaist.ac.kr; jsbang86@kaist.ac.kr; oscar04@kaist.ac.kr; sehong@kaist.ac.kr; pshui789@kaist.ac.kr; myjung@kaist.ac.kr; sanghan21c@kaist.ac.kr; kimmw@kaist.ac.kr; ghcho@kaist.ac.kr).

S.-W. Hong is with the Department of Electronics Engineering, Sookmyung Women's University, Seoul 140-742 South Korea (e-mail: hsw0930@sookmyung.ac.kr).

Color versions of one or more of the figures in this letter are available online at http://ieeexplore.ieee.org.

Digital Object Identifier 10.1109/TPEL.2017.2754651

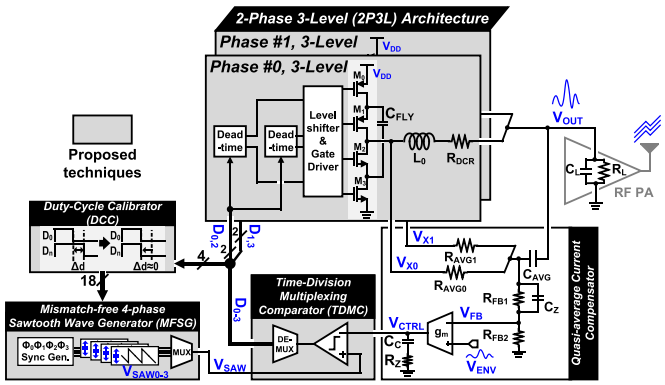

Fig. 2. Proposed 2P3L switching-converter-only ETSM.

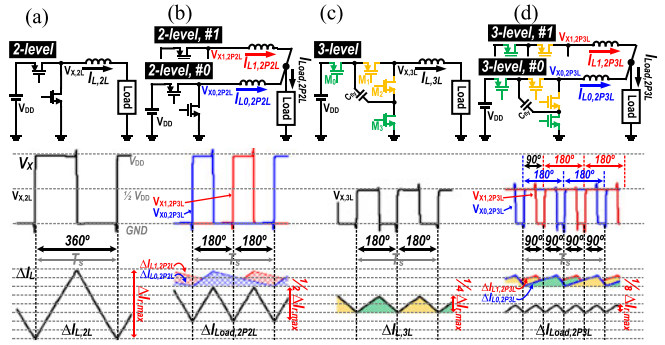

Fig. 3. Comparison of the effective switching frequency ($f_{\mathrm{SW.EFF}}$) and the maximum output current ripple ($\Delta I_{\mathrm{r.max}}$) for (a) 2-level, (b) 2P2L, (c) 3L, and (d) 2P3L buck converter.

that have a 3L operation without using an LA. To solve the mismatch problems, we suggest a time-division multiplexing comparator (TDMC) and a mismatch-free quadrature 4-phase sawtooth wave generator (MFSG) with a duty-cycle calibrator (DCC) that calibrates a 4-phase sawtooth wave generator for mismatch-free duty cycles.

The letter is organized as follows. A detailed explanation of the characteristics, operation, and implementation of the proposed 2P3L ETSM is presented in Section II. The measured and simulated results are reported in Section III, and conclusions are given in Section IV.

II. Proposed 2P3L ETSM With Mismatch-Free Duty Cycles

A block diagram of the proposed 2P3L ETSM is shown in Fig. 2. Each part of the proposed ETSM is explained below.

A. 2P3L Architecture for the ETSM

To track a high PAPR envelope signal without using an LA, the ETSM that is composed of only SCs must operate with a high switching frequency (f_{SW}). However, the high f_{SW} inherently leads to a low efficiency. One solution is a multiphase SC [15]. Fig. 3(b) shows a basic 2-phase 2-level (2P2L) SC. The effective f_{SW} ($f_{\mathrm{SW.EFF}}$) of the 2P2L SC is twice the f_{SW} of each phase SC with a 180° phase difference. This operation improves the transient response and the efficiency. Another solution is a 3L SC [12], shown in Fig. 3(c). In the 3L SC, M_0, M_3 and M_1, M_2 operate at a phase shifted by 180°, which doubles the $f_{\mathrm{SW.EFF}}$. The voltage swing at the switching node voltage [$V_{\mathrm{X,3L}}$ in Fig. 3(c)] of the 3L SC is always half of the supply voltage. So the maximum output current ripple ($\Delta I_{L,3L}$) of the 3L SC is four times smaller than that of the 2L SC ($\Delta I_{r.\mathrm{max}}$) shown Fig. 3(a). The proposed 2P3L ETSM increases $f_{\mathrm{SW.EFF}}$ further by combining two 3L SCs as the 2P architecture. Because the 3L SC already operates at a phase shifted by 180°, each phase of the 2P3L SC should operate with a 90° phase shift, as shown in Fig. 3(d). Owing to these quadrature 4-phase duty cycles for one period (T_s), the $f_{\mathrm{SW.EFF}}$ of the 2P3L architecture becomes four times higher than the f_{SW}. This increased $f_{\mathrm{SW.EFF}}$ improves the transient response and the efficiency. In addition, the maximum output current ripple ($\Delta I_{\mathrm{Load},2P3L}$) of the 2P3L SC shown in Fig. 3(d) is eight times smaller than that of 2L SC ($\Delta I_{r.\mathrm{max}}$) shown in Fig. 3(a). The maximum output current ripple (ΔI_L) of multiphase and multilevel converters can be generalized as

$$\Delta I_L = \frac{V_{\mathrm{OUT}} \cdot (1-D)}{L_0 \cdot f_{\mathrm{SW}}} \cdot \frac{\mathrm{PH} \cdot \left(D - \frac{m}{\mathrm{ND}}\right) \cdot \left(\frac{m+1}{\mathrm{ND}} - D\right)}{D \cdot (1-D)} \tag{1}$$

where D, PH, L_0, and ND are the duty cycle, the number of phase, the inductance per each phase, and the number of duty cycles per one switching period, respectively. The m is the maximum integer that does not exceed the $ND{\cdot}D$.

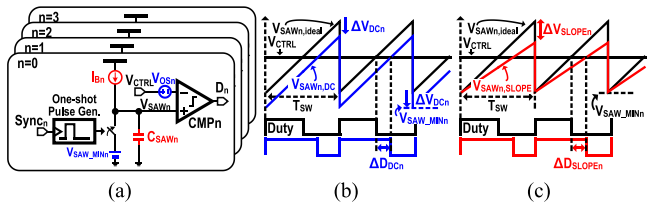

Fig. 4. Mismatch factor of conventional 4-phase PWM generator. (a) Schematic of PWM generator. (b) DC-level shift. (c) Slope difference.

B. Conventional Quadrature 4-Phase PWM Generator

Generally, four comparators are used to generate the quadrature 4-phase Pulse width modulation (PWM) signals (D_{0-3}) as shown in Fig. 4(a). When each comparator compares a control signal voltage (V_{CTRL}) and each sawtooth wave ($V_{\mathrm{SAW0-3}}$), there are two main factors that cause the mismatch between the duty cycles. One is the dc-level variation ($\Delta V_{\mathrm{DC0-3}}$) caused by the differences between comparator offsets ($V_{\mathrm{OS0-3}}$) and minimum reference voltages ($V_{\mathrm{SAW\_MIN0-3}}$), and the other is the peak voltage variation ($\Delta V_{\mathrm{SLOPE0-3}}$) caused by mismatches between each C_{SAWn} and each I_{Bn}, shown in Fig. 4(a). These factors experience variations between duty cycles ($\Delta D_{\mathrm{DC0-3}}$ and $\Delta D_{\mathrm{SLOPE0-3}}$) as shown in Fig. 4(b) and (c), respectively. If there is no mismatch between duty cycles, two inductor currents are well-balanced and the output current ripple is small. On the other hand, if the mismatch occurs in any of the duty cycles, unbalanced currents flow across individual inductors, and induce low efficiency, a slow transient response, and a large output current ripple [13], [15]. Therefore, it is important to remove the mismatch of the duty cycles. The duty-cycle mismatches

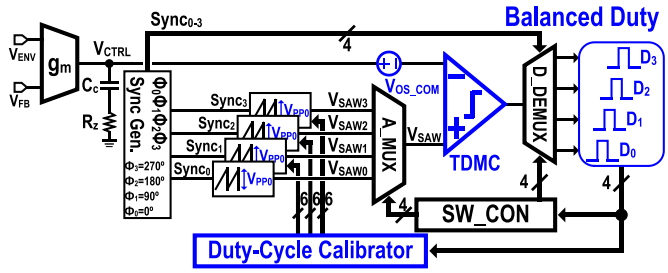

Fig. 5. Proposed mismatch-free quadrature 4-phase PWM generator.

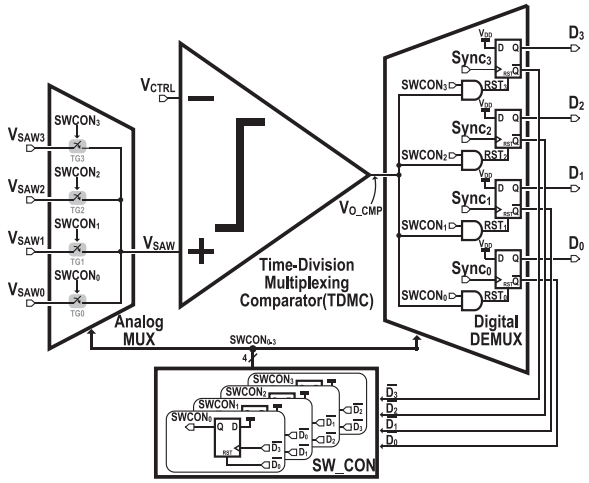

Fig. 6. Schematic of proposed TDMC.

caused by variations of $V_{\mathrm{DC}n}$ (the sum of $\Delta V_{\mathrm{SAW\_MIN}n}$ and $V_{\mathrm{OS}n}$), $C_{\mathrm{SAW}n}$, and $I_{\mathrm{B}n}$ are calculated as

$$\left(\frac{\Delta D}{D}\right)_{\mathrm{DC}} = \frac{\Delta V_{\mathrm{DC}n}}{V_{\mathrm{CTRL}} - V_{\mathrm{SAW\_MIN}n}} \tag{2}$$

$$\left(\frac{\Delta D}{D}\right)_{C} = \frac{D_i - D}{D} = \frac{\Delta C_{\mathrm{SAW}n}}{C_{\mathrm{SAW}n}} \tag{3}$$

$$\left(\frac{\Delta D}{D}\right)_{I} = \frac{D_i - D}{D} = -\frac{\Delta I_{\mathrm{B}n}}{I_{\mathrm{B}n} + \Delta I_{\mathrm{B}n}}. \tag{4}$$

According to (2)–(4), the conventional 4-phase PWM generator is significantly vulnerable to the duty-cycle mismatch, because all $V_{\mathrm{DC}n}$, $C_{\mathrm{SAW}n}$, and $I_{\mathrm{B}n}$ are easily changed due to PVT variations. Meanwhile, there is another factor that causes the duty-cycle mismatch, which is the variation of voltage driving slope rate for the gate node of power switch. However, the effect of this variation on duty-cycle mismatch can be easily ignored if the slope rate is high enough [13]. Therefore, in this letter, the duty-cycle mismatch caused by the slope rate variation has not been considered.

C. Proposed Mismatch-Free 4-Phase PWM Generator

In the proposed PWM generator, there are two important schemes to solve the mismatch problem as shown in Fig. 5. One is the TDMC and the other is the DCC.

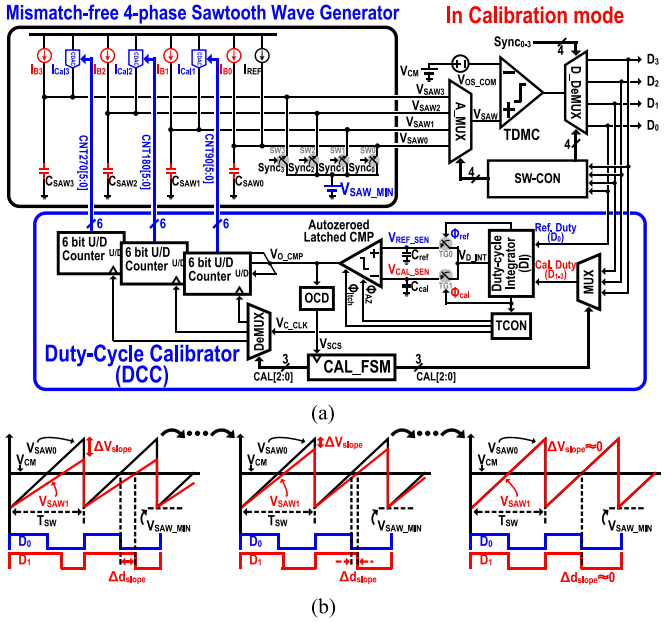

Fig. 7. (a) Schematic of proposed MFSG with DCC. (b) Calibration process.

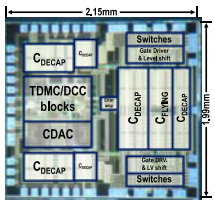

Fig. 8. Die microphoto.

1) Time-Division Multiplexing Comparator (TDMC): Generally, the start point of a duty cycle is determined by synchronized clocks ($Sync_{0-3}$). Meanwhile, the end point of each duty cycle is determined by a comparator. Since the end point of the duty cycles of 4-phase PWM signals with a 90° phase shift does not occur at the same time, the four comparators are replaced by a single comparator in the proposed PWM generator. Therefore, the proposed TDMC scheme solves the offset voltage problem with superior reliability and accuracy. The block diagram of the proposed 4-phase generator focused on the TDMC and the operation are depicted in Fig. 6. On the positive edge of $Sycn_0$, D_0 becomes high until the RST_0 signal becomes high. The RST_0 signal can be high according to the output signal of the TDMC ($V_{\mathrm{O\_CMP}}$) when the TDMC license signal for D_0 (SWCON_0) is high. When the D_0 becomes low, the SW_CON makes SWCON_0 low and SWCON_1 high. Thus, the ownership of the TDMC moves to the next phase duty-cycle (D_1). With the positive edge of Sycn_1, D_1 becomes high in a manner similar to that of D_0. D_2, and D_3 are also generated in the same way.

2) Duty-Cycle Calibrator (DCC): The other scheme is DCC, which calibrates the 4-phase sawtooth wave generator. The proposed DCC removes the mismatches between the capacitors ($C_{\mathrm{SAW}0-3}$) and the current sources ($I_{\mathrm{B}0-3}$) by calibrating three current digital-to-analog converters as shown in Fig. 7(a). In addition, each sawtooth uses the same minimum

TABLE I
PERFORMANCE COMPARISON

Publication	ISSCC '13 [7]	ISSCC '17 [17]	ISSCC '15 [16]	ISSCC '14 [9]	PE '16 [10]	PE '16 [11]	This Work
Topology	HA(SC + LA)	HA(SC + LA)	HA(SC + LA)	**SC(Slow + Fast)**	**SC(w/ SRE)**	**SC(Slow + Fast)**	**SC Only**
Input signal (MHz)	**LTE20**	**LTE20**	LTE 10	LTE 10	LTE 10	LTE 10	**LTE20**
PAPR (dB)	6.7	–	–	6.7	6	5.4	**7.4**
$f_{SW.EFF}$ (MHz)	Hysteretic	2	Hysteretic	80	80	110	116
Supply Voltage (V)	5.5	3.6-5	4	3.8	3.3	3.3	5
Max. Power (W)	0.9	2	0.8	1.8	2	1.5	2.5
Peak Dynamic Efficiency (%)	83	82	82	86.2	85.8	86.5	**88.6**
Chip Area (mm^2)	1.47	2.34	5	6.3	7.44	3.84	**4.28**
CMOS Process	180 nm	500 nm	130 nm	130 nm	180 nm	180 nm	180 nm

reference voltage (V_{SAW_MIN}). Therefore, the sawtooth generator can generate four identical sawtooth waves with the help of the DCC. The ETSM operates in calibration mode once, when it starts up. Then, a common dc voltage (V_{CM}) is applied to the negative input of the TDMC, as shown in top of the Fig. 7(a), instead of V_{CTRL}. In the calibration mode, the duty cycle D_0 is determined as a reference, and the duty cycles D_{1-3} are calibrated to be the same as D_0. For example, when the on-time of D_1 is larger than that of D_0, a slope of V_{SAW1} is more gradual than that of V_{SAW0} as shown in Fig. 7(b). Therefore, DCC increase the slope of V_{SAW1} until both slopes of V_{SAW1} and V_{SAW0} become the same. In the opposite case that the slope of V_{SAW1} is steeper than that of V_{SAW0} DCC operates in the opposite manner to make both slopes the same. This sequence is iterated until D_{1-3} becomes the same as D_0.

III. MEASUREMENT AND SIMULATION RESULTS

The proposed 2P3L ETSM is fabricated in 180-nm complementary metal-oxide-semiconductor (CMOS) process with 5-V I/O devices. The die microphoto is shown in Fig. 8. The operating conditions are tabulated in Table I. Although the chip area of this work is not the smallest among state-of-the-art ETSMs, the proposed work achieved the highest efficiency. Therefore, it can be considered that the proposed work has sufficient compatibility. For a closed-loop bandwidth over 20 MHz, two 68-nH inductors and a 1-nF output capacitor are used. Fig. 9 shows the input envelope signal (V_{ENV}) of LTE20 and the output waveform (V_{OUT}) of the ETSM with a resistive load of 5 Ω under various supply voltage conditions. Thanks to the 2P3L architecture as well as the TDMC and DCC, the V_{OUT} can accurately track the LTE20 envelope signal. The effectiveness of DCC is verified in Fig. 10. All of the waveforms in Fig. 10 are measured under the condition that one of the four capacitors used in the 4-phase sawtooth generator has a mismatch of 7%. When the ETSM operates with an input dc signal as shown in Fig. 10(a), the output voltage ripple is three times smaller and $f_{SW.EFF}$ is four times higher owing to the DCC. In addition, when the ETSM operates with an input sinusoidal signal, the distortion at V_{OUT} is drastically removed thanks to the DCC as shown in Fig. 10(b). The effectiveness of the other scheme TDMC is verified by a Monte–Carlo simulation as shown in Fig. 11. In this simulation, V_{OUT} of the proposed ETSM with the TDMC is compared to that of the ETSM with four normal comparators when the input dc signal is applied, while the DCC identically operates for both cases. As shown in this figure, the variation of V_{OUT} ripple can be much decreased due to the TDMC. Through these Monte–Carlo simulations, we can also verify the reliability of the proposed ETSM. To evaluate the linearity of the proposed ETSM, spurious free dynamic range (SFDR) is measured as shown in Fig. 12. Since the proposed ETSM achieves

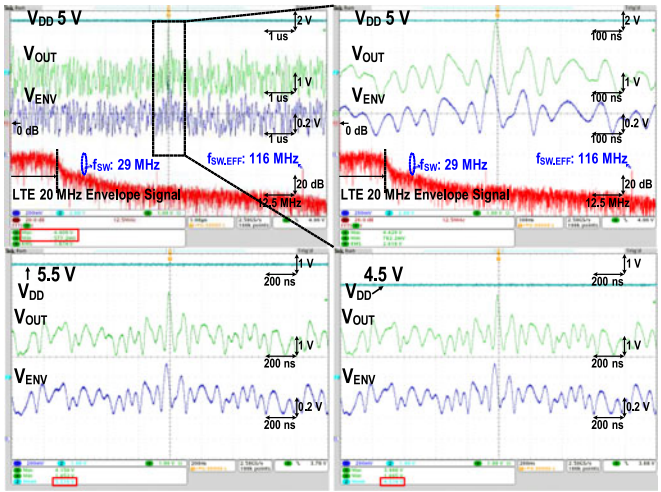

Fig. 9. Measurement output waveform of the proposed ETSM for LTE20 envelope signal under variation of supply voltage.

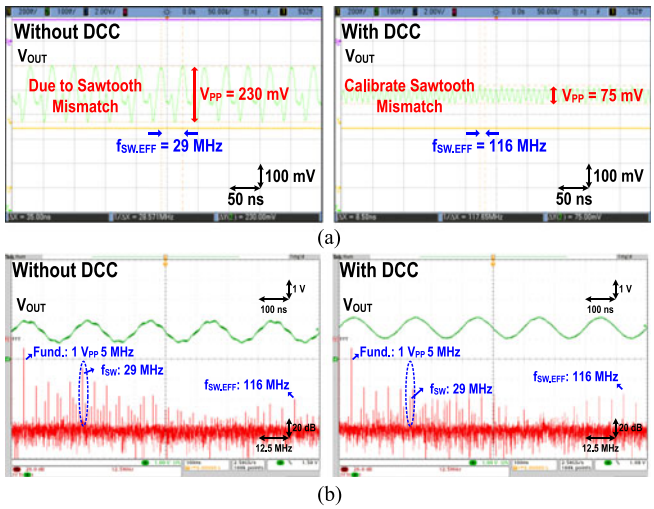

Fig. 10. Measurement for verifying the DCC operation. (a) DC input. (b) Sinusoidal input.

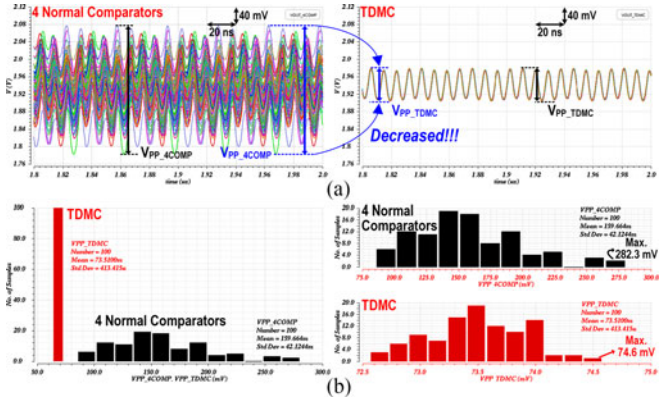

Fig. 11. Monte–Carlo simulation results of four normal comparators and TDMC. (a) Transient results. (b) Histograms of $V_{\mathrm{PP\_4COMP}}$ and $V_{\mathrm{PP\_TDMC}}$.

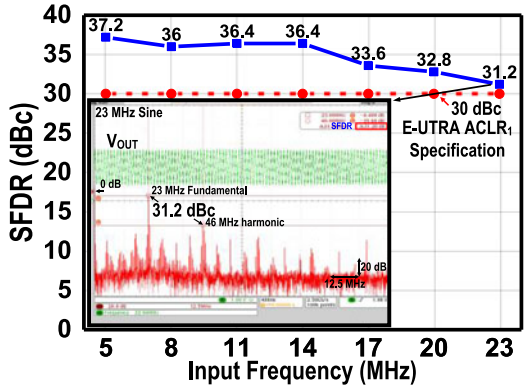

Fig. 12. SFDR plot according to sinusoidal input frequency.

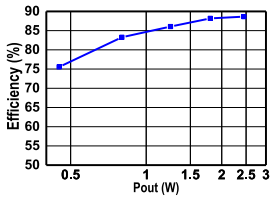

Fig. 13. Measured efficiency.

SFDR of 32.8 dBc at 20 MHz, which is higher than the RF PA output E-UTRA ACLR_1 specification for LTE, 30 dBc [18], it can be considered that the linearity of this work is good enough. To guarantee that the proposed ETSM tracks the LTE20 envelope signal without any distortion, we designed a closed loop bandwidth as around 23 MHz. Since the proposed ETSM can properly operate using only SCs without any mismatch issue, the efficiency is above 75% across an average output power range of 0.45 to 2.45 W and the peak efficiency is 88.6% at an average output power of 2.45 W, as shown in Fig. 13.

IV. Conclusion

This letter presented the 2P3L ETSM for an LTE20-MHz envelope signal. By adopting a 2P3L architecture and removing the low-efficiency LA, the efficiency was significantly improved. In addition, the proposed TDMC and DCC removed the duty-cycle mismatch, which is a critical problem in any converter topologies that adopt the multiphase or multilevel structure. As a result, the proposed ETSM can track fast LTE20 envelope signals and achieve low ripple and high efficiency. Measurement and simulation results verified the validity of the proposed ETSM.

References

[1] T. Jiang and Y. Wu, "An overview: Peak-to-average power ratio reduction techniques for OFDM signals," *IEEE Trans. Broadcast.*, vol. 54, no. 2, pp. 257–268, Jun. 2008.

[2] S. C. Cripps, *RF Power Amplifiers for Wireless Communications*, 2nd ed. Norwood, MA, USA: Artech House, 2006, pp. 285–336.

[3] T. W. Kwak, M. C. Lee, and G. H. Cho, "A 2 W CMOS hybrid switching amplitude modulator for EDGE polar transmitters," *IEEE J. Solid-State Circuits*, vol. 42, no. 12, pp. 2666–2676, Dec. 2007.

[4] P. Y. Wu and P. Mok, "A two-phase switching hybrid supply modulator for RF power amplifiers with 9% efficiency improvement," *IEEE J. Solid-State Circuits*, vol. 45, no. 12. pp. 2543–2556, Dec. 2010.

[5] M. Hassan, L. E. Larson, V. W. Leung, and P. M. Asbeck, "A combined series-parallel hybrid envelope amplifier for envelope tracking mobile terminal RF power amplifier applications," *IEEE J. Solid-State Circuits*, vol. 47, no. 5, pp. 1185–1198, May 2012.

[6] X. Huan, Q. Jin, X. Ruan, and X. Xiong, "Full feedforward of the output voltage to improve efficiency for envelope-tracking power supply using switch-linear hybrid configuration," *IEEE Trans. Power Electron.*, vol. 28, no. 1, pp. 451–456, Jan. 2013.

[7] M. Hassan, P. M. Asbeck, and L. E. Larson, "A CMOS dual-switching power-supply modulator with 8% efficiency improvement for 20 MHz LTE envelope tracking RF power amplifiers," in *Proc. Int. Conf. IEEE Solid-State Circuits*, Feb. 2013, pp. 366–367.

[8] M. Vasi´c, O. Garc´ıa, J. A. Oliver, P. Alou, and J. A. Cobos, "Theoretical efficiency limits of a serial and parallel linear-assisted switching converter as an envelope amplifier," *IEEE Trans. Power Electron.*, vol. 29, no. 2, pp. 719–728, Feb. 2014.

[9] P. Amo, M. Thomas, V. Molata, and T. Jerabek, "Envelope modulator for multimode transmitters with AC-coupled multilevel regulators," in *Proc. Int. Conf. IEEE Solid-State Circuits*, Feb. 2014, pp. 296–297.

[10] J. Sankman, M. K. Song, and D. Ma, "Switching-converter-only multiphase envelope modulator with slew rate enhancer for LTE power amplifier applications," *IEEE Trans. Power Electron.*, vol. 31, no. 1, pp. 817–826, Jan. 2016.

[11] S. Sung *et al.*, "Envelope modulator for 1.5-W 10-MHz LTE PA without AC coupling capacitor achieving 86.5% peak efficiency," *IEEE Trans. Power Electron.*, vol. 31, no. 12, pp. 8282–8292, Dec. 2016.

[12] V. Yousefzadeh, E. Alarcon, and D. Maksimovic, "Three-level buck converter for envelope tracking application," *IEEE Trans. Power Electron.*, vol. 21, no. 2, pp. 549–552, Mar. 2006.

[13] A. Peterchev, J. Xiao, and S. Sanders, "Architecture and IC implementation of a digital VRM controller," *IEEE Trans. Power Electron.*, vol. 18, no. 1, pp. 356–364, Jan. 2003.

[14] Y. S. Roh, Y. J. Moon, J. Park, M. G. Jeong, and C. Yoo, "A multiphase synchronous buck converter with a fully integrated current balancing scheme," *IEEE Trans. Power Electron.*, vol. 30, no. 9, pp. 5159–5169, Sep. 2015.

[15] S. J. Kim, R. K. Nandwana, Q. Khan, R. C. N. Pilawa-Podgurski, and P. K. Hanumolu, "A 4-phase 30–70 MHz switching frequency buck converter using a time-based compensator," *IEEE J. Solid-State Circuits*, vol. 50, no. 12, pp. 2814–2824, Dec. 2015.

[16] S.-C. Lee *et al.*, "A hybrid supply modulator with 10dB ET operation dynamic range achieving a PAE of 42.6% at 27.0dBm PA output power," in *Proc. Int. Conf. IEEE Solid-State Circuits*, Feb. 2015, pp. 42–43.

[17] S. H. Yang *et al.*, "A single-inductor dual-output converter with linear amplifier-driven cross regulation for prioritized energy-distribution control of envelope-tracking supply modulator," in *Proc. Int. Conf. IEEE Solid-State Circuits*, Feb. 2017, pp. 36–37.

[18] "3GPP," *3rd Generation Partnership Project; Technical Specification Group Radio Access Network; Evolved Universal Terrestrial Radio Access (E-UTRA); User Equipment (UE) Radio Transmission and Reception (Release 14)*, 2017, p. 242. [Online]. Available: http://www.etsi.org/deliver/etsi_ts/136100_136199/136101/14.04.00_60/ts_136101v140400p.pdf