

Switching Frequency Determination of DC–DC Converters With Hysteretic Control

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Abstract—Hysteretic control provides unique advantages in dc–dc converter applications but it is less popular than other types of control because the switching frequency depends on the operating point, the feedback ripple, and the component parasitics. Furthermore, it is difficult to predict the frequency due to the complex interaction of those factors. This paper proposes harmonic balance analysis to systematically determine the switching frequency of the buck and boost-like converters with hysteretic current control, and extends the method to buck converters with hysteretic voltage control. The analysis includes the most important second-order effects (feedback ripple, component parasitics, a second output capacitor, and switching delays). For the less complex cases the switching frequency is expressed in closed form, and for the more complex cases the paper proposes a graphical solution. The predictions are verified by simulations and, for the buck converter with hysteretic current control, by experiments. The derived results are useful for designing a converter with predictable switching frequency, and can also be employed during the design process of a converter with synchronized or stabilized frequency. Given an arbitrary control scheme or circuit variation, the switching frequency can be readily obtained by following the proposed approach.

Index Terms—Circuit parameter effect, hysteretic current control, hysteretic voltage control, switching frequency.

I. INTRODUCTION

HYSTERETIC control is one of the earliest self-oscillating control techniques for dc–dc converters. There are two main types of hysteretic control, hysteretic current control and hysteretic voltage control. Hysteretic current control was invented in the early 1960s [1] and a patent was issued to its inventor in 1984 [2]. It was reinvented in 1977 [3] and since then several papers were published about its behavior and analysis [4]–[11]. It has been established that hysteretic current control has some very interesting and practically important properties, including unconditional stability of the current loop (i.e., there is no need to add a stabilizing ramp to the current signal), a virtually constant magnitude and a negligible phase shift of the control-to-inductor current transfer function, accurate tracking of the control voltage by the average inductor current in continuous conduction mode (CCM), and a switching frequency that

is proportional to the load current in discontinuous conduction mode. That property is useful in applications where high efficiency must be maintained over a wide range of load currents. A disadvantage of hysteretic current control is that the switching frequency depends on the input and output voltages. It is possible to eliminate that dependence by stabilizing the frequency or synchronizing the converter to an external clock [12]–[16], but those measures require additional circuitry and might lead to performance compromises.

Besides the input/output voltages the switching frequency is also influenced by the ripple voltage at the output of the error amplifier and by component parasitics. The effect of the ripple voltage on the frequency was analyzed in [5] and [6], but the analysis covered only the special case of the type-II compensator with a pole frequency well above the switching frequency and a zero frequency well below the switching frequency, i.e., when the compensator gain could be approximated with a constant at the switching frequency and at its first few harmonics. The switching frequency is a critical parameter of any dc–dc converter; therefore, its accurate prediction in self-oscillating converters (e.g., the ones with hysteretic current-mode control) has a great practical value. Even if the frequency of the converter is stabilized or the converter is synchronized to an external clock, the knowledge of the self-oscillating frequency is important for the design of the stabilizing or synchronizing circuit.

Hysteretic voltage control is also known since the early 1960s [17]. It is often used for low-cost buck converters, either in its original form or combined with an error amplifier [18]. Similarly to hysteretic current control, the switching frequency strongly depends on the operating conditions, component parasitics, and, when an error amplifier is used, the feedback ripple.

This paper presents a *systematic* method to determine the switching frequency of the buck converter and various boost-like converters (BLC, e.g., boost, buck–boost, SEPIC) with hysteretic current/voltage control and with an *arbitrary* compensator. The analysis includes the effects of the equivalent series inductance (ESL) of the output capacitor, a second output capacitor with a time constant different from the first capacitor, the turn-off and turn-on delays, and the internal frequency dependence of the gain of the error amplifier.

Harmonic balance analysis (HBA) is a useful tool to investigate the steady-state operation of the converter and to determine its stability [19]. The methods used in [5], [6], and [20] attempt predicting the switching frequency by direct inspection of the signal *waveforms*. Such an approach cannot be easily extended to a converter with *parasitics* and *arbitrary compensation*. On

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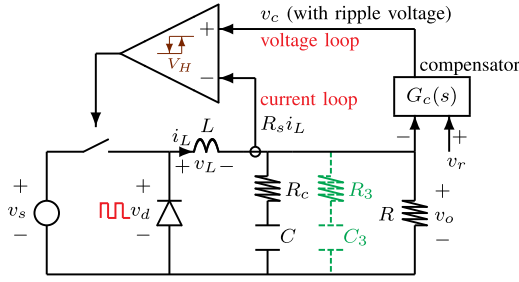


Fig. 1. A hysteretic current mode buck converter with optional C_3 and R_3 .

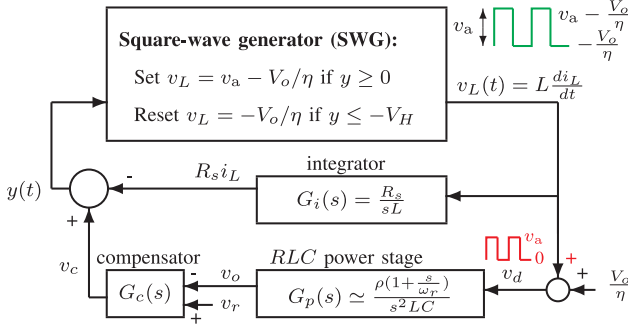


Fig. 2. Model of the buck converter with hysteretic current control.

the other hand, HBA can be easily adapted to any converter and compensator combination. In HBA, analyzing parasitic effects is straightforward.

In Section II, HBA is applied to a buck converter with hysteretic *current* control. In Section III, HBA is extended to buck converters with various second-order effects, to BLC, and to buck converters with hysteretic *voltage* control. That section also includes experimental and simulation results that verify the predictions. Section IV presents the summary.

II. BUCK CONVERTER WITH HYSTERETIC CURRENT CONTROL

Consider a buck converter with hysteretic current control (see Fig. 1) in CCM, which can be represented by a model [21] shown in Fig. 2, where v_s is the source voltage, v_d is the diode voltage, v_o is the output voltage, v_r is the reference voltage, v_c is the control voltage, v_L is the inductor voltage with an amplitude v_a , i_L is the inductor current, R_s is the sensing resistance, $y = v_c - R_s i_L$ is the feedback signal, and $G_c(s)$ is the transfer function of the voltage-loop compensator. Let the equivalent series resistance (ESR) of the output capacitor be R_c . Let $\rho = R/(R + R_c) \approx 1$. Let the ESR zero be $\omega_r = 1/R_c C$. Let the switching period be T and the duty ratio be D . Let $f_s = 1/T$, $\omega_s = 2\pi f_s$, $d = DT$, and the efficiency be η . Let the hysteresis band be V_H . The control switch of the converter is turned ON when $R_s i_L \leq v_c$ and turned OFF when $R_s i_L \geq v_c + V_H$.

Throughout the paper, all signals are assumed in steady state. As in [22], represent v_L by Fourier series,

$$v_L(t) = v_a \sum_{n=-\infty}^{\infty} c_n e^{jn\omega_s t} \quad \text{where } c_n = \frac{1 - e^{-jn\omega_s d}}{j2n\pi}. \quad (1)$$

TABLE I
D-TRANSFORMS OF TYPICAL TRANSFER FUNCTIONS

$T(s)$	$\mathcal{D}[T(s)]$	(note: $p = \omega_p/\omega_s$, $z = \omega_z/\omega_s$)
$\frac{\omega_s}{s + \omega_p}$	$\alpha(D, p) = 2 \sinh(\pi p D) \sinh(\pi p (1 - D)) \operatorname{csch}(\pi p) / p$	
$\frac{\omega_s}{s}$	$\alpha_0(D) = \alpha(D, 0) = 2\pi D(1 - D)$	
$\frac{\omega_s^2}{s^2}$	$\alpha_1(D) = 0$	
$\frac{\omega_s^3}{s^3}$	$\alpha_2(D) = -2\pi^3 D^2(1 - D)^2/3$	
$\frac{\omega_s(1 + s/\omega_z)}{s(1 + s/\omega_p)}$	$\alpha_0(D) + (\frac{p}{z} - 1)\alpha(D, p)$	
$\frac{\omega_s^2(1 + s/\omega_z)}{s^2(1 + s/\omega_p)}$	$\alpha_1(D) + (\frac{1}{p} - \frac{1}{z})(\alpha(D, p) - \alpha_0(D))$	

In the s -domain, let $T(s) := -v_a y(s)/v_L(s)$, which has two parts contributed by the current and voltage loops respectively, i.e., $T(s) = T_i(s) + T_v(s) = v_a(G_i(s) + G_c(s)G_p(s))$. Then

$$y(t) = - \sum_{n=-\infty}^{\infty} c_n e^{jn\omega_s t} T(jn\omega_s) \quad (2)$$

$$y(0) = \sum_{n=-\infty}^{\infty} \left(\frac{e^{-jn\omega_s d} - 1}{j2n\pi} \right) T(jn\omega_s) = 0 \quad (3)$$

$$y(d) = \sum_{n=-\infty}^{\infty} \left(\frac{1 - e^{jn\omega_s d}}{j2n\pi} \right) T(jn\omega_s) = -V_H \quad (4)$$

with dc offsets having no effect on the switching frequency. Define an expression of signal *difference* $\mathcal{V} = y(0) - y(d)$ with a unit of *voltage*, and a D-transform \mathcal{D} as

$$\mathcal{V} := \mathcal{D}[T(s)] := \sum_{n=-\infty}^{\infty} \left(\frac{\cos(n\omega_s d) - 1}{jn\pi} \right) T(jn\omega_s). \quad (5)$$

When \mathcal{V} is plotted as a function of a variable, such a plot is called a V-plot. In (5), $T(s)$ is evaluated at $s = jn\omega_s$ where ω_s is large compared with other component frequencies such as $1/RC$. For the D-transform purpose, a transfer function $1/(s + \omega)$, for example, can be approximated as $1/s$ because $\mathcal{D}[1/(s + \omega)] \approx \mathcal{D}[1/s]$ if $\omega_s \gg \omega$. Such approximation, denoted by \simeq in this paper, greatly simplifies the derivation of $\mathcal{D}[T(s)]$ for a complex expression of $T(s)$.

Subtracting (4) from (3) and using (5) lead to an equation to obtain f_s ,

$$\mathcal{V} := \mathcal{D}[T(s)] = y(0) - y(d) = V_H \quad (6)$$

where the dc offsets of (3) and (4) cancel each other. Let $\mathcal{V} = \mathcal{V}_i + \mathcal{V}_v$, where $\mathcal{V}_i = \mathcal{D}[T_i(s)]$ and $\mathcal{V}_v = \mathcal{D}[T_v(s)]$ are for the current and voltage loops, respectively. Note that the D-transform has a linear property such that $\mathcal{D}[aT_i(s) + bT_v(s)] = a\mathcal{D}[T_i(s)] + b\mathcal{D}[T_v(s)]$. Table I shows the D-transforms of some typical transfer functions [19], and $\mathcal{D}[e^{-s\epsilon}] = 1$ for $\epsilon \leq d \leq T - \epsilon$, which leads to $\mathcal{D}[1] = 1$.

Express $\alpha(D, p)$ in Table I as a Taylor series $\sum_{n=0}^{\infty} \alpha_n(D)(-p)^n$ and $\alpha(D, 0) = \alpha_0(D)$. Based on the plot of $\alpha(D, p)$ shown in Fig. 3, $\alpha_0(D) \geq \alpha(D, p) \geq 0$ and $\alpha(D, \infty) = 0$. For $p > 3$, $\alpha(D, p) \approx 1/p$. From [19], $\alpha_n(D) = \mathcal{D}[\omega_s^{n+1}/s^{n+1}]$. Using partial fraction decomposition, an arbitrary $T(s)$ can be generally decomposed as a summation of

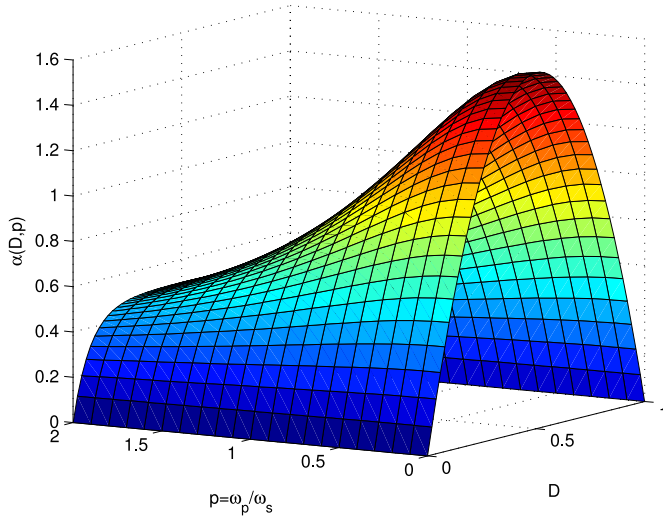
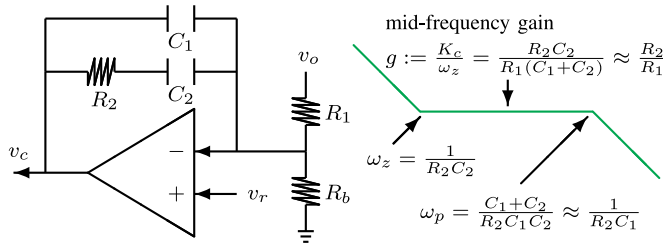
Fig. 3. Plot of $\alpha(D, p)$, for D-transform.

Fig. 4. Type-II compensator and its transfer function.

$1/(s + \omega_p)$ and $1/s^n$ (for $n \geq 1$), and $\mathcal{D}[T(s)]$ can be easily obtained from Table I. If the voltage loop is open (and $\mathcal{V}_v = 0$), from (5)

$$\begin{aligned} \mathcal{V} &= \mathcal{V}_i = \mathcal{D}[T_i(s)] = \mathcal{D}\left[\frac{v_a R_s}{sL}\right] \\ &= \sum_{n=1}^{\infty} \frac{v_a R_s (\cos(2\pi D) - 1)}{n^2 \pi^2 f_s L} = \frac{v_a R_s D(1-D)}{f_s L} = V_H \\ f_s &= \frac{v_a R_s D(1-D)}{LV_H} := f_0 \end{aligned} \quad (7)$$

agreed with [6, Table 1]. As V_H increases, f_s decreases. Now close the voltage loop. Since $\mathcal{V}_i + \mathcal{V}_v = V_H$, $f_s < f_0$ if $\mathcal{V}_v < 0$, but $f_s > f_0$ if $\mathcal{V}_v > 0$.

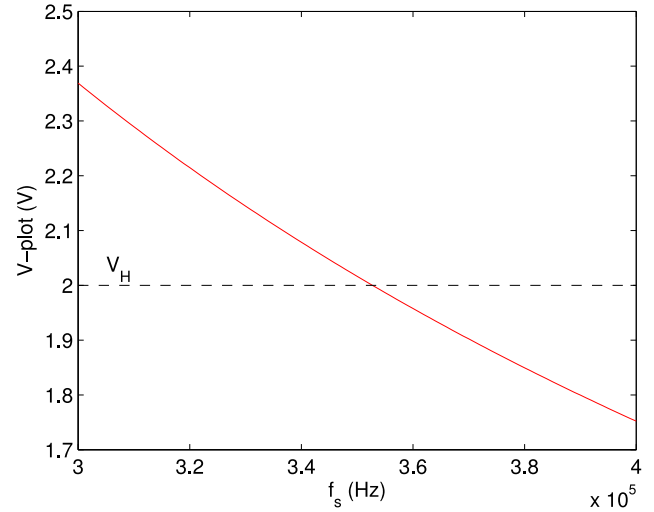
In Fig. 2, if a type-II compensator as in Fig. 4 (with ideal amplifier) is used

$$G_c(s) = \frac{K_c(1 + s/\omega_z)}{s(1 + s/\omega_p)}. \quad (8)$$

Let $g = K_c/\omega_z$. The PI compensator is a special case of the type-II compensator. Setting $\omega_p \rightarrow \infty$ in (8) leads to a PI compensator $G_c(s) = g + K_c/s$.

Generally, $\omega_z \ll \omega_s$, $G_c(s) \simeq g/(1 + s/\omega_p)$, and

$$T(s) = T_i(s) + T_v(s) \simeq \frac{v_a R_s}{sL} + \frac{v_a g(1 + s/\omega_r)}{LCs^2(1 + s/\omega_p)}. \quad (9)$$

Fig. 5. V-plot shows $f_s = 352$ kHz.

Then, from (6) and Table I

$$\begin{aligned} \mathcal{V} &= \frac{v_a R_s \alpha_0(D)}{\omega_s L} + \frac{v_a g}{LC\omega_s^2} \left(\alpha_1(D) \right. \\ &\quad \left. + \left(\frac{1}{p} - \frac{1}{r} \right) (\alpha(D, p) - \alpha_0(D)) \right) = V_H. \end{aligned} \quad (10)$$

Since $\alpha(D, p) \leq \alpha_0(D)$, $\mathcal{V}_v \geq 0$ and $f_s > f_0$ if $p > r$, but $f_s < f_0$ if $p < r$. If $p = r$, $f_s = f_0$. Introducing a pole generally decreases f_s , because decreasing p leads to decrease of \mathcal{V} , and introducing a zero increases f_s .

For $p > 3$, $\alpha(D, p) \approx 1/p$, then (10) leads to

$$f_s = \frac{\left(R_s C + g \left(\frac{1}{\omega_r} - \frac{1}{\omega_p} \right) \right) D(1-D)}{\frac{V_H LC}{v_a} + \frac{g}{\omega_p} \left(\frac{1}{\omega_r} - \frac{1}{\omega_p} \right)}. \quad (11)$$

If a PI compensator is used, setting $\omega_p \rightarrow \infty$ in (11) leads to

$$f_s = \frac{(R_s + gR_c)(1-D)Dv_a}{LV_H} = \left(1 + \frac{gR_c}{R_s} \right) f_0 > f_0 \quad (12)$$

also agreed with [6, Table 1]. Note that (10) depends on C , while (7) and (12) are independent of C .

III. CIRCUIT VARIATIONS TO SHOW PARAMETER EFFECT

A. ESL: $f_s \uparrow$

When the ESL L_c of the output capacitor is significant

$$\begin{aligned} G_p(s) &\simeq \frac{L_c C s^2 + R_c C s + 1}{LL_c C s^3 / R + LCs^2 / \rho + (L/R + R_c C)s} \\ &\simeq \frac{L_c C s^2 + R_c C s + 1}{LCs^2(1 + sL_c/R)} \simeq \frac{L_c C s^2 + R_c C s + 1}{LCs^2}. \end{aligned}$$

TABLE II
NEW EXPRESSIONS OF $\alpha(D, p)$, $\alpha_0(D)$ AND $\alpha_1(D)$ FOR THE CONVERTER WITH SWITCHING DELAY

	for $D < \delta$	for $\delta \leq D \leq 1 - \delta$	for $1 - \delta < D$
$\alpha'(D, p) := \mathcal{D}\left[\frac{e^{-s\epsilon}\omega_s}{s+\omega_p}\right]$	$-2\pi D^2 e^{-2\pi p\delta}$	$e^{2\pi p\delta}(\alpha(D, p) - \frac{1}{p}) + \frac{1}{p}$	$-2\pi(1-D)^2 e^{-2\pi p\delta}$
$\alpha'_0(D) := \mathcal{D}\left[\frac{e^{-s\epsilon}\omega_s}{s}\right]$	$-2\pi D^2$	$\alpha_0(D) - 2\pi\delta$	$-2\pi(1-D)^2$
$\alpha'_1(D) := \mathcal{D}\left[\frac{e^{-s\epsilon}\omega_s^2}{s^2}\right]$	$2\pi^2 D^2(2\delta - 1)$	$2\pi^2 \delta^2 - 2\pi\delta\alpha_0(D)$	$2\pi^2(1-D)^2(2\delta - 1)$

If the type-II compensator (8) is used with $G_p(s)$

$$\begin{aligned} \frac{\mathcal{T}(s)}{v_a} &= \frac{\mathcal{T}_i(s) + \mathcal{T}_v(s)}{v_a} \simeq \frac{R_s}{sL} + \frac{g(L_c C s^2 + R_c C s + 1)}{LC s^2(1 + s/\omega_p)} \\ &= \frac{R_s}{sL} + \frac{g}{LC} \left(\frac{1}{s^2} + \frac{R_c C - \frac{1}{\omega_p}}{s} + \frac{L_c C - \frac{R_c C}{\omega_p} + \frac{1}{\omega_p^2}}{1 + \frac{s}{\omega_p}} \right). \end{aligned}$$

Then, from (6) and Table I

$$\begin{aligned} \frac{\mathcal{V}LC}{v_a} &= \left(R_s C + g \left(R_c C - \frac{1}{\omega_p} \right) \right) \frac{\alpha_0(D)}{\omega_s} + \frac{g\alpha_1(D)}{\omega_s^2} \\ &+ g \left(L_c C - \frac{R_c C}{\omega_p} + \frac{1}{\omega_p^2} \right) p\alpha(D, p) = \frac{V_H LC}{v_a}. \end{aligned} \quad (13)$$

For $p > 3$, $p\alpha(D, p) \approx 1$, and (13) leads to

$$f_s = \frac{\left(R_s C + g \left(R_c C - \frac{1}{\omega_p} \right) \right) D(1-D)}{\frac{V_H LC}{v_a} - g \left(L_c C - \frac{R_c C}{\omega_p} + \frac{1}{\omega_p^2} \right)}. \quad (14)$$

As L_c increases, f_s increases. For $\omega_p \rightarrow \infty$, similar to [20, eq. (4)] for the hysteretic voltage control

$$f_s = \frac{(R_s + gR_c)D(1-D)}{\frac{V_H L}{v_a} - gL_c} \quad (15)$$

and $L_c < V_H L/v_a g$ is required.

B. Switching Delay: $f_s \downarrow$

If there exist a turn-on delay $\epsilon := \delta T$ and a turn-off delay ϵ_2 , then (6) becomes

$$\mathcal{V} := y(-\epsilon) - y(d - \epsilon_2) = V_H \quad (16)$$

where $y(-\epsilon)$ and $y(d - \epsilon_2)$ can be determined from (2), and f_s can be determined from (16).

Example 1: Consider a buck converter with a PI compensator: $v_s = 20$ V, $v_r = 5$ V, $\epsilon = 100$ ns, $\epsilon_2 = 0$, $L = 10$ μ H, $C = 100$ μ F, $R_c = 0.02$ Ω , $R_s = 1$ Ω , $R = 1$ Ω , $R_1 = 1$ k Ω , $C_2 = 10$ nF, $R_2 = 50$ k Ω , and $V_H = 2$ V.

The simulation shows $f_s = 350$ kHz, closely agreed with the V-plot [see Fig. 5, based on (16) and (2)], which gives a graphical solution of $f_s = 352$ kHz. ■

For symmetrical switching delay with $\epsilon = \epsilon_2$ and $\delta < 1/2$, the analysis in the previous sections still applies [19], but with $\mathcal{T}(s)$ replaced by $\mathcal{T}'(s) = e^{-s\epsilon}\mathcal{T}(s)$, and $\alpha(D, p)$, $\alpha_0(D)$ and $\alpha_1(D)$ replaced respectively by $\alpha'(D, p)$, $\alpha'_0(D)$ and $\alpha'_1(D)$ shown in Table II.

TABLE III
THE MEASURED f_s AGREES WITH HBA PREDICTIONS

Exp.	C_1 (pF)	C_3 (μ F)	measured f_s (kHz)	predicted f_s (kHz)
1	0	0	40.1	39.4
2	10	0	34	34.2
3	100	0	27.1	27.6
4	0	10	34.6	34
5	10	10	30.3	30.3
6	100	10	26.4	26.8

Take the buck converter with $G_c(s) = g$ or $g + K_c/s$, for example. From (10) and Table II

$$f_s = \frac{((R_s + gR_c)C - g\epsilon)D(1-D)}{LCV_H/v_a + (R_s + gR_c)C\epsilon - g\epsilon^2/2}. \quad (17)$$

C. Composite Capacitor: Adding a Pole $\omega_r(1 + C/C_3)$, $f_s \downarrow$

As in Fig. 1, to further reduce the ripple voltage, one may add an optional second output capacitor C_3 , which is usually a ceramic or film capacitor with negligible ESR R_3 . Then, from [23]

$$G_p(s) \simeq \frac{1 + s/\omega_r}{LCs^2} \cdot \left(\frac{C}{C + C_3} \right) \frac{1 + sR_3C_3}{1 + s/\omega_q} \quad (18)$$

where a new pole $\omega_q = \omega_r(1 + C/C_3)R_c/(R_c + R_3) \approx \omega_r(1 + C/C_3) > \omega_r$ is introduced, which causes f_s to decrease. If $R_3C_3 \ll 1/\omega_s$ and a PI compensator is used, (11) still applies but with g replaced by $gC/(C + C_3)$ and ω_p replaced by ω_q .

D. Non-ideal Amplifier: Adding a Pole, $f_s \downarrow$

Let the nonideal amplifier be $a(s) = A/(1 + s/\omega)$ with a dc gain A , a pole ω , and unity gain bandwidth $A\omega$. Based on circuit analysis, the type-II compensator transfer function (8) is modified to

$$\begin{aligned} G'_c(s) &= \frac{a(s)G_c(s)}{1 + a(s) + (1 + R_1/R_b)G_c(s)} \\ &\simeq \frac{K_c(1 + s/\omega_z)}{s(1 + s/\omega'_p)(1 + s/(g'\omega_p + A\omega))} \end{aligned} \quad (19)$$

where $g' = g(1 + R_1/R_b)$, with two well-separated poles $\omega'_p = \omega_p/(1 + g'\omega_p/A\omega) \ll g'\omega_p + A\omega$. If the PI compensator is used, $\omega_p \rightarrow \infty$ and $\omega'_p \approx A\omega/g'$ and the other pole is at infinity. The larger pole is generally much greater than ω_s and has negligible effect on the switching frequency. All the analysis above applies but with ω_p replaced by ω'_p .

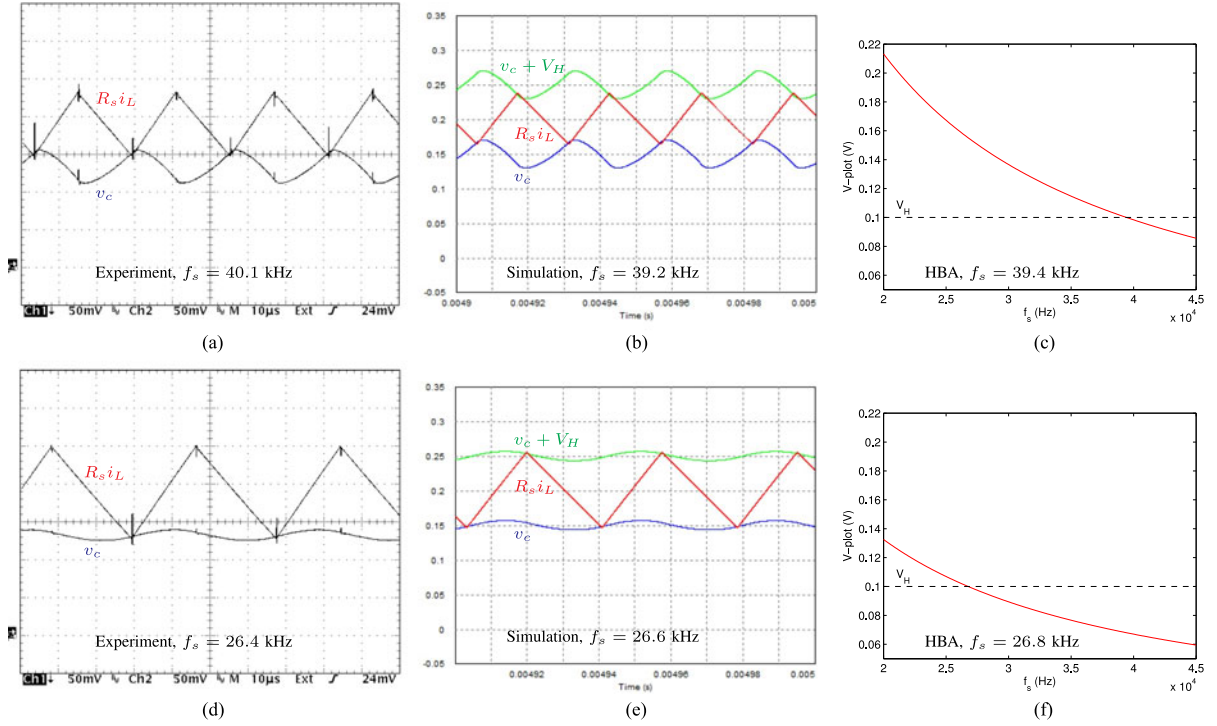


Fig. 6. The measured waveforms and f_s agree with simulations and HBA; (a)–(c) for Exp.1 and (d)–(f) for Exp.6.

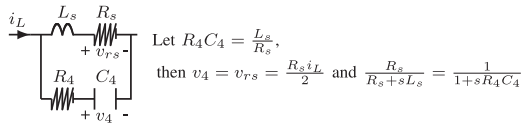


Fig. 7. Equivalent sensing circuit without changing f_s .

Example 2: (Experimental verification) Consider a buck converter with $v_s = 24$ V, $v_r = 2.5$ V, $\epsilon = \epsilon_2 = 250$ ns, $L = 200$ μ H, $C = 75$ μ F, $R_c = 0.185$ Ω , $R_s = 0.1$ Ω , $R = 5$ Ω , $R_1 = 8.2$ k Ω , $R_b = 2.7$ k Ω , $R_2 = 220$ k Ω , $C_2 = 1$ nF, and $V_H = 0.1$ V. The error amplifier has a dc gain 100 dB and unity gain bandwidth 10 MHz. There is an extra gain 0.01426 at the output of the error amplifier. Six experiments (Exp.1–6) are conducted and summarized in Table III. For Exp.4–6, a second output capacitor C_3 is added. As expected, adding C_1 or C_3 decreases f_s . Take Exp.1 and Exp.6 for example as shown in Fig. 6, the measured waveforms and f_s agree with simulations and HBA.

From (7), $f_0 = 29.24$ kHz, and f_s deviates from f_0 due to the voltage loop ripple. Here, $\omega_r = 72$ rad/s. Based on the previous discussion on (10), for $C_1 = 10$ pF, $\omega_r < \omega'_p = 257$ rad/s and $f_s > f_0$. For $C_1 = 100$ pF, $\omega_r > \omega'_p = 46$ rad/s and $f_s < f_0$. ■

E. Equivalent Current Sensing With Same f_s

The self-inductance L_s associated with R_s causes a step in the current-sense signal, which effectively reduces the hysteresis and therefore increases the frequency. To eliminate such effect, an equivalent sensing circuit [24] without changing the switching frequency is shown in Fig. 7, where v_4 is sensed for current feedback.

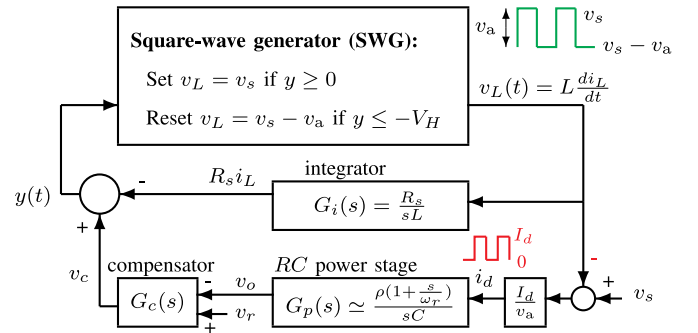


Fig. 8. Model of the BLC with hysteretic current control.

TABLE IV
 v_a FOR DIFFERENT CONVERTERS [22]

	Buck	Boost	Buck-boost	Flyback	SEPIC
v_a (v_L amplitude)	v_s	$\frac{V_o}{\eta}$	$v_s - \frac{V_o}{\eta}$	$v_s + \frac{V_o}{\eta N}$	$v_s + \frac{V_o}{\eta}$

F. BLC: Opposite Effect

For the BLC [22], the model is shown in Fig. 8 with v_a shown in Table IV for different converters [22], and (6) and (7) still apply. Here, $T_v(s) = -G_c(s)G_p(s)I_d$, where $I_d = V_o/R(1 - D)$ is the diode current [22]. The negative sign of $T_v(s)$ gives opposite effect, compared with the buck converter.

If the type-II compensator (8) is used

$$\frac{T(s)}{v_a} = \frac{T_i(s) + T_v(s)}{v_a} \approx \frac{R_s}{sL} - \frac{gI_d(1 + s/\omega_r)}{v_a C s(1 + s/\omega_p)}. \quad (20)$$

Then, from (6) and Table I

$$\begin{aligned} \mathcal{V} &= \frac{R_s v_a \alpha_0(D)}{\omega_s L} - \frac{g I_d}{C \omega_s} \left(\alpha_0(D) + \left(\frac{p}{r} - 1 \right) \alpha(D, p) \right) \\ &= V_H. \end{aligned} \quad (21)$$

Since $\alpha_0(D) \geq 0$ and $\alpha(D, p) \geq 0$, $\mathcal{V}_v \leq 0$ and $f_s \leq f_0$ if $p \geq r$. This is opposite to the buck converter case (where $f_s \geq f_0$ if $p \geq r$).

For $p < 0.2$, $\alpha(D, p) \approx \alpha_0(D) + \alpha_2(D)p^2$ and from (21)

$$f_s \approx \left(\frac{R_s(1-D)}{L} - \frac{R_c}{RR_1 C_1} \right) \frac{v_a D}{V_H}. \quad (22)$$

For $p > 3$, $\alpha(D, p) \approx 1/p$ and from (21)

$$f_s \approx \left(\frac{R_s v_a}{L} - \frac{g I_d}{C} + \frac{g v_a R_c}{2L} \right) \frac{D(1-D)}{V_H + g I_d R_c (1-r/p)}. \quad (23)$$

As a special case, if a PI compensator is used, then set $p \rightarrow \infty$ in (23) and the result agrees with [6, Table 1].

Example 3: Consider a boost converter with $v_s = 13.9$ V, $v_r = 5.94$ V, $\epsilon = \epsilon_2 = 0$, $L = 100$ μ H, $C = 75$ μ F, $R_c = 0.185$ Ω , $R_s = 0.1$ Ω , $R = 28.8$ Ω , $R_1 = 8.2$ k Ω , $R_b = 2.7$ k Ω , $R_2 = 100$ k Ω , $C_2 = 1$ nF, and $V_H = 0.1$ V. There is an extra gain 0.01426 at the output of the compensator and $g = 0.01426 K_c / \omega_z = 0.158$. For $C_1 = 0.01, 10,$ and 100 pF, the simulations show $f_s = 40.8, 40.65,$ and 48.9 kHz, respectively, closely agreed with (23), which show $f_s = 40.8, 41.9,$ and 52 kHz.

From (7), $f_0 = 58.43$ kHz. Opposite to the buck converter case, adding the voltage loop makes $f_s < f_0$. ■

G. Hysteretic Voltage Control: Special Case of Hysteretic Current Control by Setting $R_s = 0$

By setting $R_s = 0$ to cut off the current loop, all above derived expressions can be applied to the hysteretic voltage control. Consider a hysteretic V^2 controlled buck converter [18]. Let the compensator transfer function be $G_c(s) + g_2$, where $G_c(s)$ is the same as (8). Then

$$\frac{T(s)}{v_a} = (G_c(s) + g_2) G_p(s) \simeq \left(\frac{g}{1 + \frac{s}{\omega_p}} + g_2 \right) \frac{1 + \frac{s}{\omega_r}}{LC s^2}. \quad (24)$$

From (6) and Table I and for $p > 3$

$$f_s = \frac{\left(\frac{g+g_2}{\omega_r} - \frac{g}{\omega_p} \right) D(1-D)}{\frac{V_H LC}{v_a} - \frac{g}{\omega_p} \left(\frac{1}{\omega_p} - \frac{1}{\omega_r} \right)}. \quad (25)$$

Example 4: Consider a hysteretic V^2 controlled buck converter: $v_s = 5$ V, $v_r = 1.5$ V, $g_2 = 1$, $L = 2$ μ H, $C = 50$ μ F, $R_c = 0.01$ Ω , $R = 0.5$ Ω , $R_1 = 10$ k Ω , $C_1 = 100$ pF, $C_2 = 2$ nF, $R_2 = 5$ k Ω , and $V_H = 0.02$ V.

From (25), $f_s = 265$ kHz, closely agreed with the simulation, which shows $f_s = 262$ kHz. ■

TABLE V
PARAMETER EFFECTS ON f_s

Parameter	Effect	Buck	BLC
Additional $C_3 \uparrow$	Pole $\omega_q \approx \omega_r (1 + \frac{C}{C_3}) \downarrow$	$f_s \downarrow$	$f_s \uparrow$
Error amp. bandwidth $A\omega \downarrow$	Pole $\omega'_p \approx \frac{\omega_p}{1 + \frac{g/\omega_p}{A\omega}} \downarrow$	$f_s \downarrow$	$f_s \uparrow$
ESR $R_c \uparrow$	Zero $\omega_r = \frac{1}{R_c C} \downarrow$	$f_s \uparrow$	$f_s \downarrow$
ESL $L_c \uparrow$	Magnitude $ G_p(s)(j\omega) \uparrow$	$f_s \uparrow$	$f_s \downarrow$
Delay $\epsilon \uparrow$	Phase $\angle T(j\omega) \downarrow$	$f_s \downarrow$	$f_s \downarrow$

IV. SUMMARY

Hysteretic control provides unique advantages in dc–dc converter applications but it is less popular than other types of control because the switching frequency depends on the operating point, the feedback ripple and the component parasitics. Furthermore, it is difficult to predict the frequency due to the complex interaction of those factors.

This paper proposes HBA to *systematically* determine the switching frequency of the buck and boost-like converters with hysteretic current/voltage control. The analysis includes the most important second-order effects (feedback ripple, component parasitics, a second output capacitor, and switching delays). For the less complex cases, the switching frequency is expressed in closed form and for the more complex cases the paper proposes a graphical solution. The predictions are verified by simulations and, for the buck converter with hysteretic current control, by experiments. The derived results are useful for designing a converter with predictable switching frequency, and can also be employed during the design process of a converter with synchronized or stabilized frequency.

Table V summarizes the effects of the various parameters on f_s . For the buck converter, adding a pole generally decreases f_s , and adding a zero to the converter increases f_s . For BLC, the opposite is true. For both converters, adding delay decreases f_s . Given an *arbitrary* control scheme or circuit variation, the switching frequency can be readily obtained by following the approach proposed in this paper.

REFERENCES

- [1] T. A. Froeschle, "Two-state modulation techniques for power systems," Bose Corporation Semi-Annu. Rep. for US Army Electronics Command, Natick, MA, USA, Contract DA28-043-AMC-022812(E), Nov. 1968.
- [2] T. A. Froeschle, "Current-controlled two-state modulation," U.S. Patent 4 456 872, Jun. 26, 1984.
- [3] A. Weinberg and D. O'Sullivan, "LC³: Application to voltage regulation," in *ESTEC Spacecraft Power Conditioning Seminar*, 1977, pp. 165–173.
- [4] A. Capel, G. Ferrante, D. O'Sullivan, and A. Weinberg, "Application of the injected current model for the dynamic analysis of switching regulators with new concept of LC³ modulator," in *Proc. IEEE Power Electron. Spec. Conf.*, 1978, pp. 300–306.
- [5] R. Redl and I. Novak, "Current-mode control of switching voltage regulators—A new method of improving regulation parameters (in Hungarian)," *Hiradastechnika*, vol. 29, no. 11, pp. 321–334, 1978.
- [6] R. Redl and I. Novak, "Instabilities in current-mode controlled switching voltage regulators," in *Proc. IEEE Power Electron. Spec. Conf.*, 1981, pp. 17–28.

- [7] R. Redl and N. Sokal, "Current-mode control, five different types, used with the three basic classes of power converters: Small-signal AC and large-signal DC characterization, stability requirements, and implementation of practical circuits," in *Proc. IEEE Power Electron. Spec. Conf.*, 1985, pp. 771–785.
- [8] R. Redl, "Small-signal high-frequency analysis of the free-running current-mode-controlled converter," in *Proc. IEEE Power Electron. Spec. Conf.*, 1991, pp. 897–906.
- [9] Y.-F. Liu and P. C. Sen, "Large-signal modeling of hysteretic current-programmed converters," *IEEE Trans. Power Electron.*, vol. 11, no. 3, pp. 423–430, May 1996.
- [10] J. H. Park and B. H. Cho, "Small signal modeling of hysteretic current mode control using the PWM switch model," in *Proc. IEEE Workshop Comput. Power Electron.*, Jul. 2006, pp. 225–230.
- [11] C. J. Solis and G. A. Rincon-Mora, "Stability analysis & design of hysteretic current-mode switched-inductor buck DC-DC converters," in *Proc. IEEE Int. Conf. Electron., Circuits, Sys.*, 2013, pp. 811–814.
- [12] R. Redl and N. Sokal, "Frequency stabilization and synchronization of free-running current-mode-controlled converters," in *Proc. IEEE Power Electron. Spec. Conf.*, 1986, pp. 519–530.
- [13] T. Szepesi, "Stabilizing the frequency of hysteretic current-mode DC/DC converters," *IEEE Trans. Power Electron.*, vol. 2, no. 4, pp. 302–312, Oct. 1987.
- [14] Y. Wen and O. Trescases, "Analysis and comparison of frequency stabilization loops in self-oscillating current mode DC-DC converters," *IEEE Trans. Power Electron.*, vol. 28, no. 10, pp. 4753–4766, Oct. 2013.
- [15] Z. Sun, L. Siek, R. P. Singh, and M. Je, "A fixed-frequency hysteretic controlled buck DC-DC converter with improved load regulation," in *Proc. IEEE Int. Symp. Circuits Sys.*, 2014, pp. 954–957.
- [16] S. Kapat, "Parameter-insensitive mixed-signal hysteresis-band current control for point-of-load converters with fixed frequency and robust stability," *IEEE Trans. Power Electron.*, vol. 32, no. 7, pp. 5760–5770, Jul. 2017.
- [17] B. P. Schweitzer and A. B. Rosenstein, "Free running-switching mode power regulator: Analysis and design," *IEEE Trans. Aerosp.*, vol. 2, no. 4, pp. 1171–1180, Oct. 1964.
- [18] D. Goder and W. R. Pelletier, " V^2 architecture provides ultra-fast transient response in switch mode power supplies," in *Proc. HFPC Power Convers.*, Sep. 1996, pp. 19–23.
- [19] C.-C. Fang, "Critical conditions for a class of switched linear systems based on harmonic balance: applications to DC-DC converters," *Nonlinear Dyn.*, vol. 70, no. 3, pp. 1767–1789, Nov. 2012.
- [20] *Designing Fast Response Synchronous Buck Regulators Using the TPS5210*, Texas Instruments, TX, USA, 1999. [Online]. Available: www.ti.com/lit/pdf/slva044
- [21] C.-C. Fang and R. Redl, "Subharmonic instability limits for the peak-current-controlled buck converter with closed voltage feedback loop," *IEEE Trans. Power Electron.*, vol. 30, no. 2, pp. 1085–1092, Feb. 2015.
- [22] C.-C. Fang and R. Redl, "Subharmonic instability limits for the peak-current-controlled boost, buck-boost, flyback, and sepic converters with closed voltage feedback loop," *IEEE Trans. Power Electron.*, vol. 32, no. 5, pp. 4048–4055, May 2017.
- [23] C.-C. Fang and R. Redl, "Subharmonic stability limits for the buck converter with ripple-based constant on-time control and feedback filter," *IEEE Trans. Power Electron.*, vol. 29, no. 4, pp. 2135–2142, Apr. 2014.
- [24] *AN-1487 Current Mode Hysteretic Buck Regulators*, Texas Instruments, TX, USA, 2013. [Online]. Available: www.ti.com/lit/pdf/snva170b

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