Nonisolated Two-Phase Interleaved LED Driver With Capacitive Current Sharing

K. I. Hwu, *Member, IEEE*, and W. Z. Jiang, *Student Member, IEEE*

***Abstract*—In this paper, a nonisolated two-phase interleaved LED driver with capacitive current sharing is presented. In the proposed LED driver, the current sharing capacitor can be used to balance the input inductor currents and the LED currents. Furthermore, only one grounded LED string current is sensed and controlled. Moreover, under the interleaved control, the input current ripple can be reduced. Finally, the operating principles, analyses, and experimental results are provided to verify the effectiveness of the proposed LED driver.**

***Index Terms*—Current sharing, interleaved, light-emitting diode (LED) driver, two-phase.**

I. Introduction

AS COMPARED with the traditional lighting sources, such as incandescent light bulbs, fluorescent lamps, halogen lamps, etc., the high-brightness light-emitting diode (LED) have been getting more attention due to their high efficiency, compact size, low maintenance, and long life characteristics [1]–[4]. The brightness of the LED depends on the forward current. Thus, to control the brightness of the LED, it is preferable to use the constant current control. To meet the required brightness of the applications, multiple LEDs are usually connected in series and parallel. The current flowing through each LED string should be equal. However, each LED has different parameters such as forward voltage and resistance. The LED current in each string could be deviated. Therefore, LED current sharing is inevitable.

There are many literatures discussing the LED current sharing. The LED current sharing has two different methods. The first one is the active method [5]–[12], and the second one is the passive method [13]–[28]. The active method uses some control integrated circuits (ICs) and MOSFET switches, and this leads to complexity and high cost. Therefore, the passive method can be another solution since the control ICs are not necessary. This method uses the passive components such as transformers [13]–[19] or capacitors [20]–[28] to balance each LED current. For the transformer current sharing method, differential mode transformers with 1:1 turns ratio are used to balance LED currents. For the capacitor current sharing method, the current sharing is achieved based on the charge balance principle of capacitor. As compared with the transformer current sharing method, the capacitor current sharing method features a small size because the size of the current sharing transformer is usually larger than that of the current sharing capacitor. Moreover, the current sharing capacitor method can achieve precise LED current balance. In [20]–[26], the presented topologies include full-bridge and half-bridge structures, which are suitable for the high input voltage applications such as two-stage LED street lights. However, in some applications such as batteries, the input voltage is low. Consequently, an LED driver with high voltage gain is required. Moreover, a low input current ripple is preferable for battery applications. Thus, a nonisolated two-channel LED driver for low input voltage is presented as shown in Fig. 1(a) [27]. In Fig. 1(a), the capacitor C_1 is used to balance the two LED currents. Due to the combination of coupled inductor and C_1, the LED driver shown in Fig. 1(a) features a high voltage gain.

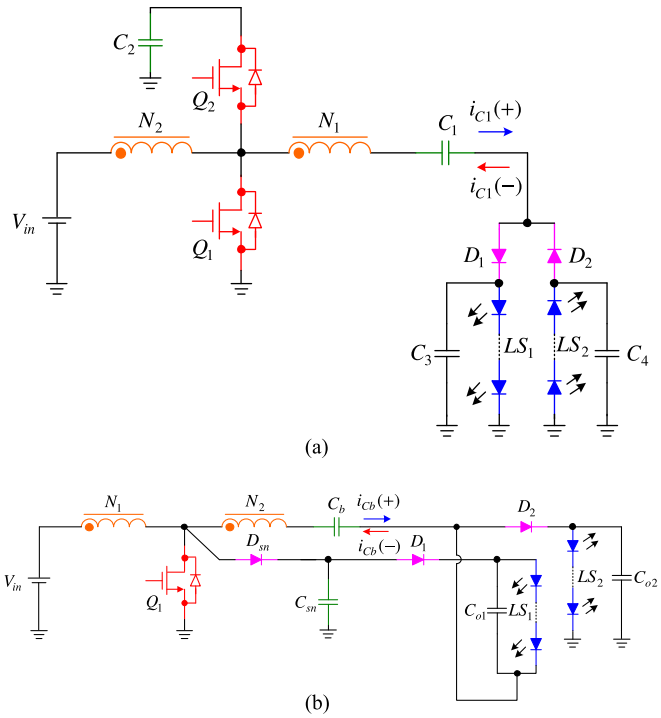

Fig. 1. Prior work: (a) Nonisolated two-channel LED driver with active clamp [27]. (b) Nonisolated single-switch two-channel LED driver with passive regenerative snubber [28].

Manuscript received October 19, 2016; revised January 7, 2017 and February 24, 2017; accepted April 7, 2017. Date of publication April 17, 2017; date of current version December 1, 2017. This work was supported by the Ministry of Science and Technology under Grant MOST 103-2221-E-027-040-MY3. Recommended for publication by Associate Editor M. Ponce-Silva. *(Corresponding author: K. I. Hwu.)*

The authors are with the Department of Electrical Engineering, National Taipei University of Technology, Taipei 10608, Taiwan (e-mail: eaglehwu@ntut.edu.tw; newjerusalem333@gmail.com).

Color versions of one or more of the figures in this paper are available online at http://ieeexplore.ieee.org.

Digital Object Identifier 10.1109/TPEL.2017.2695006

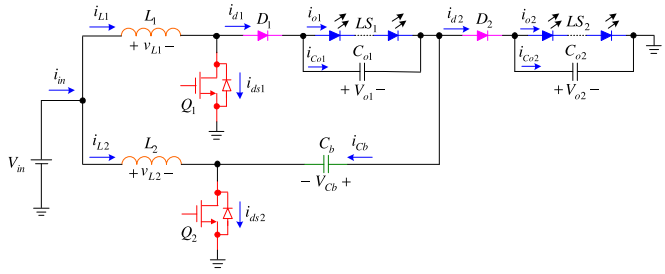

Fig. 2. Proposed two-phase interleaved two-channel LED driver.

Thus, it can be used in the low input voltage applications. Based on the topology shown in Fig. 1(a), the active clamp in Fig. 1(a) is replaced with a passive regenerative snubber as shown in Fig. 1(b) [28]. For the LED driver shown in Fig. 1(b), the leakage inductance energy is transferred to C_{sn}, and then the energy in C_{sn} can be transferred to the output LEDs. Thus, C_{sn} can be used to suppress the voltage spike as well as to improve the voltage gain. These two LED drivers are designed for a low input voltage of 3.3 V. In some applications, the battery voltage is high enough. Therefore, the use of the coupled inductor is not required. In addition, the input current ripple is expected to be as small as possible because the current ripple would have an impact on the life of batteries.

Based on the preceding discussion, a nonisolated two-phase interleaved LED driver with capacitive current sharing is presented as shown in Fig. 2. In the proposed LED driver, there are some merits. First, due to the capacitor C_b, not only the inductor currents but also the two LED string currents can be balanced. Second, under the interleaved control, the input current ripple ($i_{L1} + i_{L2}$) can be reduced. Third, as compared with the conventional boost converter, the voltage step-up gain is relatively high. Moreover, the source terminals of the MOSFET switches are connected to the ground. Thus, no isolated driver is required. Besides, due to the capacitive current sharing, only one grounded LED string current is sensed and controlled, and the isolated sensor is not required. The operating principles, analyses, and experimental results are given to demonstrate the effectiveness of the proposed LED driver.

II. Basic Analysis of the Proposed LED Driver

Fig. 2 shows the proposed two-phase interleaved two-channel LED driver, which contains two switches Q_1 and Q_2, two input inductors L_1 and L_2, one current sharing capacitor C_b, two output diodes D_1 and D_2, two output capacitors C_{o1} and C_{o2}, two LED strings LS_1 and LS_2. The input current is expressed by $i_{\rm in}$, and the currents flowing through L_1, L_2, Q_1, Q_2, C_b, D_1, D_2, LS_1, and LS_2 are signified by i_{L1}, i_{L2}, $i_{\rm ds1}$, $i_{\rm ds2}$, i_{Cb}, i_{d1}, i_{d2}, i_{o1}, and i_{o2}, respectively. The input voltage is represented by $V_{\rm in}$, and the voltages across L_1, L_2, C_b, C_{o1}, and C_{o2} are indicated by v_{L1}, v_{L2}, V_{Cb}, V_{o1}, and V_{o2}, respectively.

For analysis convenience, there are some assumptions to be made as follows:

1) the switches and components are ideal;
2) the proposed LED driver operates in the continuous conduction mode (CCM);
3) the values of the two input inductors L_1 and L_2 are identical;
4) the values of all the capacitors are large enough. Thus, the voltages are regarded as constant;
5) two gate driving signals for Q_1 and Q_2 are shifted by 180° with each other, and the corresponding duty cycles are greater than 0.5.

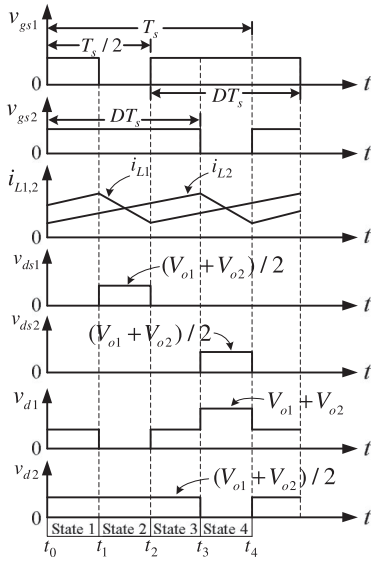

Fig. 3. Illustrated waveforms of the proposed LED driver.

The following analyses contain the 1) operating principles; 2) voltage gain; 3) boundary conditions of the input inductors; and 4) input current ripple.

A. Operating Principles

There are four operating states to be described below. Fig. 3 shows the illustrated waveforms over one switching period.

1) *State 1 [t_0, t_1]:* As shown in Fig. 4(a), the switches Q_1 and Q_2 are turned ON, and D_1 and D_2 are reverse-biased. Thus, the input voltage is imposed on L_1 and L_2, making i_{L1} and i_{L2} increase linearly. The LED strings LS_1 and LS_2 are supplied by C_{o1} and C_{o2}, respectively. This state ends when Q_1 is turned OFF at $t = t_1$.
2) *State 2 [t_1, t_2]:* As shown in Fig. 4(b), the switch Q_1 is turned OFF, and the switch Q_2 is turned ON. During this state, the energy stored in L_1 is released to LS_1 and C_b through D_1, but the input inductor L_2 is still magnetized. The diode D_2 is reverse-biased. This state ends when Q_1 is turned ON at $t = t_2$.
3) *State 3 [t_2, t_3]:* This state is the same as the state 1 as shown in Fig. 4(a). This state ends when Q_2 is turned OFF at $t = t_3$.
4) *State 4 [t_3, t_4]:* As shown in Fig. 4(c), the switch Q_1 is turned ON, and the switch Q_2 is turned OFF. During this state, the energy stored in L_2 and C_b is released to LS_2 through D_2, but the input inductor L_1 is still magnetized.

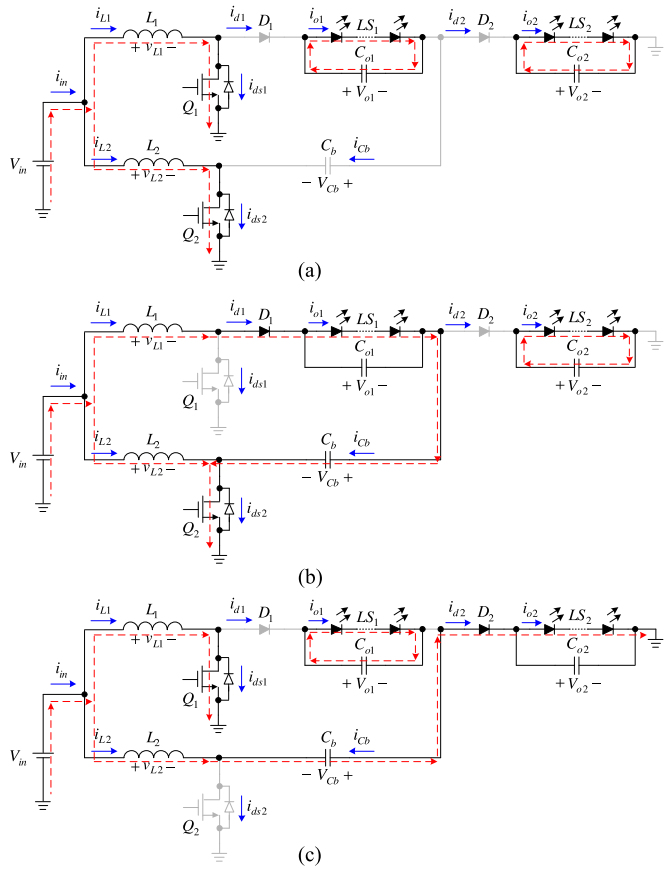

Fig. 4. Operating circuits over one switching period: (a) state 1 and 3; (b) state 2; (c) state 4.

The diode D_1 is reverse-biased. This state ends when Q_2 is turned ON at $t = t_4$.

B. Voltage Gain

The voltage gain and the voltage across C_b are analyzed in this section as follows:

$$V_{\text{in}}D + (V_{\text{in}} - V_{o1} - V_{Cb})(1-D) = 0 \tag{1}$$

$$V_{\text{in}}D + (V_{\text{in}} - V_{Cb} - V_{o2})(1-D) = 0. \tag{2}$$

By rearranging the above equations, the voltage across C_b, V_{Cb}, and the voltage gain can be obtained

$$V_{Cb} = \frac{1}{1-D} \cdot V_{\text{in}} - V_{o1} \tag{3}$$

$$\frac{V_{o1} + V_{o2}}{V_{\text{in}}} = \frac{2}{1-D} \tag{4}$$

where $0.5 < D < 1$.

C. Boundary Condition of Input Inductor

Assuming that the two input inductors are identical and the currents flowing through them are the same, the condition for the proposed LED driver operating in CCM or discontinuous conduction mode (DCM) is

$$\begin{cases} 2I_{L1} \geq \Delta i_{L1}, & \text{CCM} \\ 2I_{L1} < \Delta i_{L1}, & \text{DCM} \end{cases} \tag{5}$$

where I_{L1} and Δi_{L1} are the dc component and the peak-to-peak value of the ac component of i_{L1}, respectively.

The input current is equally shared in the input inductors. Thus

$$I_{L1} = I_{L2} = 0.5I_{\text{in}} \tag{6}$$

where I_{in} is the dc component of i_{in}. Assuming that there is no power loss, the input current I_{in} can be expressed as

$$I_{\text{in}} = \frac{2}{1-D} \times I_o. \tag{7}$$

The input current of each phase is

$$I_{L1} = I_{L2} = \frac{1}{1-D} \cdot I_o. \tag{8}$$

The current ripple of i_{L1}, Δi_{L1}, can be expressed as

$$\Delta i_{L1} = \frac{v_{L1}\Delta t}{L_1} = \frac{V_{\text{in}}DT_s}{L_1}. \tag{9}$$

As $2\Delta i_{L1} \geq \Delta i_{L1}$, i_{L1} will be in CCM. Hence, the required value of L_1 is as follows:

$$\begin{aligned} & 2\Delta i_{L1} \geq \Delta i_{L1} \\ \Rightarrow\ & 2 \cdot \left(\frac{1}{1-D} \cdot I_o \right) \geq \frac{V_{\text{in}}DT_s}{L_1} \\ \Rightarrow\ & L_1 \geq \frac{V_{\text{in}}D(1-D)T_s}{2I_o}. \end{aligned} \tag{10}$$

In the same way, the inequality of (10) holds for L_2.

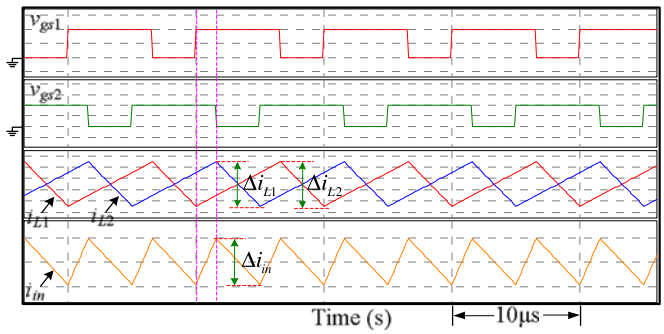

Fig. 5. Input current ripple i_{in}.

D. Input Current Ripple Without Input Filter

As shown in Fig. 5, the input current i_{in} is the sum of i_{L1} and i_{L2}. Due to the interleaved control, the input current ripple Δi_{in} is smaller than Δi_{L1} and Δi_{L2}, and can be expressed as follows:

$$\Delta i_{\text{in}} = \left(\frac{V_{\text{in}}}{L_1} + \frac{V_{\text{in}}}{L_2} \right)(D - 0.5)T_s. \tag{11}$$

TABLE I
SYSTEM SPECIFICATIONS OF THE PROPOSED LED DRIVER

System parameters	Specifications
Input voltage ($V_{\rm in}$)	12 V
Nominal LED channel voltage (V_{o1}, V_{o2})	3.45 V × 10 = 34.5 V
Nominal LED channel current (i_{o1}, i_{o2})	350 mA
Switching frequency (f_s)	100 kHz

TABLE II
COMPONENTS USED IN THE PROPOSED LED DRIVER

Components		Specifications
MOSFET switches (Q_1, Q_2)		STP120 NF10
Current sharing capacitor (C_b)		Two series 2200 μF/16 V electrolytic capacitors connected in parallel with another two series 2200 μF/16 V electrolytic capacitors, 0.1 μF/50 V ceramic capacitor × 1
Output capacitors (C_{o1}, C_{o2})		220 μF/50 V × 1, 0.1 μF/50 V ceramic capacitor × 1
Input inductors (L_1, L_2)		Core: PQ26/25-3C90 $L_1 = L_2 = 212\,\mu$H
Diodes (D_1, D_2)		V20120 C
Input filter	C_r	100 μF/25 V electrolytic capacitor × 1, 0.1 μF/50 V ceramic capacitor × 1
	L_r	T50-18 (A_L = 24 nH), 0.28 μH
Control loop	$R_{\rm sense}$	1 Ω/1 W
	OPA	LF356 N, 1 kΩ and 8.66 kΩ
	ADC	ADC7476
	FPGA	Altera EP1C3T100 C8N
	Gate drivers	TC4420

Since $L_1 = L_2$, (11) can be expressed as follows:

$$\Delta i_{\rm in} = \left(\frac{2V_{\rm in}}{L_1}\right)(D-0.5)T_s. \tag{12}$$

III. DESIGN CONSIDERATIONS

To verify the effectiveness of the proposed LED driver, a prototype is built up and tested. Table I shows the specifications of the proposed converter, whereas Table II shows the components used in the proposed converter. Moreover, the design procedures contain 1) LED strings; 2) duty cycle; 3) input inductors, 4) current sharing capacitor, 5) output capacitor; and 6) input filter.

A. LED Selection

The high-power LEDs used for the proposed LED driver are made by Everlight Electronics Ltd. The product name is EHP-AX08 EL/GT01 H-P01/5670/Y/K42. From the corresponding data sheet, it can be seen that if the constant current flowing through the LED is 350 mA, the corresponding forward voltage is about 3.45 V. In the proposed two-channel LED driver, ten LEDs are connected in series for each string. As shown in Fig. 6, an LED can be modeled as an approximately linear model with one ideal diode $D_{\rm ideal}$, one on-resistance $R_{\rm LED}$ of 2.057 Ω and one forward-biased voltage V_F of 2.73 V.

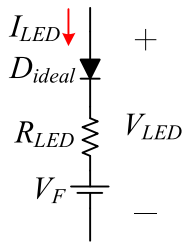

Fig. 6. Approximately linear model of an LED.

B. Duty Cycle Decision

In the proposed LED driver, the input voltage is 12 V. Based on (4), the duty cycle for the proposed LED driver can be obtained as follows:

$$D = 1 - \frac{2V_{\rm in}}{V_{o1}+V_{o2}}. \tag{13}$$

Therefore, based on the parameters, the value of D is

$$D = 1 - \frac{2\times 12}{34.5+34.5} \approx 0.652. \tag{14}$$

C. Input Inductor Design

By assuming that Δi_{L1} and Δi_{L2} are 40% of I_{L1}, the input inductors L_1 and L_2 can be found out as follows:

$$\begin{aligned} L_1 &= \frac{V_{\rm in}DT_s}{I_{L1}\cdot 40\%} \\ &= \frac{(12)(0.652)(10\ \mu)}{(1.02)(0.4)} \\ &\approx 192\ \mu{\rm H}. \end{aligned} \tag{15}$$

Hence, the values of L_1 and L_2 for design are set at 200 μH.The input current ripple $\Delta i_{\rm in}$ can be found out as follows:

$$\Delta i_m = \left(\frac{2\times 12}{200\ \mu}\right)(0.652-0.5)(10\ \mu) = 0.18\,{\rm A}. \tag{16}$$

From (16), it can be seen that $\Delta i_{\rm in}$ is 9.45% of the input current $i_{\rm in}$.The peak input inductor current in L_1 is

$$\begin{aligned} I_{L1,\,\max} &= I_{L1,\,\rm rated} + \frac{V_{\rm in}DT_s}{2L_1} \\ &= 1.02 + \frac{(12)(0.652)\left(10\times 10^{-6}\right)}{2\left(200\times 10^{-6}\right)} \approx 1.22\,{\rm A} \end{aligned} \tag{17}$$

where $I_{L1,\max}$ and $I_{L1,\rm rated}$ are the peak input inductor current and the rated average input inductor current, respectively.

The input inductor core size can be estimated by the following equation [29]. In the following design, there are some of the following assumptions to be given:

1) the fill factor K_u is assumed to be 0.4;
2) the winding resistance R is assumed to be 15 mΩ;

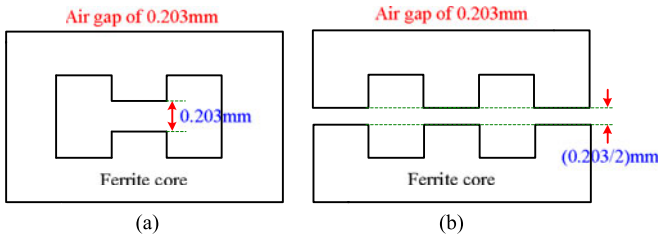

Fig. 7. Methods to form the same calculated air gap: (a) gap in the central limb; (b) gaps on three limbs.

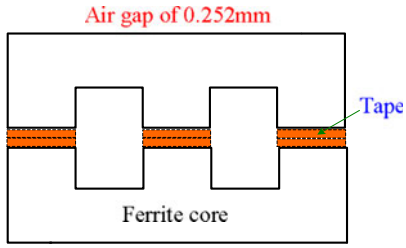

Fig. 8. Ferrite core with air gap using pieces of tape.

3) the maximum flux density $B_{\max}$ is 0.125 T

$$K_g \geq \frac{\rho L_1^2 I_{L1,\max}^2}{B_{\max}^2 R K_u} \times 10^8 = \frac{\left(1.724\times10^{-6}\right)\left(200\times10^{-6}\right)^2(1.22)^2}{(0.125)^2(15\times10^{-3})(0.4)} \times 10^8 \approx 0.109\ \text{cm}^5. \quad (18)$$

Therefore, a ferrite PQ26/25-3C90 core, which has a core geometrical constant K_g of 0.125 cm^5, is selected. The geometrical parameters for this core have a cross-sectional area A_C equal to 1.18 cm^2 and a bobbin winding area W_A equal to 0.503 cm^2. Moreover, the mean length per turn is 5.62 cm.Accordingly, the air gap can be figured out as follows:

$$l_g = \frac{\mu_0 L_1 I_{L1,\max}^2}{B_{\max}^2 A_C} \times 10^4 = \frac{\left(4\pi\times10^{-7}\right)\left(200\times10^{-6}\right)(1.22)^2}{(0.125)^2(1.18)} \times 10^4 \approx 0.203\ \text{mm}. \quad (19)$$

The number of turns N_1 can be obtained as follows:

$$N_1 = \frac{L_1 I_{L1,\max}}{B_{\max} A_C} \times 10^4 = \frac{\left(200\times10^{-6}\right)(1.22)}{(0.125)(1.18)} \times 10^4 \approx 16.54. \quad (20)$$

To create the air gap in the laboratory conveniently, the air gap is formed by adding some pieces of the electrical insulating polyester film tape. From the data sheet [30], the thickness of one piece of tape is 0.063 mm. Thus, the number of pieces of electrical insulating polyester film tape, called *n*, can be estimated as follows:

$$n = \frac{0.203\ \text{mm}}{0.063\ \text{mm}} \approx 3.22\ \text{pieces}. \quad (21)$$

There are two methods to produce the same calculated air gap as shown in Fig. 7 [31]. In the laboratory, the air gap is formed by adding some pieces of tape. Thus, the second method as shown in Fig. 7(b) is employed. Thus, each limb has the corresponding pieces as follows:

$$\frac{3.22\ \text{pieces}}{2} = 1.61\ \text{pieces}. \quad (22)$$

In this paper, two pieces of tape are used for each limb as shown in Fig. 8. As a result, the air gap becomes 0.252 mm. Thus, to maintain the input inductance unchanged ($L_1 = L_2 = 200\,\mu$H), the number of turns N_1 should be increased. Finally, the number of turns N_1 can be calculated as follows:

$$N_1 = \sqrt{L_1 \cdot \frac{l_g}{\mu_0 A_C}} = \sqrt{200\times10^{-6} \cdot \frac{0.252\times10^{-3}}{\left(4\pi\times10^{-7}\right)\left(1.18\times10^{-4}\right)}} \approx 18.4. \quad (23)$$

Thus, the number of turns N_1 is set to 20.

The RMS value of $I_{L1,\text{rated}}$ can be found as follows:

$$I_{L1,\text{rms}} = I_{L1,\text{rated}}\sqrt{1+\frac{1}{12}\left(\frac{\Delta i_{L1}}{I_{L1,\text{rated}}}\right)} \approx 1.02 \times \sqrt{1+\frac{1}{12}\left(\frac{0.4}{1.02}\right)} \approx 1.04\ \text{A} \quad (24)$$

where Δi_{L1} is the peak-to-peak value of i_{L1}.

The condition of the bare wire size of winding can be determined as follows:

$$A_w \leq \frac{K_u W_A}{N_1} = \frac{(0.4)(0.503)}{20} = 0.01006\,\text{cm}^2. \quad (25)$$

In the switching power converters, the skin effect should be taken into account. Thus, multiple thin wire strands are twisted to form the winding. The skin depth can be calculated as follows:

$$\delta = \sqrt{\frac{\rho}{\pi\mu_0 f}} = \sqrt{\frac{1.724\times10^{-8}}{\pi\times4\pi\times10^{-7}\times100\times10^3}} \approx 0.0209\,\text{cm}. \quad (26)$$

To reduce the skin effect, one should select the bare wire diameter *d* of each wire strand less than 2δ. Thus

$$d < 2\delta = 2\times0.0209 = 0.0418\,\text{cm}. \quad (27)$$

Thus, AWG#44 with a bare diameter of 0.00507 cm and a bare area of 0.0202×10^{-3} cm^2 is selected for wire K_1, and *J* is the current density. The number of strands of AWG#44 is designed to make the current density *J* smaller than 400 A/cm^2. Thus

$$K_1 > \frac{I_{L1,\text{rms}}}{\pi(d/2)^2 J} = \frac{1.04}{\pi(0.00507/2)^2\times400} \approx 130. \quad (28)$$

Based on (28), a litz wire which contains 300 strands of AWG#44 is selected for K_1. Table III shows the winding design results. The final winding resistance of N_1 called R_{N1_final} is

TABLE III
WINDING DESIGN RESULTS OF THE INPUT INDUCTORS

Winding	N_1
Turns	20
Wire # AWG	44
Total bare area (cm^2)	(300 strands)$(0.0202 \times 10^{-3}\ \text{cm}^2) = 6.06\,\text{cm}^2$

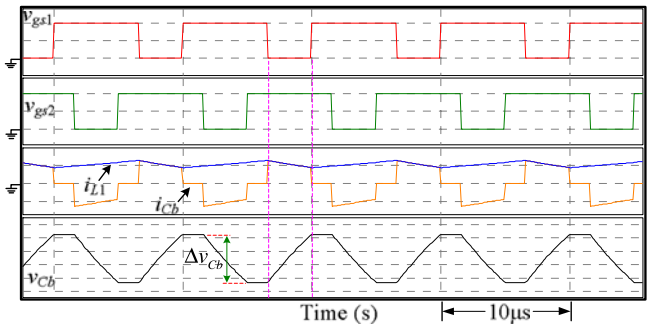

Fig. 9. Relevant waveforms for designing capacitor C_b.

calculated as follows:

$$R_{N1\_\text{final}} = \frac{\rho N_1(\text{MLT})}{A_w} = \frac{\left(1.724 \times 10^{-6}\right)(20)(5.62)}{(300)\left(0.0202 \times 10^{-3}\right)} \approx 32\,\text{m}\Omega. \quad (29)$$

The actual value of L_1 is measured to be about 212 μH at 100 kHz, and the corresponding winding resistance is 38 mΩ. Also, the design procedure for L_1 is applicable to L_2 and the actual value of L_2 is measured to be about 212 μH at 100 kHz.

D. Current Sharing Capacitor Design

The design criterion of the current sharing capacitor is based on the voltage ripple of V_{Cb}. Fig. 9 shows the waveforms relevant to designing the capacitor C_b. Therefore, (30) shows the basic formula of the voltage ripple of V_{Cb}

$$|\Delta v_{Cb}| = \frac{1}{C_b}\int_0^{(1-D)T_s} \left|i_{Cb,(1-D)T_s}\right| dt \quad (30)$$

where Δv_{Cb} is the peak-to-peak value of the voltage ripple of v_{Cb}, and $i_{Cb,(1-D)T_s}$ is the current flowing through C_b during the turn-OFF period of Q_1.In (30), the integration term $(\int_0^{DT_s} |i_{Cb,(1-D)T_s}|dt)$ can be expressed to be $[I_{L1}\cdot(1-D)T_s]$. Therefore, (30) can be expressed to be

$$|\Delta v_{Cb}| = \frac{1}{C_b}\cdot I_{L1}\cdot(1-D)T_s. \quad (31)$$

From (31), the required capacitance of C_b can be obtained by using the following inequality:

$$C_b > \frac{I_{L1}\cdot(1-D)T_s}{|\Delta v_{Cb}|}. \quad (32)$$

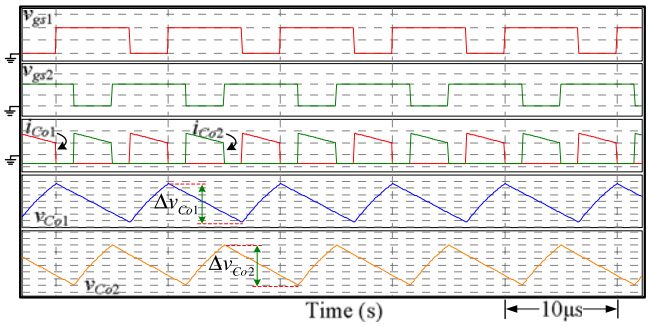

Fig. 10. Waveforms relevant to designing capacitors C_{o1} and C_{o2}.

The voltage across C_b, V_{Cb}, can be calculated as follows:

$$V_{Cb} = \frac{1}{1-0.652} \times 12 - (10 \cdot 3.45) \approx -0.0172\,\text{V}. \quad (33)$$

Based on the design parameters shown above and by assuming that Δv_{Cb} is 10% of V_{Cb}, the value range of C_b can be obtained to be

$$C_b > \frac{(1.02)(1-0.652)(10\ \mu)}{(0.1)\,|-0.0172|} \approx 2\,\text{mF}. \quad (34)$$

Then, the RMS value of i_{Cb} is calculated as follows:

$$\begin{aligned} I_{Cb,\,\text{rms}} &= \sqrt{I_{Cb,\,\text{rms}(+)}^2 + I_{Cb,\,\text{rms}(-)}^2} \\ &= \sqrt{2}\cdot I_{Cb,\,\text{rms}(+)} \\ &= \sqrt{2}\cdot\left[I_{L1,\,\text{rated}}\sqrt{D}\sqrt{1+\frac{1}{12}\left(\frac{\Delta i_{L1}}{I_{L1,\,\text{rated}}}\right)^2}\right] \\ &= \sqrt{2}\cdot\left[1.02\cdot\sqrt{0.652}\sqrt{1+\frac{1}{12}\left(\frac{0.4}{1.02}\right)^2}\right] \approx 0.86\,\text{A} \end{aligned} \quad (35)$$

where $I_{Cb,\text{rms}(+)}$ and $I_{Cb,\text{rms}(-)}$ are the RMS values of the positive portion and negative portion of i_{Cb}, respectively. Finally, two series 2200 μF/16 V electrolytic capacitors connected in parallel with another two series 2200 μF/16 V electrolytic capacitors and one 0.1 μF ceramic capacitor are selected for C_b. From the corresponding data sheet, it can be seen that the rated current ripple of the 2200 μF/16 V Nippon Chemi-Con KZE series aluminum electrolytic capacitor is 2.77 A_{rms} at 105 °C, 100 kHz.

E. Output Capacitor Design

The design criterion of the output capacitor is based on the voltage ripple of V_{o1}. Fig. 10 shows the relevant waveforms for designing the capacitors C_{o1} and C_{o2}. During the turn-ON period of Q_1, the LED string LS_1 is supplied by the output capacitor C_{o1}. Therefore, (36) shows the basic formula of the voltage ripple of V_{o1}

$$|\Delta v_{o1}| = \frac{1}{C_{o1}}\int_0^{DT_s} |i_{o1,\,DT_s}|dt \quad (36)$$

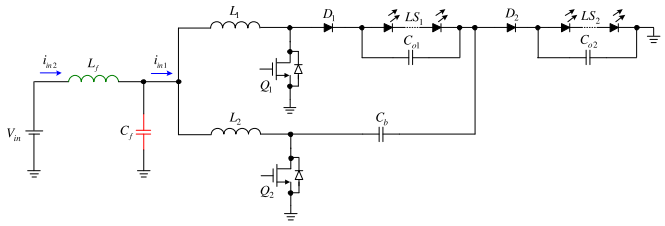

Fig. 11. Proposed LED driver with an input LC low-pass filter.

where Δv_{o1} is the peak-to-peak value of the voltage ripple of V_{o1}, and i_{o1,DT_s} is the current flowing through C_{o1} during the turn-ON period of Q_1.In (36), the integration term $(\int_0^{DT_s} |i_{o1,DT_s}|dt)$ can be expressed to be $(I_{o1} \cdot DT_s)$. Therefore, (36) can be expressed to be

$$|\Delta v_{o1}| = \frac{1}{C_{o1}} \cdot I_{o1} \cdot DT_s. \tag{37}$$

From (37), the required capacitance of C_{o1} can be obtained by using the following inequality:

$$C_{o1} > \frac{I_{o1} \cdot DT_s}{|\Delta v_{o1}|}. \tag{38}$$

Based on the design parameters shown above and by assuming that Δv_{Co1} is 0.1% of V_{Co1}, the value range of C_{o1} can be obtained to be

$$C_{o1} > \frac{(0.35)(0.652)(10\ \mu)}{(0.001)(34.5)} \approx 66\ \mu\text{F}. \tag{39}$$

The RMS value of i_{Co1} is then calculated as (40) shown at the bottom of this page, where $I_{Co1,\text{rms}(+)}$ and $I_{Co1,\text{rms}(-)}$ are the RMS values of the positive portion and negative portion of i_{Co1}, respectively.

Finally, one 220 μF/50 V Su'scon SD series aluminum electrolytic capacitor connected in parallel with one 0.1 μF ceramic capacitor is selected for C_{o1} and also for C_{o2}. From the corresponding data sheet, it can be seen that the rated current ripple of the 220 μF/50 V Su'scon SD series aluminum electrolytic capacitor is 0.65 A_{rms} at 105 °C, 100 kHz.

F. Input Filter Design

To attenuate the input current ripple of the LED driver, a low-pass filter is necessary. Fig. 11 shows an LC low-pass filter, which is added to the front end of the LED driver. The FFT of the input current without the input filter is shown in Fig. 12(a). To design the LC low-pass filter, the transfer function of $i_{\text{in}\,2}/i_{\text{in}\,1}$ in Fig. 13 can be found as follows:

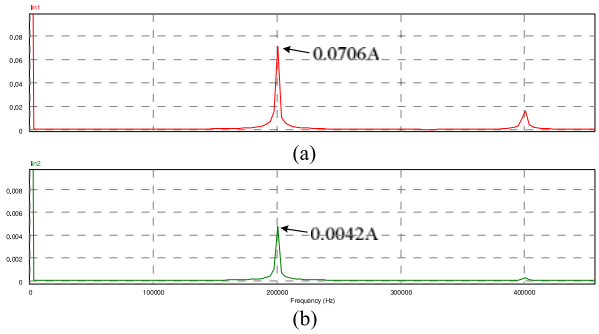

Fig. 12. FFT results of the input current by PSIM: (a) without input filter; (b) with input filter.

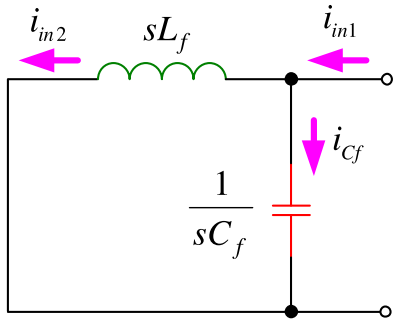

Fig. 13. Illustration of the transfer function of $i_{in\,2}/i_{in\,1}$.

$$\left|\frac{i_{\text{in}\,2}(j\omega)}{i_{\text{in}\,1}(j\omega)}\right| = \frac{1}{\sqrt{\left[1-(2\pi \times 200\ \text{k})^2 L_f C_f\right]^2}} \approx \frac{1}{(2\pi \times 200\ \text{k})^2 L_f C_f} = 0.1. \tag{42}$$

$$\begin{aligned} I_{Co1,\,\text{rms}} &= \sqrt{I_{Co1,\,\text{rms}(+)}^2 + I_{Co1,\,\text{rms}(-)}^2} \\ &= \sqrt{\left[(I_{L1,\,\text{rated}} - I_{o1,\,\text{rated}}) \cdot \sqrt{1-D}\sqrt{1+\frac{1}{12}\left(\frac{\Delta i_{L1}}{I_{L1,\,\text{rated}} - I_{o1,\,\text{rated}}}\right)}\right]^2 + \left(I_{o1,\,\text{rated}} \cdot \sqrt{D}\right)^2} \\ &= \sqrt{\left[(1.02-0.35) \cdot \sqrt{(1-0.652)}\sqrt{1+\frac{1}{12}\left(\frac{0.4}{1.02-0.35}\right)}\right]^2 + \left(0.35 \cdot \sqrt{0.652}\right)^2} \\ &\approx 0.494\ \text{A} \end{aligned} \tag{40}$$

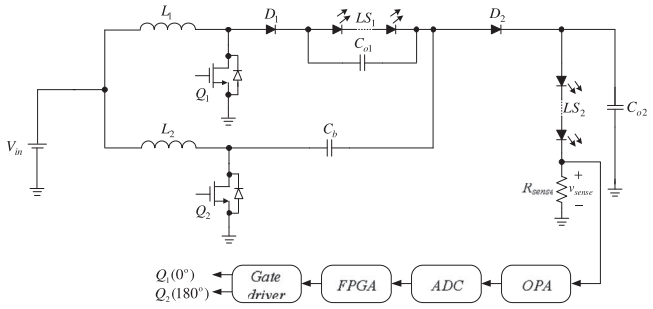

Fig. 14. Overall system block diagram of the proposed LED driver.

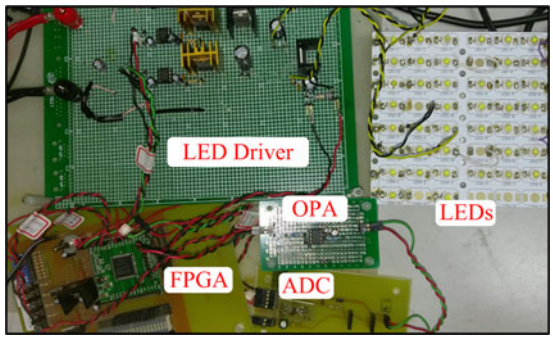

Fig. 15. Photo of the experimental setup.

The filter capacitor C_f is selected to be 100 μF. The filter inductor L_f can be found as follows:

$$\frac{1}{(2\pi \times 200\ \text{k})^2 (0.1)(100\ \mu)} \approx 0.063\ \mu\text{H}. \quad (43)$$

The filter inductor L_f is selected to be 0.1 μH. The attenuation ratio at 200 kHz becomes

$$\left|\frac{i_{\text{in}\,2}(j\omega)}{i_{\text{in}\,1}(j\omega)}\right| = \frac{1}{(2\pi \times 200\ \text{k})^2 (0.1\ \mu)(100\ \mu)} \approx 0.063. \quad (44)$$

Hence, the amplitude of $i_{\text{in}2}$ at 200 kHz becomes 0.0042 A as shown in Fig. 12(a).

The RMS value of i_{Cf} is 0.056 A. Finally, one 100 μF/25 V Nippon Chemi-Con KMG series aluminum electrolytic capacitor connected in parallel with one 0.1 μF ceramic capacitor is selected for C_f. From the corresponding data sheet, it can be seen that the rated current ripple of the 100 μF/25 V Nippon Chemi-Con KMG series aluminum electrolytic capacitor is 0.13 A_{rms} at 105 °C, 100 kHz. The filter inductor L_f is measured to be 0.28 μF at 100 kHz.

G. Switch Choice

Without considering the voltage spikes, the voltage stresses across Q_1, Q_2, D_1, and D_2 can be obtained as follows:

$$V_{ds1} = V_{ds2} = \frac{1}{2} \cdot (V_{o1} + V_{o2}) = \frac{1}{2} \cdot (34.5 + 34.5) = 34.5\ \text{V} \quad (45)$$

$$V_{d1} = V_{o1} + V_{o2} = 34.5 + 34.5 = 69\ \text{V} \quad (46)$$

$$V_{d2} = \frac{1}{2} \cdot (V_{o1} + V_{o2}) = \frac{1}{2} \cdot (34.5 + 34.5) = 34.5\ \text{V}. \quad (47)$$

For analysis convenience, the current flowing through Q_1, Q_2, D_1, and D_2 can be estimated by the simulation software PSIM. Their current values are estimated to be 0.86, 1.37, 0.62, and 0.62 A, respectively. The MOSFETs selected for Q_1 and Q_2 are named STP120 NF10. The specifications of STP120 NF10 have the voltage rating V_{DS} of 100 V, the current rating I_D of 100 A, and the static drain-source on resistance $R_{\text{DS(on)}}$ of 9 mΩ. The diodes selected for D_1 and D_2 are named V20120 C. The specifications of V20120 C have the maximum repetitive peak reverse voltage V_{RRM} of 120 V, the maximum average forward rectified current $I_{F(\text{AV})}$ of 2 × 10 A, and the forward voltage of 0.54 V at I_F = 5 A.

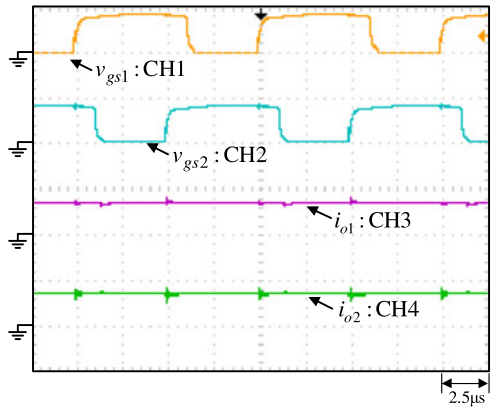

Fig. 16. Waveforms at rated load: (1) v_{gs1} [20 V/div]; (2) v_{gs2} [20 V/div]; (3) i_{o1} [500 mA/div]; and (4) i_{o2} [500 mA/div].

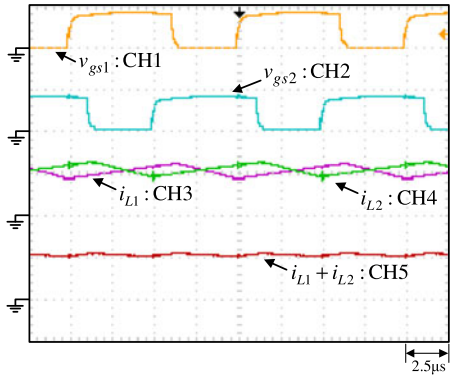

Fig. 17. Waveforms at rated load: (1) v_{gs1} [20 V/div]; (2) v_{gs2} [20 V/div]; (3) i_{L1} [1 A/div]; and (4) i_{L2} [1 A/div]; (5) $i_{L1} + i_{L2}$ [2 A/ div].

H. Current Regulation

Each LED is modeled as a linear model as shown in Fig. 6. The LED currents I_{o1} and I_{o2} can be expressed by

$$I_{o1} = I_{o2} = \frac{\frac{2}{1-D} V_{\text{in}} - \sum V_{F,\,\text{LED}\,1,\,2}}{\sum R_{F,\,\text{LED}\,1,\,2}} \quad (48)$$

where $\sum V_{F,\,\text{LED}\,1,\,2}$ and $\sum R_{F,\,\text{LED}\,1,\,2}$ are the sum of the forward-biased voltages and sum of the forward-biased resistances for the LED strings 1 and 2, respectively.

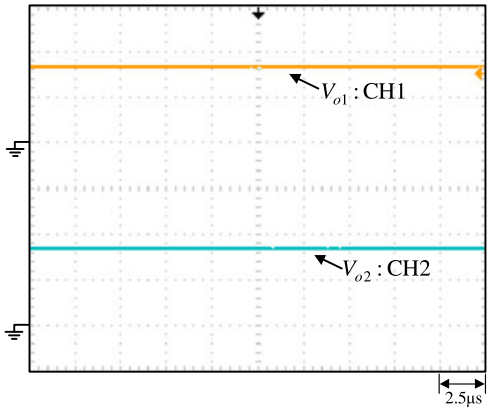

Fig. 18. Waveforms at rated load: (1) V_{o1} [20 V/div]; and (2) V_{o2} [20 V/div].

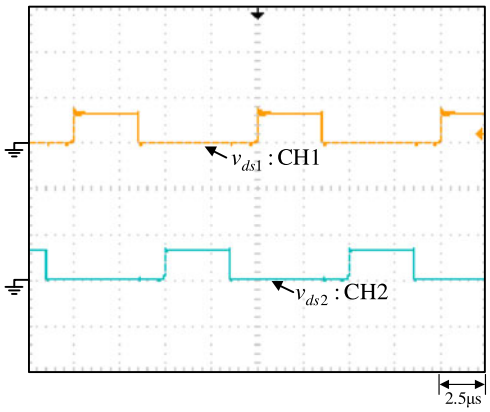

Fig. 19. Waveforms at rated load: (1) v_{ds1} [50 V/div]; and (2) v_{ds2} [50 V/div].

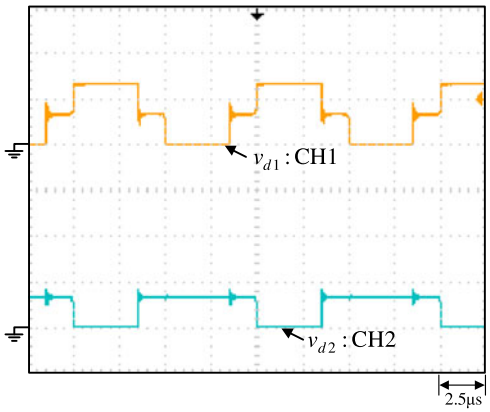

Fig. 20. Waveforms at rated load: (1) v_{d1} [50 V/div]; and (2) v_{d2} [50 V/div].

From (48), it can be seen that the LED currents I_{o1} and I_{o2} can be regulated by pulse width modulation (PWM). Fig. 14 shows the overall system block diagram of the proposed LED driver. The current control is used to maintain a given constant current. The noninverting operational amplifier (OPA) is used to amplify the voltage across the sensing resistor $R_{\rm sense}$, $v_{\rm sense}$. Next, the analog signal $v_{\rm sense}$ is sent to the analog-to-digital converter (ADC) to create a digital signal. Then, the digital signal is sent to the field programmable gate array (FPGA), which contains a serial peripheral interface, a proportional-integral (PI) compensator and a digital PWM generator. Eventually, two gate driving signals with 180° shifted are generated to control the duty cycles of Q_1 and Q_2, respectively.

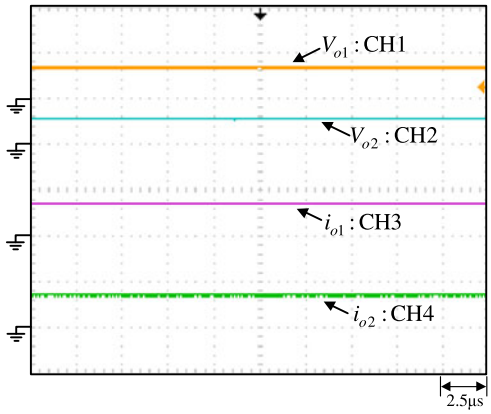

Fig. 21. Waveforms with different LED counts: (1) V_{o1} [50 V/div]; (2) V_{o2} [50 V/div]; (3) i_{o1} [500 mA/div]; and (4) i_{o2} [500 mA/div].

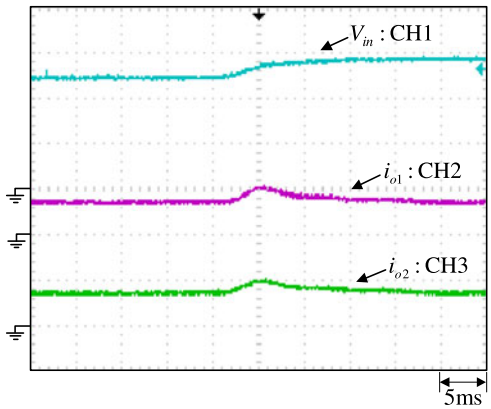

Fig. 22. LED current transitions with the input voltage $V_{\rm in}$ being from 12 to 14 V: (1) $V_{\rm in}$ [5 V/div]; (2) i_{o1} [500 mA/div]; and (3) i_{o2} [500 mA/div].

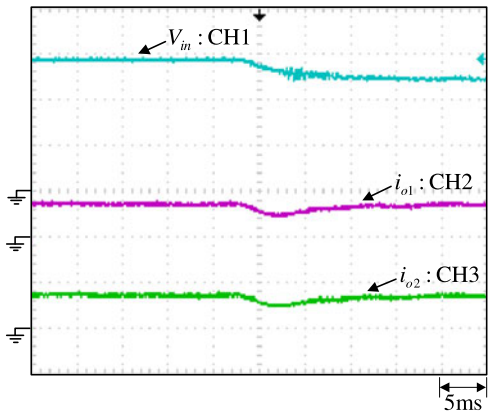

Fig. 23. LED current transitions with the input voltage $V_{\rm in}$ being from 14 to 12 V: (1) $V_{\rm in}$ [5 V/div]; (2) i_{o1} [500 mA/div]; and (3) i_{o2} [500 mA/div].

TABLE IV
COMPARISON WITH THE EXISTING CAPACITIVE CURRENT SHARING LED DRIVERS

LED driver		[27]	[28]	Proposed
Voltage gain		$\frac{1+(N_1/N_2)}{1-D}$	$\frac{2+(N_2/N_1)}{1-D}$	$\frac{2}{1-D}$
MOSFET switch voltage stress		$\frac{V_{o1}+V_{o2}}{1+(N_1/N_2)}$	$\frac{V_{o1}+V_{o2}}{2+(N_2/N_1)}$	$\frac{V_{o1}+V_{o2}}{2}$
LED current sharing method		Capacitor	Capacitor	Capacitor
Input current ripple		Higher (Highly influenced by turns ratio and power level)	Higher (Highly influenced by turns ratio and power level)	Lower (Almost the same)
Component count		Coupled inductor × 1 MOSFET × 2 Capacitor × 4 Diode × 2 Total number = 9	Coupled inductor × 1 MOSFET × 1 Capacitor × 4 Diode × 3 Total number = 9	Input inductor × 2 MOSFET × 2 Capacitor × 3 Diode × 2 Total number = 9
LED current control method		Current control	Current control	Current control
Duty cycle range		$0 < D < 1$	$0 < D < 1$	$0.5 < D < 1$
Complexity		Easy	Easy	Medium
Cost		Low	Low	Medium
Extension		Fig. 24(a)	Fig. 24(b)	Fig. 24(c)
Fault	One string short	Can work	Can work	Can work
	One string open	Cannot work	Cannot work	Cannot work

The parameters of the PI controller embedded in the FPGA are obtained by offline tuning, which is widely used in the industry. There are two steps to be mentioned as follows:

1) Step 1: the proportional gain k_p is tuned from zero to the value which makes the LED current close to about 80% of the desired value;
2) Step 2: the integral gain k_i is also tuned from zero to the value which makes the LED current very close to the desired value.

IV. EXPERIMENTAL RESULTS

Fig. 15 shows the photo of the experimental setup. Figs. 16–21 show the experimental results of the proposed LED driver at rated load. Fig. 16 shows the LED currents i_{o1} and i_{o2}. From Fig. 16, it can be seen that due to the current sharing capacitor, the currents in LED strings are both regulated as about 350 mA. Fig. 17 shows the input inductor currents. With the help of the current sharing capacitor, not only the LED currents but also the inductor currents are balanced. Since the interleaved control, the ripple of $i_{L1} + i_{L2}$ can be reduced, and the dc input current is about 2.13 A. Fig. 18 shows the voltages across LED strings 1 and 2. The LED string voltage V_{o1} is about 33.2 V, and the LED string voltage V_{o2} is about 33.8 V. Fig. 19 shows the voltage stresses across Q_1 and Q_2. From Fig. 19, it can be seen that the voltage stresses across Q_1 and Q_2 are approximately 33.5 V$[=(33.2\text{ V} + 33.8\text{ V})/2]$. Fig. 20 shows the voltage stresses across D_1 and D_2. From Fig. 20, it can be seen that the voltage across D_1 is approximately 67 V ($=$ 33.2 V + 33.8 V), and the voltage across D_2 is approximately 33.5 V$[=(33.2\text{ V} + 33.8\text{ V})/2]$. Fig. 21shows the voltages and currents of the LED strings with different LED counts. The LED count of LS_1 is 10, but the LED count of LS_2 is 8. From Fig. 21, it can be seen the LED string voltage V_{o1} is about 33.2 V, and the LED string voltage V_{o2} is about 28 V. Although the LED counts are not equal, the LED currents are balanced. Based on the measured information, the efficiency of the proposed LED driver is about 91.7%. Figs. 22 and 23 show the LED current transitions when the input voltage changes. From Fig. 22, when the input voltage changes from 12 to 14 V, the corresponding current overshoot is around 160 mA and the resulting recovery time is around 8 ms, whereas from Fig. 23, when the input voltage changes from 14 to 12 V, the corresponding current undershoot is around 156 mA and the resulting recovery time is around 10.4 ms. From Figs. 22 and 23, one can know that when the input voltage increases, the LED currents will increase to a certain value and the current controller will regulate the LED currents to a reference value of 350 mA, whereas when the input voltage decreases, the LED currents will decrease to some value and the current controller will regulate the LED currents to a reference value of 350 mA.

Table IV shows a comparison of the proposed LED driver and the existing LED drivers presented in [27] and [28]. The comparing items contain: 1) voltage gain; 2) MOSFET switch voltage stress; 3) LED current sharing method; 4) input current ripple; 5) component; 6) LED current control method; 7) duty cycle range; 8) complexity; 9) cost; 10) extension; and 11) fault problem. From Table IV, it can be seen that the LED drivers in [27] and [28] use a coupled inductor. Thus, their voltage gains can be adjusted by changing the turns ratio of the coupled inductor. But, a leakage inductance energy recycling circuit is required to suppress the voltage spike. For the input current ripple, due to two-phase interleaved control, the proposed converter has a lower input current ripple. Three LED drivers have the same component counts. It should be noted that in order to achieve input current sharing and LED current sharing, the proposed LED driver should be operated under the condition that the duty cycle *D* is larger than 0.5. Based on the specifications, the duty cycle for the proposed LED driver is calculated to be 0.652. Fig. 24 shows the LED string extensions of the proposed LED driver and the existing LED drivers presented in [27] and [28]. The capacitive LED drivers achieve LED current balance based on the ampere-second balance. Therefore, even though one LED string is short, the LED driver can still work. However, if one LED

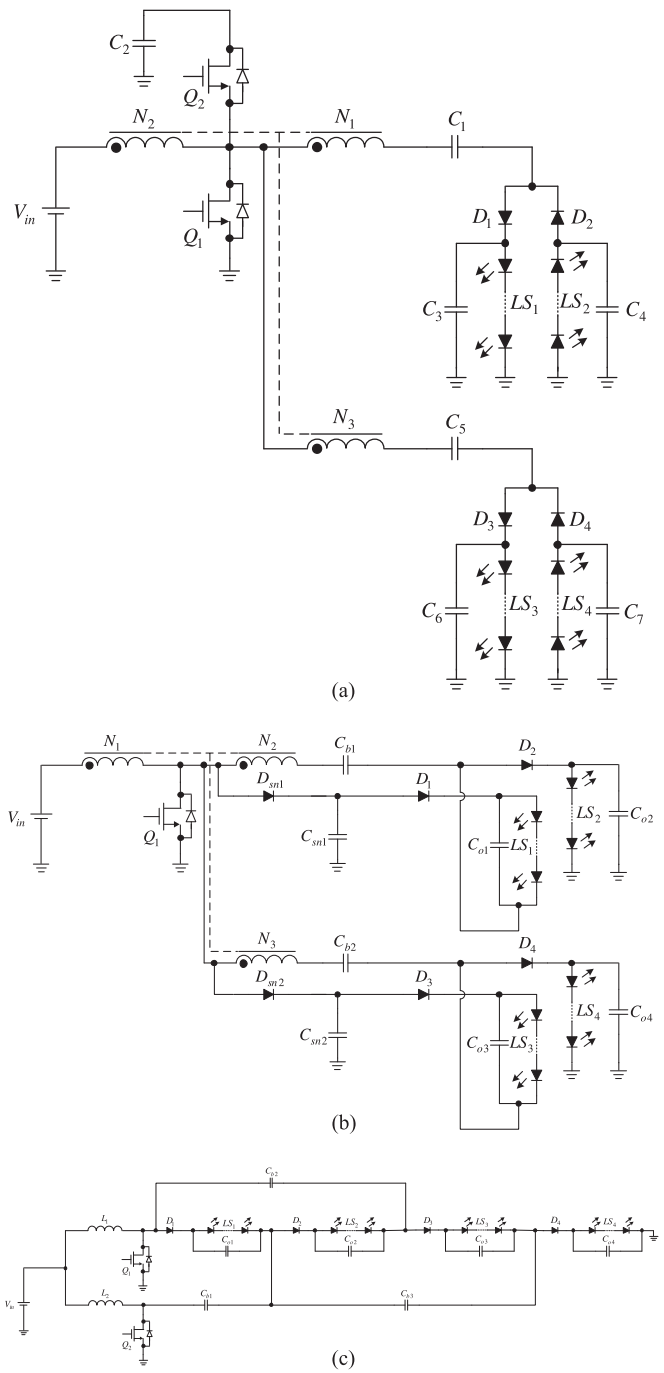

Fig. 24. Extension to more LED strings from: (a) nonisolated two-channel LED driver with active clamp [27]; (b) nonisolated single-switch two-channel LED driver with passive regenerative snubber [28]; (c) proposed nonisolated two-phase interleaved two-channel LED driver.

string is open, the ampere-second balance cannot be realized. Consequently, the LED driver cannot work.

V. Conclusion

A nonisolated two-phase interleaved LED driver with capacitive current sharing is presented. Based on the current charge balance of the current sharing capacitor, not only the input inductor currents but also LED currents can be balanced. The proposed LED driver has the following advantages:

1) the capacitor C_b is used to balance input inductor currents and the LED currents;
2) due to the interleaved control, the input current ripple can be reduced;
3) the LED currents can be balanced under different LED counts;
4) only one grounded LED string current is sensed and controlled. The design procedures of magnetic components and capacitors of the proposed LED driver are shown in the paper.

The inductor design in this paper is shown for reference. Generally, in the laboratory, the air gap is formed by adding some pieces of electrical insulating polyester film tape. One can also grind the air gap in the middle leg by using the machine, or can use ring cores to design the input inductors. In this paper, the capacitor C_b is designed based on the voltage ripple, which is assumed to be 10% of V_{Cb}. Therefore, to reduce the capacitance, the assumed voltage ripple can be chosen to be larger. On the other hand, the value of the capacitor C_b can be reduced if the switching period based on (32) is decreased, but some other circuit components should be redesigned. The experimental results verify the LED currents as well as the input inductor currents are balanced. The voltage stresses of Q_1, Q_2, D_1, and D_2 match the theoretical analysis. Moreover, the current controller can regulate the LED currents when the input voltage changes. Furthermore, a comparison of the proposed LED driver and the existing LED drivers [27] and [28] is presented. Above all, the extensions of the proposed LED driver and the existing LED drivers are given.

References

[1] M. G. Craford, "LEDs challenge the incandescents," *IEEE Circuits Device Mag.*, vol. 8, no. 1, pp. 24–29, Aug. 1992.
[2] N. Narendran and Y. Gu, "Life of LED-based white light sources," *IEEE Display Technol.*, vol. 1, no. 1, pp. 167–171, 2005.
[3] P. S. Almeida, D. Camponogara, M. Dalla Costa, H. Braga, and J. M. Alonso, "Matching LED and driver life spans: a review of different techniques," *IEEE Ind. Electron. Mag.*, vol. 9, no. 2, pp. 36–47, Jun. 2015.
[4] M. Rico-Secades *et al.*, "Evaluation of a low-cost permanent emergency lighting system based on high-efficiency LEDs," *IEEE Trans. Ind. App.*, vol. 41, no. 5, pp. 1386–1390, Sep./Oct. 2005.
[5] B. Ke and W. Lin, "A novel current sharing method without the signal line for multi-output LED driver," in *Proc. 11th China Int. Forum Solid Sate Lighting*, 2014, pp. 19–22.
[6] H. J. Chiu and S. J. Cheng, "LED backlight driving system for large-scale LCD panels," *IEEE Trans. Ind. Electron.*, vol. 54, no. 5, pp. 2751–2760, Oct. 2007.
[7] K. I. Hwu and Y. T. Yau, "Applying one-comparator counter-based sampling to current sharing control of multi-channel LED strings," in *Proc. IEEE Appl. Power Electron. Conf.*, 2010, pp. 737–742.
[8] H. J. Chiu, Y. K. Lo, J. T. Chen, S. J. Cheng, C. Y. Lin, and S. C. Mou, "A high-efficiency dimmable LED driver for low-power lighting applications," *IEEE Trans. Ind. Electron.*, vol. 57, no. 2, pp. 735–743, Feb. 2010.
[9] U. Hu and M. M. Jovanovic, "LED driver with self-adaptive drive voltage," *IEEE Trans. Power Electron.*, vol. 23, no. 6, pp. 3116–3125, Nov. 2008.
[10] K.-I. Hwu, W.-C. Tu, and C.-Y. Lai, "Light-emitting diode driver with low-frequency ripple suppressed and dimming efficiency improved," *IET Power Electron*., vol. 7, no. 1, pp. 105–133, Jan. 2014.
[11] W. Yu, J.-S. Lai, H. Ma, and C. Zhang, "High-efficiency DC-DC converter with twin bus for dimmable LED lighting," *IEEE Trans. Power Electron.*, vol. 26, no. 8, pp. 2095–2100, Aug. 2011.

[12] H. Ma, J.-S. Lai, C. Zhang, and P. Sun, "A high efficiency quasi-single-stage bridgeless electrolytic capacitor-free high-power AC-DC driver for supplying multiple LED strings in parallel," *IEEE Trans. Power Electron.*, vol. 31, no. 8, pp. 5825–5836, Aug. 2016.
[13] K. I. Hwu and S. C. Chou, "A simple current balancing converter for LED lighting," in *Proc. 24th Appl. Power Electron. Conf. Expo.*, 2009, pp. 587–590.
[14] Y. Hu and M. M. Jovanovic, "A new current-balancing method for paralleled LED strings," in *Proc. IEEE Appl. Power Electron. Conf.*, 2011, pp. 705–712.
[15] K. I. Hwu, W. C. Tu, and M. J. Hong, "A LED current balancing driver with magnetizing inductance energy recycling considered," in *Proc. 27th Appl. Power Electron. Conf. Expo.*, 2012, pp. 975–979.
[16] K. I. Hwu, W. C. Tu, and M. J. Hong, "A dimmable LED driver based on current balancing transformer with magnetizing energy recycling considered," *IEEE Display Technol*., vol. 10, no. 5, pp. 388–395, May 2014.
[17] X. Wu, Z. Wang, and J. Zhang, "Design considerations for dual-output quasi-resonant flyback LED driver with current-sharing transformer," *IEEE Trans. Power Electron.*, vol. 28, no. 10, pp. 4820–4830, Oct. 2013.
[18] Y. L. Lin, H. J. Chiu, Y. K. Lo, and C. M. Leng, "LED backlight driver circuit with dual-mode dimming control and current-balancing design," *IEEE Trans. Ind. Electron.*, vol. 61, no. 9, pp. 4632–4639, Sep. 2014.
[19] Y. L. Lin, H. J. Chiu, Y. K. Lo, and C. M. Leng, "Light-emitting diode driver with a combined energy transfer inductor for current balancing control," *IET Power Electron*., vol. 8, no. 10, pp. 1834–1843, Sep. 2015.
[20] X. Wu, J. Zhang, and Z. Qian, "A simple two-channel LED driver with automatic precise current sharing," *IEEE Trans. Ind. Electron.*, vol. 58, no. 10, pp. 4783–4788, Oct. 2011.
[21] C. Zhao, X. Xie, and S. Liu, "Multioutput LED drivers with precise passive current balancing," *IEEE Trans. Power Electron.*, vol. 28, no. 3, pp. 1438–1448, Mar. 2013.
[22] J. Wang, J. Zhang, X. Huang, and L. Xu, "A family of capacitive current balancing methods for multi-output LED drivers," in *Proc. 26th Annu. IEEE Appl. Power Electron. Conf. Expo.*, Fort Worth, TX, USA, Mar. 2014, pp. 2040–2046.
[23] X. Wu, C. Hu, J. Zhang, and C. Zhao, "Series-parallel autoregulated charge-balancing rectifier for multioutput light-emitting diode driver," *IEEE Trans. Ind. Electron.*, vol. 61, no. 3, pp. 1262–1268, Mar. 2014.
[24] W. Feng, F. C. Lee, and P. Mattavelli, "Optimal trajectory control of LLC resonant converters for LED PWM dimming," *IEEE Trans. Power Electron.*, vol. 29, no. 2, pp. 4820–4830, Feb. 2014.
[25] X. Wu, C. Hu, J. Zhang, and Z. Qian, "Analysis and design considerations of LLCC resonant multioutput DC/DC LED driver with charge balancing and exchanging of secondary series resonant capacitors," *IEEE Trans. Power Electron.*, vol. 30, no. 2, pp. 780–789, Feb. 2015.
[26] X. Chen, D. Huang, Q. Li, and F. C. Lee, "Multichannel LED driver with CLL resonant converter," *IEEE Trans. Emerg. Sel. Opt. Power Electron.*, vol. 3, no. 3, pp. 979–987, Sep. 2015.
[27] K. I. Hwu and W. Z. Jiang, "Non-Isolated two-channel LED driver with automatic current balance and zero voltage switching," *IEEE Trans. Power Electron.*, vol. 31, no. 12, pp. 8359–8370, Dec. 2016.
[28] K. I. Hwu and W. Z. Jiang, "Single-switch coupled-inductor-based two-channel LED driver with a passive regenerative snubber," *IEEE Trans. Power Electron.*, vol. 32, no. 6, pp. 4482–4490, Jun. 2017.
[29] R. W. Erickson and D. Maksimovic, *Fundamental of Power Electronics*, 2nd ed. Norwell, MA, USA: Kluwer, 2001.
[30] Data sheet: 3M 1350F-1, 1350F-2 Tape Flame-Retardant Tape with Polyester Film and Acrylic Pressures-Sensitive Adhesive, 2000.
[31] S. Maniktala, *Switching Power Supply Design & Optimization*, 2nd ed. New York, NY, USA: McGraw-Hill, 2014.

K. I. Hwu (M'06) was born in Taichung, Taiwan, on August 24, 1965. He received the B.S. and Ph.D. degrees in electrical engineering from National Tsing Hua University, Hsinchu, Taiwan, in 1995 and 2001, respectively.

From 2001 to 2002, he was the Team Leader of the Voltage-Regulated Module (VRM) at AcBel Company. From 2002 to 2004, he was a Researcher at the Energy and Resources Laboratories, Industrial Technology Research Institute. He is currently a Professor with the Institute of Electrical Engineering, National Taipei University of Technology, Taipei, Taiwan, where he was the Chairman of the Center for Power Electronics Technology from 2005 to 2006. His fields of research interests include converter topologies, magnetic component applications, power factor correction rectifiers, sustainable energy applications, LED lighting drivers, and digital control.

Dr. Hwu has been a member of the Program Committee of the IEEE Applied Power Electronics Conference and Exposition since 2005. He has also been a member of the Technical Review Committee of the Bureau of Standards, Metrology, and Inspection since 2005. Since 2008, he has been a member of the IET.

W. Z. Jiang (S'12) was born in Changhua, Taiwan, on May 9, 1989. He received the B.S. and M.S. degrees in electrical engineering, in 2011 and 2013, respectively, from National Taipei University of Technology, Taipei, Taiwan, where he is currently working toward the Ph.D. degree.

His fields of research interests include converter topologies, magnetic component applications, power factor correction rectifiers, sustainable energy applications, LED lighting drivers, and digital control.