Leakage Current Suppression of Three-Phase Flying Capacitor PV Inverter With New Carrier Modulation and Logic Function

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***Abstract*—Flying capacitor photovoltaic (PV) inverters have been widely discussed in the literature. However, the relevant leakage current issues have not received much attention. In this paper, the modulation techniques for a transformerless three-phase flying capacitor PV inverter are investigated for the leakage current suppression. First, the theoretical analysis of the system common mode model and leakage current is presented. Second, three kinds of conventional carrier-based modulation techniques are evaluated, and results indicate that they fail to effectively suppress the leakage current. Third, a new carrier modulation and logic function is presented. It is able to maintain the constant common mode voltage, and consequently, the leakage current can be significantly reduced. Finally, the experimental tests are conducted on a transformerless three-phase flying capacitor PV inverter to verify the effectiveness of the proposed method.**

***Index Terms*—Leakage current, pulse width modulation (PWM), three-phase flying capacitor (FC) photovoltaic (PV) inverter, transformerless PV system.**

I. Introduction

In RECENT years, the power generation from renewable energy resources, such as photovoltaic (PV) and wind energies, has received more attention [1]–[8]. Conventional PV systems with isolated transformers suffer from the high cost, large size, and low efficiency. That is why the transformerless PV systems have been receiving more and more attention in recent years. The early relevant research might date back to 1981. The Sandia National Laboratories presented a technical report, which revealed that the efficiency of a PV system without transformer could be higher [9]. A couple of years later, Baeberlin investigated the evolution of grid-connected PV inverter systems from 1989 to 2000. He pointed out there was an efficiency increase around 2% by omission of the transformer, and about 1995, new PV systems without transformer appeared on the market [10].

Compared with the conventional PV systems, the transformerless ones have advantages of the small size, low cost, and high efficiency. However, some technical challenges arise such as the leakage current suppression [11], [12]. In order to solve the problem, many interesting topologies and modulation solutions have been reported in the literature [13]–[18]. They can be classified into two groups: single-phase and three-phase solutions. For single-phase applications, one basic idea is to achieve both the unipolar three-level pulse width modulation (PWM) and constant common mode voltage by integrating the auxiliary switches into an H-bridge inverter. It has the advantages such as the small filter inductor due to the low current ripple and negligible leakage current. However, all the above-mentioned topologies operate in the hard-switching mode. In order to further increase the efficiency, Xiao *et al.* proposed the soft-switching transformerless PV inverter [19], [20]. It can achieve the higher efficiency with the leakage current suppression capability.

On the other hand, for three-phase applications, Kerekes *et al.* evaluated three-phase transformerless PV inverter topologies [21], which revealed that the leakage current could be very low by connecting the supply neutral to the middle of the dc-link capacitors. However, the leakage current could dramatically increase, and would be higher than the limited level in case of a very small neutral line inductance [21]. Another three-phase four-leg topology was presented to reduce the common mode voltage [22]. In this way, the leakage current could be effectively suppressed. However, most of above-mentioned solutions are limited to three-phase two-level PV inverters, while the solutions for three-phase multilevel PV inverters have not received much attention. In fact, the multilevel PV inverters have been investigated in many publications [23]–[27], but few papers discuss their leakage current issues. In general, there are three typical multilevel inverter topologies [28]–[30], such as the neutral point clamped (NPC), cascaded H-bridge (CHB), and flying capacitor (FC). In comparison to NPC inverters, the FC inverter does not need many clamped diodes. Also, unlike CHB inverters, it does need a transformer for multiple isolated dc sources. Therefore, it is attractive for transformerless PV

Manuscript received August 18, 2016; accepted October 3, 2016. Date of publication April 12, 2017; date of current version December 1, 2017. This work was supported in part by the National Natural Science Foundation of China under Grant 51677161, in part by the Science Foundation for Distinguished Young Scholars of Hebei Province under Grant E2016203133, and in part by the Hundred Excellent Innovation Talents Support Program of Hebei Province under Grant SLRC2017059. Recommended for publication by Associate Editor M. Vitelli. *(Corresponding author: Zhigang Lu.)*

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Digital Object Identifier 10.1109/TPEL.2017.2692753

systems. Unfortunately, up to now, there is no literature considering the leakage current issue for the transformerless three-phase FC multilevel PV inverters.

The objective of this paper is to present a new carrier modulation solution for the transformerless three-phase FC multilevel PV inverter for the leakage current suppression. The main contributions of this paper include:

1) A detailed evaluation and comparison of the three typical carrier-based modulation methods for the leakage current suppression, which has not been comparatively evaluated so far in three-phase FC PV inverters.
2) Presenting a new leakage current suppression solution with a new modulation strategy. It can be implemented with a very simple but effective carrier-based modulation and logic function (MLF).
3) Testing and verifying the leakage current suppression capabilities of the typical and new carrier-based modulations to serve as a useful reference to researchers and engineers working in the area of transformerless PV applications.

The rest of the paper is organized as follows: First, the system leakage current analysis is presented in Section II. Second, a theoretical analysis of the conventional carrier modulations and corresponding common mode voltages is provided in Section III. Third, a new carrier modulation with logic functions is presented in Section IV. This is followed by the experimental verification in Section V. Finally, the concluding remarks are presented in Section VI.

II. Leakage Current Analysis in a Flying Capacitor PV Inverter

The schematic diagram of the transformerless three-phase FC multilevel PV inverter is illustrated in Fig. 1, where $C_{\rm PV}$ is the parasitic capacitance between the PV paneland ground. $C_{\rm hg}$ is the parasitic capacitance between the converter output points and the ground. The leakage current will arise if the capacitor voltage is time-varying, due to the fact that $i = C_{\rm PV}(dV/dt)$. The simplified model is shown in Fig. 1(b), from which it can be observed that the parasitic capacitor voltage depends on the phase voltages $V_{\rm AN}$, $V_{\rm BN}$, and $V_{\rm CN}$.

In order to simplify the analysis, the common mode and differential mode model between each phase is derived, as shown in Fig. 2(a), where the common mode and differential mode voltage of AB phase are defined as follows:

$$V_{\rm CM\_AB} = \frac{V_{\rm AN} + V_{\rm BN}}{2} \tag{1}$$

$$V_{\rm DM\_AB} = V_{\rm AN} - V_{\rm BN}. \tag{2}$$

With (1) and (2), the phase voltages $V_{\rm AN}$ and $V_{\rm BN}$ can be rewritten as

$$V_{\rm AN} = V_{\rm CM\_AB} + \frac{V_{\rm DM\_AB}}{2} \tag{3}$$

$$V_{\rm BN} = V_{\rm CM\_AB} - \frac{V_{\rm DM\_AB}}{2}. \tag{4}$$

In practice, the parasitic capacitor $C_{\rm hg}$ is so small that its influence on the leakage current can be neglected. The

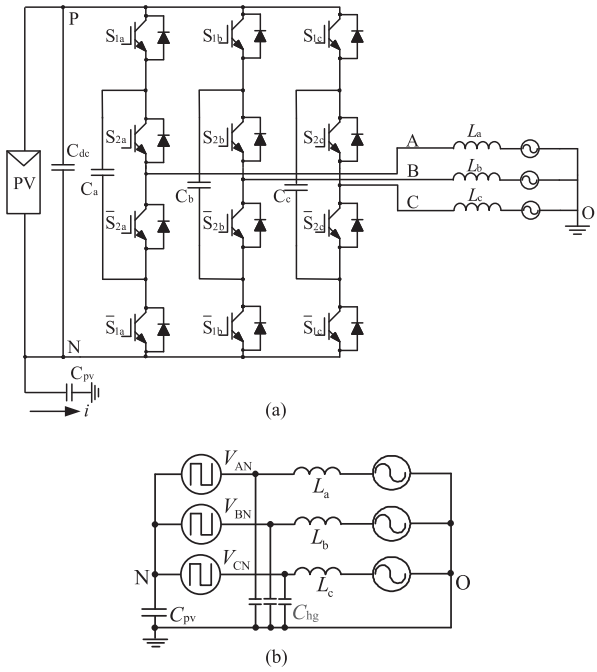

Fig. 1. Transformerless flying capacitor multilevel PV inverter. (a) Schematic diagram and (b) simplified model.

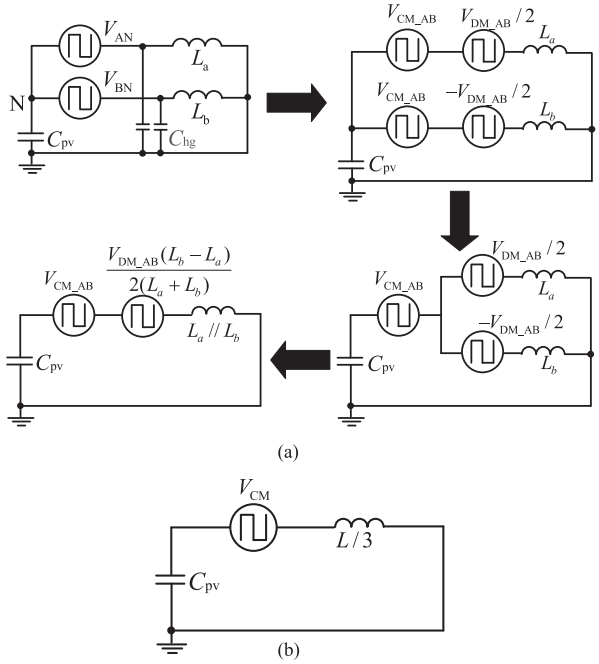

Fig. 2. System model. (a) Step-by-step procedure for AB phase. (b) Simplified model for three-phase system.

inductances of L_a and L_b in Fig. 2(a) are designed equal to each other, so the effect of the differential mode voltage $V_{\rm DM\_AB}$ can be neglected. In this way, the simplified model three-phase system can be obtained by considering all common mode models of AB, BC, and CA phases. As shown in Fig. 2(b), the parasitic capacitor voltage depends on three-phase common mode voltage $V_{\rm CM}$, which is defined as

$$V_{\rm CM} = \frac{V_{\rm AN} + V_{\rm BN} + V_{\rm CN}}{3}. \tag{5}$$

In (5), each phase voltage in Fig. 1(a) can be expressed as three states, as shown in (6), where the FC voltage is assumed to be $V_d/2$ for simplicity of the analysis:

$$V_{\mathrm{xN}} = \begin{cases} V_d & S=2 \quad S_{1x}\ S_{2x}\ \mathrm{ON},\ \bar{S}_{1x}\ \bar{S}_{2x}\ \mathrm{OFF} \\ \dfrac{V_d}{2} & S=1 \begin{cases} \bar{S}_{1x}\ S_{2x}\ \mathrm{ON},\ S_{1x}\ \bar{S}_{2x}\ \mathrm{OFF} \\ \bar{S}_{1x}\ S_{2x}\ \mathrm{OFF},\ S_{1x}\ \bar{S}_{2x}\ \mathrm{ON} \end{cases} \\ 0 & S=0 \quad S_{1x}\ S_{2x}\ \mathrm{OFF},\ \bar{S}_{1x}\ \bar{S}_{2x}\ \mathrm{ON} \end{cases} \tag{6}$$

where $x = A, B, C$, and V_d is the dc bus voltage.

Substituting (6) into (5), it can be concluded that the common mode voltage V_{CM} cannot be kept constant if the switching states are not properly selected, which mainly depends on the modulation strategies. Therefore, the next section will analyze the effect of different modulation strategies on the common mode voltage.

III. Conventional Modulations

As discussed in the previous section, the common mode voltage should be controlled constant to suppress the leakage current. This section will provide an analysis of common mode voltage with the conventional modulation methods, namely, in-phase disposition (IPD) modulation, opposite phase disposition (OPD) modulation, and phase shift (PS) modulation.

A. IPD Modulation

Fig. 3(a) shows the schematic diagram of IPD modulation. During the positive half-cycle, the modulation wave of m_a is always greater than the lower carrier, so S_{2a} remains ON and $\bar{S}_{2a}$ is OFF. On the other hand, in case the modulation wave of m_a is greater than the upper carrier S_{1a} is ON, $\bar{S}_{1a}$ is OFF, and $V_{\mathrm{AN}} = V_d$. While m_a is lower than the upper carrier, S_{1a} is OFF and $\bar{S}_{1a}$ is ON, and $V_{\mathrm{AN}} = V_d/2$.

During the negative half-cycle, the modulation wave of m_a is always smaller than the upper carrier, so S_{1a} maintains OFF and $\bar{S}_{1a}$ is ON. On the other hand, S_{2a} is ON, $\bar{S}_{2a}$ is OFF and $V_{\mathrm{AN}} = V_d/2$ if m_a is greater than the lower carrier. On the contrary, if m_a is smaller than the lower carrier, $S_{2a}$is OFF, $\bar{S}_{2a}$is ON and $V_{\mathrm{AN}} = 0$.

The operation principles of phases B and C are similar to that of phase A, and thus not duplicated here for simplicity.

Considering that the switching frequency is high enough, each phase modulation wave of m_a, m_b, or m_c can be assumed constant during one switching cycle. In this case, each phase voltage and corresponding common mode voltage are illustrated in Fig. 3(b), from which it can be observed that the common mode voltage is time-varying within a switching cycle, and the pk–pk value is $5V_d/6 - V_d/3 = V_d/2$.

B. OPD Modulation

Fig. 4(a) shows the schematic diagram of OPD modulation. During the positive half-cycle, the operation principle is similar to that of IPD modulation. However, it is different within the negative half-cycle. Fig. 4(b) shows each phase voltage and corresponding common mode voltage. Compared with Fig. 3(b), it can be observed that the common mode voltage pk–pk amplitude is reduced from $V_d/2$ to $V_d/3$.

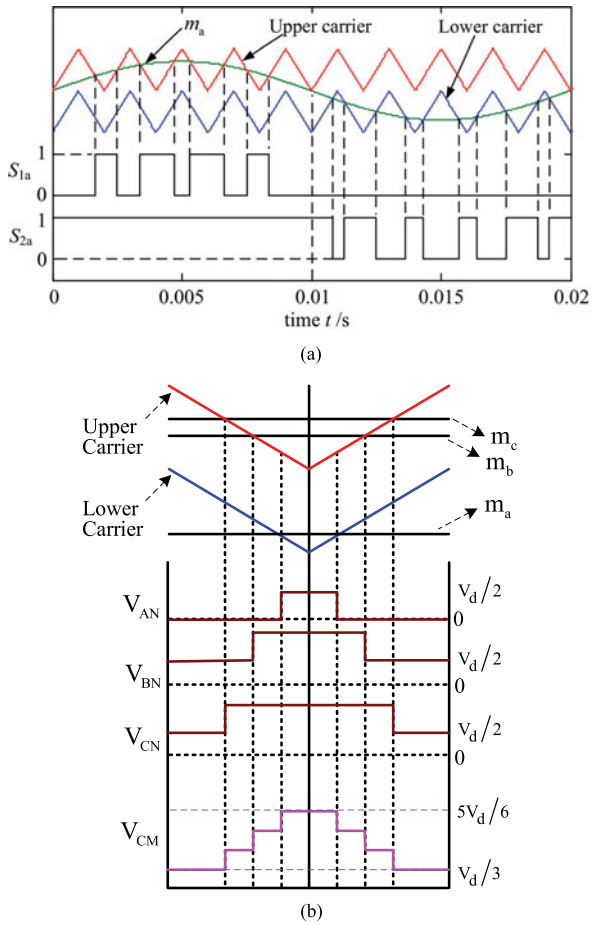

Fig. 3. In-phase disposition modulation. (a) The principle of the modulation and (b) each phase voltage and corresponding common mode voltage.

C. PS Modulation

Fig. 5(a) shows the schematic diagram of PS modulation. Different from the in-phase and opposite disposition modulations mentioned above, all switches operate in high-frequency mode during the entire cycle. Fig. 5(b) shows each phase voltage and corresponding common mode voltage, whose pk–pk value is $2V_d/3 - V_d/3 = V_d/3$.

In summary, the conventional IPD modulation, OPD modulation, and PS modulation fail to achieve the constant common mode voltage. Therefore, the leakage current cannot be effectively suppressed.

IV. Proposed Carrier Modulation

In order to solve the above-mentioned problem, a new modulation with constant common mode voltage is presented in this section. From (6) in Section II, it can be concluded that there are $3 \times 3 \times 3 = 27$ operation states for the three-phase system. First of all, a brief review of all the 27 operation states and corresponding common mode voltage is provided in Table I. It can be observed that the common mode voltage can be controlled to be constant with the specific seven operation states.

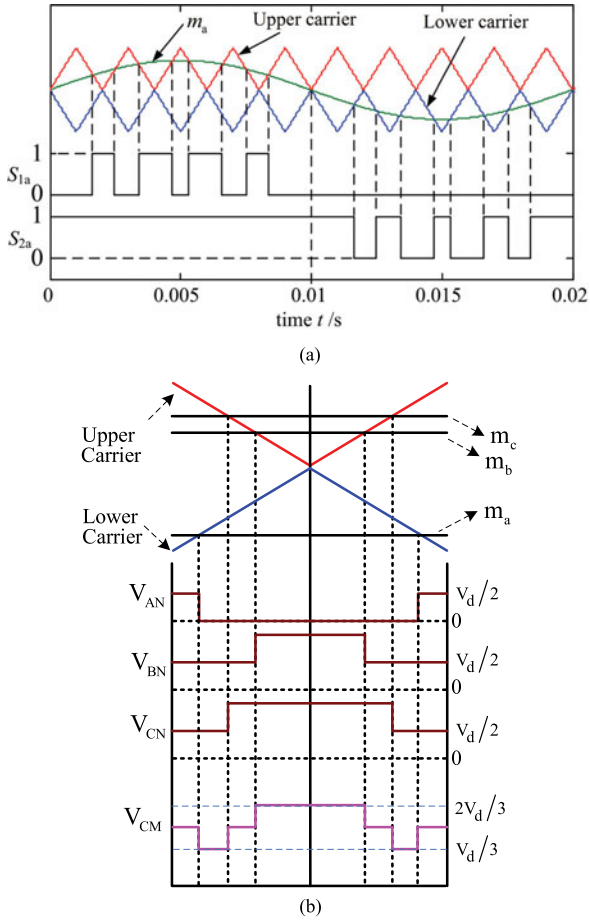

Fig. 4. Opposite phase disposition modulation. (a) The principle of the modulation and (b) each phase voltage and corresponding common mode voltage.

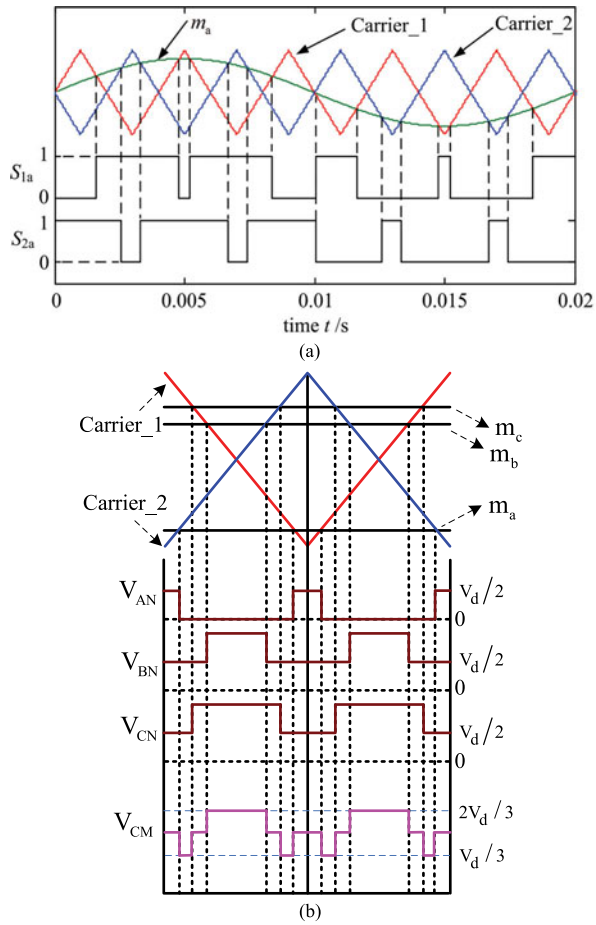

Fig. 5. Phase shift modulation. (a) The principle of the modulation and (b) each phase voltage and corresponding common mode voltage.

It is interesting to note that there is a logic relationship between these seven operation states and the switching states, as shown in Table II. And the proposed MLF is presented in Fig. 6. The logic function is defined as

$$\begin{aligned} S_{1a} &= X(X \oplus Y) + XYZ \quad S_{2a} = \overline{Y(X \oplus Y) + XYZ} \\ S_{1b} &= Y(Y \oplus Z) + XYZ \quad S_{2b} = \overline{Z(Y \oplus Z) + XYZ} \\ S_{1c} &= Z(Z \oplus X) + XYZ \quad S_{2c} = \overline{X(Z \oplus X) + XYZ}. \end{aligned} \tag{7}$$

For example, in the second row of Table I, the input state of *XYZ* is 111. With the logic manipulation of (7), the output switching states will be 101010 for S_{1a}–S_{2c}, see (8) as shown at the bottom of this page.

In the fourth row of Table I, the input state of *XYZ* is 011. With the logic manipulation of (7), the output switching states will be 000111 for S_{1a}–S_{2c}, see (9) as shown at the bottom of the next page.

Similarly, the rest six cases can also be derived and not duplicated here for simplicity.

It should be noted that, in order to suppress the leakage current in an effective way, only seven operation states are used in the proposed modulation. In order to explain the use of the vectors, the limitations, link with redundant vectors, the use of the dc bus in case of seven operation states, a space vector diagram is provided in Fig. 7.

From Fig. 7, it can be observed that seven operation states are symmetrically distributed. The inverter modulation index range or dc-bus utilization is smaller than that of the traditional space vector pulse width modulation (SVPWM). However, by using the zero sequence injection in Fig. 6(a), the dc-bus utilization will be increased. It should be noted that the traditional SVPWM results in the very high leak-

$$\begin{aligned} S_{1a} &= X(X \oplus Y) + XYZ = 1 \quad S_{2a} = \overline{Y(X \oplus Y) + XYZ} = 0 \\ S_{1b} &= Y(Y \oplus Z) + XYZ = 1 \quad S_{2b} = \overline{Z(Y \oplus Z) + XYZ} = 0 \\ S_{1c} &= Z(Z \oplus X) + XYZ = 1 \quad S_{2c} = \overline{X(Z \oplus X) + XYZ} = 0 \end{aligned} \tag{8}$$

TABLE I
OPERATION STATES AND COMMON MODE VOLTAGE

States	V_{AN}	V_{BN}	V_{CN}	V_{CM}
222	V_d	V_d	V_d	V_d
111	$V_d/2$	$V_d/2$	$V_d/2$	$V_d/2$
000	0	0	0	0
200	V_d	0	0	$V_d/3$
220	V_d	V_d	0	$2V_d/3$
020	0	V_d	0	$V_d/3$
022	0	V_d	V_d	$2V_d/3$
002	0	0	V_d	$V_d/3$
202	V_d	0	V_d	$2V_d/3$
210	V_d	$V_d/2$	0	$V_d/2$
120	$V_d/2$	V_d	0	$V_d/2$
021	0	V_d	$V_d/2$	$V_d/2$
012	0	$V_d/2$	V_d	$V_d/2$
102	$V_d/2$	0	V_d	$V_d/2$
201	V_d	0	$V_d/2$	$V_d/2$
211	V_d	$V_d/2$	$V_d/2$	$2V_d/3$
100	$V_d/2$	0	0	$V_d/6$
221	V_d	V_d	$V_d/2$	$5V_d/6$
110	$V_d/2$	$V_d/2$	0	$V_d/3$
121	$V_d/2$	V_d	$V_d/2$	$2V_d/3$
010	0	$V_d/2$	0	$V_d/6$
122	$V_d/2$	V_d	V_d	$5V_d/6$
011	0	$V_d/2$	$V_d/2$	$V_d/3$
112	$V_d/2$	$V_d/2$	V_d	$2V_d/3$
001	0	0	$V_d/2$	$V_d/6$
212	V_d	$V_d/2$	V_d	$5V_d/6$
101	$V_d/2$	0	$V_d/2$	$V_d/3$

TABLE II
SWITCHING LOGIC STATES AND OPERATION STATES

XYZ	S_{1a}	S_{2a}	S_{1b}	S_{2b}	S_{1c}	S_{2c}	States defined in (6)
111	1	0	1	0	1	0	111
000	0	1	0	1	0	1	
011	0	0	0	1	1	1	012
010	0	0	1	1	0	1	021
001	0	1	0	0	1	1	102
101	1	1	0	0	0	1	201
110	0	1	1	1	0	0	120
100	1	1	0	1	0	0	210

age current, which restricts it applications in transformerless PV systems. While the proposed method can significantly reduce the leakage current to comply with standard VDE-0126-1-1. Therefore, the proposed method is attractive for transformerless PV systems. In summary, the proposed modulation is very easy to implement. Meanwhile, it can achieve the constant common mode voltage with the negligible leakage current, which will be verified in the following section.

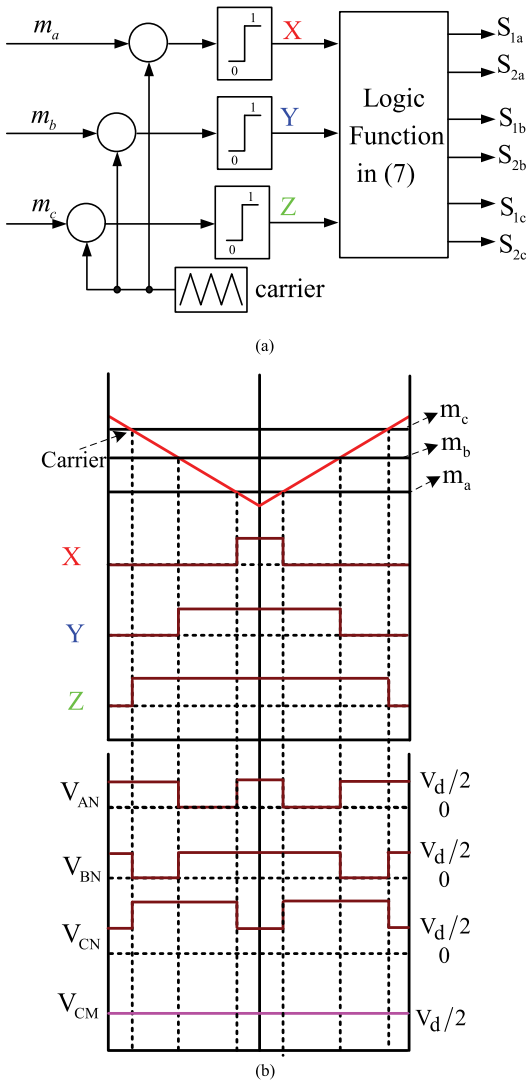

Fig. 6. Proposed modulation. (a) Schematic diagram and (b) each phase voltage and corresponding common mode voltage.

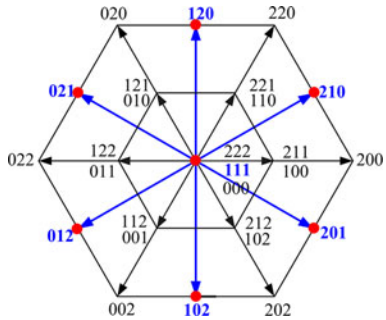

Fig. 7. Space vector diagram.

$$\begin{aligned} S_{1a} &= X(X\oplus Y)+XYZ=0 \quad & S_{2a} &= \overline{Y(X\oplus Y)+XYZ}=0 \\ S_{1b} &= Y(Y\oplus Z)+XYZ=0 \quad & S_{2b} &= \overline{Z(Y\oplus Z)+XYZ}=1 \\ S_{1c} &= Z(Z\oplus X)+XYZ=1 \quad & S_{2c} &= \overline{X(Z\oplus X)+XYZ}=1 \end{aligned} \tag{9}$$

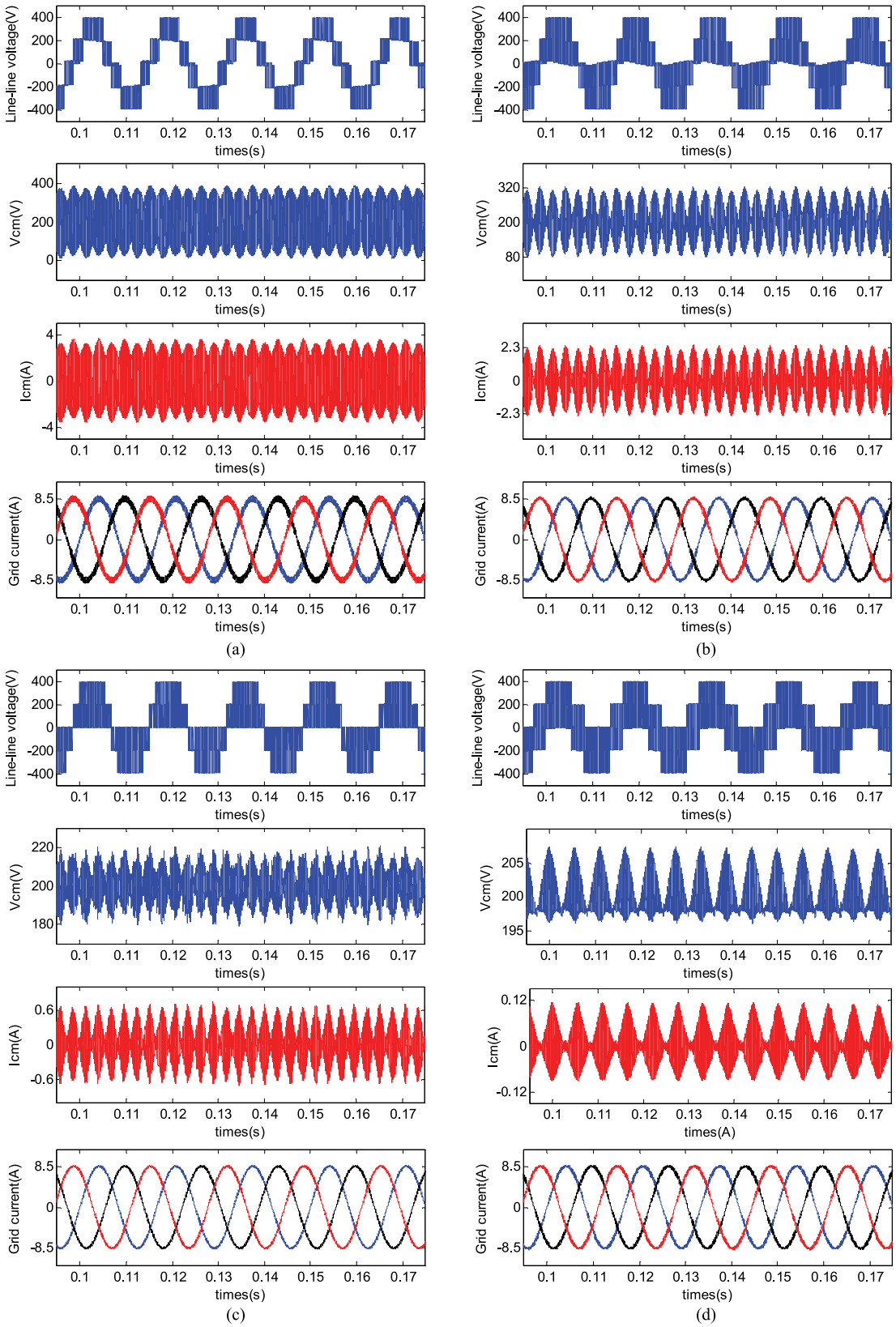

Fig. 8. Simulation results of line–line voltage, common monde voltage, common-mode current, and grid current. (a) In-phase disposition modulation, (b) opposite phase disposition modulation, (c) phase shift modulation, and (d) proposed modulation (MLF).

TABLE III
SUMMARY OF DIFFERENT MODULATION METHODS IN TERMS OF THD AND LEAKAGE CURRENT

	Current THD (%)	Voltage THD (%)	Leakage current (Max)
IPD	8.49%	40.69%	4000 mA
OPD	5.54%	59.96%	2300 mA
PS	2.13%	59.89%	600 mA
MLF	3.5%	70.03%	120 mA

V. SIMULATION AND EXPERIMENTAL RESULTS

In this section, simulations are carried out with MATLAB/Simulink. The dc bus voltage V_d is 400 V, the grid voltage is 208 V/60 Hz, and the rated power is 2 kW. The switching frequency is 10 kHz, and the filter inductor is 4 mH. According to [21], the parasitic capacitance between PV array and ground is from 50 to 150 nF/kW. Considering that the rated power is 2 kW, the parasitic capacitor value is selected as 300 nF in this paper.

Fig. 8 shows the simulation results of four different carrier-based modulations. It can be observed that the conventional IPD, OPD, and PS modulations result in the high leakage current, whose maximum value is beyond 300 mA and fails to comply with the standard VDE-0126-1-1. On the contrary, the proposed new method leads to a negligible leakage current. Its maximum value is well below 300 mA.

Table III shows the summary of different modulation methods in terms of total harmonic distortion (THD) and leakage current regarding the simulation results in Fig. 8. It should be noted that the voltage THD value is that of the line–line voltage without the PV inverter output filter. Generally, the higher voltage THD may lead to more high-frequency harmonics on the converters. However, the output filter is typically installed in the PV inverters. So the high-frequency harmonics can be well attenuated, as shown in the following simulation and experimental results.

From Fig. 8, it can be observed that the conventional IPD modulation has the lowest THD of *differential-mode* line–line voltage before filtering, which theoretically means the lowest current THD. However, it is not the case, as shown in Fig. 8(a). The reason is that the grid current consists of the *differential-mode* and *common-mode* components. The common mode current (leakage current) is very high, and the grid current is interfered by the common mode leakage current [21]. Therefore, the conventional IPD modulation has the highest current THD. The common mode leakage current is still high with the OPD modulation, so the current THD is as high as 5.54%. Both the PS and proposed modulation methods have smaller current THD, but only the proposed modulation method can effectively reduce the leakage current well below 300 mA, which meets the standard VDE-0126-1-1.

In order to further validate the effectiveness of the proposed modulation solution, an experimental platform is built with a 32-bit floating point DSP (TMS320F28335) and field-programmable gate array (Xilinx Spartan3 series XC3S400). The experimental parameters are the same as those in the simulation.

Fig. 9 shows the experimental results of different modulation solutions. From the phase–phase voltages waves, all the output phase–phase voltages are five-level waveforms, except that there is a slightly asymmetrical level in Fig. 9(a-1) and (b-1). The reason behind that is the FC voltage fluctuates in a fundamental frequency manner, due to which the switch state remains unchanged during the positive or negative half-cycle, as shown in Figs. 3(a) and 4(a). On the contrary, all of the switches operate in high-frequency mode with the PS modulation and proposed

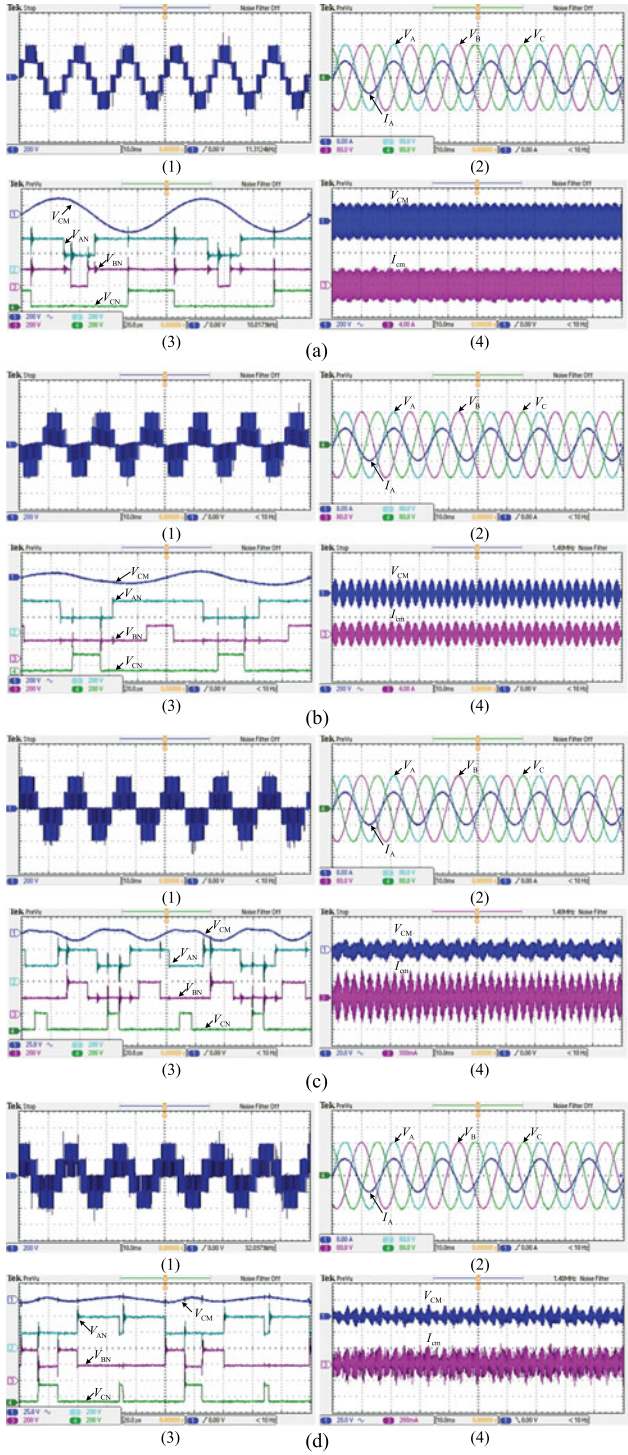

Fig. 9. Experimental results of different modulations: (a) In-phase disposition modulation, (b) opposite phase disposition modulation, (c) phase shift modulation, and (d) proposed modulation.

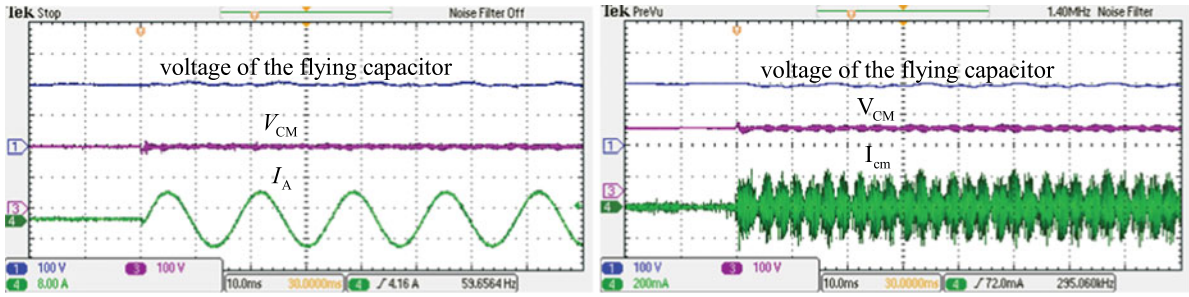

Fig. 10. Experimental results of dynamic test.

modulation. Therefore, there is no asymmetrical level problem in the phase–phase voltage, as shown in Fig. 9(c-1) and (d-1). The measured line–line voltage THDs of four different modulations are 42.52%, 62.51%, 63.86%, and 74.1%. On the other hand, all the filtered output voltage and current are sinusoidal, which indicates that all the above-mentioned modulations can achieve the high quality output waveforms.

Fig. 9(a-3), (b-3), (c-3), and (d-3) shows the experimental waveforms of each phase voltage $V_{\rm AN}$, $V_{\rm BN}$, $V_{\rm CN}$ and corresponding common mode voltage during two switching cycle (200 μs). In agreement with the theoretical analysis in Section III, the common mode voltage with the IPD modulation has the largest amplitude, as shown in Fig. 9(a-3). With the OPD modulation and PS modulation, the common mode voltage is reduced, but still fluctuating, as shown in Fig. 9(b-3) and (c-3). It is interesting to note that the common mode voltages experience a high-frequency sinusoidal fluctuation [e.g., Fig. 9(a-3)], which is different from the theoretical waveform [e.g., Fig. 3(b)] in Section III. The main reason is that there is a resonant circuit, which consists of the parasitic capacitor $C_{\rm PV}$ and filter inductor. That is why the common mode voltages vary in a high-frequency sinusoidal way.

The experimental results of the common mode voltage and leakage current with different modulation solutions are shown in Fig. 9(a-4), (b-4), (c-4), and (d-4). It can be observed that the common mode voltage fluctuation amplitude is the largest with IPD modulation, and consequently the maximum value of leakage current is very high, as shown in Fig. 9(a-4). With the OPD modulation and PS modulation, the common mode voltages are reduced, as shown in Fig. 9(b-4) and (c-4), but the maximum value of the leakage currents is still high and exceeds 300 mA, which fails to meet the standard VDE-0126-1-1. Fig. 9(d-4) shows the experimental results with the proposed solution. The common mode voltage fluctuates slightly so that the maximum value of the leakage current is about 200 mA, which is below 300 mA specified in VDE-0126-1-1.

In order to further verify the dynamic performance of the proposed modulation method, the output current is stepped from zero to a certain level in the experimental test, as shown in Fig. 10. It can be observed that the FC voltage is balanced to half the dc bus voltage under the current step, and the common mode voltage remains around $V_d/2$(200 V). The leakage current is well below 300 mA. In summary, the proposed modulation has a superior steady-state and dynamic performance in terms of leakage current suppression.

On the other hand, the effect of maximum power point tracking (MPPT) techniques on the leakage current is an interesting topic, which is neglected in most papers. There are many MPPT methods, so the effect of different MPPT algorithms on the leakage current is very complicated. However, if the dc-link voltage is slowly changed with the MPPT algorithm, its effect on the leakage current will be small, due to the fact that the leakage current is dependent of the high-frequency components, instead of low-frequency ones. It should be noted that this paper mainly concentrates on the different carried-based modulation solutions to reduce the leakage currents. Other issues such as grid synchronization [31]–[34], current control [35]–[38], islanding detection [39], fault ride through control [40], and other space vector modulations [41]–[42] are beyond the scope of this paper.

VI. Conclusion

This paper has presented the theoretical analysis and experimental verification of carrier-based modulations, instead of the complex space vector modulations, for the leakage current suppression in a transformerless three-phase FC multilevel PV inverter system. The findings reveal that the conventional carried-based modulations cannot keep the common mode voltage constant, and thus fail to reduce the leakage current in an effective way. On the other hand, the proposed modulation solution can achieve the constant common mode voltage, and the leakage current can be significantly suppressed well below 300 mA, as specified in the standard VDE-0126-1-1. In addition, the proposed modulation is simple to implement by digital signal processors or analog circuits.

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