Isolated Modular Multilevel DC–DC Converter With DC Fault Current Control Capability Based on Current-Fed Dual Active Bridge for MVDC Application

Yuxiang Shi, *Member, IEEE*, and Hui Li, *Senior Member, IEEE*

***Abstract*—In this paper, a current-fed modular multilevel dual-active-bridge (CF-MDAB) dc–dc converter is proposed for medium-voltage dc (MVDC) application. The proposed converter inherits favorite characteristics of DAB circuits including soft switching and small passive components. Thereby, high efficiency and high power density can be achieved. Moreover, with direct input and output dc current control, the CF-MDAB is suitable for a breakerless MVDC system since it can realize dc fault ride-though operation. In addition, the *dv/dt* in the converter is mitigated with the quasi-three-level modulation. In this paper, the proposed converter is applied to integrate the battery energy storage to a MVDC grid as an example to illustrate its operation principles and fault current control capability. The operation principles are presented for both normal and dc fault conditions; the dynamic models are also derived not only under normal operation mode but under dc fault operation mode as well. The control systems under different operation modes are designed, respectively, based on the developed mathematical models. A downscaled 40-kHz 3-kW CF-MDAB prototype was built in the laboratory. The experimental results under both normal condition and dc fault condition verified the analysis as well as the control performance of the proposed converter.**

***Index Terms*—Battery energy storage system (BESS), current-fed dual active bridge (CF-DAB), dc fault ride through (FRT), modular dc–dc converter, zero-voltage switching (ZVS).**

NOMENCLATURE

BESS	Battery energy storage system.
CB	Circuit breaker.
CF-DAB	Current-fed dual active bridge.
CF-MDAB	Current-fed modular dual active bridge.
CF-Q3LC	Current-fed quasi-three-level converter.
DAB	Dual active bridge.
ESR	Equivalent series resistance
FBSM	Full-bridge submodule.
FRT	Fault ride through.
FTF	Front-to-front.
HBSM	Half-bridge submodule.
HVS	High-voltage side.
IM2DC	Isolated modular multilevel dc–dc converter.
ISOP	Input series–output parallel.
ISOI	Input series–output independent.
LVS	Low-voltage side.
MVDC	Medium-voltage dc.
MMC	Modular multilevel converter.
OD	Output disable.
Q2L	Quasi two level.
Q2LC	Quasi-two-level converter.
Q3L	Quasi three level.
Q3LC	Quasi-three-level converter.
SOC	State of charge.
SPS	Shipboard power system.
TDR	Total device rating.
ZVS	Zero voltage switching.
D	Duty cycle.
d	Ratio of dc-link voltage of battery and dc sides.
D_h	HVS duty cycle.
D_l	LVS duty cycle.
$L_{\rm dc}$	DC inductance.
L_s	AC inductance.
M	LVS submodule number in one arm.
m	Ratio of dc inductance and ac inductance.
N	HVS submodule number in one arm.
p	LVS FBSM number or LVS inserted battery unit number in one arm for BESS application.
q	HVS FBSM number in one arm.
ϕ	Phase-shift angle.
ω	Angular switching frequency.

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Y. Shi is with ABB Corporate Research Center, Raleigh, NC 27606 USA (e-mail: yuxiang.shi@us.abb.com).

H. Li is with the Center for Advanced Power Systems, Florida State University, Tallahassee, FL 32310 USA (e-mail: hli@caps.fsu.edu).

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I. INTRODUCTION

DUE to simple structure, high efficiency, and high reliability, dc systems are widely accepted in low-voltage commercial and residential applications. They are also proven to be cost effective in high-voltage power transmissions, e.g., the offshore wind power transmission [1]–[3]. Recently, with the unprecedented deployments of renewable generation, dc

systems at medium-voltage distribution level are drawing increasing attention, especially for dc collector grids in wind and PV farms [2], [4]. The medium-voltage dc (MVDC) systems are also of great interest in the future shipboard power distribution system (SPS) because of the saving in fuel consumption and the increase in cargo capacity [5], [6].

The dc power conversion efficiency and dc fault clearance are the major challenges existing against the widespread adoption of MVDC systems [7]–[9]. As an interface to integrate various loads (e.g., renewables and energy storages) as well as to connect subsystems at different voltage levels, dc–dc converters, often termed as dc transformers, are the essential devices to determine the system efficiency and fault performance. Due to safety consideration, galvanic isolation is usually required for the dc–dc converters [5]. The resulted dc–ac–dc multistage power conversion indicates additional loss over the single-stage ac transformer, making the soft-switching technique crucial for the high-efficiency operation of the dc–dc converters. It is widely recognized that fast dc fault clearance is a critical technical obstacle for a MVDC system [8], [9]. Conventionally, a circuit breaker (CB) is used for fault current interruption. Because of the low impedance and the absence of zero-current crossing in MVDC faults, dc CBs have to interrupt high fault current within milliseconds. Conventional mechanical CBs for ac fault are slow and not fast enough for dc fault interruption, while the solid-state CBs have fast response but suffer from high on-state conduction loss [10]–[12]. Hybrid CBs, consisting of a mechanical CB and a solid-state CB in parallel, integrate the advantages of both type CBs; however, the high capital cost and relatively large footprint limit their applications [12], [13]. As an alternative solution, coordinated control of power converters and mechanical contactors enables fast dc fault clearance without using CBs [8]. Based on this approach, a possible dc fault clearance process has been proposed for a shipboard breakerless MVDC system in [14]. The key of such a fault management system lies in a power converter that can provide a controlled dc fault current for fault location identification and supply uninterrupted power to zonal loads if applicable, i.e., with dc fault ride-through (FRT) capability. In a breakerless MVDC system, the dc FRT capability is a desired feature for dc–dc converters.

A dual-active-bridge (DAB) dc–dc converter, employing two H-bridges connected through an ac transformer, has the advantages of bidirectional power flow, inherent zero-voltage switching (ZVS), and low total device rating (TDR) [15]. Hence, high efficiency can be achieved. The high-frequency operation allows a significant reduction of size and weight of passive components, leading to a high power density. Due to these favorite features, DAB converter is one of the most popular converters for industry applications and has been considered as a promising topology for solid-state transformers, which are expected as key components in future smart grids [16]–[18]. Extensive research has been conducted for applying DAB converters at medium-voltage level [18]–[29]. The advance in SiC devices enables direct employment of DAB converters in MVDC system, where the major challenge is the extremely high *dv*/*dt* associated with high-frequency switching [18]–[21]. On the other hand, modular DAB structures, such as input-series–output-parallel and input-series–output-independent configurations, allow the use of low-voltage commercial power devices with high switching speed, while the downside is the control complexity [22]–[24]. Both types of modular DAB converters lack dc FRT capability and inject uncontrollable fault current due to the terminal capacitors when dc fault occurs. Moreover, the completely discharged capacitor prevents the system from fast recovery after the fault clearance. Recently, a quasi-two-level (Q2L) modular DAB converter has been proposed for the application of high-voltage dc (HVDC) transformer [25]–[28], of which arms consisting of multiple half-bridge cells are adopted. The cell-based structure reduces the *dv*/*dt* in the circuit and makes fast recovery possible since excessive capacitor discharge can be avoided. Nonetheless, the converter still cannot provide dc FRT operation.

With great flexibility and superior fault tolerance, modular multilevel converter (MMC) has become a popular technology for high-voltage high-power dc–ac/ac–dc applications, such as medium-voltage drive and HVDC transmission [29]–[32]. Taking advantages of MMC, isolated modular multilevel dc–dc converters (IM2DC) comprising two MMCs in front-to-front (FTF) connection through a transformer have been reported [33]–[40]. Conventional sinusoidal modulation methods are adopted in [33]–[39], where one MMC is emulated as an ac voltage source and the other one is controlled as a current source at the ac terminals. As a result, all the existing control algorithms of MMC can be applied. Although the size and weight of passive components can be significantly reduced with the medium-frequency operation, the converter has the downsides of MMC that the TDR is relatively high while the efficiency is relatively low because of hard-switching and high-conduction loss. Two-level (2L) modulation has been proposed in [35] and [40], operating the IM2DC as an "electronic dc tap changer," where each MMC has a voltage stepping ratio in addition to the transformer. Since the duty cycle is fixed at 0.5, the converter does not have direct dc current control, therefore cannot realize dc FRT operation.

As a sibling to voltage-fed DAB converter, the current-fed DAB (CF-DAB) converter inherits the inherent ZVS condition [41], [42]. Moreover, the converter has direct dc current control at the current-fed terminal, making it possible to realize dc FRT operation. Inspired from the CF-DAB, a current-fed modular DAB (CF-MDAB) converter is proposed in this paper. The topology looks similar to the MMC-based IM2DC, but the operation principle is totally different and TDR is much smaller. A novel quasi-three-level (Q3L) modulation method and control strategy based on duty cycle and phase-shift angle are proposed to operate the converter in CF-DAB mode, hence ZVS can be realized and dc FRT operation is achieved. Like a modular DAB converter, half-bridge submodules (HBSMs) are preferred for high-efficiency operation. By sequential switching of cells in one arm, the *dv*/*dt* in the circuit is controllable. Under Q3L modulation, the cell capacitor of the upper switch in a HBSM functions as a voltage clamper or high-frequency filter with low-current stress, enabling the use of a small capacitor and a low-current rating device. In the proposed modulation, the dc loop frequency is higher than the switching frequency (e.g., twice for single-phase case), which reduces the value of dc inductors. The ZVS and small passive components allow the

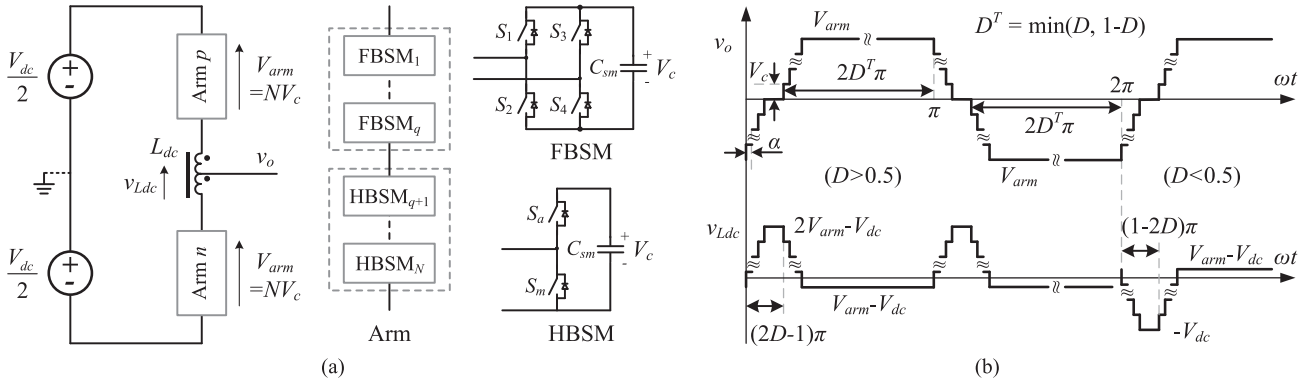

Fig. 1. Single-leg CF-Q3LC: (a) Structure, and (b) output and dc inductor voltage waveforms.

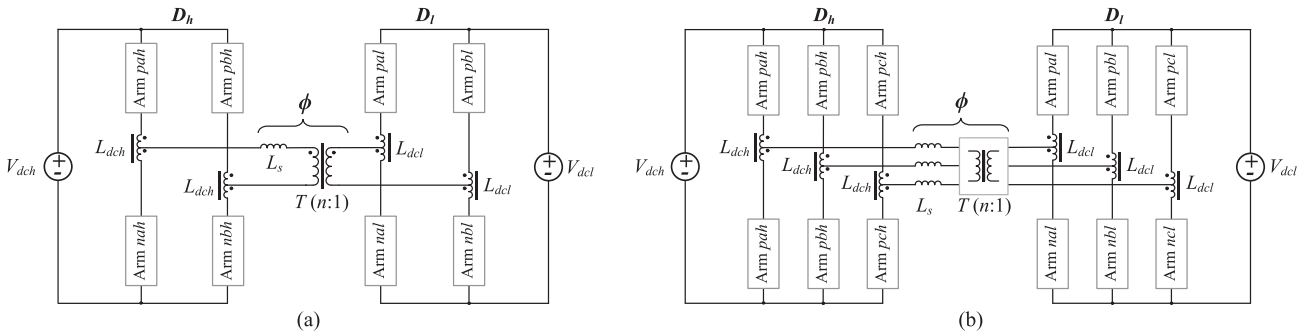

Fig. 2. CF-MDAB converters: (a) Single-phase, and (b) three-phase.

converter to achieve high efficiency and high power density. To realize the dc FRT operation, hybrid cells consisting of HBSMs and a necessary number of full-bridge submodules (FBSMs) are implemented for each arm, where the FBSMs are only for dc FRT purpose and operated as HBSMs under normal conditions. Through duty cycle regulation, the dc current can be controlled in both normal operation mode and dc fault operation mode.

In this paper, the CF-MDAB converter is applied to interface the battery energy storage, an indispensable device in MVDC collection grids and SPS, for demonstration of the operation principle and control capability of the converter. The rest of this paper is organized as follows. The proposed CF-MDAB converter is described in Section II, where the current-fed quasi-three-level converter (CF-Q3LC) is first introduced as a subconverter. Section III presents a single-phase CF-MDAB converter for BESS application. The operation principles and the ZVS conditions are explained in details. In Section IV, the dynamics of a CF-MDAB converter is analyzed based on the derived small-signal model under normal operation mode. The control systems are then developed accordingly. DC FRT operation is described in Section V and the corresponding control system is developed as well. Experimental verifications are provided in Section VI. Section VII summarizes the main contributions of this study.

II. CF-MDAB Converter Description

A CF-Q3LC converter, a subconverter of CF-MDAB, is first proposed in this paper to achieve direct dc current control capability. The CF-Q3LC can be treated as dual to the voltage-fed Q2LC presented in [25]. The single-leg CF-Q3LC is illustrated in Fig. 1(a). Compared to a voltage-fed Q2LC, a coupled dc inductor is introduced in the leg, of which the center tap is led out as the ac output terminal. Hybrid submodules are adopted in each arm, where the FBSMs are only used at dc fault operation mode to achieve dc FRT and are operated as HBSMs under normal condition. In Q3L modulation, the upper and lower arms are 180° phase shifted with duty cycle D, and trapezoidal Q2L modulation is applied for each arm. Fig. 1(b) shows the voltage waveforms of ac output and dc inductor, with staircase Q3L and Q2L patterns, respectively. By selecting proper cell number and dwell angle α, the dv/dt stress in the circuit can be alleviated, while maintaining minimum cell capacitance and maximum dc voltage utilization. Meanwhile, the interleaving of arm output voltages generates Q2L voltage on the dc inductor; as such a boost-type converter is integrated into the dc loop. Through duty cycle regulation, the dc current can be directly controlled. The dc loop frequency is twice of the switching frequency which allows using a small dc inductance. The magnitude of each voltage step is determined by the voltage of a submodule capacitor. In a single-phase or three-phase CF-Q3LC, the legs are interleaved just as conventional converters. For a single-phase CF-Q3LC, the dc currents in the two legs are in the same phase after interleaving, thereby the total dc current ripple is twice of that in each leg; while the three-phase CF-Q3LC enjoys much lower current ripple due to the cancellation effect of interleaving, resulting in small value of dc inductors. As will be illustrated later, the small dc inductance can benefit the proposed CF-MDAB converter with enhanced ZVS condition.

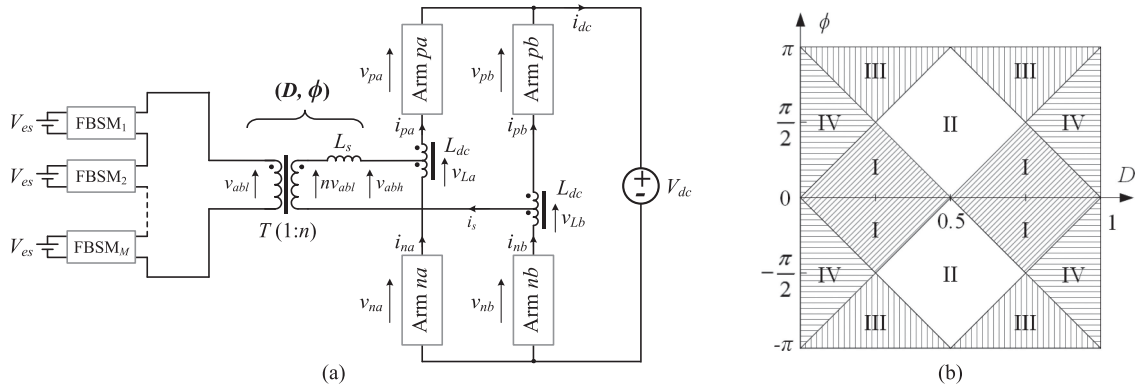

Fig. 3. Single-phase CF-MDAB-based BESS: (a) Circuit configuration, and (b) operation area.

The CF-MDAB converter can be treated as two CF-Q3LCs in FTF connection through medium- or high-frequency transformer *T*, as shown in Fig. 2. The high-voltage-side (HVS) and low-voltage-side (LVS) CF-Q3LCs have independent duty cycle control with D_h and D_l, respectively. For applications where the current-fed characteristic is unnecessary in one side, the dc inductors can be omitted with 50% duty cycle in the corresponding side. The ac-side operation of CF-MDAB converter is very similar to that of the DAB converter. The transferred power flow is determined by the phase-shift angle ϕ between the ac voltages applied on the inductor L_s, which here represents all the applicable inductance in the ac loop. Like CF-DAB converter, the CF-MDAB converter has inherent ZVS condition; the cell capacitor $C_{\rm sm}$ and auxiliary switch $\rm S_a$ in HBSMs act as soft-voltage clamp, with much lower current stress than the main switch $\rm S_m$ (labeled in Fig. 1(a)). Detailed operation principle and ZVS condition will be presented in Section III, using the CF-MDAB-based BESS as an example.

III. CF-MDAB-Based BESS Steady-State Analysis

Considering the symmetry of CF-MDAB topology, a single-phase CF-MDAB converter-based BESS is adopted in the following analysis, as shown in Fig. 3(a), where the LVS CF-Q3LC is replaced by an arm with battery units integrated to the FBSMs. The operation principle of the CF-MDAB-based BESS is the same as that of the CF-MDAB as shown in in Fig. 2, except that the duty cycle of the LVS arm is set to the same as HVS duty cycle (i.e., $D_l = D_h = D$) since no dc loop exists on the battery side.

A. Operation Principle

The possible operation modes of the CF-MDAB BESS converter are shown in Fig. 3(b). Like CF-DAB in [42], there are four operation modes I–IV, and each one has four subareas with $D \geq 0.5$ or $D < 0.5$, and $\phi \geq 0$ or $\phi < 0$. For high-efficiency operation, the duty cycle is designed around 0.5, and the phase-shift angle is usually within $[-\pi/6, \pi/6]$. Thereby, the converter will operate mainly in mode II, and sometimes in mode I at light load. The key waveforms of the CF-MDAB BESS converter in mode II when $\phi \geq 0$ are illustrated in Fig. 4(a), in which the arms are considered as switching elements with multilevel output voltage in the step of V_c.

For battery side, in each switching cycle, *p* ($p < M$) FBSMs are inserted discharging their batteries, while the rest *M-p* submodules are bypassed. This mechanism helps us to realize the charge balancing of battery units. With more bypassed FBSMs, the balancing capability can be improved, however it lowers the conversion efficiency and increases the system cost. Usually, *p* can be set as $M-1$.

In dc side, the two arms in a leg are 180° phase shifted with the same duty cycle *D*. As a result, there will be overlap state of which both the upper and lower arms have positive output voltage when $D > 0.5$, and shoot-through state of which both the upper and lower arms have zero output voltage when $D < 0.5$. In the dc loop, during the nonoverlap or nonshoot-through state, the sum of upper and lower arm output voltage, namely the phase voltage, equals to the arm average voltage $V_{\rm arm} = NV_c$. While during the overlap and shoot-through states, a phase voltage of $2V_{\rm arm}$ and zero will be generated, respectively. Therefore, pulse voltage will be applied to the dc inductor ($v_{\rm La}$, $v_{\rm Lb}$ in Fig. 3(a)), regulating the dc current $i_{\rm dc}$. Through this way, a boost-type converter is integrated and the dc current is fully controllable. The relation between the dc grid voltage $V_{\rm dc}$ and average arm voltage $V_{\rm arm}$ is given as

$$\begin{aligned} V_{\rm dc} &= D\left(V_{\rm arm,pa} + V_{\rm arm,na}\right) = D\left(V_{\rm arm,pb} + V_{\rm arm,nb}\right) \\ &= 2DV_{\rm arm} \end{aligned} \tag{1}$$

where $V_{\rm arm,pa}$, $V_{\rm arm,pb}$, $V_{\rm arm,na}$, and $V_{\rm arm,nb}$ are the corresponding arm voltages, and $V_{\rm arm} = (V_{\rm arm,pa} + V_{\rm arm,pb} + V_{\rm arm,na} + V_{\rm arm,nb})/4$. The corresponding nominal voltage of cell capacitors is $V_{\rm arm}/N$. As can be seen, the equivalent dc ripple is twice of the switching frequency, and the dc current ripple can be calculated by

$$\Delta I_{\rm dc} = \begin{cases} \dfrac{2\pi V_{\rm dc}}{\omega L_{\rm dc}}\left(1-2D\right), & D \leq 0.5 \\ \dfrac{2\pi V_{\rm dc}}{\omega L_{\rm dc}}\left(3-2D-\dfrac{1}{D}\right), & D > 0.5 \end{cases} \tag{2}$$

where ω is the angular switching frequency, and $L_{\rm dc}$ is the dc inductance. The dc current ripple is small with *D* close to 0.5, and when $D = 0.5$, $\Delta I_{\rm dc} = 0$.

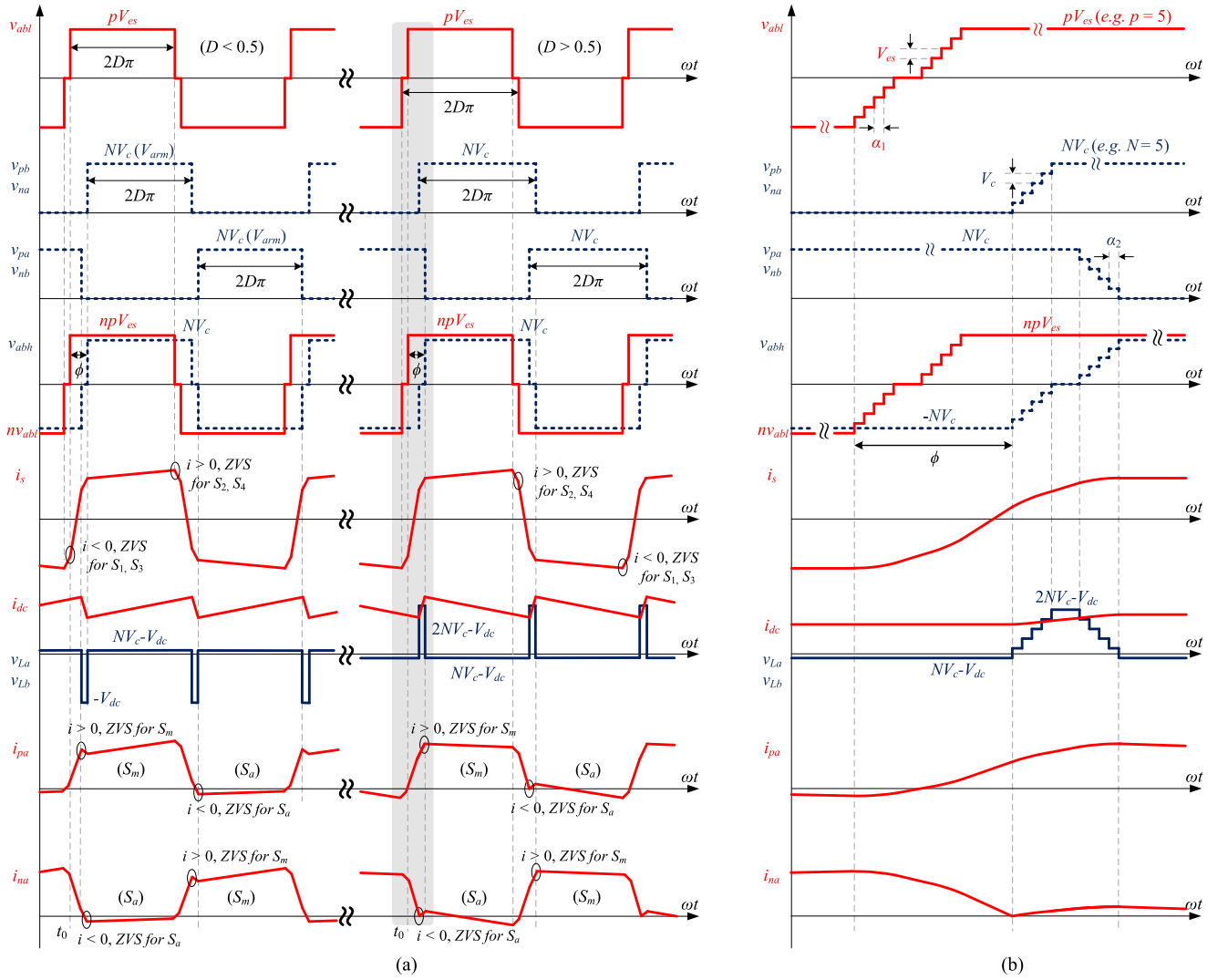

Fig. 4. Key waveforms of the CF-MDAB BESS converter in mode II when $\phi > 0$: (a) Voltage and current, and (b) Zoomed view of the shaded phase range in (a).

Similar to MMC, each leg shares half of the dc current and the ac current equally spreads in the upper and lower arms. As shown in arm currents, the current stress of S_a is much smaller than that of S_m due to the cancellation of dc current and ac current. This implies that the power exchanges directly between the ac and dc sides without buffered in cell capacitors, and, thus, small cell capacitors can be implemented.

The Q3L voltage waveforms are shown in Fig. 4(b) which is the zoomed view of the shaded phase range of (a). For battery side, each FBSM is operated with duty cycle D, while FBSMs in one arm are switched in sequence with dwell angle α_1 to generate Q3L output voltage. In dc side, the CF-Q3LC is operated with a dwell angle α_2. As a result, the ac voltages $v_{\rm abh}$ and $v_{\rm abl}$ present in a staircase pattern with reduced dv/dt. Small dwell angles with acceptable dv/dt are preferred since a large dwell angle will reduce the dc voltage utilization and make ZVS difficult to be maintained in all submodules. In this paper, α_1 and α_2 are assumed to be much smaller than ϕ, such that they are neglected in deriving the power flow equations and ZVS conditions. Without considering the dwell angle effect, the ac voltage and current waveforms are exactly the same as those of CF-DAB. Table I lists the power flow and transformer rms current equations of CF-MDAB in different operation modes, where d is HVS-referred LVS-to-HVS arm voltage ratio, i.e., $d = npV_{\rm es}/V_{\rm arm}$.

B. ZVS Condition

As shown from Fig. 4(a), the ZVS condition of battery-side switches S_1-S_4 (as labeled in Fig. 1(a)) in mode II when $\phi > 0$ can be expressed in

$$\begin{cases} i_{s(t_0)} < 0, & \text{for } S_1S_3, D \le 0.5 \\ i_{s(t_0+\pi+2D^T\pi)} < 0, & \text{for } S_1S_3, D > 0.5 \\ i_{s(t_0+2D^T\pi)} > 0, & \text{for } S_2S_4, D \le 0.5 \\ i_{s(t_0+\pi)} > 0, & \text{for } S_2S_4, D > 0.5 \end{cases}. \tag{3}$$

By substituting instantaneous current, the ZVS condition for LVS arm in mode II with $\phi > 0$ can be obtained. Similarly, the ZVS conditions are derived for all modes and are listed in Table II, where ZVS boundaries of upper and lower switches

TABLE I
POWER AND TRANSFORMER CURRENT OF THE CF-MDAB DC–DC CONVERTER

Mode	Throughout Power	Transformer rms current
I	$\frac{{V_{\rm arm}}^2}{\omega L_s} d\phi \left(2D^T - \frac{\lvert\phi\rvert}{2\pi}\right)$	$\frac{V_{\rm arm}}{\omega L_s}\sqrt{(1-\frac{4}{3}D^T)[(1-d)D^T\pi]^2 + \frac{d(6D^T\pi-\lvert\phi\rvert)\phi^2}{3\pi}}$
II	$\frac{{V_{\rm arm}}^2}{\omega L_s} d\phi \left[1 - \frac{\lvert\phi\rvert}{\pi} - \frac{\pi(1-2D^T)^2}{2\lvert\phi\rvert}\right]$	$\frac{V_{\rm arm}}{\omega L_s}\sqrt{(1-\frac{4}{3}D^T)[(1-d)D^T\pi]^2 + \frac{d\{(6D^T\pi-\lvert\phi\rvert)\phi^2-[\lvert\phi\rvert-(1-2D^T)\pi]^3\}}{3\pi}}$
III	$\frac{{V_{\rm arm}}^2}{\omega L_s} d\phi(\pi-\lvert\phi\rvert)\left(\frac{1}{2\pi} - \frac{1-4D^T}{2\lvert\phi\rvert}\right)$	$\frac{V_{\rm arm}}{\omega L_s}\sqrt{(1-\frac{4}{3}D^T)[(1-d)D^T\pi]^2 + \frac{d\{(3\lvert\phi\rvert-2D^T\pi)(2D^T\pi)^2-[\lvert\phi\rvert-(1-2D^T)\pi]^3\}}{3\pi}}$
IV	$\frac{2{V_{\rm arm}}^2}{\omega L_s}\frac{\phi}{\lvert\phi\rvert} d\pi (D^T)^2$	$\frac{V_{\rm arm}}{\omega L_s}\sqrt{(1-\frac{4}{3}D^T)[(1-d)D^T\pi]^2 + \frac{d(3\lvert\phi\rvert-2D^T\pi)(2D^T\pi)^2}{3\pi}}$

TABLE II
ZVS CONDITION OF BATTERY-SIDE SWITCHES

Modes		S_1, S_3 when $\phi<0$ S_2, S_4 when $\phi\geq 0$	S_1, S_3 when $\phi\geq 0$ S_2, S_4 when $\phi<0$
$D\leq 0.5$	I	$d>\frac{D\pi-\lvert\phi\rvert}{D\pi}$	$d>1$
	II		$d>\frac{(1-D)\pi-\lvert\phi\rvert}{D\pi}$
	III	Always satisfied	
	IV		$d>1$
$D>0.5$	I	$d>1$	$d>\frac{(1-D)\pi-\lvert\phi\rvert}{(1-D)\pi}$
	II	$d>\frac{D\pi-\lvert\phi\rvert}{(1-D)\pi}$	
	III		Always satisfied
	IV	$d>1$	

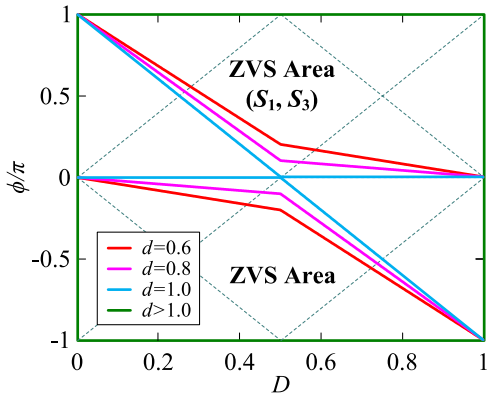

Fig. 5. ZVS boundaries of LVS upper switches.

TABLE III
ZVS CONDITION OF DC-SIDE SWITCHES

Modes		S_m when $\phi\geq 0$ or S_a when $\phi<0$	S_a when $\phi\geq 0$ or S_m when $\phi<0$
$D\leq 0.5$	I	$d<\frac{4\pi^2D^2(2-4D+m)}{m(2\pi D-\lvert\phi\rvert)^2}$	$d<\frac{4\pi^2D^2(2-4D+m)}{m(4\pi^2D^2-\phi^2)}$
	II	$d<\frac{4\pi^2D^2(2-4D+m)}{m[\pi^2-2\pi(2D+1)\lvert\phi\rvert+2\phi^2]}$	$d<\frac{4\pi^2D^2(2-4D+m)}{m[4\pi^2D-\pi^2-2\pi(2D-1)\lvert\phi\rvert-2\phi^2]}$
	III	$d<\frac{4\pi^2D^2(2-4D+m)}{m(\pi^2-4\pi^2D^2-2\pi\lvert\phi\rvert+\phi^2)}$	Always satisfied
	IV	Always satisfied	
$D>0.5$	I	$d<\frac{4\pi^2D(1-D)(4D-2+m)}{m[4\pi^2D(1-D)-4\pi\lvert\phi\rvert+\phi^2]}$	$d<\frac{4\pi^2D(1-D)(4D-2+m)}{m[4\pi^2D(1-D)-4\pi(D-1)\lvert\phi\rvert-\phi^2]}$
	II	$d<\frac{4\pi^2D(1-D)(4D-2+m)}{m[\pi^2-2\pi(2D+1)\lvert\phi\rvert+2\phi^2]}$	$d<\frac{4\pi^2D(1-D)(4D-2+m)}{m[4\pi^2D-\pi^2-2\pi(2D-1)\lvert\phi\rvert-2\phi^2]}$
	III	$d<\frac{4\pi^2D(1-D)(4D-2+m)}{m[4\pi^2D^2-3\pi^2-2\pi(2D-1)\lvert\phi\rvert+\phi^2]}$	$d<\frac{4\pi^2D(1-D)(4D-2+m)}{m[4\pi^2D(D-1)+3\pi^2-2\pi\lvert\phi\rvert-\phi^2]}$
	IV	Always satisfied	$d<\frac{D(4D-2+m)}{m}$

are symmetrical with respect to $\phi = 0$. Fig. 5 illustrates the ZVS boundaries for upper switches under different d, which are symmetrical to the point $(D, \phi) = (0.5, 0)$. A larger d will extend the ZVS area, and when $d > 1$, ZVS can be always achieved for LVS arm.

For HVS arms, the arm current comprises both ac and dc currents, making the ZVS conditions more complicated. As labeled on the upper and lower arm currents in Fig. 4(a), the ZVS conditions for the main and auxiliary switches in mode II when $\phi > 0$ are given in

$$\begin{cases} i_{s(t_0+\phi+2D^T\pi-\pi)} - i_{\mathrm{dc}(t_0+\phi+2D^T\pi-\pi)} < 0, & \text{for } \mathrm{S}_m, D \leq 0.5 \\ i_{s(t_0+\phi)} - i_{\mathrm{dc}(t_0+\phi)} < 0, & \text{for } \mathrm{S}_m, D > 0.5 \\ i_{s(t_0+\phi+\pi)} - i_{\mathrm{dc}(t_0+\phi+\pi)} > 0, & \text{for } \mathrm{S}_a, D \leq 0.5 \\ i_{s(t_0+\phi+2D^T\pi)} - i_{\mathrm{dc}(t_0+\phi+2D^T\pi)} > 0, & \text{for } \mathrm{S}_a, D > 0.5 \end{cases} \tag{4}$$

Similarly, the ZVS condition in other operation modes can be obtained, and the results are summarized in Table III. The ZVS boundaries of S_m and S_a are also symmetrical with respect to $\phi = 0$, and Fig. 6 plots the ZVS boundaries for S_m under different d and m, where m is the ratio of dc inductance and ac inductance, i.e., $m = L_{\mathrm{dc}}/L_s$. Like CF-DAB, the ZVS area will be extended with a smaller d; when $d < 1$, ZVS can be always maintained for $D < 0.5$. However, $d < 1$ will reduce the ZVS area of LVS arm. Therefore, $d = 1$ is preferred. The ZVS area will also increase when m decreases. Nevertheless, the smaller dc inductance may result in larger dc current ripple. Fortunately, as given in (2), the dc current ripple will not increase much for small dc inductor in MVDC application where D is

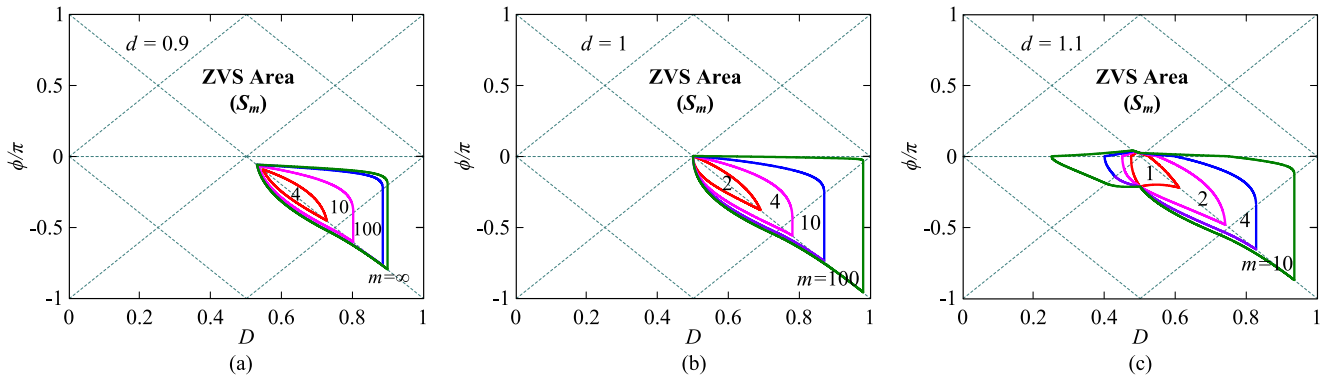

Fig. 6. ZVS boundaries of S_m under different d and m ($m = L_{\rm dc}/L_s$): (a) $d = 0.9$, (b) $d = 1$, and (c) $d = 1.1$.

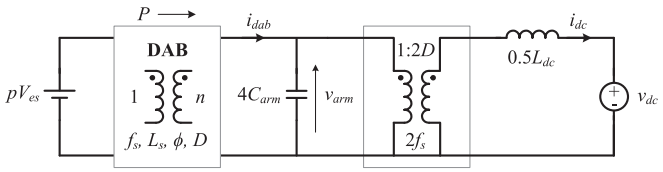

Fig. 7. Averaged circuit model of the CF-MDAB BESS converter.

around 0.5. For CF-MDAB in Fig. 2, $d = 1$ and $D_h, D_l < 0.5$ will ensure ZVS for switches of both side arms.

IV. Control System Design

In order to develop the control system, the averaged circuit model of the CF-MDAB converter is first derived. Based on the state-space equation, the system dynamics can be analyzed using small-signal model. Phase-shift angle is chosen to control the dc current, while duty cycle controls the arm average voltage. PI controllers are employed for both control loops, with additional notch filter inserted to suppress the intrinsic resonance between dc inductors and cell capacitors. The arm voltage balance model is also developed, and a phase-shift angle difference is introduced in upper and lower arms to realize arm voltage balance. The cell voltage and state-of-charge (SOC) balancing is implemented through the pulse width modulation (PWM) generation mechanism.

A. System Dynamics

Like CF-DAB, the CF-MDAB converter can be considered as a step-up converter cascaded with a DAB converter. The corresponding averaged circuit model for dc-grid integration is developed in Fig. 7, where the boost converter with equivalent capacitance and dc inductance features the current-fed port, and the $i_{\rm dab}$ determined by power equations in Table I represents the output current of DAB stage. To verify the developed averaged circuit model, both the circuit-based model and averaged circuit model are simulated in MATLAB/Simulink with the experimental parameters of a 3-kW prototype listed in Table IV. The step response results of the two models are compared in Fig. 8. The averaged model matches very well with the circuit-based model, demonstrating the validity of the derived model. Based on the developed averaged circuit model, the small-signal state-space equations can be derived in (A1)–(A3). Accordingly, the

TABLE IV
Circuit Parameters of the CF-MDAB BESS Converter Prototype

Items	Descriptions	Specifications
P_N	Rated power	3 kW
$V_{\rm es}$	Input voltage	125 V
$V_{\rm dc}$	HVS dc-link voltage	250 V
n	Transformer turns ratio	1
L_s	AC inductance	20 μH
$L_{\rm dc}$	DC inductance	100 μH
$C_{\rm sm}$	Cell capacitance	20 μF
$f_{\rm sw}$	Switching frequency	40 kHz
α_1, α_2	Dwell time	100 ns
[p, p']	Inserted submodule number under normal and dc fault condition	[2, 2]
S_1–S_4	Submodule MOSFETs	IRFP260N
S_L	Short-circuit IGBT	CM600HA-24A
R_L	Load resistor	18.17 Ω

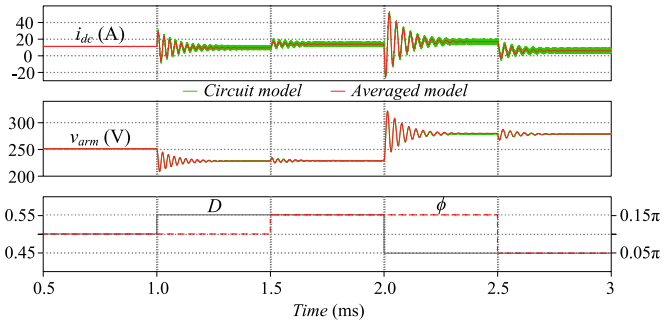

Fig. 8. Simulation waveform of CF-MDAB dynamics: Circuit model versus averaged model.

control-to-output transfer functions are derived in

$$G_{\rm idc\_d}(s) = \frac{4V_{\rm arm}C_{\rm arm}s + 2D(X - I_{\rm dc})}{L_{\rm dc}C_{\rm arm}s^2 + R_{\rm Ldc}C_{\rm arm}s + 2D^2} \tag{5}$$

$$G_{\rm varm\_\phi}(s) = \frac{Y\left(L_{\rm dc}s + R_{\rm Ldc}\right)}{4\left(L_{\rm dc}C_{\rm arm}s^2 + R_{\rm Ldc}C_{\rm arm}s + 2D^2\right)} \tag{6}$$

$$G_{\rm varm\_d}(s) = \frac{(X - I_{\rm dc})(L_{\rm dc}s + R_{\rm Ldc}) - 4DV_{\rm arm}}{2(L_{\rm dc}C_{\rm arm}s^2 + R_{\rm Ldc}C_{\rm arm}s + 2D^2)} \tag{7}$$

$$G_{\rm idc\_\phi}(s) = \frac{DY}{L_{\rm dc}C_{\rm arm}s^2 + R_{\rm Ldc}C_{\rm arm}s + 2D^2} \tag{8}$$

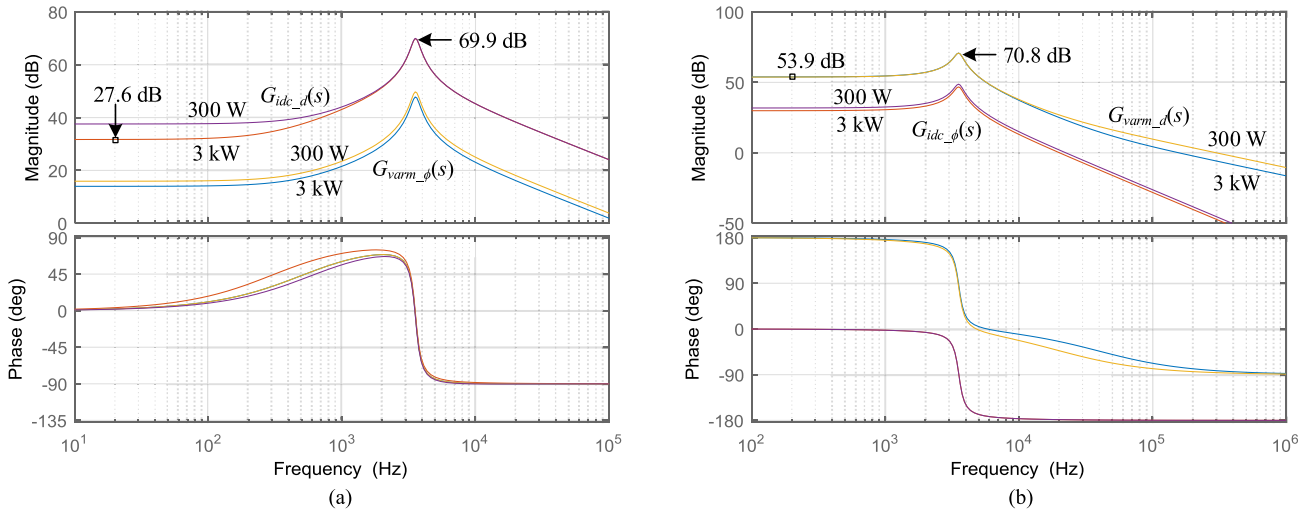

Fig. 9. Bode plots of CF-MDAB transfer functions: (a) $G_{\mathrm{idc\_}d}(s)$ and $G_{\mathrm{varm\_}\phi}(s)$, and (b) $G_{\mathrm{idc\_}\phi}(s)$ and $G_{\mathrm{varm\_}d}(s)$.

where R_{Ldc} is the equivalent series resistance (ESR) of the dc inductors, C_{arm} is the arm capacitance (i.e., $C_{\mathrm{arm}} = C_{\mathrm{sm}}/N$), *X*, *Y*, and *Z* are defined in A3. As a second-order system, the transfer functions have conjugated poles, and the natural frequency ω_n of the *LC* network is

$$\omega_n = \frac{\sqrt{2}D}{\sqrt{L_{\mathrm{dc}}C_{\mathrm{arm}}}}. \tag{9}$$

Since *D* is close to 0.5, ω_n is mainly determined by the *LC* parameters. With small passive components of CF-MDAB, ω_n may go close to control bandwidth, causing potential resonance issue. Based on the experimental parameters in Table IV, the bode plots of $G_{\mathrm{idc\_}d}(s)$, $G_{\mathrm{varm\_}\phi}(s)$, $G_{\mathrm{idc\_}\phi}(s)$, and $G_{\mathrm{idc\_}d}(s)$ under different load power when $D = 0.5$ are drawn in Fig. 9. As shown, the resonant frequency is around 3.6 kHz, which is close to 1/10 of the switching frequency. On the other hand, both $G_{\mathrm{idc\_}d}(s)$ and $G_{\mathrm{varm\_}\phi}(s)$ have low-frequency zeros, resulting in relatively low gain at the low-frequency range (see Fig. 9(a)). This makes it difficult for the controller design to achieve high bandwidth while maintaining sufficient suppression of the resonance. However, $G_{\mathrm{idc\_}\phi}(s)$ does not have zero, and the zero in $G_{\mathrm{varm\_}d}(s)$ is around switching frequency range, having a little effect on the system dynamics. Thereby, the controller design can be simplified.

B. Power Flow Control

In this paper, $G_{\mathrm{idc\_}\phi}(s)$ and $G_{\mathrm{varm\_}d}(s)$ are selected for the controller design, i.e., using ϕ and *D* to regulate i_{dc} and v_{arm}, respectively. Based on the derived small-signal model, the power flow control block diagrams are designed and shown in Fig. 10. $T_d(s)$ represents the delay effect in the control. $H_r(s)$ is the transfer function of the feedback filters, which in the experiment is a second-order Sallen–Key low-pass filter with the cutoff frequency around 30 kHz and *Q* factor of 0.707. $G_{c\phi}(s)$ and $G_{\mathrm{cd}}(s)$ are the compensators for dc current loop and arm average voltage loop, respectively, which are given in (10) and (11). PI controllers are implemented for both control loops; particularly, to suppress the intrinsic resonance of the *LC* network, notch filters are inserted in both loop at the resonant frequency ω_n

$$G_{c\phi} = \left(0.0033 + \frac{33\pi}{s}\right) \cdot \frac{s^2 + {\omega_n}^2}{s^2 + \omega_n s/Q + {\omega_n}^2} \tag{10}$$

$$G_{\mathrm{cd}}(s) = \left(-0.0001 - \frac{\pi}{s}\right) \cdot \frac{s^2 + {\omega_n}^2}{s^2 + \omega_n s/Q + {\omega_n}^2}. \tag{11}$$

The bode plots of the compensated loops at $V_{\mathrm{arm}} = 250\,\mathrm{V}$ and $P = 3\,\mathrm{kW}$ are shown in Fig. 11. The dc current loop has a cutoff frequency of 518 Hz, while the arm voltage loop has a bandwidth of 250 Hz. The notch filters cancel out the resonant peak of $G_{\mathrm{idc\_}\phi}(s)$ and $G_{\mathrm{varm\_}d}(s)$, providing a great attenuation for the potential resonance. Since ω_n is load independent, the notch filters are designed to work over the entire operation range.

C. Arm Voltage Balancing

There are two levels of arm voltage balancing: one is between the upper arms or the lower arms, the other is between the upper and lower arms. The arm voltage balancing between the upper arms or the lower arms is automatically achieved through the ac loop. Considering imbalance between the upper two arms, the resulted differential voltage will excite dc circulating current in the ac loop. The steady-state arm voltage error $\Delta V_{\mathrm{arm},p}$ depends on the ESR in ac loop and the required balancing current ΔI

$$\Delta V_{\mathrm{arm},p} = V_{\mathrm{arm,pa}} - V_{\mathrm{arm,pb}} = \Delta I \cdot \mathrm{ESR}_{\mathrm{ac}}/D. \tag{12}$$

As the ESR is quite small, the arm voltage error is very small compared to arm voltage which can be neglected. Since the current flows through the transformer, the balancing dynamics is mainly determined by the magnetizing inductance. As fast dynamics is not required, no extra control is necessary for balancing the upper or lower arms.

The balancing control between the upper and lower arm voltages is required. Generally, there are two balancing strategies

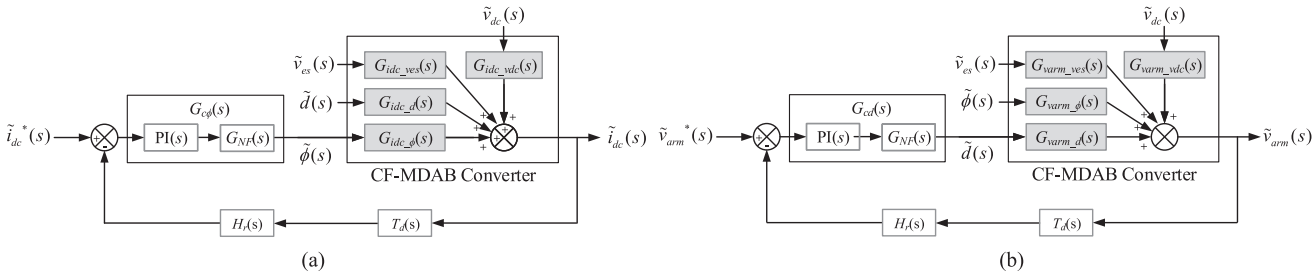

Fig. 10. Control block diagrams of the CF-MDAB converter: (a) DC current control, and (b) averaged arm voltage control.

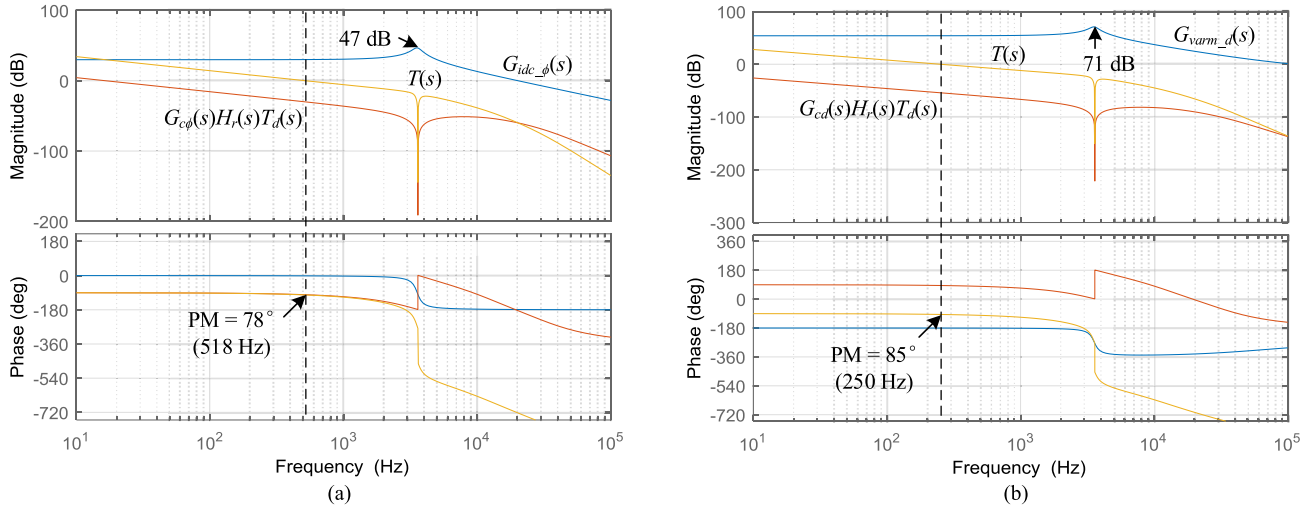

Fig. 11. Bode plots of CF-MDAB control loops at $V_{\rm arm} = 250\,\text{V}$, $P = 3\,\text{kW}$: (a) DC current loop, and (b) averaged arm voltage loop.

based on dc circulating current and ac circulating current, respectively. The method based on ac circulating current is load independent, thus simpler and more reliable. In order to generate the ac circulating current, phase-shift angles with a slight difference can be applied for upper arms and lower arms. The induced $\Delta\phi$ will excite ac circulating current in the arms which redistributes the ac power in upper and lower arms, thus balancing the arm voltage. The phase-shift angle of the upper and lower arms can be rewritten as

$$\begin{cases} \phi_p = \phi + \Delta\phi/2 \\ \phi_n = \phi - \Delta\phi/2 \end{cases}. \tag{13}$$

The equivalent circuit of arm voltage balancing with ac circulating method is shown in Fig. 12, where the CF-MDAB BESS converter is divided into three subcircuits: A, P, and N, and any two subcircuits with the equivalent ac inductor can be considered as a DAB (see Fig. 12(a)). The arm voltage balancing performance is determined by the nonisolated DAB_{PN}, of which the equivalent circuit is illustrated in (b). The equivalent DAB current $i_{\rm dab}$ and dc load current $i_{\rm load}$ are equally distributed in upper arms and lower arms. $R_{\rm eq}$ represents the power loss in the circuit corresponding to ESR in the loop. Based on the equivalent circuit, the transfer function from $\Delta\phi$ to the average arm voltage difference in upper and lower arms $\Delta v_{{\rm arm},pn} = v_{{\rm arm},p} - v_{{\rm arm},n}$ is expressed in (14), which is further simplified since the required $\Delta\phi$ for arm voltage balancing is very small and D is close to 0.5

$$\begin{aligned} &G_{\Delta V\,{\rm arm}pn\_\Delta\phi}(s) \\ &= \begin{cases} -\frac{V_{\rm arm}}{\omega L_{\rm dc}(2C_{\rm arm}s+1/R_{\rm eq})}\left(2D_T - \frac{|\Delta\phi|}{\pi}\right), & \text{Mode I} \\ -\frac{V_{\rm arm}}{\omega L_{\rm dc}(2C_{\rm arm}s+1/R_{\rm eq})}\left(1 - \frac{|\Delta\phi|}{2\pi}\right), & \text{Mode II} \end{cases} \\ &\approx -\frac{V_{\rm arm}}{\omega L_{\rm dc}(2C_{\rm arm}s+1/R_{\rm eq})}. \end{aligned} \tag{14}$$

The dynamics of DAB_{PN} for arm voltage balancing behaviors like a capacitor. A simple PI controller can be implemented for achieving voltage balancing in upper and lower arms since fast dynamic is not necessary here.

D. Cell Voltage and SOC Balancing

The cell voltage and SOC balancing for CF-MDAB are realized through sorting algorithm, which is embedded in the Q3L PWM generation block illustrated in Fig. 13. With the obtained control variables, the arm-level driving signals PWM_h and PWM_l are generated using the proposed three-level modulation method. These signals are then sent to Q2L PWM sequence generation for the corresponding arm, which applies multiple phase-delay units.

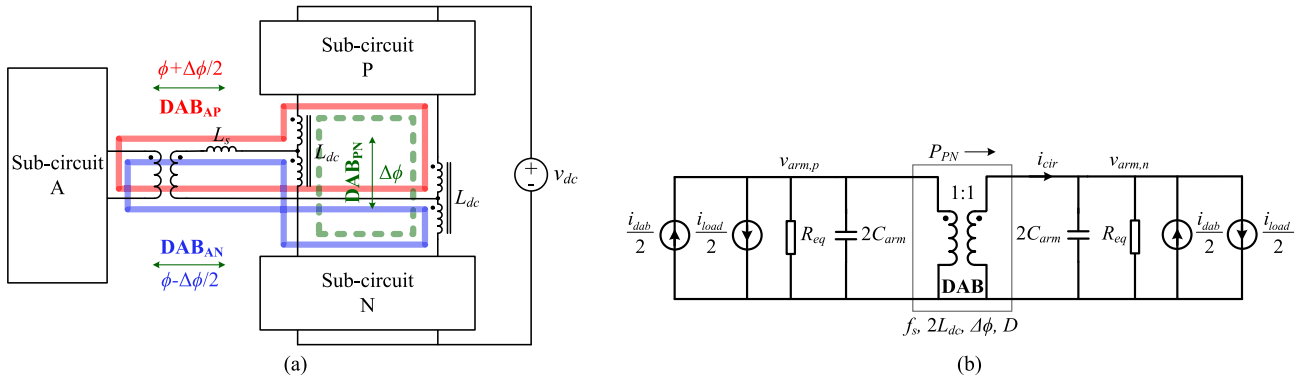

Fig. 12. Equivalent circuit of the CF-MDAB converter for arm voltage balancing: (a) DAB circuit loops, and (b) averaged circuit model.

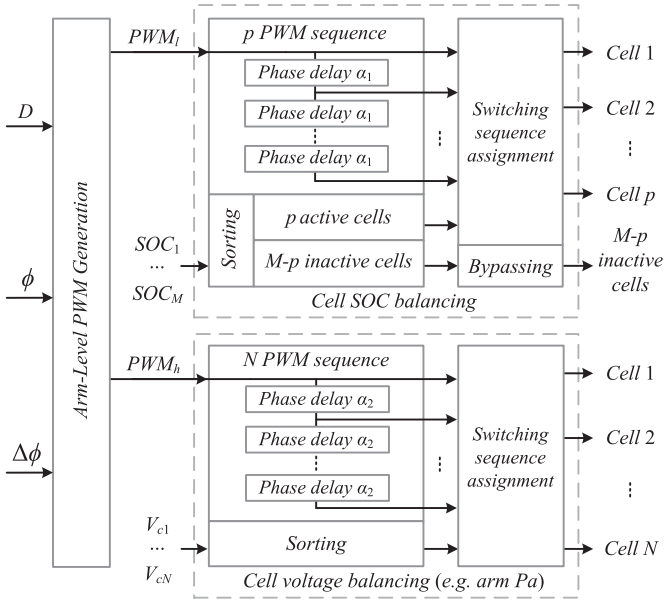

Fig. 13. Q3L PWM generation with cell SOC and voltage balancing.

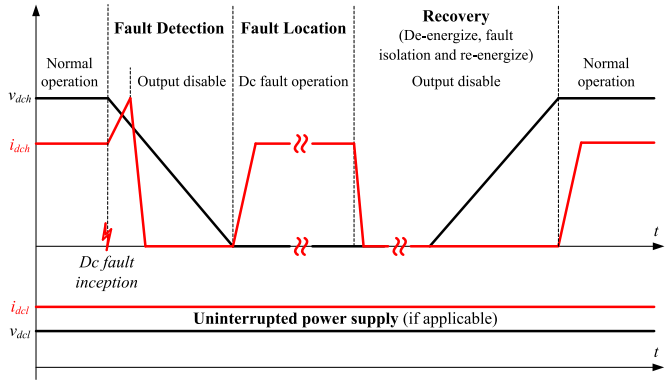

Fig. 14. DC FRT operation process of the CF-MDAB converter in a breaker-less MVDC system.

To balance the cell voltage, the N submodules inside a HVS arm are sorted by voltage in ascending or descending order, and then paired with the N PWM sequence. The slight phase difference of α_2 will cause power difference in each cell, which serves balancing purpose. The SOC information of LVS battery units are collected from the battery management system, and sorting algorithm is used to determine M-p submodules with lowest SOC during discharging or with highest SOC during charging. These selected submodules are bypassed from charging or discharging, thus balancing the cell SOCs. The p inserted FBSMs are paired with p Q2L PWM sequence. With redundant cells in "$N+1$" or "$N+2$" configuration, the cell voltage and SOC balancing capability can be significantly improved.

V. DC FRT Operation

To enable dc FRT operation, the modulation has to be adapted accordingly, resulting in different system dynamics and control strategies. Unlike normal operation, the duty cycle D is used to control the dc current, while the phase-shift angle ϕ controls the arm average voltage. Since the upper arms or lower arms are no longer autobalanced under dc fault operation, additional arm balancing control is designed to achieve voltage balancing.

A. DC FRT Operation Process

Based on the dc fault clearance process in [14], a general dc FRT operation period of the CF-MDAB converter is illustrated in Fig. 14, with the HVS dc fault as an example. It consists of three stages: dc fault detection, dc fault location, and recovery. When a dc fault occurs, the dc fault current rises quickly due to the dc bus voltage drop. Once the dc current exceeds the threshold, the dc fault is detected triggering the dc FRT operation. In the first stage, the fault-side CF-Q3LC is disabled by blocking the gating signal to avoid excessive ripple current because of the small dc inductors, and the dc current decreases very quickly to zero. When the dc voltage is below the threshold, the CF-Q3LC starts the dc fault operation mode, providing continuous dc fault current per request to assist the fault segment location. After the fault is located, the converter disables again to deenergize the system for isolating the fault segment. Once the dc bus has been restored, the converter switches back to normal operation mode. During the dc FRT process, the nonfault-side CF-Q3LC can provide uninterrupted power supply to loads. To decouple

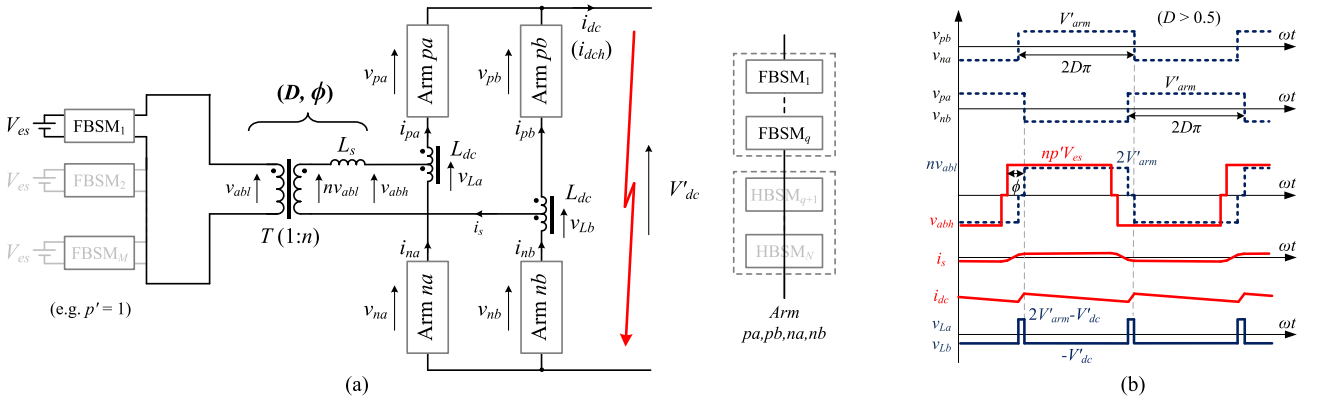

Fig. 15. DC fault operation of the CF-MDAB BESS converter: (a) Schematic, and (b) voltage and current waveforms.

the operation of two CF-Q3LCs during the fault, the legs in a CF-Q3LC can operate in phase instead of interleaving, which also realizes autobalancing of the upper or lower arms. When CF-MDAB converter is used for BESS application, the battery side can be simply disabled, or operated coordinately to support the dc-side CF-Q3LC during the fault as adopted in this paper.

B. DC Fault Operation Mode for BESS Converter

The operation principle of CF-MDAB-based BESS under dc fault is similar to that of normal operation, but with reduced arm output voltage. Fig. 15(a) illustrates the dc fault operation mode of CF-MDAB-based BESS and (b) depicts the typical operating waveforms, where " $'$ " denotes the dc fault condition for the variables. Under normal operation, the HVS FBSMs are modulated in half-bridge mode with one leg always bypassed. Under dc fault operation mode, all the HBSMs are bypassed and the FBSMs start operating in full-bridge mode with ± 2L output. As a result, the ac voltage is reduced to $2qV_c$. Correspondingly, the LVS ac voltage is matched by lowering the inserted submodule number p'. With the upper and lower arm 180° phase shifted, the averaged dc output voltage is determined by duty cycle D. Through duty cycle regulation, the dc fault current can be controlled. The relation between the dc fault voltage $V'_{\rm dc}$ and the averaged arm voltage $V'_{\rm arm}$ is given in (15). For $V'_{\rm dc} = 0$, D will be 0.5 regardless of $V'_{\rm arm}$

$$V'_{\rm dc} = (2D-1)\,V'_{\rm arm}. \tag{15}$$

C. System Dynamics

The averaged circuit model of CF-MDAB under dc fault operation mode is depicted in Fig. 16, where the arm capacitor now includes only the inserted FBSM cell capacitors (i.e., $C'_{\rm arm} = C_{\rm sm}/q$), and the dc grid under fault is modeled as a voltage source. As shown in Fig. 16, the equivalent circuit is the same as that in Fig. 7 at normal operation mode but with different parameters, thereby the small-single model can be obtained by modifying (A1)–(A3) accordingly. Since D is independent of the arm voltage under dc fault, it is selected for dc fault current control. The corresponding control-to-output transfer functions

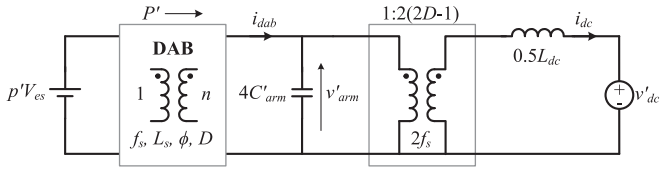

Fig. 16. Averaged circuit model of the CF-MDAB under dc fault operation mode.

are given as

$$G'_{\rm idc\_d}(s) = \frac{8V'_{\rm arm}C'_{\rm arm}s + 2\,(2D-1)\,(X' - 2I_{\rm dc})}{L_{\rm dc}C'_{\rm arm}s^2 + R_{\rm Ldc}C'_{\rm arm}s + 8D^2 - 8D + 2} \tag{16}$$

$$G'_{\rm varm\_\phi}(s) = \frac{Y'\,(L_{\rm dc}s + R_{\rm Ldc})}{4\,(L_{\rm dc}C'_{\rm arm}s^2 + R_{\rm Ldc}C'_{\rm arm}s + 8D^2 - 8D + 2)}. \tag{17}$$

The natural frequency ω'_n of LC network under dc fault operation is

$$\omega'_n = \frac{\sqrt{2}\,|2D-1|}{\sqrt{L_{\rm dc}C'_{\rm arm}}}. \tag{18}$$

As D is around 0.5, ω'_n is or close to zero under dc fault operation regardless of the LC parameters, such that it has a little effect on the system dynamics and can be ignored. Actually, with $D = 0.5$, the zero and pole in (16) and (17) will cancel out each other, resulting a first-order system.

D. Control System Design

Based on the small-signal model, the power flow control block diagrams are derived in Fig. 17. $G'_{\rm cd}(s)$ and $G'_{c\phi}(s)$ are the compensators for dc current loop and arm average voltage loop, respectively. As the converter is expected to provide dc fault current for fault location right after dc fault occurrence, fast response is required for the current control loop; while the dynamic of the arm voltage loop is not critical since only circulating power exists in the converter under dc fault operation. Based on the experimental circuit parameters of Table IV, PI compensators $G'_{\rm cd} = 0.002 + 1.2\pi/{\rm s}$ and $G'_{c\phi} = 0.005 + 0.1\pi/{\rm s}$

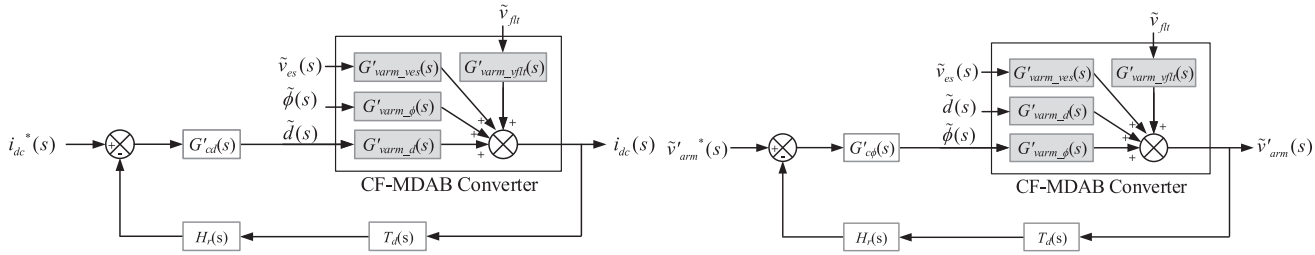

Fig. 17. Control block diagrams of the CF-MDAB under dc fault operation mode: (a) DC current control, and (b) averaged arm voltage control.

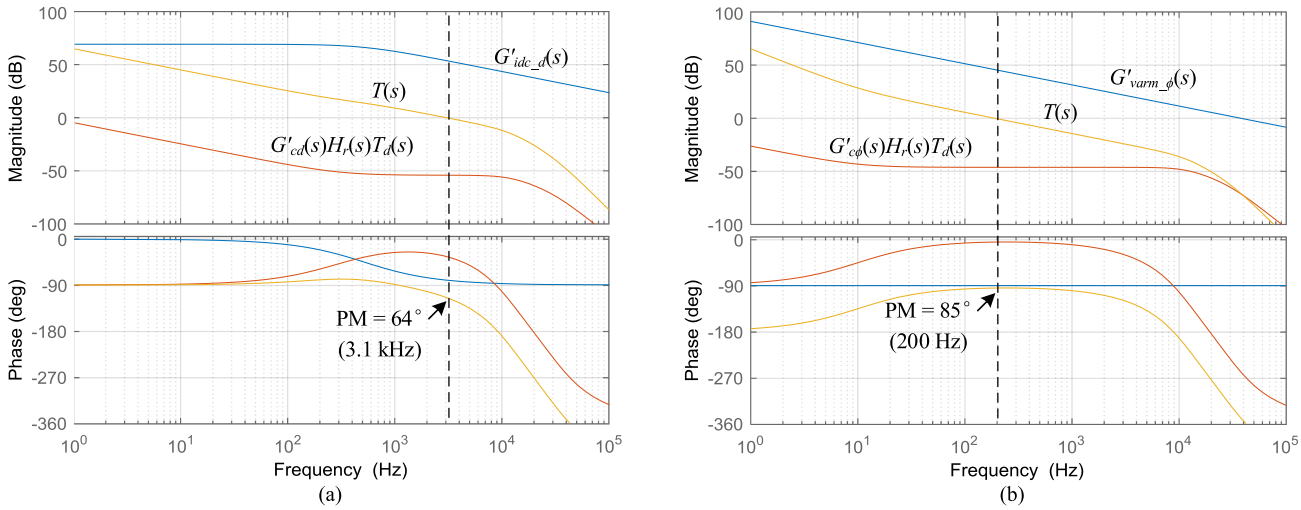

Fig. 18. Bode plots of CF-MDAB control loops under dc fault operation mode with $V'_{\rm arm} = 125\,{\rm V}$, $V'_{\rm dc} = 0$, $I_{\rm dc} = 12\,{\rm A}$: (a) DC current loop, and (b) averaged arm voltage loop.

are implemented for the dc current and arm voltage control loops. The bode plots are depicted in Fig. 18, with $V_{\rm es} = 125\,{\rm V}$, $V'_{\rm dc} = 0$ and $I_{\rm dc} = 12\,{\rm A}$. The dc current loop has a cutoff frequency of 3.1 kHz, while the arm voltage loop has a bandwidth of 200 Hz.

E. Arm Voltage Balancing

Under dc fault operation mode, the autobalancing of the upper two arms or low two arms cannot be achieved in the fault-side CF-Q3LC, since (12) is revised as

$$\left(V'_{\rm arm,pa} - V'_{\rm arm,pb}\right)(2D-1) = \Delta I \cdot {\rm ESR}_{\rm ac}. \tag{19}$$

As long as $D = 0.5$, no dc circulating current would be generated in the ac circuit, no matter how much the voltage difference in the arms. Therefore, additional balance control has to be implemented. To achieve voltage balancing of four arms, three constraints need to be satisfied. A feasible set of constraints can be

$$\begin{aligned}\Delta V'_{\rm arm,pn} &= \left(V'_{\rm arm,pa} + V'_{\rm arm,pb}\right) - \left(V'_{\rm arm,na} + V'_{\rm arm,nb}\right)\\ &= 0 \end{aligned} \tag{20}$$

$$\begin{aligned}\Delta V'_{{\rm arm},ab} &= \left(V'_{\rm arm,pa} + V'_{{\rm arm},na}\right) - \left(V'_{\rm arm,pb} + V'_{{\rm arm},nb}\right)\\ &= 0 \end{aligned} \tag{21}$$

$$\Delta V'_{{\rm arm},a} = V'_{\rm arm,pa} - V'_{\rm arm,na} = 0. \tag{22}$$

Generally, dc circulating currents can be utilized to fulfill (20)–(22), by introducing duty cycle difference in arms. The duty cycle difference will produce dc output power difference in arms which balances the arm voltages. Particularly, for CF-MDAB BESS converter, (20) can be satisfied with ac circulating current by $\Delta\phi$ regulation, and (21), (22) can be satisfied with the duty cycle for each arm adjusted as

$$\begin{cases} D_{pa} = D + {\rm sgn}(I_{\rm dc}) \cdot (\Delta D_{\rm ab} + \Delta D_a)/2 \\ D_{na} = D + {\rm sgn}(I_{\rm dc}) \cdot (\Delta D_{\rm ab} - \Delta D_a)/2 \\ D_{pb} = D_{nb} = D - {\rm sgn}(I_{\rm dc}) \cdot \Delta D_{\rm ab}/2 \end{cases} \tag{23}$$

where $\Delta D_{\rm ab}$ is the phase duty cycle difference used to balance the two legs, and ΔD_a is the arm duty cycle difference used to balance two arms in leg a. With the small cell capacitance of CF-MDAB, fast response is required for adapting with the dc current direction, thus only the proportional controller is used. In the experiment, instead of using current direction to determine the polarity of $\Delta D_{\rm ab}$ and ΔD_a, an autonomous algorithm based on hysteresis control is implemented to avoid the sensing error and the impact of the ac current when the dc current is low. $K_p = 0.001$ and $K_p = 0.002$ are applied for $\Delta D_{\rm ab}$ and ΔD_a controls, respectively.

VI. Experimental Results

The experimental setup of a downscaled 3-kW CF-MDAB BESS hardware testbed is shown in Fig. 19, with detailed cir-

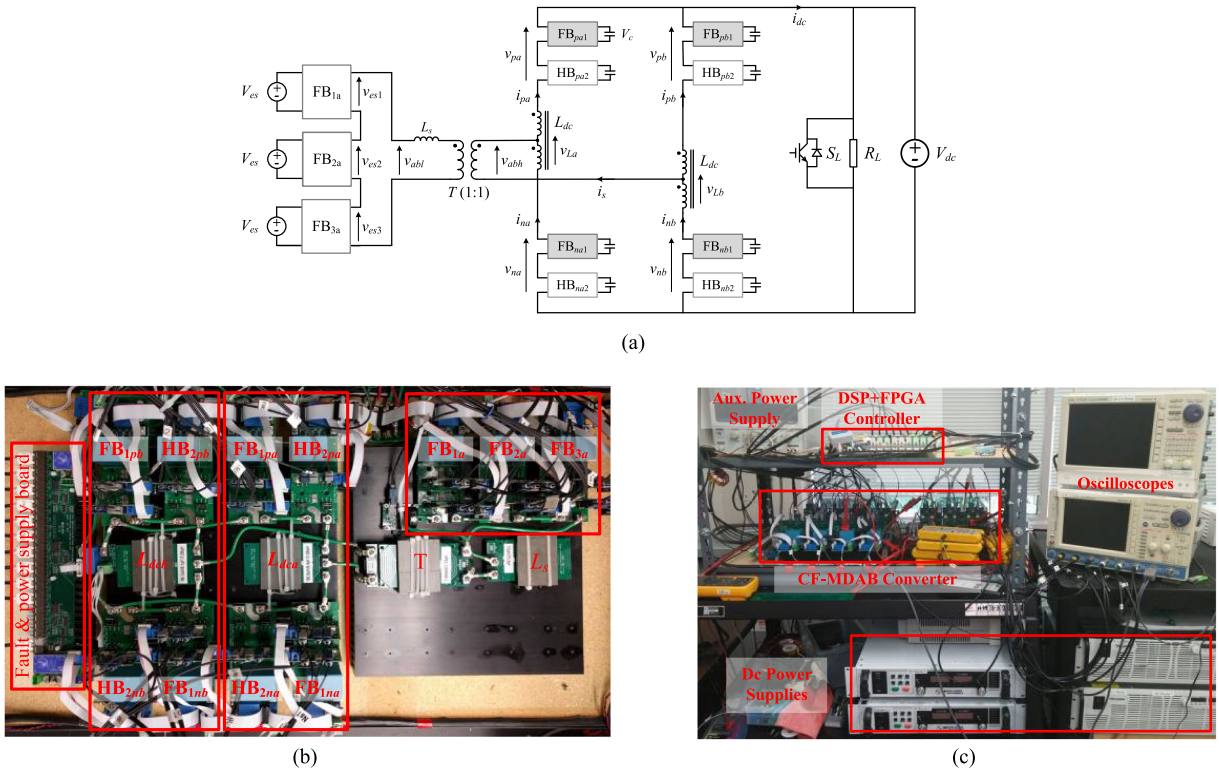

Fig. 19. Experiment setup of 3-kW CF-MDAB BESS converter: (a) Schematic, (b) CF-MDAB prototype, and (c) testbed setup.

cuit parameters listed in Table IV. The switching frequency is selected as 40 kHz considering the tradeoff between efficiency and power density. The dc bus is emulated using a dc power supply paralleled with resistive loads. In the experiment, the battery units are represented by isolated dc power supplies for conceptual verification. A 1200-V 600-A insulated-gate bipolar transistor (IGBT) is used to create dc short-circuit scenario. Experimental results under discharging mode are provided for validation.

Fig. 20 shows steady-state operating waveforms with different dc current at $V_{\rm dc} = V_{\rm arm} = 250\,{\rm V}$ and $V_{\rm es} = 125\,{\rm V}$. The current flowing through the auxiliary switch is only the ac ripple current which is much smaller than that of the main switch. The dc current ripple is very small with D around 0.5, as the arm average voltage is set as the dc bus voltage. In HVS, ZVS is achieved for the main switches under different load conditions, while partial hard switching is observed for auxiliary switches at low power due to insufficient energy stored in the ac inductor, as shown in (c). In LVS, ZVS is achieved for the upper switches over a wide operation range, while hard switching is observed for the lower switches at medium to low load power. This is because the effective d is less than 1 due to the voltage drop on the ESR in the ac loop, although the LVS and HVS arm voltages are both 250 V. As analyzed, $d < 1$ will result in a nonflat-top ac current, which helps HVS arms to achieve ZVS but makes more difficult for ZVS operation in the LVS arm. Staircase waveforms can be clearly observed in the voltages, where the dwell time is labeled. The ac voltage waveforms are somehow distorted at light load, with unsymmetrical duty cycles in LVS and HVS. This is mainly because of the dead time effect ($t_d \sim 300\,{\rm ns}$). Under partial ZVS operation at light load, the dead time will reduce the effective duty cycle. With closed-loop compensation in HVS, this dead time effect all reflects in the LVS voltage waveforms. Resulting from the reduced LVS effective duty cycle, the ac current is forced for earlier commutation, which makes it difficult for LVS arm but easy for HVS arms to achieve full ZVS operation.

Fig. 21 illustrates the cell SOC balancing and the formation of LVS Q3L output voltage. To achieve SOC balancing, one of the three battery units is bypassed in each switching. For demonstration, the bypassed FBSM is rotated among the submodules every two switching cycles. As shown, the transit of inserting or bypassing submodule is seamless and transparent for the ac voltage of transformer. With full ZVS of LVS switches, the Q3L ac voltage waveforms are exactly as expected with a dwell time α_1 between the leading and lagging submodule.

Fig. 22 presents the measured efficiency curve when $V_{\rm dc} = V_{\rm arm} = 250\,{\rm V}$ and $V_{\rm es} = 125\,{\rm V}$. A peak efficiency of 95.8% is achieved at around 1.7 kW, and the full load efficiency is 94.2%.

Fig. 23 shows the dc current and arm voltage waveforms with and without notch filters. Before notch filter is enabled, large resonance can be observed, especially in the dc current. Due to the capacitor tolerance and stray parameters, the resonant frequency is about 3.3 kHz in experiment instead of 3.6 kHz as calculated. After the notch filters are enabled, the resonance is attenuated immediately and no obvious resonance can be observed, demonstrating the effectiveness of the notch filter.

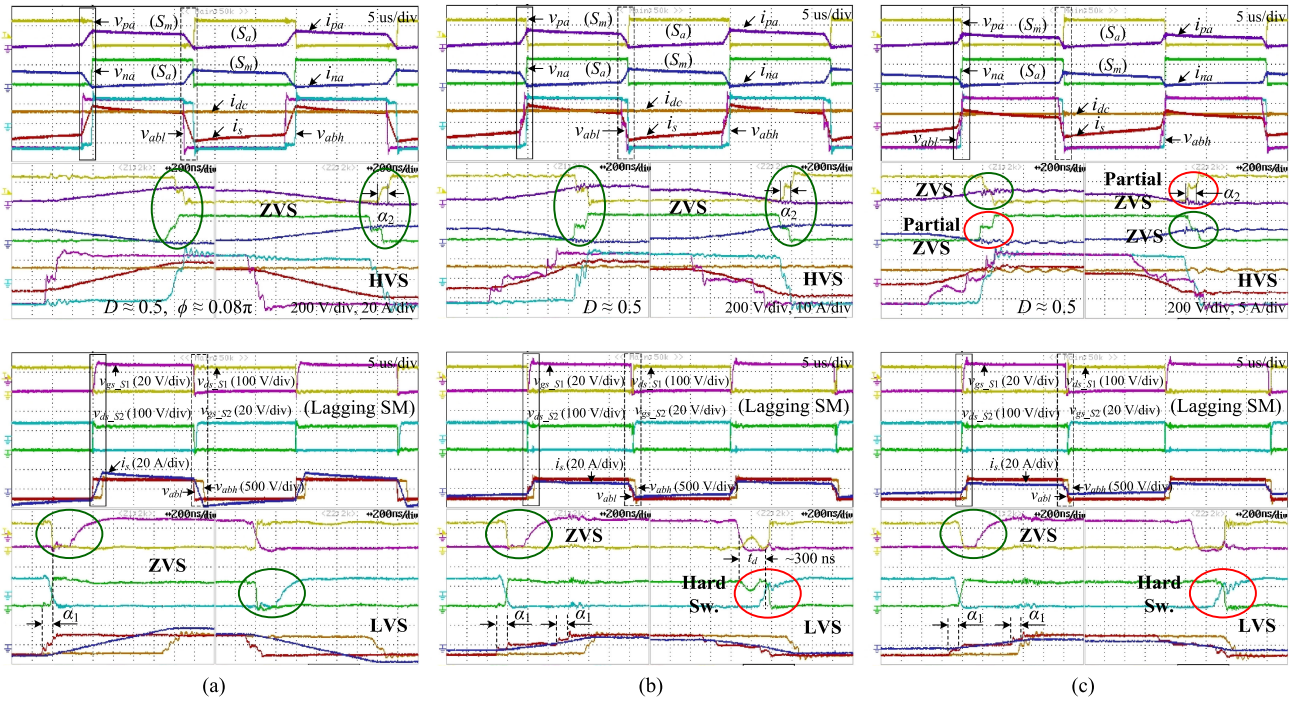

Fig. 20. Operating waveforms of the CF-MDAB converter under different load at $V_{\rm dc} = V_{\rm arm} = 250\,{\rm V}$, $V_{\rm es} = 125\,{\rm V}$: (a) $I_{\rm dc} = 12\,{\rm A}$ (100% load), (b) $I_{\rm dc} = 6\,{\rm A}$ (50% load), and (c) $I_{\rm dc} = 2\,{\rm A}$ (17% load).

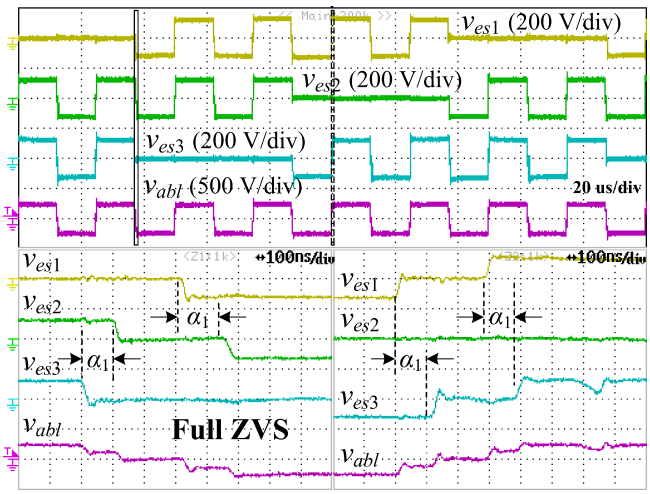

Fig. 21. Cell SOC balancing at $V_{\rm dc} = V_{\rm arm} = 250\,{\rm V}$, $V_{\rm es} = 125\,{\rm V}$, $I_{\rm dc} = 12\,{\rm A}$.

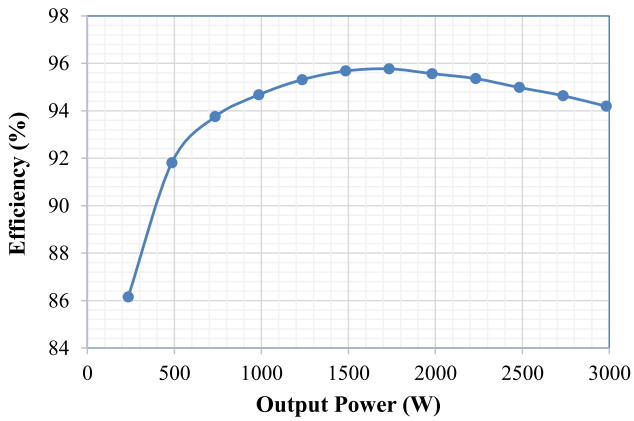

Fig. 22. Efficiency curves of the CF-MDAB converter at $V_{\rm dc} = V_{\rm arm} = 250\,{\rm V}$, $V_{\rm es} = 125\,{\rm V}$.

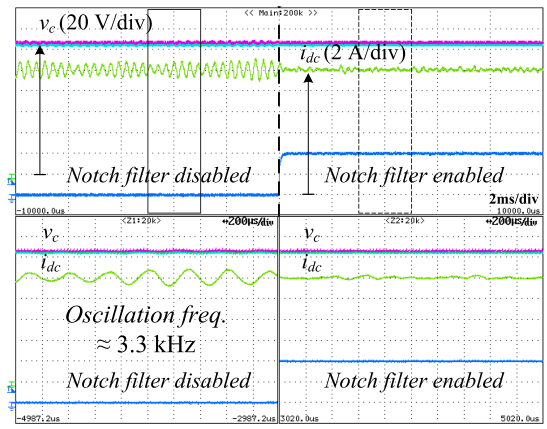

Fig. 23. Resonance attenuation with notch filter at $V_{\rm arm} = V_{\rm dc} = 250\,{\rm V}$, $V_{\rm es} = 125\,{\rm V}$, $I_{\rm dc} = 12\,{\rm A}$.

The system dynamics are shown in Fig. 24 with step load change. In (a), the output power has a step change from zero to full power, while in (b), the output power has a step change from full power to zero. The dc current in both case response quickly, taking about 1 ms to completely follow the reference. The arm voltage has similar dynamics as the dc current. During the transient, the voltage variation on capacitor is less than 5 V, and the capacitor voltages are well balanced. It can be noted that the cell capacitor voltage inside arms are slightly unbalanced when the power is low. About 5 V difference can be observed in some arms at zero load (see Fig. 24(a)). This is because the cell voltage balancing capability depends on the load current.

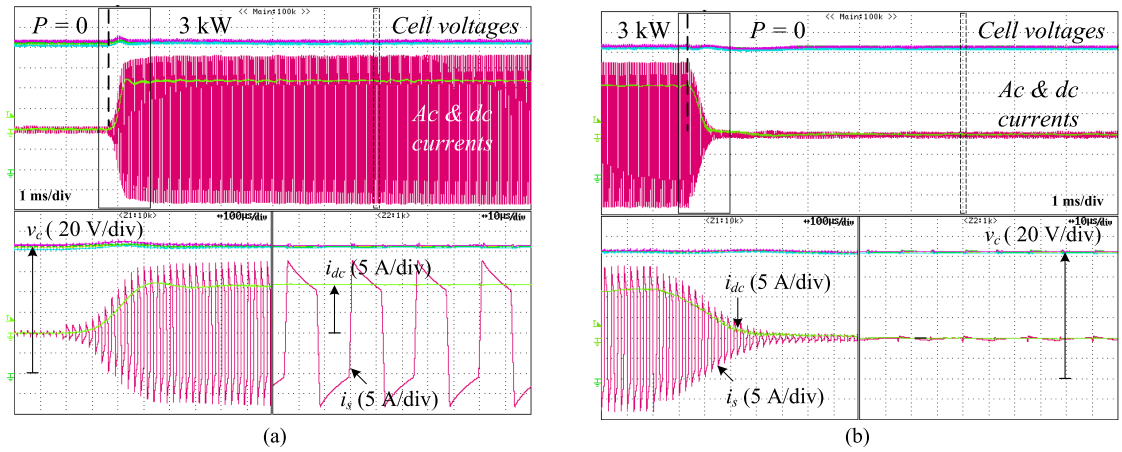

Fig. 24. Dynamic response of the CF-MDAB converter with step $i^*_{\rm dc}$ change at $V_{\rm dc} = V_{\rm arm} = 250$ V, $V_{\rm es} = 125$ V: (a) 0 to 12 A, and (b) 12 A to 0.

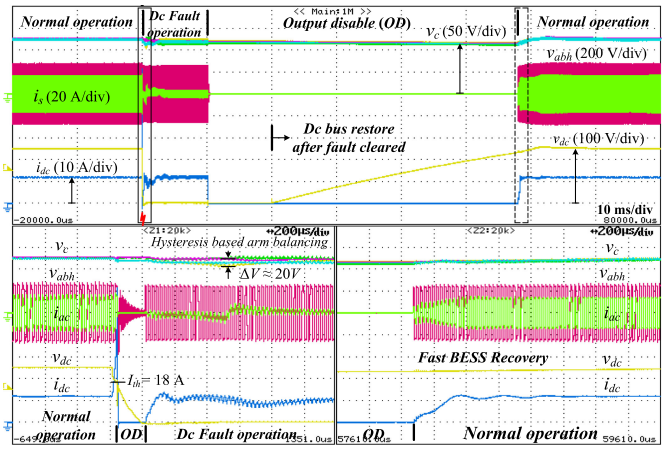

Fig. 25. DC FRT operation of the CF-MDAB BESS converter at $V_{dc} = V_{arm} = 250$ V, $V_{es} = 125$ V, $I_{dc} = 12$ A.

When the load is very light, it cannot provide enough power during the short dwell time to balance the cell voltage. With the redundancy cells in real applications, the cell voltage balancing capability can be significantly improved since the balancing can be performed over the full switching cycle.

Fig. 25 illustrates the dc FRT operation of the CF-MDAB BESS converter, with substages labeled according to Fig. 14. When fault happens, a voltage dip shows up immediately on the dc voltage due to the *di/dt* associated with the rising of fault current. With the sudden voltage drop applied on the dc inductors, the dc current $i_{\rm dc}$ rises quickly, reaching the threshold of 18 A. However, as no additional fast dc fault detection circuit is implemented, this fault current can be only detected by the current sampling performed each switching cycle, resulting a maximum one cycle delay in the dc fault detection. Around 30 μs after the fault inception, the dc fault is detected, the converter is disabled immediately and $i_{\rm dc}$ decrease to zero within microseconds. Due to the delay in dc fault detection, the peak dc current in the experiment is much higher than the threshold, causing saturation in dc inductors. This large dc fault current causes slightly voltage unbalance in the arms, including the FB-SMs. The converter is kept in output disable mode until the dc voltage $v_{\rm dc}$ drops below a certain threshold that is safe for dc fault operation. During this time, parasitic ringing among HVS arms occurs to dump the residual energy stored in the loop inductance. At $t \approx 175$ μs, the dc voltage is detected below the threshold of 25 V, and the converter switches to dc fault operation mode after a switching cycle delay. With the designed duty cycle control, the dc current is regulated to the preset value at 12 A with fast response. The average cell voltage of FBSMs is regulated to follow the average cell voltage of the bypassed HB-SMs through phase-shift control such that the transient in arm voltage control is minimized. Meanwhile, the arm voltage balancing control is performed. In the first 500 μs, the arm voltage (i.e., v_c since $q = 1$) diverges due to the opposite initial polarity in ΔD_a regulation, and a maximum 20-V voltage difference is observed. At $t \approx 700$ μs, the hysteresis-based autonomous algorithm corrects the polarity, and the arm voltage converges quickly. As can be seen from the ac current i_s, the ΔD_a regulation actually generates dc circulating current in the ac loop to balance the upper and lower arms within a leg. Under dc fault operation mode, the switching ripple of the cell capacitor voltage is much higher compared to that of normal operation mode since all the load current flows through the capacitors. After providing dc fault current for 10 ms, the converter is disabled again and $i_{\rm dc}$ decreases quickly to zero. At $t \approx 20$ ms, the dc fault was cleared by turning off S_L, and the bus voltage starts to restore with the intrinsic characteristics of the dc power supply. At $t \approx 58$ ms, the dc bus voltage reaches the arm voltage and the converter switche back into normal operation. The dc current is restored in half a millisecond, while the arm voltage increases with the dc bus voltage and finally settles to the reference.

VII. Conclusion

This paper proposed a new type of IM2DC, the CF-MDAB concreter, which combines the advantages of both DAB-based and MMC-based dc–dc converters, i.e., the soft-switching operation, small passive components, and the dc FRT capability. The dynamics of DAB-based converters are simple, yet they have no direct dc current control capability. Although the MMC-based

IM2DC converter has superior current control capability, it has high system order, multiple control variables, and strong coupling of dc- and ac-side dynamics. As a result, the derivation of mathematical model is complicated and a control system design becomes difficult. The proposed converter can be treated as a variant of CF-DAB; therefore, the modeling method of CF-DAB can be applied to CF-MDAB to derive accurate dynamic models and design control system at both normal and dc fault operation modes. Moreover, the modulation method, soft-switching condition, and the arm voltage balancing strategy of CF-MDAB are also based on the concept/analysis of CF-DAB. The proposed converter not only can be utilized as a BESS but also a dc transformer for MVDC applications when a dc fault current control capability of the converter is required or preferred.

APPENDIX

State-space equations for the small-signal model of CF-MDAB converter

$$\begin{cases} \dot{\tilde{x}} = A\tilde{x} + B\tilde{u} \\ y = \tilde{x} \end{cases}, \quad \begin{cases} x = [i_{\rm dc}, v_{\rm arm}]^T \\ u = [D, \phi, v_{\rm dc}, v_{\rm es}]^T \end{cases} \tag{A1}$$

$$A = \begin{bmatrix} \frac{-R_{\rm Ldc}}{L_{\rm dc}} & \frac{4D}{L_{\rm dc}} \\ \frac{-D}{2C_{\rm arm}} & 0 \end{bmatrix} B = \begin{bmatrix} \frac{4V_{\rm arm}}{L_{\rm dc}} & 0 & -\frac{2}{L_{\rm dc}} & 0 \\ \frac{X-I_{\rm dc}}{2C_{\rm arm}} & \frac{Y}{4C_{\rm arm}} & 0 & \frac{Z}{4C_{\rm arm}} \end{bmatrix} \tag{A2}$$

where

$$X = \begin{cases} \operatorname{sgn}(0.5-D)\,\phi n p V_{\rm es}/\omega L_s, & \text{Mode I} \\ \operatorname{sgn}[\phi(0.5-D)]\left(1-2D^T\right)\pi n p V_{\rm es}/\omega L_s, & \text{Mode II} \end{cases}$$

$$Y = \begin{cases} \left(2D^T\pi - |\phi|\right) n p V_{\rm es}/\pi\omega L_s, & \text{Mode I} \\ (\pi - 2|\phi|)\, n p V_{\rm es}/\pi\omega L_s, & \text{Mode II} \end{cases}$$

$$Z = \begin{cases} np\phi\left(4\pi D^T - |\phi|\right)/2\pi\omega L_s, & \text{Mode I} \\ \frac{np\left[2\phi(\pi-|\phi|)-\operatorname{sgn}(\phi)\left(1-2D^T\right)^2\pi^2\right]}{2\pi\omega L_s}, & \text{Mode II} \end{cases}. \tag{A3}$$

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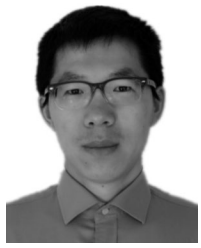

Yuxiang Shi (S'13–M'17) received the B.S. degree in electrical engineering from Xi'an Jiaotong University, Xi'an, China, in 2007, the M.S. degree in electrical engineering from Zhejiang University, Hangzhou, China, in 2010, and the Ph.D. degree in electrical engineering from Florida State University, Tallahassee, FL, USA, in 2016.

From 2010 to 2011, he was an Electrical Engineer with Philips Lighting Electronics, Shanghai, China. Since November 2016, he has been a Research Scientist with ABB Corporate Research Center, Raleigh, NC, USA. His current research interests include widebandgap devices and their applications in renewables, battery energy storages, and motor drives.

Hui Li (S'97–M'00–SM'01) received the B.S. and M.S. degrees in electrical engineering from Huazhong University of Science and Technology, Wuhan, China, in 1992 and 1995, respectively, and the Ph.D. degree in electrical engineering from the University of Tennessee, Knoxville, TN, USA, in 2000.

She is currently a Professor in the Department of Electrical and Computer Engineering, College of Engineering, Florida State University, Tallahassee, FL, USA. Her research interests include photovoltaic converters applying widebandgap devices, bidirectional dc–dc converters, cascaded multilevel inverters, and power electronics applications in hybrid electric vehicles.