Letters

High-Frequency, High-Power Resonant Inverter With eGaN FET for Wireless Power Transfer

Jungwon Choi, *Student Member, IEEE*, Daisuke Tsukiyama, *Member, IEEE*, Yoshinori Tsuruda, *Member, IEEE*, and Juan Manuel Rivas Davila, *Member, IEEE*

***Abstract*—This letter presents a high-power resonant inverter using an enhancement mode gallium nitride (eGaN) device with magnetic resonant coupling (MRC) coils at 13.56 MHz for wireless power transfer (WPT). The power inverter driving the transmitting coils is based on a class Φ_2 inverter, a single-switch topology with low switch-voltage stress, and fast transient response. The implementation utilizes a recently available eGaN device in a low-inductance package that is compatible with operation in the 10 s of MHz switching frequency. In this letter, we present experimental measurements of the inverter in a WPT application and characterize the system performance over various distances and operating conditions. Before using MRC coils, we evaluated the performance of the class Φ_2 inverter with the eGaN FET. It delivered 1.3-kW output to a 50-Ω load with an efficiency of 95% when a 280-V input voltage was applied. For WPT operation, we added the open-type four-coil unit with a diameter of 300 mm to deliver power over 270-mm distance. With the addition of MRC coils, the class Φ_2 inverter provided 823-W output power with 87% efficiency over 270-mm distance between coils.**

***Index Terms*—Enhancement mode gallium nitride (eGaN) FET, high-frequency power inverter, magnetic resonant coupling (MRC), resonant inverter.**

I. Introduction

DESIGNING wireless power transfer (WPT) systems for high-power applications such as electric vehicles (EVs) or battery-powered automated guide vehicles (AGVs) have been attracting a lot of attention in the last few years because WPT is a more convenient way to charge batteries. The high-power applications require WPT systems that not only deliver high power over midrange distances, but are also small enough to be embedded in the vehicles. Because the volume and weight of the energy storage elements are inversely proportional to switching frequency, increasing the switching frequency by 10 s of MHz allows a reduction in weight and an improvement in power density. However, in conventional converters with hard switching operation, fast switching is not favored because switching losses are proportional to the switching frequency.

In order to overcome this issue, many researchers demonstrate soft-switching inverters for WPT systems. By overlapping current and voltage while we turn devices ON and OFF, soft-switching inverters can reduce switching losses. A class E inverter [1] is commonly used as a resonant inverter for various applications at high-frequency operation. However, this kind of inverter is not suitable for high-power systems because the high-voltage stress across the switching device limits input voltage and output power of the inverter. By adding a pair of passive elements consisting of an inductor and a capacitor in parallel to the switching device, a class Φ_2 inverter provides a lower maximum voltage stress than a class E inverter. Moreover, a class Φ_2 inverter requires only a single switching device with a simple gate-driving circuit. In this letter, we present the design and implementation of a class Φ_2 inverter [2], which operates at 13.56 MHz to deliver 1.3-kW output power for WPT applications. Whereas we simply presented initial experimental results in the previous letter [3], here deeper discussion and analysis are provided to support the advantage of the inverter and MRC (magnetic resonant coupling) coil designs.

Selecting suitable switching devices for power inverters is also crucial to the efficiency of inverters. Silicon (Si) MOSFETs have been introduced as switching devices in resonant inverters for many applications because of their stability and electrical performance. However, it is rare to find Si MOSFETs capable of reaching kW output power for high-frequency operation. Previous work [4] shows preliminary implementation of a WPT system, which consists of class Φ_2 inverter driving a tuned set of transmitting and receiving coils. However, the transmitted power was only 218 W that cannot reach kW level output power for high-power applications because the breakdown voltage of the Si MOSFET was limited to 500 V. In addition, the Si MOSFET had a relatively large $R_{DS,ON}$, resulting in high conduction losses. The advent of wideband gap (WBG) devices and their commercial availability offer a promising way to solve the difficulties of Si MOSFETs in high-voltage, high-power applications. WBG devices show better electrical performance and lower device

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J. Choi and J. M. Rivas Davila are with Stanford University, Stanford, CA 94305 USA (e-mail: jwonchoi@stanford.edu; jmrivas@stanford.edu).

D. Tsukiyama is with Daihen Corporation, Osaka 532-8512, Japan (e-mail: d_tsukiyama@daihen-ac.com).

Y. Tsuruda is with Kabushiki Kaisha Daihen, Osaka 230173, Japan (e-mail: y.tsuruda@daihen.co.jp).

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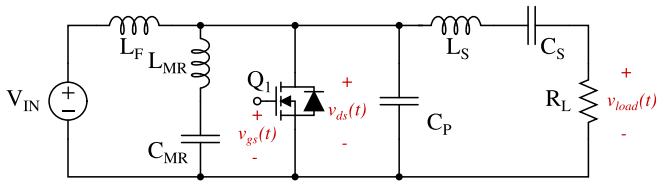

Fig. 1. Class Φ_2 inverter topology.

capacitance than Si MOSFETs, enabling faster switching, improved power density, and high efficiency. Specifically, eGaN FETs are becoming widely used in high-frequency power converters [5], [6]. In this letter, we use the GS66508 from GaN System [7] that can deliver kW output power while operating at 13.56 MHz.

In addition, we must carefully design coupling coils to reduce losses to develop high-power WPT systems. WPT through MRC coils has been studied and demonstrated as a way of delivering power to a load over a midrange distance with relatively high efficiency [8], [9]. While we can obtain high efficiency with MRC coils, it may cause capacitors to break down because of high peak voltage. Previous study [4] presents the MRC coil design using external capacitors to provide resonant coupling. However, the maximum breakdown voltage of the capacitors was 1.5 kV, which is not suitable for high-power applications. In this letter, we demonstrate open-type coils, whose parasitic capacitances can be used instead of discrete ones to prevent voltage breakdown across capacitors while providing high efficiency.

II. Resonant Inverter Topology

The class Φ_2 [2], shown in Fig. 1, is a single-ended resonant inverter in order to address the issues in a class E inverter. Although similar to the class E inverter, this topology uses additional resonant elements to significantly reduce the switch-voltage stresses by as much as 40%–50%. It allows for the use of a lower voltage-rated device with better electrical characteristics and packages, such as DE-150 for high-frequency operation. The additional components, $L_{\rm MR}$ and $C_{\rm MR}$, are responsible for shaping the device voltage to have a lower peak. Similarly, to the class E inverter, the resonant components of the class Φ_2 inverter are tuned to provide zero voltage switching (ZVS) and zero dv/dt switching to minimize switching losses.

More specifically, the impedance at the drain node of a class Φ_2 inverter in frequency domain is determined by tuning passive components. If the impedance satisfies specific conditions shown in [10], we can achieve low voltage stress, ZVS, and zero dv/dt switching across the device. $L_{\rm MR}$ and $C_{\rm MR}$ are selected to suppress the second harmonic of the switching frequency. This plus other characteristics of the components selected result in a trapezoidal drain voltage with a peak $\approx 2V_{\rm IN}$.

We can express the drain-to-source impedance $\rm Z_{DS}(\mathit{w})$ in frequency domain as

$$Z_{\rm DS}(w) = Z_{\rm MR}//Z_L \tag{1}$$

$$Z_{\rm MR}(w) = wL_f// \left(jwL_{\rm MR} + \frac{1}{jwC_{\rm MR}}\right)//\frac{1}{jw(C_{\rm OSS}+C_P)} \tag{2}$$

$$Z_L(w) = jwL_S + \frac{1}{jwC_S} + R_L \tag{3}$$

where w is the switching frequency, $Z_{\rm MR}$ is the impedance consisting of L_F, $L_{\rm MR}$, $C_{\rm MR}$, $C_{\rm OSS}$ and C_P, and Z_L is the impedance consisting of L_S, C_S, and R_L. The tuning process has two steps: 1) selecting components in the load $\rm Z_L$; and 2) tuning the drain impedance by selecting and adjusting components in $Z_{\rm MR}$.

First, the components in Z_L are fixed and easily calculated based on the design parameters $V_{\rm IN}$, $P_{\rm OUT}$, and R_L. C_S can be negligible during the tuning process since it generally has a large capacitance to block dc voltage. L_S is an impedance divider to deliver power to the load as shown below

$$|V_L| = \frac{R_L}{\sqrt{(wL_S)^2 + R_L^2}} * |V_{\rm DS,rms1}| \tag{4}$$

$$V_{\rm DS,rms1} = \frac{4}{\pi\sqrt{2}} * V_{\rm IN} \tag{5}$$

where V_L is the output voltage and $\rm V_{DS,rms1}$ is the fundamental component of $\rm V_{DS}$ when we assume the drain waveform a square wave. $V_{\rm OUT}$ is a function of $P_{\rm OUT}$ and R_L. Then, we can derive L_S

$$L_S = \frac{1}{w}\sqrt{R_L * \left(\frac{8}{\pi^2}\frac{V_{\rm IN}^2}{P_{\rm OUT}} - R_L\right)}. \tag{6}$$

After selecting L_S, other components are chosen to fulfill the requirements as described below. First, $L_{\rm MR}$ and $C_{\rm MR}$ are tuned to resonate at the second harmonic of the switching frequency as shown below

$$Z_{\rm MR}(2w_{\rm sw}) = j2w_{\rm sw}L_{\rm MR} + \frac{1}{j2w_{\rm sw}C_{\rm MR}} = 0 \tag{7}$$

where $w_{\rm sw}$ is the switching frequency. Then, the impedance at the fundamental frequency is inductive to achieve a ZVS operation by adjusting the L_F

$$30^\circ < \angle Z_{\rm DS}(w_{\rm sw}) < 60^\circ. \tag{8}$$

Generally, we design the inverter having 40° at the fundamental frequency. Finally, the impedance at the third harmonic is tuned to be capacitive and several dB below the impedance magnitude at the fundamental frequency as shown below

$$|Z_{\rm DS}(w_{\rm sw})| - |Z_{\rm DS}(3w_{\rm sw})| < 8 \text{ dB} \tag{9}$$

$$\angle Z_{\rm DS}(3w_{\rm sw}) < -80^\circ. \tag{10}$$

In order to adjust the magnitude, an additional capacitance C_P is connected parallel to the switch device. These last two considerations play an important role in setting the overall shape of impedance (a trapezoidal waveform) and the maximum peak voltage across the switching device.

Fig. 2 shows the simulated gate and drain voltages of class E and Φ_2 inverters when the input voltage is 200 V. The maximum

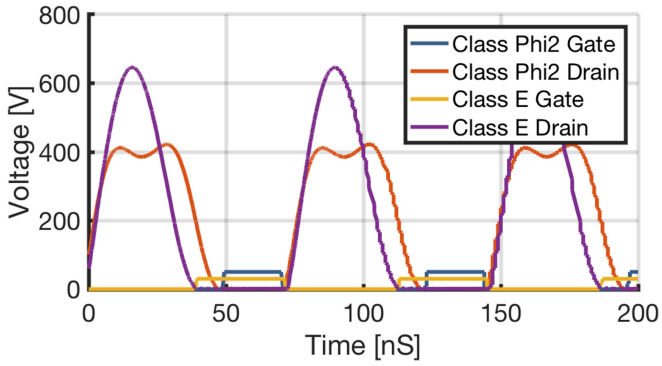

Fig. 2. Comparison of the simulated drain voltages of a class E versus a class Φ_2 inverter at 13.56 MHz and running with the same input voltage.

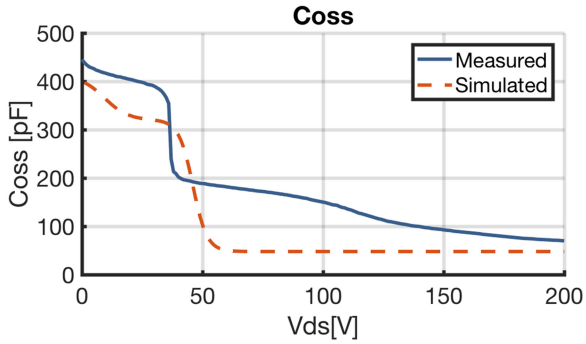

Fig. 3. Comparison of measured and simulated $C_{\rm OSS}$ of GS66508 (an eGaN FET).

voltage of each gate signal is 8 V, but we magnified the gate waveforms in the plot. The class Φ_2 inverter requires 30% duty cycle while 50% duty cycle is applied to the class E inverter. As shown in the figure, maximum voltage across the switch of a class Φ_2 inverter is 40%–50% lower than in a class E inverter. Notice that both waveforms show ZVS and zero dv/dt at the time the switch is turned ON, which makes designing the gate drive simpler. Furthermore, in a class Φ_2 topology, it is possible for the input inductor L_F, as shown in Fig. 1, to take an active role in shaping the drain waveform so it does not need to act as an input choke. This allows for much smaller inductance value and correspondingly faster transient response. Another advantage of a class Φ_2 inverter is its ability to maintain ZVS and low voltage stress even when the load changes substantially. It thus can also retain high efficiency over a larger load range than a class E inverter.

However, in order to design and tune the inverter, an accurate model of switching device has to be provided because the inverter utilizes the output capacitance of the switching devices during the tuning process. In the following section, we describe the importance of modeling a switching device. In addition, while operating the inverter with a single-ended device provides a simple gate-drive circuitry, high voltage across the device or high current through the device should be considered for high-power applications. Specifically, a device in a small package has to effectively dissipate heat. It may therefore require additional heat sinks.

III. Characteristics of eGaN FET

WBG devices such as eGaN FETs are becoming available with higher voltage ratings than Si devices, making the former suitable for operation at 10 s of MHz. To be specific, while some of Si MOSFETs have high breakdown voltage (above 700 V), most are packaged in TO-247, which is not suitable for MHz switching operation. On the other hand, GS66508 (an eGaN FET) can handle higher drain voltage than ARF521 (a Si MOSFET) and provide faster switching because it has low input capacitance, gate resistance, and GaNpx package having extremely low inductance. Moreover, it has $R_{\rm DS,ON} = 52$ mΩ at room temperature, while $R_{\rm DS,ON} = 136$ mΩ at $T_j = 150$ °C. These electrical characteristics of GS66508 make it suitable for high-frequency and high-power operation.

In our design, the output device capacitance $C_{\rm OSS}$ is critical for modeling and tuning the circuit. As we mentioned in Section II, when we designed the class Φ_2 inverter, as shown in Fig. 1, the inverter was tuned to have a specific impedance at the drain node. In the tuning process, C_P must be carefully selected to obtain a proper ratio between the fundamental and third harmonic. First, we simulated a class Φ_2 inverter in LTSPICE to measure the impedance of the inverter at the drain node without any additional C_P when a switch is OFF. For this step, we used a SPICE model of the switch, which includes the output capacitance. Based on the simulated result, we calculated what value of C_P the inverter requires. Additional tuning is sometimes needed to adjust the impedance after calculation. If an output capacitance in SPICE model is incorrect, the inverter will easily lose ZVS and have low efficiency. Therefore, we found it necessary to measure and model the device. And then, we modified the manufacturer's SPICE model to provide a better match between $C_{\rm OSS}$ measurements at various bias voltages.

Fig. 3 shows a comparison between the simulated $C_{\rm OSS}$ using the manufacturer's SPICE model and the experimentally measured $C_{\rm OSS}$ of the GS66508. We applied voltages 0–200 V to the drain-to-source node while measuring the capacitance by using the impedance analyzer, E5061B from Agilent. More than 10 devices were measured before we obtained the figure. In the provided SPICE model, $C_{\rm OSS}$ is 48 pF at $V_{\rm DS} = 400$ V, $V_{\rm GS} = 0$ V, and $f = 1$ MHz. However, the measured $C_{\rm OSS}$ is 70 pF under the same conditions. A more than 30% difference between the SPICE models can result in inaccurate tuning, and this inaccuracy can cause a device to break down because it loses ZVS.

Fig. 4 shows drain voltages in the class Φ_2 inverter with different C_Ps. If we use the provided model that has a $C_{\rm OSS}$ of 48 pF, we need an additional 360 pF of capacitance as a C_P, based on the tuning process of the class Φ_2 inverter. On the other hand, when we use the measured $C_{\rm OSS}$ values, a 320 pF C_P is required to obtain ZVS in the inverter. We assume that the measured $C_{\rm OSS}$ values are correct. Then, we simulated the inverter in LTSPICE with the modified SPICE model while changing the C_P. As shown in Fig. 4, adding 30 pF more at the drain-to-source node causes to lose ZVS condition in the inverter. The

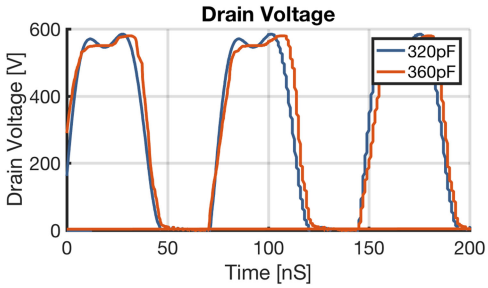

Fig. 4. Comparison of simulated drain voltage of class Φ_2 inverter with the modified SPICE model when we added a C_P of 320 and 360 pF.

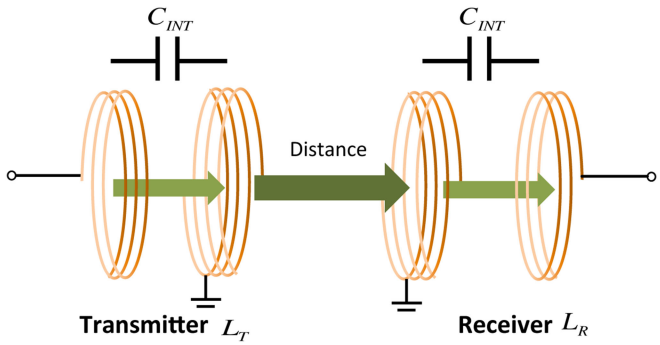

Fig. 5. Simplified representation of open-type four-coil unit consisting of MRC coils, transmitter, and receiver.

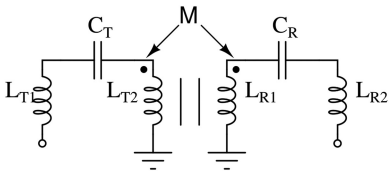

Fig. 6. Electrical model of the transmitting coils ($L_T = L_{T1} + L_{T2}$) and the receiving coils ($L_R = L_{R1} + L_{R2}$) in an open-type four-coil unit.

experimental results with the modified SPICE model are shown in Section V.

IV. Magnetic Resonant Coupling

MRC systems for midrange applications require near-field magnetic coupling and resonance techniques not only to compensate for leakage inductance, but also to obtain high energy efficiency.

In order to deliver power with high efficiency over a midrange coil distance, we designed an open-type four-coil unit, as shown in Fig. 5. This unit consists of two coils with internal capacitance on the transmitting side and two coils with internal capacitance on the receiving side. To create MRC coils, external or internal capacitors must be added to obtain a resonance. Using external capacitors is a well-known method to provide a resonance for WPT systems. Not only is it convenient, it is also easy to modify a capacitance value when we tune the system. However, this method is not suitable for high-power applications because external capacitors can easily break down when high voltage

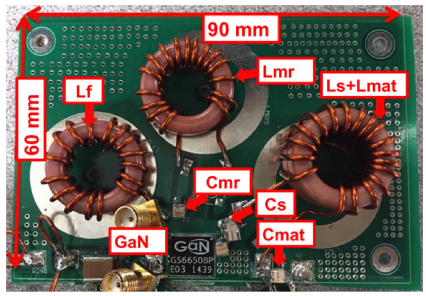

Fig. 7. Implemented class Φ_2 inverter with matching network. $L_f = 260$ nH, $L_{\mathrm{MR}} = 300$ nH, $L_S = 386$ nH, $C_{\mathrm{MR}} = 114$ pF, $C_p = 300$ pF, $C_s = 1$ nF, $L_{\mathrm{mat}} = 293$ nF, and $C_{\mathrm{mat}} = 232$ pF.

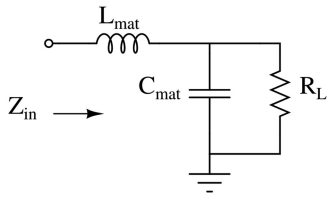

Fig. 8. Matching network consisting of L_{mat} and C_{mat}.

resulting from a resonant operation stresses them. In high-power applications, internal capacitors, as shown in this letter, are preferred because they do not break down under those conditions.

Our open-type four-coil unit is different from a standard four-coil system because each coil in a four-coil system requires its own external capacitor(s) to provide a resonance. In our unit, the coils allow us to change the resonant frequency by adjusting the length of copper wire, distance between two coils, and so on. Also, using this type of coil unit helps eliminate the use of external capacitance that incurs additional losses.

Fig. 6 shows the electrical model of resonant coils in an open-type four-coil unit. When a radio frequency (RF) load is connected to a receiving coil, the impedance seen by a power source is resistive since each coil with capacitors is resonant at switching frequency. The impedance of the electrical model is measured to tune a resonant inverter that is designed for a specific load value. We assume that the resistance of each coil is zero. When a resistive load is connected to the receiving coil L_{R2} in Fig. 6, the impedance of the equivalent circuit is

$$Z_{\mathrm{IN}} = j\left(wL_T - \frac{1}{wC_T}\right) + \frac{(wM)^2}{R_L + j(wL_R - \frac{1}{wC_R})} \quad (11)$$

where w is the switching frequency, R_L is a load value, and M is a mutual inductance between L_T and L_R. Because both coils are in resonance, we can rewrite this equation as

$$Z_{\mathrm{IN}} = \frac{(wM)^2}{R_L}. \quad (12)$$

As shown in this equation, the impedance of the coil unit is determined by a frequency, mutual inductance, and load value. In our experiments, the impedance was 100 Ω with 270-mm distance at 13.56-MHz switching frequency when we connected a 50-Ω resistive load to the receiving coil.

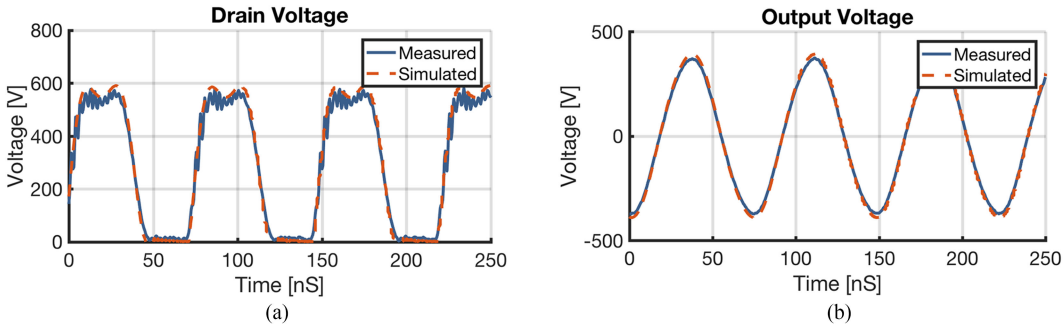

Fig. 9. (a) Simulated and measured drain voltage of the class Φ_2 inverter without MRC coils. (b) Simulated and measured output voltage in the class Φ_2 inverter without MRC coils.

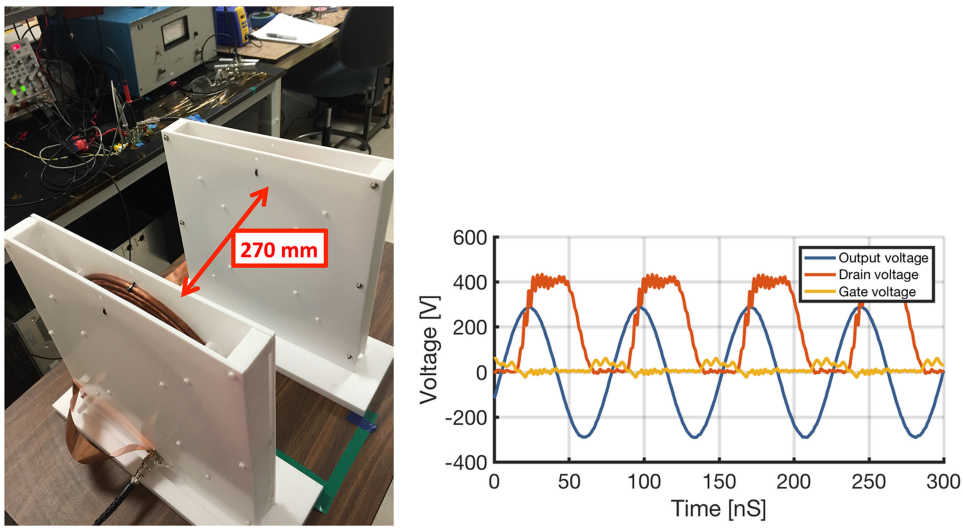

Fig. 10. (a) Coils in the WPT system. The optimal distance between coils is 270 mm. (b) Measured gate, output, and drain voltages of the class Φ_2 inverter with MRC coils at $V_{\rm IN} = 200$ V.

TABLE I
PARAMETERS OF MRC COILS

Parameter	Value
Material	Copper
Pipe thickness	1 mm
Diameter	300 mm
Turns	3
L_T	13.8 μH
C_T	10 pF
L_R	14.5 μH
C_R	9.4 pF

V. EXPERIMENTAL IMPLEMENTATION

A. Preliminary Experiments of the Class Φ_2 Inverter With RF Resistive Load

First, we implemented and tested the class Φ_2 inverter with the eGaN FET to evaluate their performance, the maximum output power and efficiency, before connecting the designed MRC coils to the inverter. Fig. 7 shows an assembled printed circuit board (PCB) prototype including the eGaN FET GS66508. By operating the inverter at high frequency, we were able to implement air–core inductors that eliminate core losses. In order to avoid voltage breakdown in capacitors, we selected high voltage-rated (1 kV or 1.5 kV) capacitors from ATC. LM5114, a gate driver from TI, was used to turn the switching device ON.

The class Φ_2 inverter was connected to a 2-kW water-cooled 50-Ω RF-resistive load. We applied an input voltage of 280 V to the inverter with a switching frequency of 13.56 MHz. In this experiment, a matching network is required because the inverter was designed to provide power to a 25-Ω load, but the actual load was 50 Ω. The matching network consists of $L_{\rm mat}$ and $C_{\rm mat}$, as shown in Fig. 8. Assuming the load is resistive, then the impedance $Z_{\rm IN}$ is

$$Z_{\rm IN} = jwL_{\rm mat} + \left(\frac{1}{jwC_{\rm mat}} || R_L\right) \tag{13}$$

$$= \frac{R_L}{1+(wR_LC_{\rm mat})^2} + j\left[wL_{\rm mat} - \frac{wR_L^2C_{\rm mat}}{1+(wR_LC_{\rm mat})^2}\right] \tag{14}$$

where $Z_{\rm IN}$ is $R_{\rm IN} + jX_{\rm IN}$. While the resistance $R_{\rm IN}$ is set as the impedance that the inverter is designed to handle, the reactance

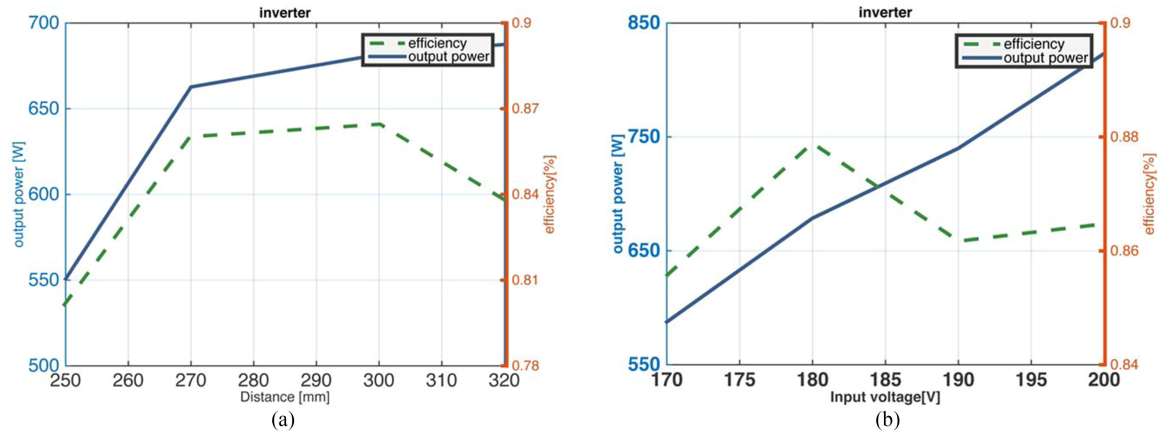

Fig. 11. (a) Power and efficiency of the class Φ_2 inverter with MRC coils when the distance between coils changes; (b) Power and efficiency of the class Φ_2 inverter with MRC coils when the input voltage changes.

$X_{\rm IN}$ has to be zero because the inverter is designed to operate with a pure resistive load as described in the following equations:

$$R_{\rm IN} = \frac{R_L}{1 + (wR_L C_{\rm mat})^2} \tag{15}$$

$$X_{\rm IN} = wL_{\rm mat} - \frac{wR_L^2 C_{\rm mat}}{1 + (wR_L C_{\rm mat})^2} = 0. \tag{16}$$

By solving (15) and (16), we obtain $L_{\rm mat}$ and $C_{\rm mat}$. L_S in the class Φ_2 inverter is combined with the matching network inductance $L_{\rm mat}$.

In simulation, we used the modified SPICE model of the eGaN FET, which includes the measured $C_{\rm OSS}$. Fig. 9(a) and (b) shows the simulated and measured drain and output voltage waveforms of the class Φ_2 inverter. These figures show that the experimental measurements match the simulated results. Also, we found out that the drain-voltage waveform maintains ZVS in both cases. This result indicates that the measured $C_{\rm OSS}$ is correct and significantly different from the manufacturer's SPICE model.

The dc power supply N5771A was utilized to apply dc input voltage to the inverter. We were able to obtain input power through the power supply, which showed not only voltage, but also current information. The current probe, N2783B from Agilent, was also used to measure the dc input current. To measure the output power, we used the voltage probe, HVP120 from LeCroy, and calculated the output power, $P_{\rm OUT} = V_{\rm OUT}^2/R_{\rm load}$. With a 50-Ω load, input power was 1450 W and output power was 1371 W, which leads to an efficiency of around 95% at $V_{\rm IN}$ of 280 V. The result indicates that the inverter with the eGaN FET is capable of delivering kW output power with high efficiency while operating at 10s of MHz switching frequency. Thanks to the matching network between the inverter and load, we obtained a pure sine waveform of output voltage at the load.

B. Class Φ_2 Inverter With Coils

After testing the inverter with a resistive load, we implemented the MRC coils and connected them to the inverter. Fig. 10(a) shows the transmitting and receiving coils for the WPT system. All coil parameters are presented in Table I. We measured the equivalent inductance and capacitance of the coils by using the impedance analyzer. They were made of 1-mm-thick copper wires with a 300-mm diameter. The distance between the coils was 270 mm and each coil has three turns. In order to provide high transmitting efficiency in the coils, the distance between them was shorter than the diameter of each coil.

Before connecting the inverter to the MRC coils, we first measured the coil impedance. When we connected the transmitting coil side to the 50-Ω load, the coil impedance seen by the class Φ_2 inverter was 100 Ω, which is the impedance R_L in (15). The matching network had to be modified to transform the coil impedance to 25 Ω, $C_{\rm mat} = 202$ pF and $L_{\rm mat} = 508$ nH. We connected the transmitting coils to the inverter and the receiving coils to 50-Ω load.

The measured gate, output, and drain voltages with the MRC coils are shown in Fig. 10(b). The waveforms were measured when we applied 200-V input voltage to the inverter. We amplified the gate waveform in the figure because the maximum gate voltage is only 10 V, which is much smaller than the drain and output voltages. As shown in Fig. 10(b), we maintained ZVS with the coils.

The maximum drain voltage of the class Φ_2 inverter should be considered even during the start-up transient, especially as the input voltage increases. For example, when the RF load was connected to the inverter, the maximum drain voltage reached 621 V with a 280-V input voltage. But when using the resonant coil, the inverter experienced a start-up transient that reached 600 V even with an input voltage as low as 200 V. Because the eGaN FET does not have an avalanche breakdown rating, it cannot be operated with a higher voltage than the breakdown voltage it is rated for.

Fig. 11(a) shows the output power and efficiency with different distances between coils. Total measured efficiency is

$$\eta_{\rm total} = \eta_{\rm inv} * \eta_{\rm coil}. \tag{17}$$

where $\eta_{\rm inv}$ is the inverter's efficiency and $\eta_{\rm coil}$ is the MRC coils' efficiency. While the distance between coils varies, the

impedance seen by the inverter also changes. In other words, Fig. 11(a) shows the output power and efficiency over different load values. Maximum efficiency was 87% when the coils were separated by 300 mm, but the class Φ_2 inverter did not maintain ZVS under this condition. The optimal distance between two coils was 270 mm because it enabled the WPT system to maintain ZVS and operate with high efficiency. The variations in performance with input voltage are shown in Fig. 11(b). Efficiency was 87%, input power was 950 W, and output power was 823 W when 200 V input voltage was applied.

VI. Conclusion

This letter presents the design and implementation of a high-frequency, high-power WPT system using an eGaN FET switching device in a class Φ_2 inverter with MRC coils. An eGaN FET allows us to increase input voltage and output power at frequencies exceeding 10 MHz and reduce losses; thanks to its low on-resistance and parasitic capacitances. A single-ended class Φ_2 inverter topology provides not only low voltage stress on the switching device, but also a simple gate-driving circuitry. The dc-to-RF inverter stage achieved efficiency that reached 95% and output power of 1371 W with a $50-\Omega$ load when we applied $V_{\mathrm{IN}} = 280$ V to the input node without MRC coils. The inverter was then connected to a set of MRC coils. Each coil has 300 mm in diameter and 270 mm apart between transmitting and receiving coils to implement the WPT system. The efficiency of the WPT system including the inverter and MRC coils was 87% and output power was 823 W with 200-V input voltage when the distance between coils was 270 mm. The result is a step toward showing that the WPT system described in this letter may contribute to increase power density and system efficiency for developing WPT applications such as EVs or AGVs.

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