# Graphical Evaluation of Time-Delay Compensation Techniques for Digitally Controlled Converters

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***Abstract*—A main design constraint of the digitally controlled power electronics converters is the time delay of control systems, which may lead to the reduced control loop bandwidth and even unstable dynamics. Numerous time-delay compensation methods have been developed, of which the model-free schemes are independent to model accuracy whereas the model-based alternatives are sensitive to system modeling. This paper first presents a graphical illustration of four model-free delay compensation techniques, where their principles and performances are intuitively elaborated and compared by means of the impulse area equivalence method. An improved time-delay compensation approach is then proposed based on additional area insertion, which provides a wider frequency of phase compensation. Finally, the dynamic response of an *LCL*-filtered grid-connected inverter was tested with the studied delay compensation methods. Simulations and experimental test results validate the effectiveness of the graphical comparisons and the proposed approach.**

***Index Terms*—Delay compensation schemes, digital time delay, graphical evaluation, power-electronics converters.**

## I. Introduction

POWER-ELECTRONICS converters have been extensively used and installed in modern industrial applications, such as renewable energy generations [1], [2], uninterruptible power supplies [3], motor drives [4], electric transportation [5], etc. The control of those converters has been increasingly executed by digital microprocessors thanks to the recent advances in digital signal processing technology [6]. Compared to the analog control, the digital realization provides many distinctive advantages, such as higher reliability, more control flexibility, and quick reprogramability [7]. Yet, it also has some demerits with the critical one being the phase lag induced by the time delays, which mainly consist of the computation time and the zero-order hold effect of the digital pulse-width modulation (PWM) [6]. Such a phase lag tends to reduce the phase margin of the control loop and the control bandwidth, degrading the control system performance. While this delay may be small for a high speed digital controller (i.e., a digital signal processor), the measured current/voltage should be sampled exactly at the transition of each control interrupt interval to avoid sampling the switching ripple current, the one-step delay $z^{-1}$ still exists in the control loop [8]. The time-delay effect and its compensation have always been an important issue, and extensive research efforts have been made for decades [6]–[22].

In recent years, the research interests in the influence of time delay are renewed by the stability analysis of current control for grid-tied converters with *LCL*-filters [8]–[16]. In [8], it has been reported that the time delay plays a key role in designing the ac current regulator. Then, a *critical frequency* concept, which is delay-dependent, is introduced for the *LCL*-filter resonance frequency in order to ensure a stable current control [9]. A more systematical analysis of the time-delay effect on the converter- or grid-side current control of *LCL*-filters is presented later in [10] and [11]. Similarly, the impact of time delay on the feedback-type active damping control of *LCL*-filters has also been discussed in [12]–[17]. To alleviate such adverse influences of time delay, numerous compensation techniques, e.g., the well-known *Smith predictor* [18] and *linear predictor* [19], have thus been developed. In general, the predictive control and compensation methods can be divided into two major categories, i.e., 1) the model-based control, and 2) the model-free (-independent) alternatives.

The model-based predictive controls, mainly including the *Smith predictor*, the *state observer* [20], and the *dead-beat control* [21], [22], have frequently been adopted to optimize the digital control performance. Among them, the *Smith predictor* is more readily implemented [18], where a paralleled compensator designed based on the delayed plant is inserted to cancel out the delay effect. However, the effectiveness of this method is highly dependent on the modeling accuracy, both in terms of model parameters and actual operating conditions. In contrast, the essence of the *state observer* and the *deadbeat control* is to calculate the control variables ahead of time based on the difference equations, and in such a way that the error can be canceled out in a number of sampling periods. Theoretically, those control algorithms can completely compensate the time delay, provided that a precise model can be built for the system. Thus, the *observer*-based control is usually needed to mitigate the modeling errors, which in turn imposes more computation burdens [18].

To avoid the model dependence, a number of model-free delay compensation schemes have also been developed. The *linear predictor* is one of the commonly used methods [19],

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which utilizes the linear extrapolation concept [23] to predict the forthcoming values of control variables. It has been shown that this predictor results in an increase in the system controller bandwidth, yet with a necessary requirement of $\omega \cdot T_d < 0.05$ (delay time $T_d$) for a better accuracy in the linear extrapolation [19]. It implies that the *linear predictor* cannot ensure a satisfactory compensation effect at the high frequencies. Another simple approach for the time-delay reduction is to *shift the sampling instant* toward the duty-cycle updating instant [3], [12], [24]. The computation delay can thus be minimized, yet the undesirable harmonic contents may be increased due to the asynchronous sampling process [25]. As a consequence, hardware or software anti-aliasing filters are required for reducing the measurement noises [26], [28], [29]. It has also been suggested in [12] that a shift of the sampling instant to the middle of sampling period is preferred for reduced harmonic disturbances.

Alternatively, the digital-filter-based delay compensation schemes have recently been introduced in [13]–[15]. A first-order digital filter, i.e., $W(z) = 1/(1 + z^{-1})$, is reported in [13], in fact, its essence is a recursive infinite impulse response (IIR) filter configured in a feedback structure. An effective phase lag compensator is provided by this simple filter, yet it tends to amplify the measurement noises nearby the Nyquist frequency due to the infinite gain there. To avoid noise amplifications, additional hardware or software filter may, therefore, be needed. A modified form of the first-order digital filter is formulated in [15], where two coefficients are added, which leads to $W'(z) = 1/(m + (1 - m) \cdot z^{-1})$. By adjusting the coefficients, a compromise between the noise attenuation and phase compensation can be obtained. In [12], a second-order digital filter based on the so-called second-order generalized-integrator (SOGI) [14] is applied to mitigate the delay effect, where the basic idea is to utilize the phase-lead of the SOGI near its resonance frequency. By tuning the damping term of the SOGI, an effective phase compensator with the limited gain response around the Nyquist frequency can be realized.

The success of the model-based methods is quite dependent upon the modeling accuracy, both in terms of system model parameters and actual operating conditions. Compared to model-based ones, model-free methods do not require the model information and are much easier to implement, in addition, have the advantage that the control parameters do not have to be redesigned, which makes this technique attractive to practicing engineers who want to improve on existing designs (*plug and play*). This paper focuses on the model-free compensation methods. This paper presents first a graphical evaluation of the above-mentioned model-free delay compensation methods, where their compensation performances are intuitively compared by means of the impulse area equivalence principle [15]. Based on the graphical comparison, the compensation limit of the digital-filter-based compensation schemes is then revealed and identified in this paper. The maximum phase lag compensation position is the middle of the ideal signal and delayed signal. To overcome this compensation limit, an improved delay compensation scheme is then proposed on the basis of the analysis above. The advantages of the proposed scheme are: 1) readily implemented and simple controller form, and 2) a wider frequency range of compensation and better compensation effects. An application example based on an *LCL*-filtered grid-tied converter is set up, where the delay compensation methods are tested for improving the transient performance of the current control loop. Simulations and laboratory test results confirm the presented graphical comparisons and the effectiveness of the proposed approach.

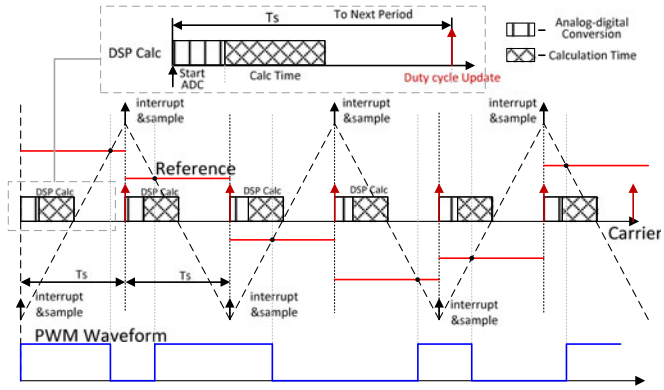


Fig. 1. Control and modulation process in a digital microprocessor.

## II. Time Delay in a Digitally Controlled System

### A. Digital Time Delays

Most modern power-electronics converter control systems use digital processors to flexibly implement the control and modulation process. Fig. 1 shows the detailed modulation duty update process at every single sampling period, where the asymmetrical regular sampled PWM strategy is adopted. The commanded modulation reference is congealed at the start of each half-carrier period (*one sampling period*) and compared against a triangular carrier ramp using a digital comparator that toggles the PWM output as the ramp crosses the command reference [8]. The synchronous sampling is adopted, where the measured variables should be sampled exactly at the transition of each half-carrier interval to avoid sampling the switching ripple component as well as low order harmonics components. During the practical implementation, nonzero time is required to execute the control algorithm and compute a new modulation value. The obtained modulation duty should be updated and loaded at the beginning of the next sampling period instead of immediately after the calculation process. This process will introduce one-sample computation delay ($z^{-1}$) into the control loop. It is worth mentioning that although this time delay may be small for a high speed digital controller, it equals to one single sampling period $T_s$ regardless of the speed of the processor.

### B. Graphical Representation

Following the illustration in Fig. 1, Fig. 2 provides a more concise graphic representation, where the ideal modulation signal $r(k)$ represents the calculated duty based on the measurement at current step, while the real modulation signal $s(k)$ takes the computational delay into consideration. Obviously, $s(k)$ one step lags behind $r(k)$ and the relationship between $r(k)$ and $s(k)$

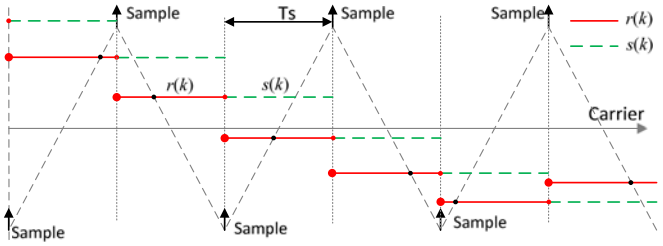


Fig. 2. Ideal modulation signal and real modulation signal with one sample delay.

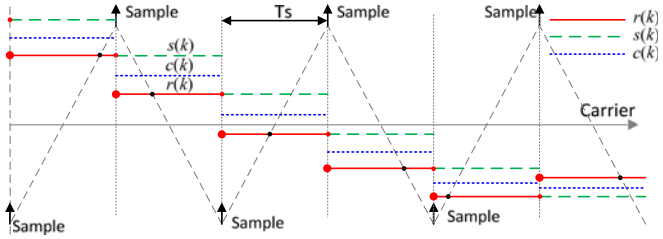


Fig. 3. Graphical representation for the delay-compensated modulation signal.

is written as

$$s(k) = r(k-1) = r(k) \cdot z^{-1}. \tag{1}$$

## III. Graphical Evaluation of Time-Delay Compensation Schemes

### A. Principle of the Graphical Evaluation

In order to ideally compensate the delay $z^{-1}$, a pure phase lead element $z^{1}$ is expected to exactly cancel out $z^{-1}$. However, the element $z^{1}$ means the data in the future step is required, which is impossible in a real digital controller. To obtain the future step data, [27] uses the data stored in the memory one fundamental period (20 ms) ago. However, this scheme would further degrade the dynamic response and system stability because another fundamental period delay is introduced. In fact, the original intent in many delay compensation methods in previous publications [13]–[15], [19] is to replace and emulate the phased lead element $z^{1}$.

With this viewpoint, a graphical-based method to estimate the proximity of the compensated signal $c(k)$ to the original signal $r(k)$ is introduced. For example, as illustrated in Fig. 3, $r(k)$ and $s(k)$ are the ideal and real modulation signal, the same definition as Fig. 2. Intuitively, if the compensated $c(k)$ is geometrically closer to $r(k)$ than $s(k)$, thus, indicating the equivalent phase of $c(k)$ is closer to the ideal signal $r(k)$, the undesirable phase lag is then reduced, which demonstrates the delay compensation ability of the compensation method. In following sections, four existing compensation schemes are evaluated and compared through this graphical-based method.

### B. Comparative Evaluation of the Different Compensators

*Linear predictor:* One well-known method to compensate such time delays is so called *linear predictor*, which was earlier

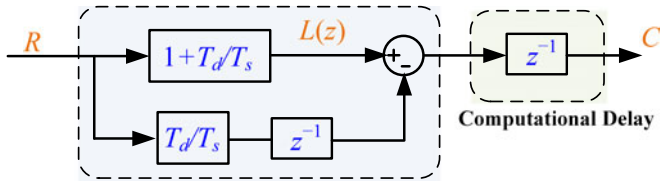


Fig. 4. Block structure diagram for the linear predictor $L(z)$.

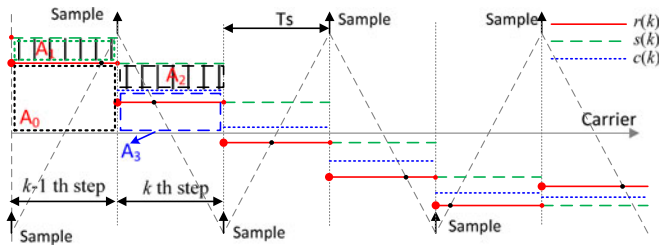


Fig. 5. Graphical representation for linear predictor $L(z)$.

proposed and analyzed in [19] based on the linear extrapolation technique. If the time delay to be compensated is $T_d$, the discrete transfer function $L(z)$ can be expressed as

$$L(z) = 1 + \frac{T_d}{T_s} - \frac{T_d}{T_s} \cdot z^{-1}. \tag{2}$$

Fig. 4 shows the structure of the linear predictor $L(z)$, $R$ is the original modulation signal, whereas $C$ is the compensated signal through $L(z)$ and delay $z^{-1}$. According to the figure, the signal $c(k)$ can be deduced as

$$\begin{aligned} \frac{C(z)}{R(z)} &= \left(1 + \frac{T_d}{T_s} - \frac{T_d}{T_s} \cdot z^{-1}\right) \cdot z^{-1} \\ &= \left(1 + \frac{T_d}{T_s}\right) \cdot z^{-1} - \frac{T_d}{T_s} \cdot z^{-2} \end{aligned} \tag{3}$$

$$c(k) = \left(1 + \frac{T_d}{T_s}\right) \cdot r(k-1) - \frac{T_d}{T_s} \cdot r(k-2). \tag{4}$$

To understand how the linear predictor $L(z)$ works, an impulse-area equivalence method is presented to provide an intuitive explanation: The equation mentioned above remains true when both sides are simultaneously multiplied by the same variable $T_s$, as shown in (5). According to the voltage-second balance principle, the delay compensation process is illustrated during every single step by the relationship of the equivalent areas $A_0$, $A_1$, $A_2$, $A_3$ as shown in Fig. 5

$$\underbrace{c(k)}_{A_3} = \underbrace{r(k-1) \cdot T_s}_{A_0} - \overbrace{\underbrace{\frac{T_s}{T_s} \cdot \{r(k-2) - r(k-1)\} \cdot T_s}_{A_1}}^{A_2}. \tag{5}$$

In Fig. 5, the waveform $r(k)$ is supposed to be an ideal modulation signal without time delay, while the dashed line $s(k)$ includes the one-step delay. The dotted line $c(k)$ is generated through the area calculation according to (5). It can be observed that the area $A_0$ represents the impulse area activated by

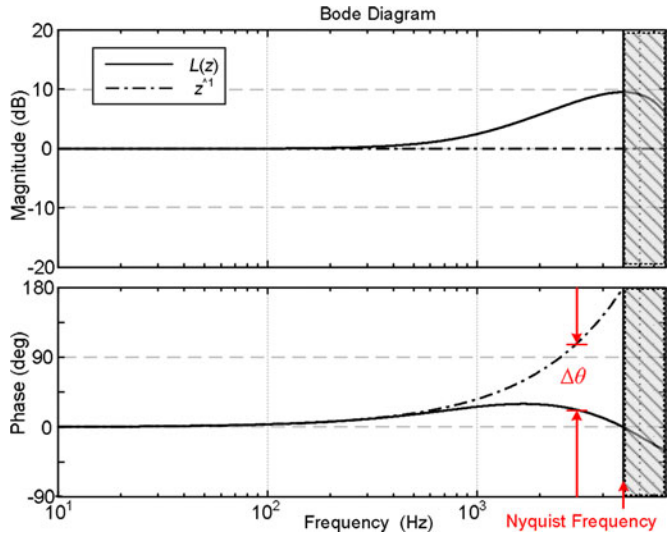


Fig. 6. Bode diagram comparison between linear predictor $L(z)$ and pure phase lead $z^1$.

$r(k-1)$, whereas the area $A_1$ stands for the area generated by the difference value of $r(k-2)$ and $r(k-1)$. The area $A_2$ is $T_d/T_s$ times of the area $A_1$, e.g., they are equal to each other $A_1 = A_2$ when delay time $T_d = T_s$. From the geometrical point of view, the area $A_3$ is calculated and predicted through subtracting the area $A_2$ from the area $A_0$, the equivalent phase of $c(k)$ is closer to $r(k)$.

1) If $r(k-2) > r(k-1)$, it means the original signal has a negative slope at the $k$ step, as the case in Fig. 5. $A_3 = A_0 - A_2$, $c(k)$ is closer to $r(k)$ due to the area loss.
2) If $r(k-2) < r(k-1)$, similar conclusion will be obtained, the term $r(k-2) - r(k-1)$ is negative, making $c(k)$ approach $r(k)$.

This method works without knowledge of the system that is being controlled and simply predicts the future value by a linear function based on the past values. However, a necessary requirement is to have $\omega \cdot T_d < 0.05$ (delay time $T_d$) to generally guarantee that the linear extrapolation is accurate enough [19] so that the prediction error is negligible. Suppose $T_d = T_s$, Fig. 6 presents the Bode diagram of $L(z)$. It can be seen that the phase difference $\Delta\theta$ increases with the frequency, implying that linear predictor $L(z)$ cannot provide satisfactory compensation effect in the relatively high-frequency range.

The analysis mentioned above is verified by plotting the time-domain compensation result for the linear predictor, as shown in Fig. 7. Within the zero-crossing vicinity, the area $A_2$ is almost the same at every single step, it shows that the delayed signal $s(k)$ is well-compensated by linear predictor. However, near the peak parts, over-compensation phenomenon is brought due to rapid change of the area $A_2$. During the rising steps as shown I part in Fig. 7, $c(k)$ leads the ideal signal $r(k)$, while $c(k)$ lags the ideal signal $r(k)$ during the declining steps. Obviously, it does not meet the requirement of accurate phase compensation.

*Shifting sampling instant*: This technique is proposed to directly reduce the time delays through shifting the sampling time

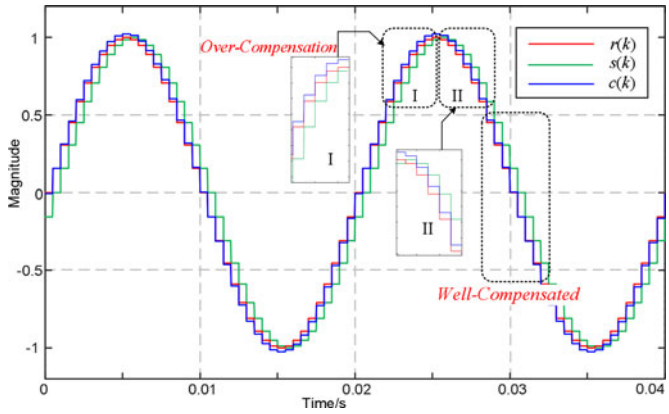


Fig. 7. Compensation results through the linear predictor $L(z)$.

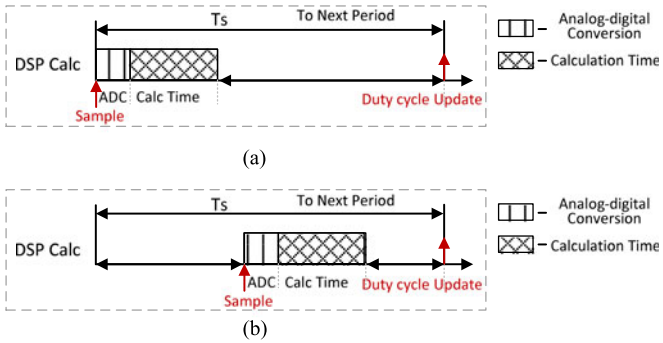


Fig. 8. Principle of the *reduced computation delay*: (a) synchronous sampling and (b) shifting sampling instant.

of the control variables toward the duty cycle update instant, as shown in Fig. 8(b). This method is adopted in [3] for the uninterruptible power systems application to significantly increase voltage-loop bandwidth; in [12] to improve the capacitor-current-feedback active damping effects; and in [24] to improve system stability through minimizing the delay in voltage feed-forward path. This idea is actually quite simple and easy to implement in the digital processor. At first, the conventional synchronous sampling is presented in Fig. 8(a), where one sample delay exists. If the measurement or sampling point is shifted as shown in Fig. 8(b), it can be observed that the time interval between the sampling point and the duty cycle update point is hence reduced. Fundamentally, the prerequisite is that the control algorithm and duty cycle calculation should be finished before next step.

It is reported that the middle of the sampling period $(\lambda = 0.5)$ is the preferred sample instant to maintain a relatively small harmonics. However, the practicability of this approach would be limited by the sampling-induced aliasing problem [12], [26]. Based on the graphical method, the *shifting sampling instant* method can be presented by Fig. 9. The compensated signal is equivalent to the dotted line $c(k)$ which is shifted down from the delayed signal-dashed line $s(k)$. The proportion downwards depends on the sampling point. Definitely, this technique can provide the phase lag compensation ability.

Fig. 9(b) presents the time-domain simulation when $\lambda = 0.5$, the signal after compensation is in middle of the $r(k)$ and $s(k)$,

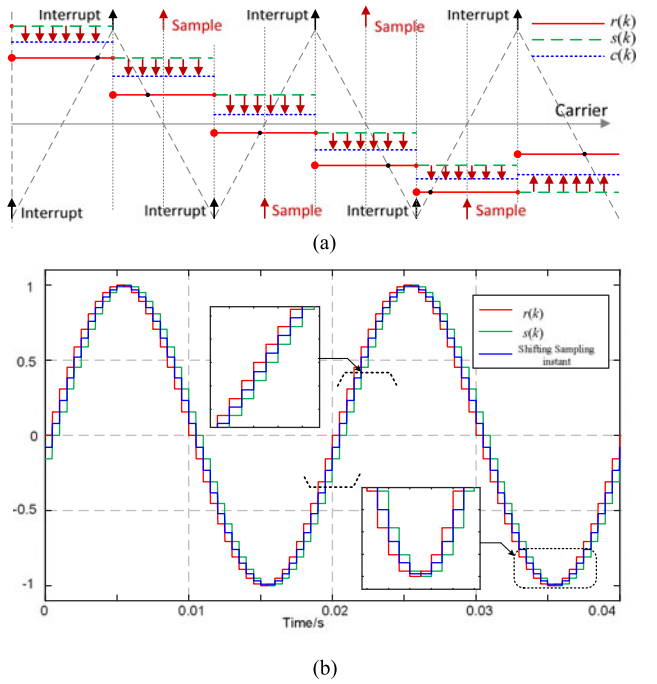


Fig. 9. Graphical explanation for the shifting sampling instant technique: (a) graphical illustration and (b) time-domain simulation.

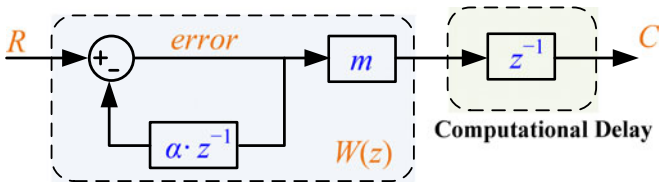


Fig. 10. Block diagram of the FOF compensation method.

hence the equivalent phase is closer to the ideal signal $r(k)$, the phase lag is compensated.

*First-order-filter compensation scheme*: To widen the damping region, a first-order-filter (FOF) scheme, i.e., $W(z) = 1/(1 + z^{-1})$, is reported in [13]. In fact, its essence is a recursive IIR digital filter [31] configured in a feedback structure as shown in Fig. 10. $R$ is the input signal and $C$ is the output signal. The compensation effect is achieved through using the feedback of the previous step of the error.

The discrete transfer function of the compensation block can be expressed as

$$W(z) = \frac{m}{1+z^{-1}} \quad \Rightarrow \quad \frac{m}{1+\alpha\cdot z^{-1}} \tag{6}$$

where the left part of equation mentioned above is the original expression of FOF scheme [13], the coefficient $m$ is set to 2 in order to assure the unity magnitude at the low frequencies because $z^{-1}$ equals to 1 at such frequencies. To avoid the infinite magnitude at Nyquist frequency ($f_{\mathrm{sam}}/2$, half the sampling frequency $f_{\mathrm{sam}}$) and guarantee the system stability, a coefficient $\alpha$ ($\alpha < 1$ but close to 1) is often added in the block as shown at the right part of (6), then, the gain $m$ is selected as

$$m = 1 + \alpha. \tag{7}$$

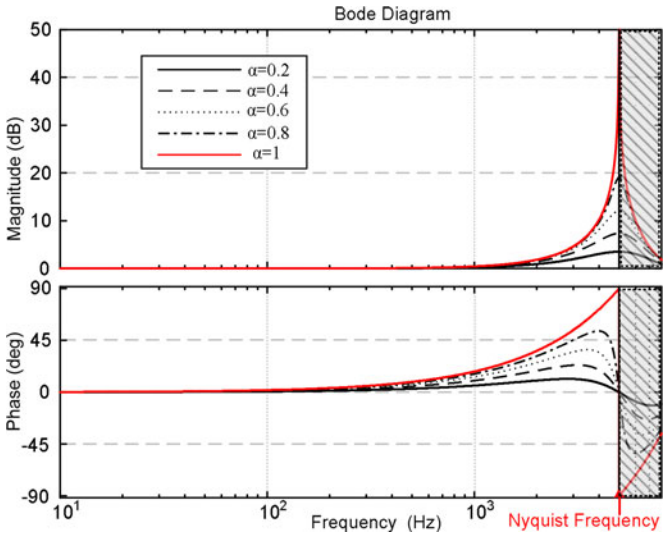


Fig. 11. Different Bode diagrams for different $\alpha$ values.

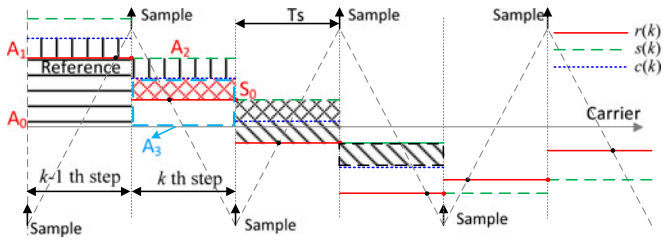


Fig. 12. Graphical explanation of the compensation block shown in (10).

It also can be observed from Fig. 11, different coefficients $\alpha$ will contribute to different delay compensation effects. The closer the coefficient $\alpha$ is to 1, the larger magnitude at Nyquist frequency and the better compensation results the compensation block obtains. It is shown that when $\alpha = 1$ as presented in [13], infinite magnitude appears at Nyquist frequency, the system is sensitive to the noise around specific frequency. A tradeoff between the magnitude amplification at Nyquist frequency and phase lag compensation should be taken into consideration in parameter $\alpha$ selection.

The relationship between the output signal $C(z)$ and input signal $R(z)$ is given by

$$\frac{C(z)}{R(z)} = \frac{m}{1+\alpha\cdot z^{-1}}\cdot z^{-1} \tag{8}$$

$$\begin{aligned} c(k) &= (1+\alpha)\cdot r(k-1) - \alpha\cdot c(k-1) \\ &= r(k-1) + \alpha\cdot\{r(k-1) - c(k-1)\}. \end{aligned} \tag{9}$$

Both sides of the equation mentioned above are multiplied by the same variable $T_s$, the equation remains true, as written in (10). Fig. 12 shows the detailed illustration, the waveform $r(k)$ is ideal modulation signal from the digital controller, the dashed line $s(k)$ includes the one-sample time delay caused by the algorithm computational time. The dotted line $c(k)$ is generated by deriving (10). The area $A_0$ represents the impulse activated by $r(k-1)$, the area $A_1$ represents the impulse difference generated by the difference value of $r(k)$ and $c(k)$ at the $(k-1)$th step. The area $A_2$ is $\alpha$ times of the area $A_1$, and they are almost equal

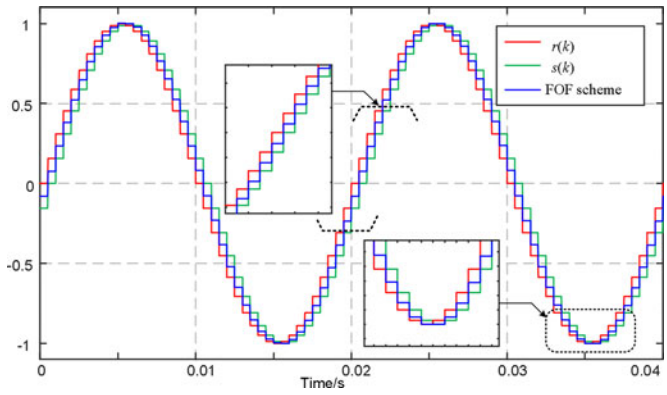


Fig. 13. Compensation result for the FOF time-delay compensation scheme.

to each other when $\alpha$ is close to 1. Therefore, the impulse $A_3$ brought by $c(k)$ can be calculated and predicted exactly as (10). The same derivation also applies to the right next step as shown in Fig. 12, then extending to the whole control steps

$$\underbrace{c(k)\cdot T_s}_{A_3}=\underbrace{r(k-1)\cdot T_s}_{A_0}-\overbrace{\alpha\cdot\underbrace{\{c(k-1)-r(k-1)\}\cdot T_s}_{A_1}}^{A_2}. \tag{10}$$

Fig. 13 shows the time-domain results for verifying the delay compensation effect. For this case, $\alpha$ and $m$ are selected to 0.95 and 1.95, respectively. An ideal 50 Hz sinusoidal modulation waveform acts as the input signal. The high-frequency carrier is not plotted for better graphical presentation. The sampling frequency is set to 2 kHz in order to have a better visual observation on the phase lead characteristic of the compensation block. It can be observed that the value of the compensated waveform $c(k)$ at almost every step approximately equals to the middle value of the ideal waveform $r(k)$ and one-sample delayed one $s(k)$, implying that phase lead has been added by the compensation block. It offers more accurate phase compensation within the peak vicinity than *linear predictor*. The feedback structure of FOF scheme contributes to the delay compensation effect, which is similar to the *shifting sampling instant* method.

Although the obvious compensation effects are obtained, a compensation limit still exists for this technique. For every sampling step $T_s$, it is reasonable to assume that area $A_2$ changes little from ($k$ – 1)th step to $k$th step, and then (10) can be expressed by

$$\begin{aligned} c(k) &= r(k-1) \ +\alpha\cdot\{r(k-1)-c(k-1)\} \\ &\approx r(k-1) \ +\alpha\cdot\{r(k)-c(k)\} \end{aligned} \tag{11}$$

$$c(k)\approx\frac{r(k-1)+\alpha\cdot r(k)}{1+\alpha}. \tag{12}$$

In (12), $\alpha$ is the proportional factor to weigh the extent $c(k)$ approaching $r(k)$ or $r(k-1)$. It is worth noting that $0\leq\alpha\leq1$ is required to assure no unstable poles in the system. It indicates the compensated signal $c(k)$ is closer to the $r(k)$: If $\alpha=0$, $c(k)=r(k-1)$, no compensation functions; if the maximum value $\alpha=1$, $c(k)=r(k-1)+r(k)/2$, the compensation works, the signal is in the middle of $r(k)$ and $r(k-1)$. Due to the linearity

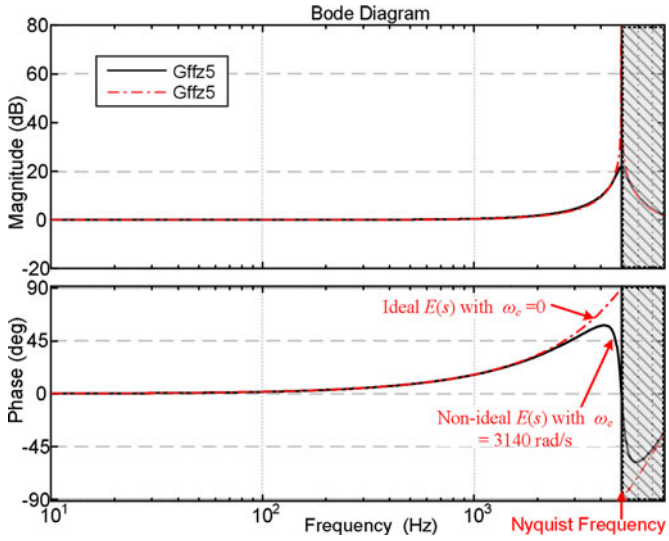


Fig. 14. Bode diagram comparison of the SOGI-based delay compensation scheme.

of (12), therefore, the limit position after delay compensation is the middle of ideal signal $r(k)$ and one-sample delayed signal $r(k-1)$. Fig. 13 shows the compensation result verifying the analysis mentioned above where $\alpha$ is set to 0.95. Therefore, the maximum compensation of this method is the middle of the ideal signal $r(k)$ and delayed signal $c(k)$.

*SOGI-based time-delay compensator*: This method is recently proposed in [14] to compensate the time delay in the grid current feedback control for the *LCL*-filtered grid converters. Intrinsically, the SOGI-based scheme utilizes the phase lead characteristics of the second-order resonant term as shown in Fig. 14, where ideal cases with $\omega_c=0$ rad/s and nonideal case $\omega_c=3140$ rad/s are compared. After digital discretization, the essence is a second-order IIR digital filter. The compensation block transfer function is expressed as

$$E(s)=1+\frac{k\cdot\omega'\cdot s}{s^2+\omega'^2}\Rightarrow1+\frac{k\cdot\omega'\cdot s}{s^2+\omega_c\cdot s+\omega'^2} \tag{13}$$

where the delay compensation block $E(s)$ consists of a constant 1 plus a damped second-order resonant part, where $\omega'$ is the natural frequency, $\omega_c\cdot s$ is the damping term, and $k$ is an adjustable gain. Hence, the expression mentioned above has three degrees of freedom, and the selection guidelines for these coefficients are discussed below.

To avoid the phase sudden change of the resonant part in (13) while performing delay compensation in the frequency range (0, $\omega_{\mathrm{Nyquist}}$), $\omega'$ should be set higher than or equal to Nyquist frequency $\omega_{\mathrm{Nyquist}}$. $\omega'$ is chosen as Nyquist frequency to maintain better compensation ability in [14]. The tuning of value $k$ is analyzed and discussed in [30] and [14]: For a given sinusoidal input signal, $k$ should be smaller than 2 ($k<2$) to guarantee the output signal is solvable [30]. The gain $k$ is set to $\sqrt{2}$, which results in an optimal tradeoff between settle time, overshooting. From Fig. 14, it can be observed that the infinite magnitude exists at Nyquist frequency for the ideal $E(s)$ case ($\omega_c=0$), making it sensitive to noise. Then, $\omega_c=3140$ rad/s is

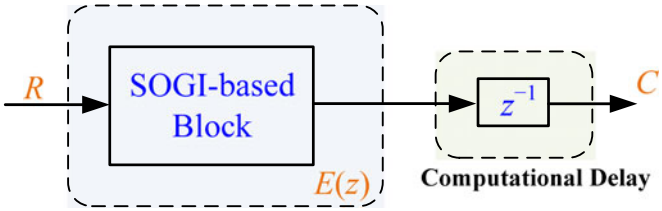


Fig. 15. SOGI-based time-delay compensation scheme.

chosen to give a satisfactory trade-off between noise attenuation and phase lead performance.

For detailed analysis, (13) can be written as the first-order hold discretized form as (14), where second-order element $z^{-2}$ is introduced [12]. The symbols $a, b, c, d, e$ are constants varying with the value $\omega_c$, out of them constant $c$ is a small value ($c < 0.1$) for the $\omega_c$ ranges from 0 to 10 000 rad/s. Note that these constants are restricted by the requirement in (15) to guarantee the unit magnitude at the low-frequency range

$$E(z) = \frac{a + b \cdot z^{-1} + c \cdot z^{-2}}{1 + d \cdot z^{-1} + e \cdot z^{-2}} \tag{14}$$

$$a + b + c = 1 + d + e. \tag{15}$$

According to the structure shown in Fig. 15, the relationship between the output signal $c(k)$ and input signal $r(k)$ can be written as (16). The impulse contribution is divided into five parts. Compared to the linear predictor, the data from further previous steps $z^{-2}$ are needed

$$\begin{aligned} \underbrace{c(k) \cdot T_s}_{A5} = {} & \underbrace{r(k-1) \cdot T_s}_{A_0} \\ & + \underbrace{(a-1) \cdot \{r(k-1) - c(k-1)\} \cdot T_s}_{A_1} \\ & + \underbrace{(d+1-a-c) \cdot \{r(k-2) - c(k-1)\} \cdot T_s}_{A_2} \\ & + \underbrace{e \cdot \{r(k-2) - c(k-2)\} \cdot T_s}_{A_3} \\ & + \underbrace{c \cdot \{r(k-3) - c(k-1)\} \cdot T_s}_{A_4}. \end{aligned} \tag{16}$$

To better illustrate the compensation effect, the ideal case $\omega_c = 0$ with best delay compensation performance as shown in Fig. 14, $k$ equals to 1.414 is studied. Other cases with different $\omega_c$ values have poorer compensation effect. $E(z)$ can be expressed as (17), only $z^{-1}$ remains after removing the common factor $(1 + z^{-1})$. And it is quite similar to the FOF method written in (6). Fig. 16 shows the graphical explanation, similar to the previous illustration, the areas $A_0$, $A_1$, $A_2$, $A_3$ are plotted, and $c(k)$ is estimated according to (18)

$$E(z) = \frac{1.9 + 2 \cdot z^{-1} + 0.1 \cdot z^{-2}}{1 + 2 \cdot z^{-1} + z^{-2}} = \frac{1.9 + 0.1 \cdot z^{-1}}{1 + z^{-1}}. \tag{17}$$

In fact, the SOGI-based method is similar to the FOF method apart from $0.1 \cdot z^{-1}$. Contrarily, the "+" sign before the term $A_2$ in

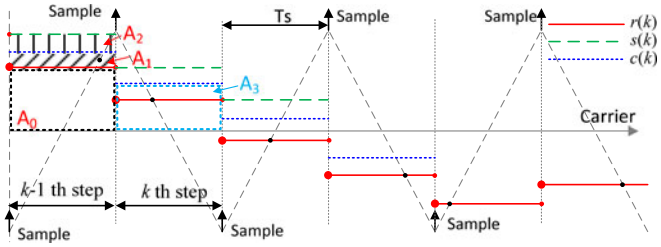


Fig. 16. Graphical representation for the SOGI-based time-delay compensation scheme.

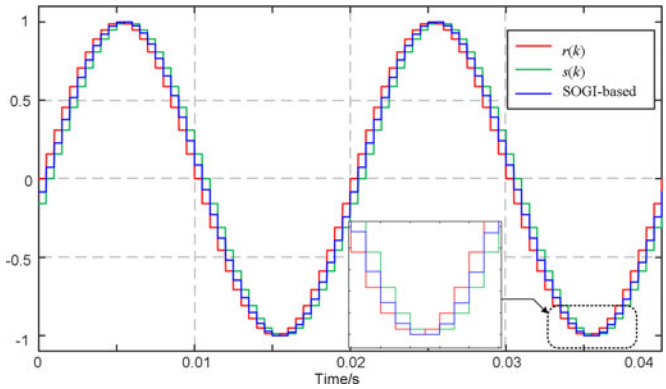


Fig. 17. Compensation result for the SOGI-based time-delay compensation scheme.

(18) makes the compensated signal $c(k)$ further away from $r(k)$; therefore, compared to FOF scheme, SOGI-based scheme has a little poorer compensation ability. Thus, the compensation limit restricting the compensation of FOF scheme also exists in SOGI-based scheme. Fig. 17 shows the compensation result of the SOGI-based scheme. In agreement with the analysis, it exhibits quite similar compensation ability. Almost, the compensated signal is in the middle position of the ideal signal $r(k)$ and delayed signal $s(k)$

$$\begin{aligned} \underbrace{c(k) \cdot T_s}_{A_3} = {} & \underbrace{r(k-1) \cdot T_s}_{A_0} - 0.9 \underbrace{\{c(k-1) - r(k-1)\} \cdot T_s}_{A_1} \\ & + 0.1 \cdot \underbrace{\{r(k-2) - c(k-1)\} \cdot T_s}_{A_2}. \end{aligned} \tag{18}$$

## IV. Proposed Time-Delay Compensation Scheme

This section introduces a new idea on the time-delay compensation based on the graphical evaluation mentioned in the previous section. The principle and implementation of the proposed scheme are also presented.

### A. Principle of the Proposed Compensation Scheme

Since delay compensation limit exists for FOF-based scheme and SOGI-based scheme mentioned in previous section, a natural question coming to mind is whether it is possible for the compensated signal to further approach the ideal delay-free signal. Next part will introduce such an improved time-delay compensation scheme based on the graphical evaluation. Referring to (10) and Fig. 12, the compensated signal is supposed to further

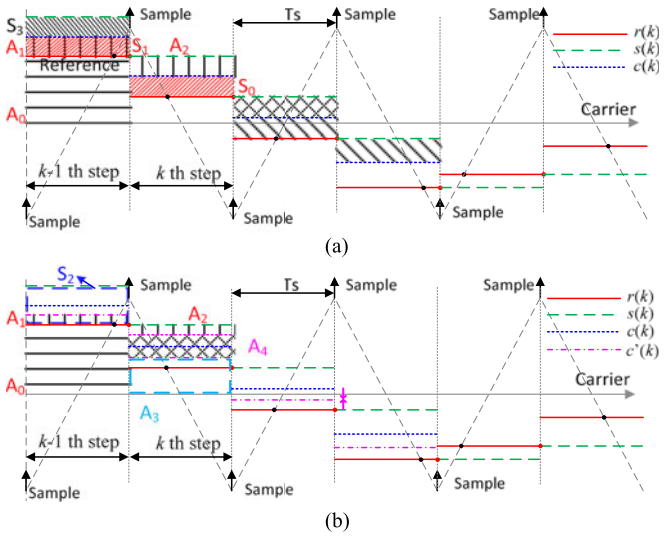


Fig. 18. Graphical explanation of the proposed compensation block: (a) the expression of area difference $S_0$ and (b) area term $A_4$ to replace $S_0$.

approach the ideal signal through mathematically subtracting the area $S_0$ shown in Fig. 18(a)

$$S_0 = \{c(k) - r(k)\} \cdot T_s \;\Rightarrow S_1 = \{c(k-1) - r(k-1)\} \cdot T_s \tag{19}$$

where the essential area difference between compensated signal $c(k)$ and $r(k)$ can be expressed as $S_0$. $S_1$ means the area difference at the $k-1$ step. Unfortunately, both the values $r(k)$ and $c(k)$ are the data at current step, of which $r(k)$ has not been calculated out yet and $c(k)$ is the value needed to be calculated for the final compensation result. Hence, it is impossible to implement such a mathematical subtraction directly. Note that only the data at the previous steps can be used to replace the area $S_0$ and then further compensate the time delays. Therefore, it is an alternative to substitute the area $S_0$ using the data at $k-1$ step, whose expression is written at the right part of expression (19). However, this substitution will bring an unstable pole outside the unit circle, whose derivation is presented in Appendix I.

This paper proposes a simple and practical area $S_0$ substitution option presented in Fig. 18(b). There are two possibilities: 1) A proportion of area $S_2$ can be used to achieve the goal and 2) A proportion of the area $S_3 = r(k-2) - c(k-1) \cdot T_s$. The substitution can be expressed by using the area $A_4$ as written in (20). In diametric contradiction to the SOGI-based delay compensation method, the sign "–" is added before the area term $A_4$. The symbols $\beta$ and $\gamma$ are the proportion factors

$$\begin{aligned} A_4 &= \beta \cdot S_2 = \beta \cdot \{r(k-2) - r(k-1)\} \cdot T_s \\ \text{or } A_4 &= \gamma \cdot S_3 = \gamma \cdot \{r(k-2) - c(k-1)\} \cdot T_s. \end{aligned} \tag{20}$$

For the first possibility, an additional part area $A_4$ is inserted, and the expression after delay compensation is written as

$$\underbrace{c(k) \cdot T_s}_{A3} = \underbrace{r(k-1) \cdot T_s}_{A_0} - \overbrace{\alpha \cdot \{c(k-1) - r(k-1)\} \cdot T_s}^{A_2}_{A_1} - \overbrace{\beta \cdot \{r(k-2) - r(k-1)\} \cdot T_s}^{A_4}. \tag{21}$$

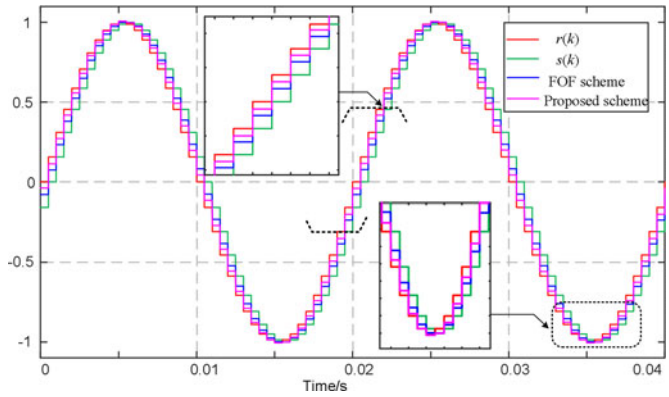


Fig. 19. Compensation result for the proposed delay compensation scheme.

Fig. 18(b) shows the detailed illustration of the improved time-delay compensation. The same with the definition before, the waveform $r(k)$ represents ideal modulation signal, and the dashed line $s(k)$ includes the one-sample delay. The dotted line $c(k)$ is generated by the conventional compensation block shown in (21). The similar illustration as Fig. 18(a), the area $A_0$ represents the impulse by $r(k-1)$, and the area $A_1$ represents the impulse difference generated by the difference value of $r(k)$ and $c(k)$ at the $(k-1)$th step. The area $A_2$ is $\alpha$ times of the area $A_1$. Besides, an additional area $A_4$ is removed to further approach the ideal one. Finally, the impulse $A_3$ brought by $c'(k)$ can be calculated and predicted exactly as (21). Compared to the conventional compensation method (the blue), the improved waveform is even closer to the ideal signal, which is the ideal modulation waveform without computation delay.

Fig. 19 shows the real time results for the proposed compensator. The same setting of sampling frequency and $\alpha$ value is made with the previous section. For this case, the coefficient $\beta$ is set to 0.5. An ideal 50 Hz sinusoidal modulation waveform acts as the input signal. Two-period waveforms are shown. In comparison to the conventionally compensated signal, the signal through the proposed compensator is closer approximated to the ideal signal, demonstrating the better compensation ability of the proposed method.

For the second possibility, a proportion of the area $S_3 = r(k-2) - c(k-1) \cdot T_s$ is subtracted to make the compensated signal approach the ideal signal. The area expression can be written as (22), from where it can be seen that the same area components correspond to (21) except the proportion factors. If $(\alpha - \gamma)$ and $\gamma$ in (22) are set to be $\alpha$ and $\beta$ in (21), then the same compensation effects are obtained. Therefore, no more analysis for this possibility will be presented

$$\begin{aligned} &\overbrace{c(k) \cdot T_s}^{A_3} = \overbrace{r(k-1) \cdot T_s}^{A_0} - \overbrace{\alpha \cdot \{c(k-1) - r(k-1)\} \cdot T_s}^{A_2} \\ &- \overbrace{\gamma \cdot \{r(k-2) - c(k-1)\} \cdot T_s}^{S_3} = r(k-1) \cdot T_s - (\alpha - \gamma) \\ &\cdot \{c(k-1) - r(k-1)\} \cdot T_s - \gamma \cdot \{r(k-2) - r(k-1)\} \cdot T_s. \end{aligned} \tag{22}$$

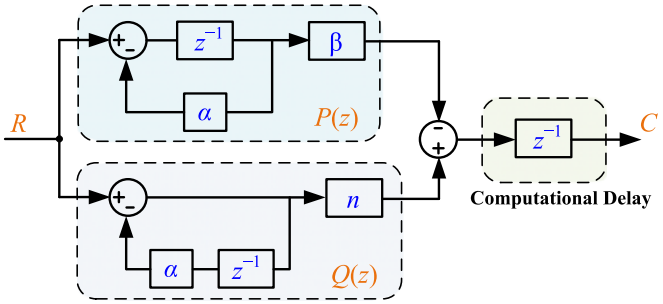


Fig. 20. Block diagram of the proposed compensation method.

### B. Implementation of the Proposed Method

In the digital microprocessor, the data collected from the past steps can be put in the buffer, and these data can be used for future data prediction. For the prediction of the $k$th step $c(k)$, the data at $(k-1)$th step, i.e., $r(k-1)$ and $c(k-1)$ are required along with the data at $(k-2)$th step $r(k-2)$. Equation (21) will provide the calculation rule for $c(k)$. Deduced from (21), the discrete transfer function of the compensation block can be expressed as

$$\frac{C(z)}{R(z)} = \frac{(1+\alpha+\beta)-\beta\cdot z^{-1}}{1+\alpha\cdot z^{-1}}\cdot z^{-1}$$

$$H^*(z) = \frac{(1+\alpha+\beta)-\beta\cdot z^{-1}}{1+\alpha\cdot z^{-1}}. \tag{23}$$

From (24), the proposed scheme actually is also an IIR digital filter. According to the transfer function mentioned above, the block diagram of the improved compensator is presented in Fig. 20. The coefficient $n$ is equal to $1+\alpha+\beta$.

### C. Parameter $\beta$ Tuning

When the coefficient $\beta = 0$, then the proposed compensation scheme returns to the FOF method. The introduction of $\beta$ makes the compensated signal closer to the ideal signal. The $\beta$ value determines the phase lead extent of the proposed method. A high value of $\beta$ leads to better compensation effects, but would have a larger magnitude near the Nyquist frequency, reducing its immunity to the effects of harmonics in the input signal. On the contrary, a low value for $\beta$ makes the compensation effects unsatisfactory. Fig. 21 shows the Bode diagrams for different $\beta$ values from 0 to 2 with a fixed $\alpha = 0.95$. Considering these constrains, the value of $\beta$ is set to below 1.

### D. Comparison of Time-Delay Compensation Schemes

Fig. 22 compares the frequency responses of the delay compensation schemes mentioned in previous sections. The parameters are listed in Table I. For the shifted sampling instant method, the middle of the sampling period ($\lambda = 0.5$) is selected, whose equivalent expression can be written as $z^{\wedge}0.5$. It can be seen that all these methods can provide phase lead to compensate the delay. Among them, the proposed method provides the best compensation effect, next is shifted sampling instant method and the FOF scheme, then is the SOGI-based scheme and worst is the linear predictor. On the other hand, all the digital-filter-based methods but the *linear predictor* are sensitive to the magnitude amplifications nearby the Nyquist frequency. A compromise between the magnitude gain and phase lead is thus needed in their parameter design.

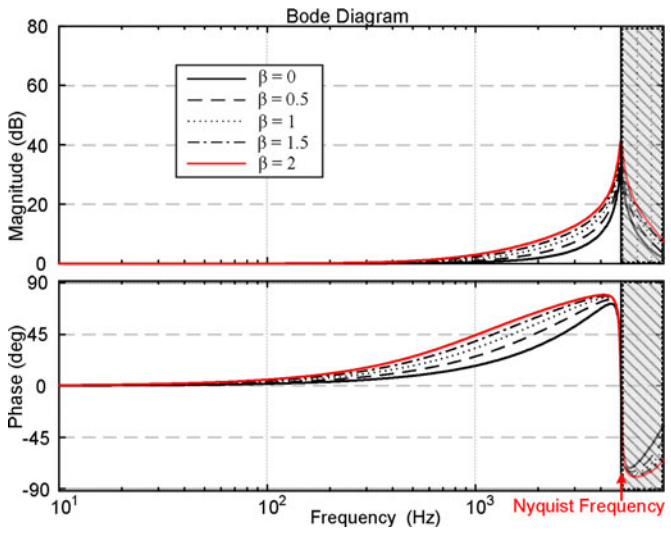


Fig. 21. Different $\beta$ values for the proposed delay compensation scheme.

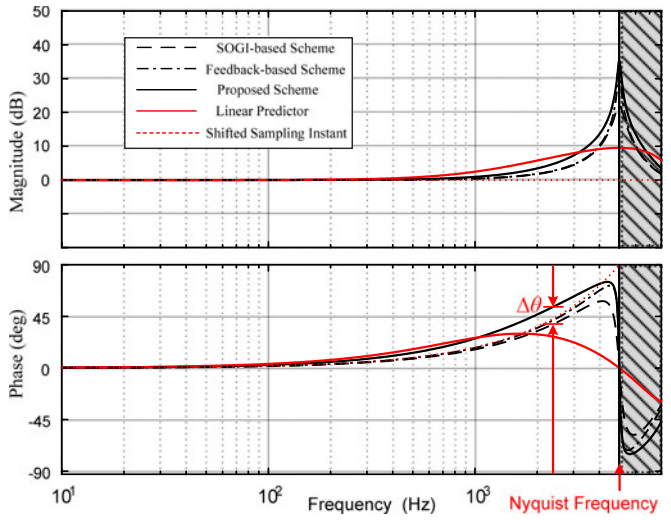


Fig. 22. Comparison of the phase lead of four compensation schemes.

TABLE I
SYSTEM PARAMETERS

| SOGI-Based Scheme | | FOF Scheme | |
|---|---|---|---|
| $\omega'$ | 5000 rad/s | $\lambda$ | 1 |
| $k$ | 1.414 | $\alpha$ | 0.95 |
| $\omega_c$ | 3140 rad/s | $m$ | 1.95 |
| **Linear Predictor** | | **Proposed Scheme** | |
| $T_d$ | $T_s$ | $\alpha$ | 0.95 |
| $L(z)$ | $2-z^{-1}$ | $\beta$ | 0.5 |

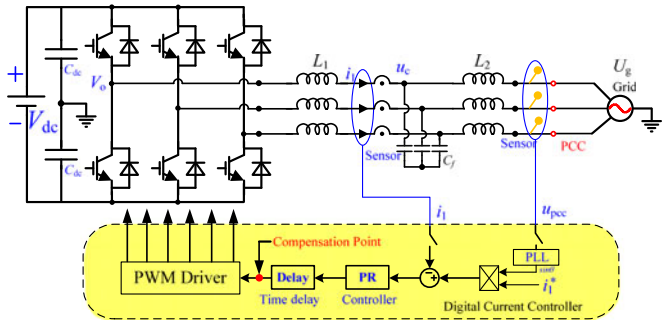


Fig. 23. Application example with the grid-connected inverter.

## V. Application Example for the Proposed Method

### A. Basic Analysis

In order to verify the effectiveness of the proposed method and compare the compensation results of different methods, an application example is, therefore given, and analyzed, whose topology is presented in Fig. 23—a three-phase voltage source inverter connected to the power grid through an output *LCL* filter, along with the basic control diagram, where the proportional resonant (PR) controller is adopted. The current control regulates the current injected into the utility grid to improve the current waveform quality. $L_1$ is the inverter-side inductor, $C_f$ is the ac capacitor to filter the switching frequency harmonics, and $L_2$ is the grid-side inductor. The converter-side current $i_1$ is the controlled variable for current control and also inverter protection. The point of common coupling voltage is measured for grid synchronization.

By neglecting equivalent series resistance (ESR) of filtering elements [32], the transfer function of the system mentioned above can be obtained

$$G_{i1}(s) = \frac{i_1(s)}{V_0(s)} = \frac{s^2 L_2 C_f + 1}{s^3 L_1 L_2 C_f + sL_1 + sL_2} \tag{24}$$

where $V_0$ and $i_1$ are bridge mid-point voltage and inverter-side current, respectively. To match the discrete expressions of these delay compensation methods, the analysis is purposely progressed in $z$-domain. The open-loop transfer function in discrete domain is

$$G_{\text{open}}(z) = K_p \cdot z^{-1} \cdot Z\left[\frac{s^2 L_2 C_f + 1}{s^3 L_1 L_2 C_f + sL_1 + sL_2}\right] \tag{25}$$

where $K_p$ is the proportional gain, $z^{-1}$ is the time delay, and the impact of resonant part in the PR controller is omitted because it functions at the fundamental frequency.

As concluded in [10], the system is always stable regardless of the *LCL* and controller parameters without considering delay. Thus, decreasing the delay is straightforward to stabilize the system. Therefore, the compensation effects of the methods mentioned in previous section can be demonstrated through turning an unstable system to a stable system. Fig. 24 shows the root loci when different compensation methods are applied. The system parameters are listed in Table II. It can be observed that two poles of the system are always out of the unit circle when no compensation method is added, then the system is unstable. When previously mentioned four delay compensation schemes are added respectively, different system stable ranges and poles locations are observed in Fig. 24. All the four delay compensation methods can pull these unstable poles re-entering the unit circle. In agreement with the analysis in Section III, the proposed compensation provides best compensation result and stability enhancement.

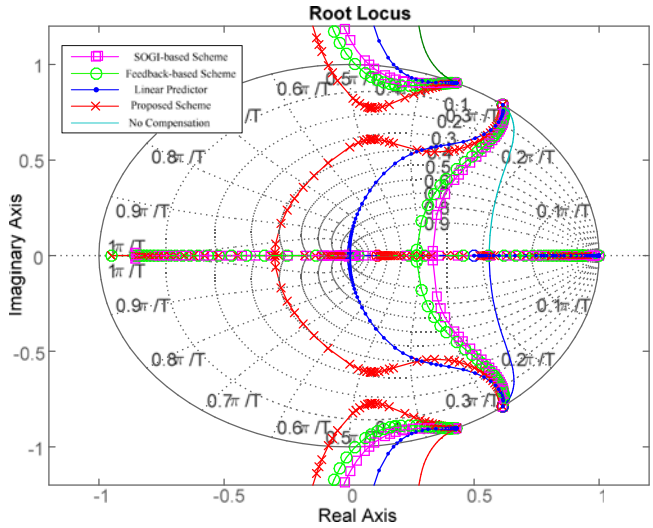


Fig. 24. Root loci for different compensation schemes.

TABLE II
*LCL*-Filtered Inverter Parameters

| | | |
|---|---|---|
| **Nominal System Parameters** | | |
| Power Rating | $S$ | 10 kW |
| Grid Voltage | $U_g / f_g$ | 220 V/50 Hz |
| DC voltage | $V_{\text{dc}}$ | 730 V |
| Current reference | $I_{\text{ref}}$ | 10–5 A |
| Sampling frequency | $f_s$ | 10 kHz |
| Switching frequency | $f_{\text{sw}}$ | 10 kHz |
| **Parameters of *LCL*-filter** | | |
| Converter-side inductor | $L_1$ | 3 mH |
| Filter capacitor | $C_f$ | 7 $\mu$F |
| Grid-side inductor | $L_2$ | 1.8 mH |
| Resonance frequency | $f_r$ | 1.80 kHz |

### B. Simulation Results

Time-domain simulations have been performed by using the parameter listed in Table II. It is worth mentioning that sampling frequency chosen for this analysis is equal to switching frequency. In fact, the analysis also applies to the double sampling frequency case. In the simulation model, the ESRs of the inductors are set to 0.2 Ω to emulate the real system. Fig. 25(a) and (b) shows the grid voltage $U_g$ and grid currents with linear predictor, SOGI-based scheme, respectively. Looking at the grid current behavior after turning the current reference from 10 to 5 A, it can be observed that the system dynamics differ from each other with different delay compensation methods.

In Fig. 25(a), the system exhibits significant current oscillations, indicating that the phase margin is relatively lower. This situation clearly indicates the importance of digital time-delay

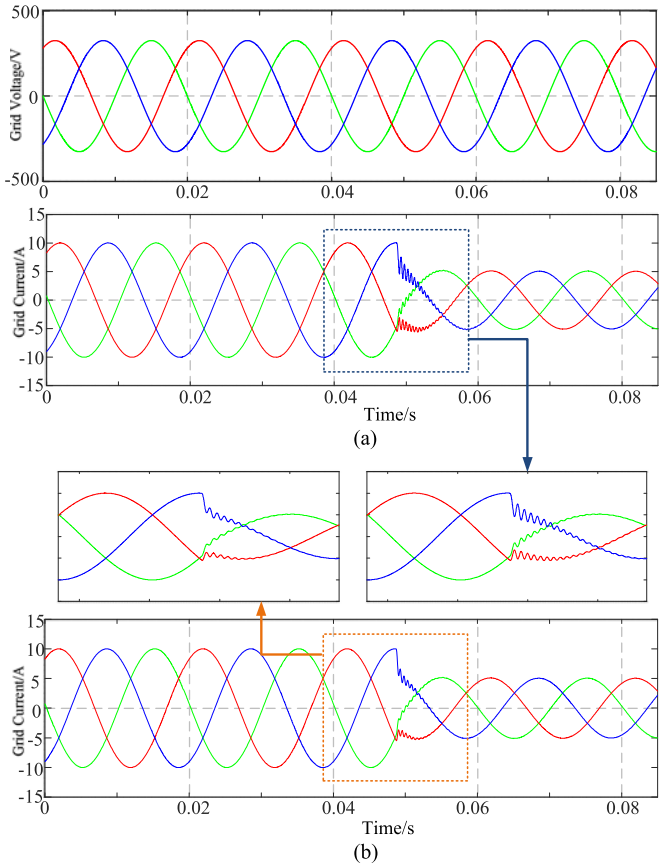


Fig. 25. Simulation results (a) linear predictor and (b) SOGI-based scheme.

minimization in the current loop for grid connected inverter applications. Fig. 25(b) shows the simulation results where the linear predictor is replaced by the SOGI-based method. Clearly, the dynamic response gets improved with shorter settling time. This improvement is, of course, brought by the current control loop bandwidth broadened. Fig. 26(a) and (b) shows the same operating conditions and the same control parameters but using the FOF delay compensation scheme and proposed method. For the proposed scheme, the dynamic improvement is significant, which is in agreement with the root loci analysis in Fig. 24.

### C. Experimental Results

The control scheme is realized with a dSPACE DS1007 platform, whose output PWM signals are channeled through fiber optic cables to the Danfoss inverter. The inverter is then connected to the Chroma 61800 grid simulator acting as the ideal grid, while the input dc-link voltage is provided by a Yaskawa D1000 regenerative converter. Four compensation methods as presented in Fig. 27, including linear predictor, SOGI-based method, FOF method, and the proposed scheme in this paper have been prepared for the testing.

At first, Fig. 28 shows the experiment results on accurately measuring digital delays in the loop gain. An ideal continuous sinusoidal signal from a signal generator (BK Precision

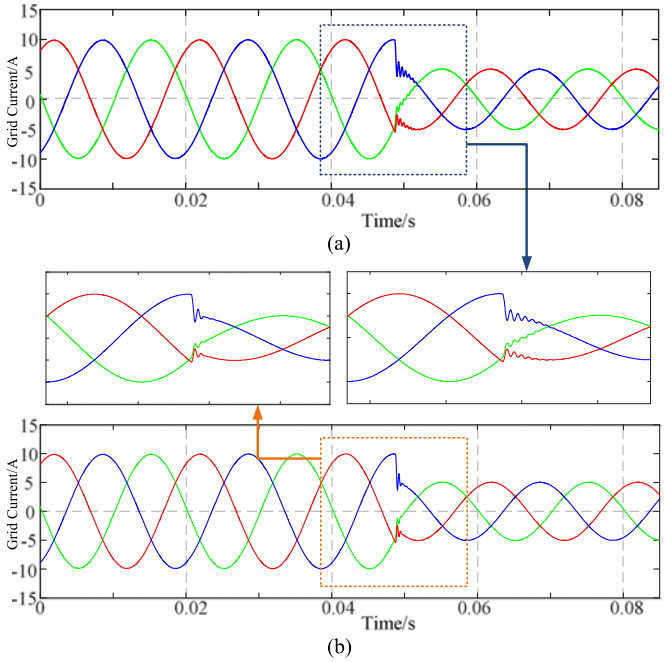


Fig. 26. Simulation results (a) FOF scheme and (b) proposed scheme.

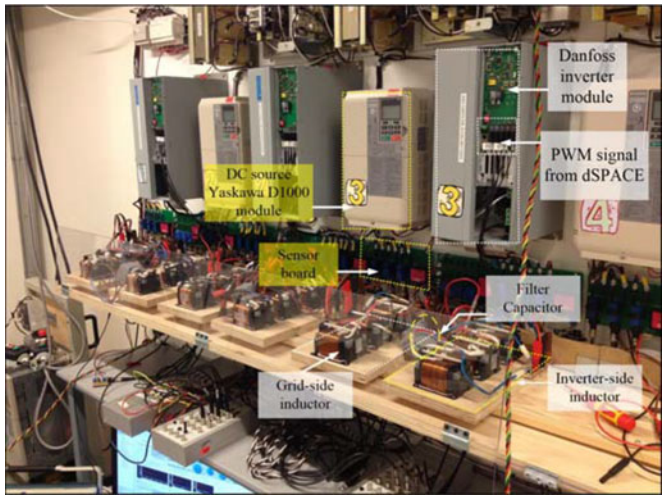


Fig. 27. Experiment setup photo with the three-phase grid inverter.

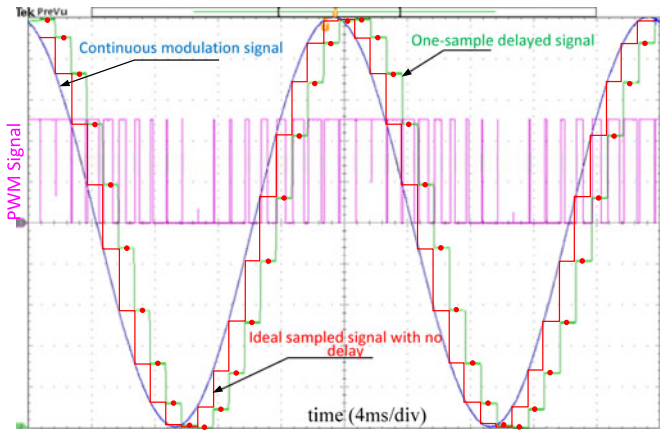


Fig. 28. Time delay in the digital controller.

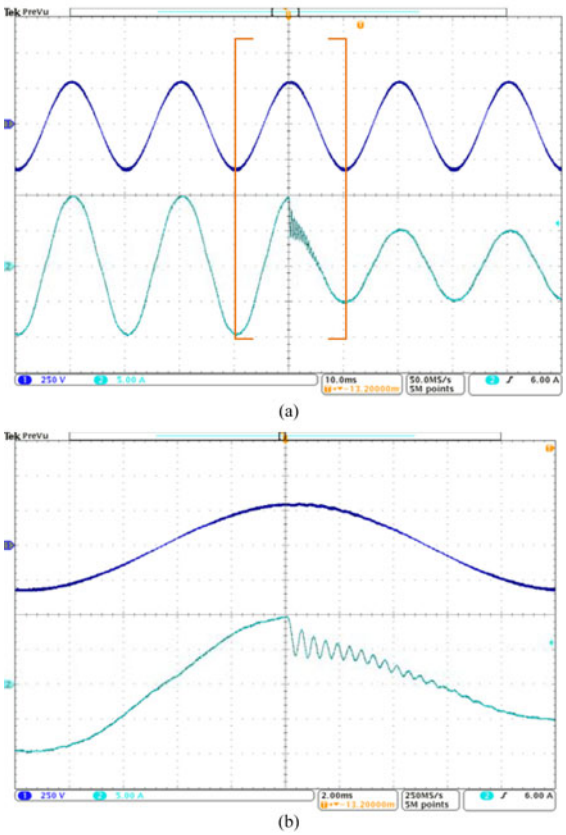


Fig. 29. Dynamic response with the linear predictor: (a) 10–5 A and (b) zoom in.

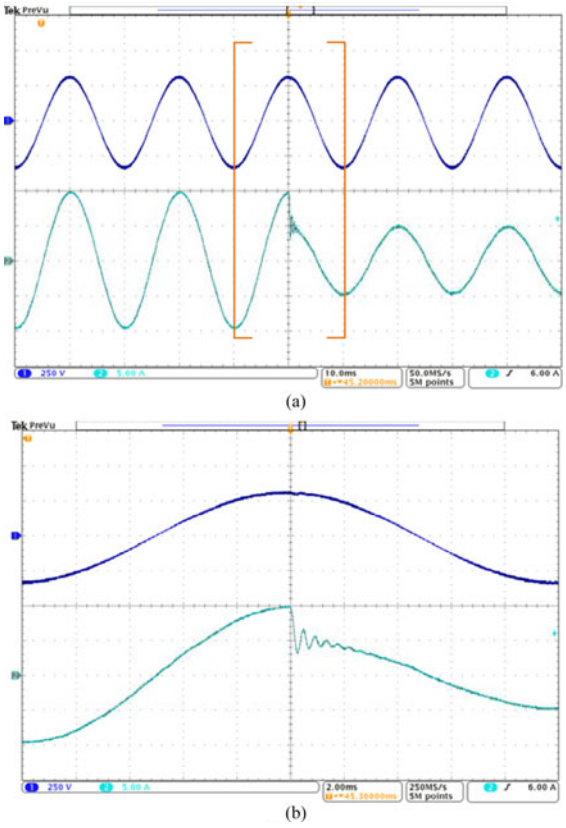


Fig. 30. Dynamic response with SOGI-based method scheme: (a) 10–5 A and (b) zoom in.

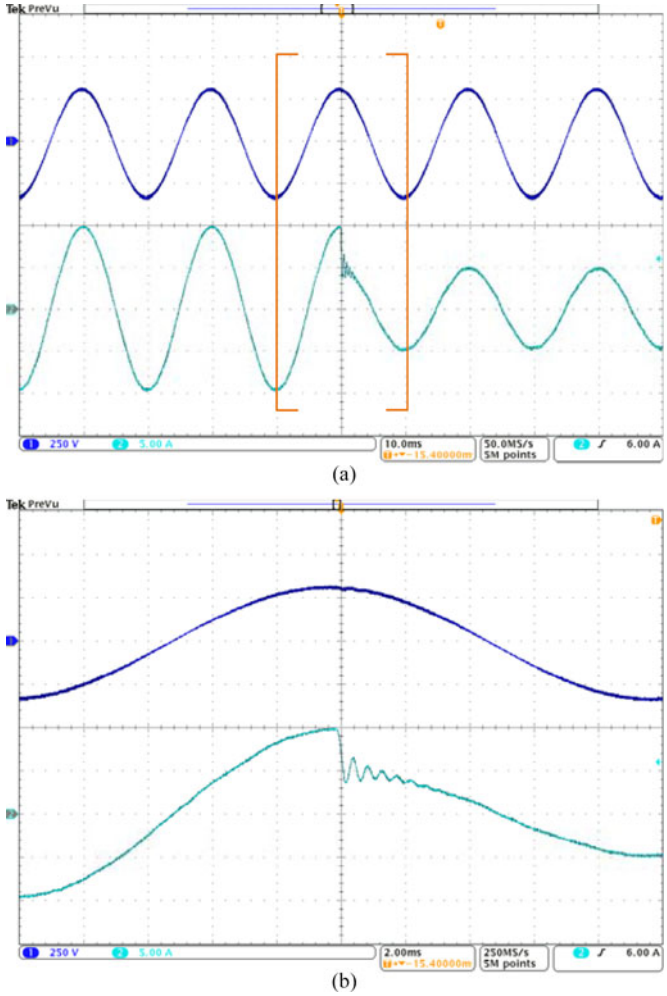


Fig. 31. Dynamic response with the FOF scheme: (a) 10–5 A and (b) zoom in.

4065) acts as the modulation waveform. The stair-step waveform is the actual digital modulation signal in the digital controller compared with triangular carrier to generate PWM signal. It is delivered and displayed on the scope by means of digital to analog convertor. From the voltage-second balance point of view, the digital modulation signal is equivalent to the dashed sinusoidal signal. To clearly display the digital delays, both the switching frequency and sampling frequency are selected as 1 kHz.

To compare the delay compensation effects of these delay compensation methods, it should be assured that the external conditions are the same: the same filter parameters, the same control parameters, and the same operating conditions. The dynamic responses of the grid current from 10 to 5 A are compared. Figs. 29–32 present the dynamic response results for these four delay compensation methods. The comparison results are presented: The linear predictor presents more than 10 settling cycles; the SOGI-based scheme has about 5 settling cycle; similarly, the FOF scheme presents about 5 settling cycles. The proposed scheme has the best dynamic performance; it only has one settling cycle. The experimental results are in agreement with the simulations and the analysis outcomes.

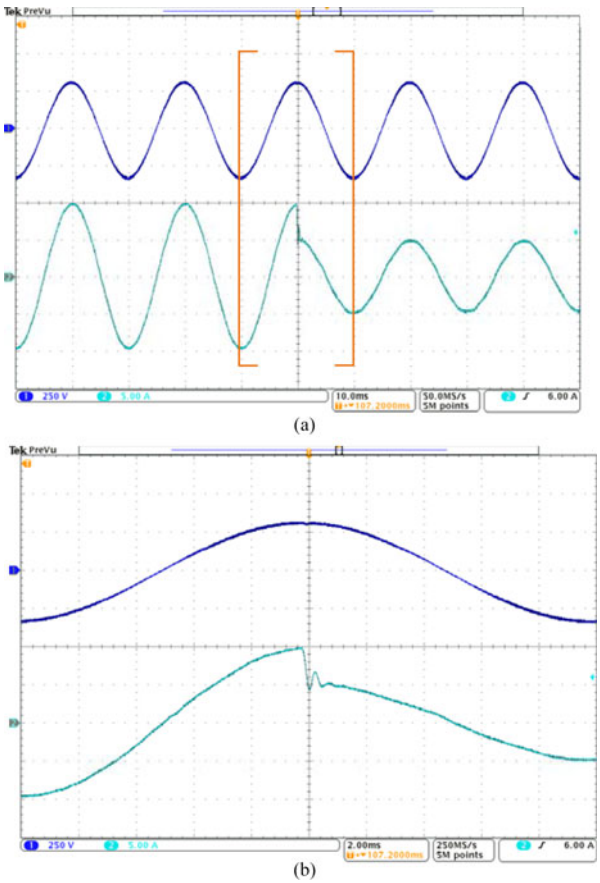


Fig. 32. Dynamic response with proposed compensation scheme: (a) 10–5 A and (b) zoom in.

## VI. Conclusion

The paper investigates the time-delay compensation methods for the digitally controlled power-electronics converters. The essence of various time-delay compensation methods is revealed through a graphical comparative evaluation. A practical and straightforward compensation method with superior compensation effect is proposed in this paper. Compared with existing delay compensation strategies, the proposed time-delay compensation scheme is supposed to be a potentially attractive alternative to the conventional methods. An application example is prepared to verify the theoretical analysis in the paper. Experimental results comparing the dynamic responses of four compensation schemes verify the effectiveness of the proposed compensation method.

## Appendix I

If the area $S_1$ is used to substitute the area $S_0$ as shown in Fig. 12, the relationship between the compensated $c(k)$ and previous data can expressed as follows:

$$\underbrace{c(k)\cdot T_s}_{A_3} = \underbrace{r(k-1)\cdot T_s}_{A_0} + \overbrace{\alpha\underbrace{\{r(k-1)-c(k-1)\}\cdot T_s}_{A_1}}^{A_2} + \overbrace{\beta\cdot\{r(k-1)-c(k-1)\}\cdot T_s}^{A_4}. \quad \text{(A.1)}$$

According to (A.1), the discrete transfer function can be deduced as

$$\frac{C(z)}{R(z)} = \frac{1+\alpha+\beta}{1+(\alpha+\beta)\cdot z^{-1}}\cdot z^{-1}. \quad \text{(A.2)}$$

Then, the obtained compensator $H*(z)$ is given as

$$H^*(z) = \frac{1+\alpha+\beta}{1+(\alpha+\beta)\cdot z^{-1}}. \quad \text{(A.3)}$$

It is noteworthy that $H*(z)$ has a similar mathematical formulation with FOF compensation scheme shown in (6). The only difference is the additional coefficient $\beta$. Therefore, it has the delay compensation ability. However, the additional coefficient $\beta$ makes the term $\alpha+\beta$ larger than the unit value, bringing an unstable pole outside of the unit circle in the $z$-domain.

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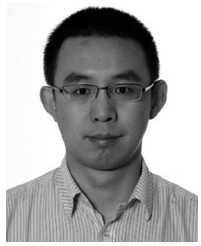

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