Design of Class E Power Amplifier with New Structure and Flat Top Switch Voltage Waveform

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***Abstract*—In this paper, a new topology of the class E power amplifier (PA) is proposed. The output circuit in the proposed PA is different from that in the conventional class E PA. The conventional output circuit of class E PA consists of shunt capacitor, resonant capacitor, resonant inductor, and shifting inductor. An additional shunt capacitance is added between the resonant capacitance and the shifting inductor to shape the reduced switch voltage. The peak switch voltage of the proposed class E PA is approximately 78% of that of the conventional one, which shows a reduction in peak switch voltage. The lower peak switch voltage reduces the breakdown voltage of the active device. Also, the proposed structure can introduce a new family of switching PAs with interesting specifications. Several values of switch voltage reduction and output power capability could be achieved by varying the circuit elements. Zero voltage and zero derivative switching conditions are achieved in the switch voltage of the designed circuit. The simulation of the proposed circuit is performed using PSpice software. For verification, the presented PA is fabricated and measured.**

***Index Terms*—Class E power amplifier (PA), flat top switch voltage, high efficiency, MOSFET , shunt capacitance, zero voltage and zero derivative switching (ZVS and ZDS) conditions.**

I. Introduction

HIGH operating frequency and high power conversion efficiency are the most important figures of merits for evaluating the power amplifiers (PAs) [1]–[3]. According to the growing demand for high-efficiency PAs [4]–[6], the class E PA has become more popular due to high conversion efficiency and good performance at high frequencies [7]. It has many applications at high frequencies, such as mobile and portable communications systems, fluorescent lamp ballasts, RF heating, induction generation of plasma, lasers, portable light sources, dc/dc converters, LED drivers, frequency multipliers, rectifiers, etc. [8]–[12].

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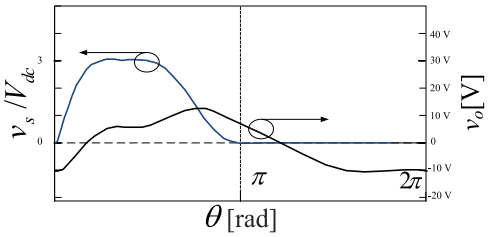

Fig. 1. Obtained results from the circuit presented in [26].

The zero voltage and zero derivative switching (ZVS and ZDS) conditions are essential for class E PA to achieve zero switching loss, low noise, and high efficiency at high frequencies [10]. ZVS high-efficiency PA will be achieved by shaping the output voltage and current waveforms [13].The maximum theoretical drain voltage in the conventional ZVS class E PA with only external linear capacitance is 3.56 $V_{\rm dc}$ [7], where $V_{\rm dc}$ is the dc supply voltage of the amplifier. However, this value in ZVS-type class E amplifiers may be obtained as high as 4.5 $V_{\rm dc}$, considering the MOSFET parasitic capacitances [14]–[17]. Therefore, this value is higher than 3.56 $V_{\rm dc}$ in practice. High peak drain voltage is a limitation of class E PA. For instance, the drain voltage cannot exceed a significant value, because of breakdown drain-to-source voltage of the MOSFET, which limits the output power of the PA. Moreover, the high peak switch voltage results in a lower power output capability, considering constant peak switch current.

Several methods have been presented to reduce the peak switch voltage of the class E PA. Zener diodes are used in [18] to reduce the peak switch voltage; however, a loss is occurred in the Zener diode. Recently, an inverse class E PA has been introduced, which produces 20% lower peak switch voltage than the conventional class E PA [19]–[21]. Also, family of E/F amplifiers have been presented with reduced switch voltage as compared to the conventional class E [22]–[25]. In [26], a class E PA with flat top switch voltage is introduced using an extra output resonant circuit, tuned to second harmonic. In this approach, a peak switch voltage of about $3V_{\rm dc}$ is achieved. However, the output voltage is not pure sinusoidal and it is extremely deformed in this amplifier. The waveforms of this approach are shown in Fig. 1. So far, several class E new structures have been

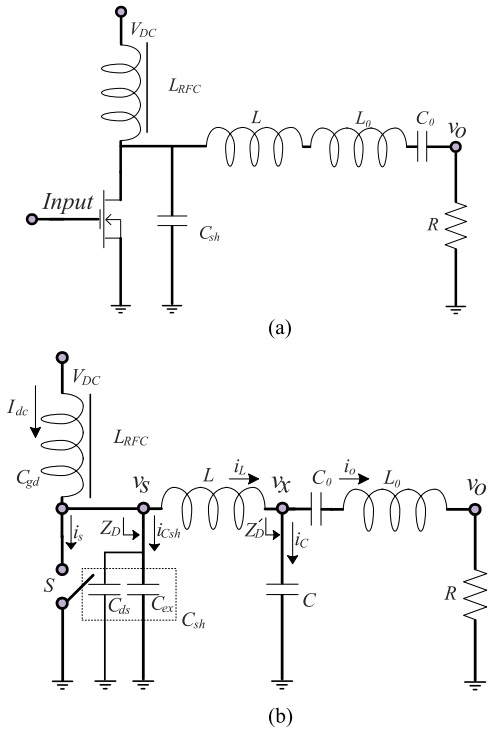

Fig. 2. Equivalent circuit of (a) conventional and (b) proposed class E power amplifiers.

introduced to improve the amplifier specifications [27]–[31]. However, to the best of authors' knowledge, there is no structure to reduce the voltage stress without deficiencies of other amplifier parameters.

The flat top switch voltage waveform leads to reduction of transistor peak voltage and peak current, compared with the values in conventional class E. Therefore, more output power can be achieved with the same amount of stress [26]. Lower peak switch voltage also reduces the possibility of the device failure due to the transistor breakdown mechanisms and therefore relaxes the breakdown voltage constraints of the active device [19]. In this paper, a new structure of PA is presented in order to reduce the peak switch voltage, compared with the conventional class E PA.

II. Structure of the Proposed Power Amplifier

A conventional class E PA structure is shown in Fig. 2(a). It consists of dc supply voltage ($V_{\rm dc}$), MOSFET device, shifting inductor (*L*), resonant inductor (L_0), resonant capacitance (C_0), shunt capacitance ($C_{\rm sh}$), load resistance (*R*), and dc-feed inductance ($L_{\rm RFC}$). The shifting inductor (*L*) shifts the phase of the output current, while resonant inductor (L_0) with resonant capacitance (C_0) form an ideal filter to resonate at the operating frequency [14]. An equivalent circuit of the proposed switching PA is depicted in Fig. 2(b). In this figure, the MOSFET is modeled with an ideal switch and the MOSFET intrinsic shunt capacitance ($C_{\rm ds}$). As seen in Fig. 2(b), unlike the conventional circuit, a shunt capacitance (*C*) is added between the resonant capacitance (C_0) and the shifting inductor (*L*). The shifting inductor shifts the output voltage phase

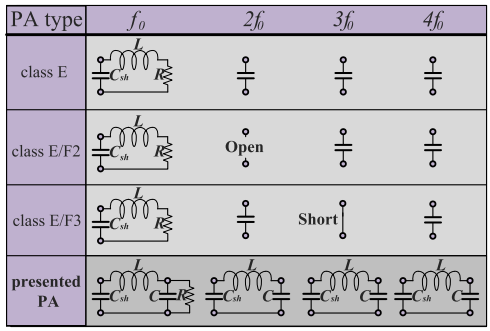

Fig. 3. Comparison between different switching PAs versus harmonics.

and also shapes the drain voltage waveforms with capacitances *C* and $C_{\rm sh}$. The resonant circuit is designed to resonate at the operating frequency, which is 1 MHz. In this paper, the intrinsic MOSFET parasitic capacitance ($C_{\rm ds}$), along with the external capacitance ($C_{\rm ex}$), is considered as the shunt capacitance ($C_{\rm sh}$).

In the proposed PA, the ZVS and ZDS conditions can be satisfied, which guarantee high efficiency and zero-switching loss at high frequencies. As seen in Fig. 3, the presented circuit shows different behavior versus harmonics, compared with other structures. In the main harmonic, the series resonant circuit (L_0C_0) will be shorted, and in the other harmonics, series resonant circuit will be opened. According to Fig. 3, the presented *LC* network placed between the switching node and the load can be designed to have different impedances at different frequencies, which results in different switch voltage shapes. Therefore, other variations of the switch voltage waveform can be obtained by changing the values of circuit elements. In a special case of the presented structure, when the *L* and *C* elements resonate at third harmonic, the circuit will be similar to class $\rm E/F_3$ PA in second, third, and fourth harmonic, but it is different in the fundamental harmonic. Full detailed study of class E/F family amplifiers could be found in [22]–[25].

III. Analysis of the Presented Circuit

The assumptions, which are considered to analyze the designed amplifier, are presented in Table I. During the first half of the period, the input voltage is zero and the switch is OFF. Therefore, a KCL node equation for v_s node according to Fig. 2(b) gives the following equation:

$$I_{\rm dc} = i_L + i_{C_{\rm sh}}. \tag{1}$$

Another KCL node equation for v_x gives

$$i_L = i_C + i_o \tag{2}$$

where i_o is the output current and can be assumed as a pure sinusoidal waveform due to the output series resonant circuit

$$i_o = I_m \sin(\theta + \varphi). \tag{3}$$

In (3), I_m is output current amplitude, $\theta = \omega t$ is angular time, and φ is the phase shift between the source voltage and the output current. Substituting (2) and (3) into (1) and applying the

TABLE I
ASSUMPTIONS OF THE ANALYSIS

	Assumptions
1	INPUT VOLTAGE DUTY CYCLE IS CONSIDERED $D = 0.5$
2	INPUT VOLTAGE IS A SQUARED VOLTAGE, WHICH IS ZERO DURING$0 \leq \theta < \pi$. THE INPUT VOLTAGE IS HIGH DURING$\pi \leq \theta < 2\pi$.
3	THE MOSFET parasitic capacitance is assumed linear.
4	THE MOSFET is assumed as an ideal switch and the on resistance is not considered in the analysis.
5	VALUE OF DC CURRENT IS CONSIDERED CONSTANT, ACCORDING TO HIGH VALUE OFL_{RFC}.
6	ACCORDING TO HIGH VALUE OF LOADED QUALITY FACTOR (Q), the output current is assumed pure sinusoidal.
7	ZVS AND ZDS CONDITIONS ARE SATISFIED IN THE AMPLIFIER.
8	VALUE OF$1/\omega\sqrt{LC}$ is assumed to be 3, due to the flattop switch voltage waveform.

currents of capacitors result in

$$I_{\mathrm{dc}} = \omega C_{\mathrm{sh}} \frac{dv_s}{d\theta} + \omega C \frac{dv_x}{d\theta} + I_m \sin(\theta + \varphi). \tag{4}$$

The shunt capacitance in this paper is assumed to be linear for the sake of simplicity. Using the inductance voltage relation and substituting i_L from (1) lead to

$$v_L = v_s - v_x = \omega L \frac{di_L}{d\theta} = -\omega^2 LC_{\mathrm{sh}} \frac{d^2 v_s}{d\theta^2}. \tag{5}$$

Integrating both sides of (4) gives

$$v_s + G v_x = h(\theta) \tag{6}$$

where G and $h(\theta)$ are defined as

$$G = \frac{C}{C_{\mathrm{sh}}} \tag{7}$$

and

$$h(\theta) = \frac{\theta I_{\mathrm{dc}} + I_m [\cos(\theta + \varphi) - \cos(\varphi)]}{\omega C_{\mathrm{sh}}} + G v_{x0}. \tag{8}$$

The switch voltage differential equation can be obtained using (5) and (6)

$$\frac{d^2 v_s}{d\theta^2} + \frac{1 + G}{\omega^2 LC} v_s = \frac{h(\theta)}{\omega^2 LC}. \tag{9}$$

The switch voltage equation of the proposed circuit can be achieved by solving (9) as follows:

$$\begin{aligned} v_s = {} & C_1 \sin\left(\theta \sqrt{\frac{1 + G}{\omega^2 LC}}\right) + C_2 \cos\left(\theta \sqrt{\frac{1 + G}{\omega^2 LC}}\right) \\ & + \frac{\theta I_{\mathrm{dc}}}{\omega C_{\mathrm{sh}}(1 + G)} - \frac{I_m \cos(\theta + \varphi)}{\omega C_{\mathrm{sh}}(\omega^2 LC - (1 + G))} \\ & - \frac{I_m \cos\varphi}{\omega C_{\mathrm{sh}}(1 + G)} + \frac{G v_{x0}}{(1 + G)}. \end{aligned} \tag{10}$$

The ZVS and ZDS conditions can be satisfied in the achieved switch voltage in (10). Parameters of the switch voltage equations can be calculated using boundary conditions.

In the next step, the switch current will be analyzed in order to determine the unknown coefficients of the switch voltage. The switch current is zero during the first half of the period ($0 \leq \theta < \pi$). At the second half of the period ($\pi \leq \theta < 2\pi$), the switch current can be written as

$$I_{\mathrm{dc}} = i_s + i_L. \tag{11}$$

The waveform of i_L can be obtained from (2)

$$i_L = \omega C \frac{dv_x}{d\theta} + I_m \sin(\theta + \varphi). \tag{12}$$

The following equation could be written for the voltage of L:

$$v_x = -\omega L \frac{di_L}{d\theta}. \tag{13}$$

Using (11), v_x can be written as

$$v_x = \omega L \frac{di_s}{d\theta}. \tag{14}$$

From (11) and (12), the switch current can be determined as

$$i_s = I_{\mathrm{dc}} - i_L = I_{\mathrm{dc}} - \omega C \frac{dv_x}{d\theta} - I_m \sin(\theta + \varphi). \tag{15}$$

According to (14) and (15), the switch current differential equation can be obtained as

$$\omega^2 LC \frac{d^2 i_s}{d\theta^2} + i_s = I_{\mathrm{dc}} - I_m \sin(\theta + \varphi). \tag{16}$$

By solving (16), the switch current can be achieved

$$\begin{aligned} i_s = {} & C_1{}' \sin\left(\frac{\theta}{\omega\sqrt{LC}}\right) + C_2{}' \cos\left(\frac{\theta}{\omega\sqrt{LC}}\right) \\ & + I_{\mathrm{dc}} - \frac{I_m \sin(\theta + \varphi)}{1 - \omega^2 LC}. \end{aligned} \tag{17}$$

The current is zero during the switching time. Therefore, the coefficient $C_2{}'$ can be obtained, as written in (18). In the design of the presented structure, the value of $1/\omega\sqrt{LC}$ is equal to 3, due to the third harmonic existence in the switch current. Also, this value consideration results in flat top switch voltage for class E amplifier

$$C_2{}' = I_{\mathrm{dc}} + \frac{I_m \sin(\varphi)}{1 - \omega^2 LC}. \tag{18}$$

The coefficient $C_1{}'$ can be calculated using Fourier formula, which is given by

$$I_{\mathrm{dc}} = \frac{1}{2\pi} \int_0^{2\pi} i_s(\theta)\, d\theta. \tag{19}$$

After applying (17) and (18) in (19), the coefficient $C_1{}'$ is achieved, which is written as

$$C_1{}' = \frac{3}{2} \left[\frac{2 I_m \cos(\varphi)}{1 - \omega^2 LC} - \pi I_{\mathrm{dc}} \right]. \tag{20}$$

According to (14) and (17), the voltage v_x can be written as

$$v_x = 3\omega LC_1{}' \cos(3\theta) - 3\omega LC_2{}' \sin(3\theta) - \frac{\omega LI_m \cos(\theta+\varphi)}{1-\omega^2 LC}. \quad (21)$$

The boundary conditions of v_x can be calculated using (20) and (21), which are

$$v_{x_0} = v_{x_{2\pi}} = -v_{x_\pi} = \frac{I_m \cos(\varphi) - I_{\rm dc}(\pi/2)}{\omega C}. \quad (22)$$

Comparing (4) at $\theta = 0$ and (15) at $\theta = 2\pi$ results in

$$i_s(2\pi) = \omega C_{\rm sh} \frac{dv_s}{d\theta}\,|_{\theta=0}\ . \quad (23)$$

From (17), $i_s(2\pi)$ can be found as

$$i_s(2\pi) = 2I_{\rm dc}. \quad (24)$$

Using (23) and (24) in (10), the first coefficient of switch voltage C_1 can be obtained

$$C_1 = \frac{1}{q\omega C_{\rm sh}}\left[2I_{\rm dc} - \frac{I_{\rm dc}}{(1\ +\ G)} - \frac{I_m \sin(\varphi)}{\omega^2 LC - (1\ +\ G)}\right]. \quad (25)$$

In order to find C_2, the boundary condition of switch voltage can be applied. The switch voltage is zero at $\theta = 0$. Therefore

$$C_2 = \frac{I_m \cos(\varphi)}{\omega C_{\rm sh}}\left[\frac{1}{\omega^2 LC - (1\ +\ G)} + \frac{1}{1\ +\ G}\right] - \frac{Gv_{x_0}}{1\ +\ G}. \quad (26)$$

The ZVS and ZDS conditions must be also satisfied in (10), which result, respectively, in

$$C_1 \sin(q\pi) + C_2 \cos(q\pi) + \frac{\pi I_{\rm dc}}{\omega C_{\rm sh}(1+G)} + \frac{I_m \cos(\varphi)}{\omega C_{\rm sh}}\left[\frac{1}{\omega^2 LC-(1+G)} - \frac{1}{1+G}\right] + \frac{Gv_{x_0}}{1+G} = 0 \quad (27)$$

and

$$qC_1 \cos(q\pi) - qC_2 \sin(q\pi) + \frac{I_{\rm dc}}{\omega C_{\rm sh}(1\ +\ G)} - \frac{I_m \sin(\varphi)}{\omega C_{\rm sh}[\omega^2 LC - (1\ +\ G)]} = 0 \quad (28)$$

where q is defined as

$$q = \sqrt{\frac{1\ +\ G}{\omega^2 LC}}. \quad (29)$$

According to 100% efficiency and zero switching loss in the amplifier, the following relation between input and output powers can be written:

$$I_{\rm dc}V_{\rm dc} = \frac{1}{2}R{I_m}^2. \quad (30)$$

Applying the obtained C_1 and C_2 in (28), I_m and $I_{\rm dc}$ can be obtained

$$\alpha I_{\rm dc} = \beta I_m \quad (31)$$

where α and β are defined as

$$\alpha = \frac{2(1\ +\ G)\cos(q\pi) - \cos(q\pi) - \frac{q\pi}{2}\sin(q\pi) + 1}{(1\ +\ G)} \quad (32)$$

and

$$\beta = \frac{\cos(q\pi)\sin\varphi + q\sin(q\pi)\cos\varphi + \sin\varphi}{\omega^2 LC - (1\ +\ G)}. \quad (33)$$

Using (30)–(33), the amplitude of the output current can be determined

$$I_m = \frac{2\beta V_{\rm dc}}{\alpha R}. \quad (34)$$

Also, $I_{\rm dc}$ can be found as

$$I_{\rm dc} = \frac{2\beta^2 V_{\rm dc}}{\alpha^2 R}. \quad (35)$$

Due to the zero dc supply voltage drop across the dc-feed, the average value of v_s over the period is equal to

$$V_{\rm dc} = \frac{1}{2\pi}\int_0^{2\pi} v_s(\theta)\,d\theta. \quad (36)$$

The two unknown parameters of φ and R can be calculated using (27) and (36). After finding all of the design parameters, the specifications of class E could be studied according to the obtained equations. One of the important specifications of class E amplifier is output power capability (C_P) parameter. The output power capability is usually used to study the output power of the amplifier. The C_P equation could be defined as [10]

$$c_P = \frac{P_{o(\max)}}{v_{s(\max)} i_{s(\max)}} = \frac{1}{\frac{v_{s(\max)}}{V_{\rm dc}}\frac{i_{s(\max)}}{I_{\rm dc}}} \quad (37)$$

where $v_{s(\max)}$ and $i_{s(\max)}$ are maximum switch voltage and maximum switch current, respectively. The impedance of the output structure, which is shown in Fig. 2 as Z_D, explains the harmonic behavior of the presented amplifier switch voltage. To calculate the value of Z_D at the operating frequency, at first, the value of Z_D' is calculated in (38) and then, the value of Z_D is obtained. The series resonant circuit will be shorted in the operating frequency

$$Z_D' = \frac{R}{jRC\omega + 1}. \quad (38)$$

Therefore, value of Z_D will be obtained as

$$Z_D = \left(jL\omega + \frac{R}{jRC\omega + 1}\right)\left\|\frac{1}{jC_{\rm sh}\omega}\right.. \quad (39)$$

Equation (39) could be rewritten as follows:

$$Z_D = \frac{R\left(1-\omega^2 LC\right) + jL\omega}{(1-\omega^2 LC_{\rm sh}) + jR\omega\left(C + C_{\rm sh} - LCC_{\rm sh}\omega^2\right)}. \quad (40)$$

IV. Current and Voltage Waveforms

After finding all of the unknown design parameters from the presented analysis, switch voltage and switch current are plotted using (10) and (17), respectively. The normalized switch voltage and current waveforms of the designed amplifier are illustrated in Fig. 4. As can be seen in this figure, the switch

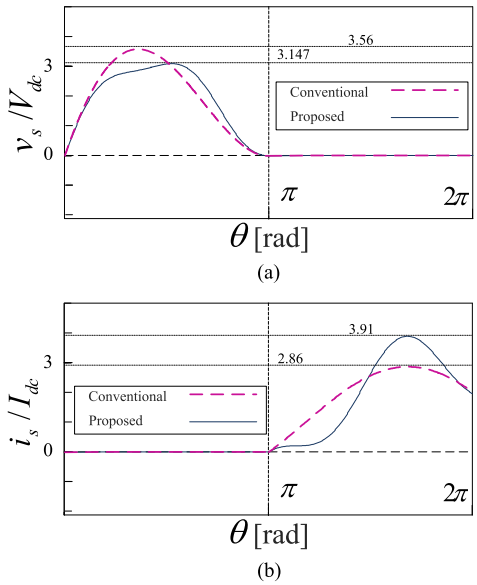

Fig. 4. Obtained normalized (a) switch voltage and (b) switch current waveforms of the designed amplifier.

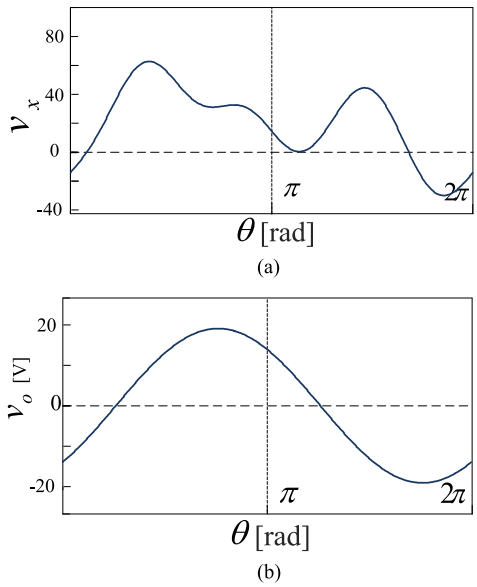

Fig. 5. Obtained waveforms of (a) v_x and (b) v_o for the proposed amplifier.

voltage is reduced, compared with the conventional amplifier. This reduction in the switch voltage is due to the harmonics existence in the switch voltage. The maximum normalized values of the switch voltage and current are obtained 3.147 and 3.91, respectively, at operating frequency of $f = 1$ MHz, the dc supply voltage of $V_{\rm dc} = 20$ V, $C_{\rm ds} = 250$ pF, and $C_{\rm ex} = 1220$ pF. The normalized values of the switch voltage and current of the conventional class E amplifier are 3.56 and 2.86, respectively. The rms values of the switch current for the presented and conventional class E amplifiers are 1.05 and 0.95 A, respectively. The same input voltage and the same output power are considered for presented and conventional class E amplifiers to obtain the switch waveforms.

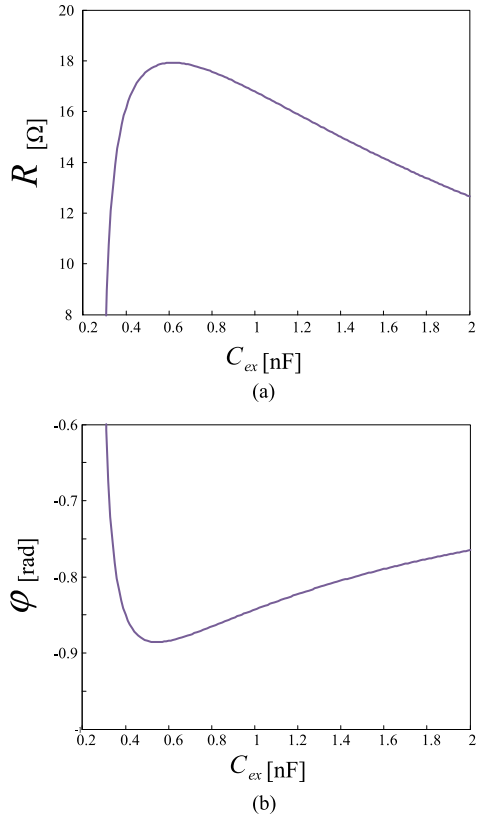

Fig. 6. Values of the obtained (a) R and (b) φ versus different values of external capacitance.

The obtained waveforms at nodes v_x and v_o for the designed amplifier are shown in Fig. 5. According to this figure, the values of v_x at the beginning and the end of the period are equal. The amplitude of the obtained output voltage is approximately equal to conventional structure output voltage, but with different value of phase shift.

Obtained values of R and φ versus different values of external capacitance are illustrated in Fig. 6. According to these values, the switch voltage and current waveforms can be obtained versus different external capacitances.

The effects of different values of the external capacitance on the normalized switch voltage and current waveforms for the presented amplifier are shown in Fig. 7. As can be seen, various shapes of voltage and switch waveforms can be achieved using different values of the external capacitance due to effects of different harmonics. As the value of external capacitance increases, the normalized switch voltage and current waveforms will be reduced.

The maximum values of the normalized switch voltage and current versus different values of the external capacitance are illustrated in Fig. 8(a). Increasing external capacitance leads to the reduced switch voltage of the presented circuit. The maximum normalized switch current decreases, as the value of external capacitance increases. Therefore, larger values of the output power capability can be achieved with larger values of external capacitance, as shown in Fig. 8(b). In the proposed amplifier, the values of the normalized switch voltage and current are

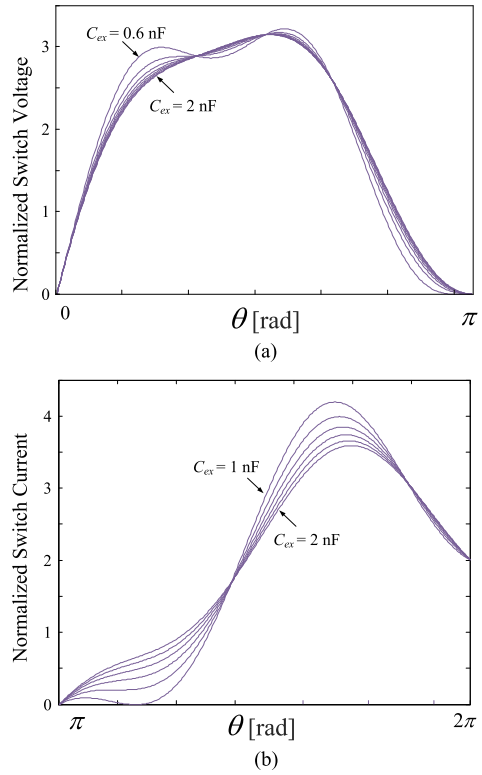

Fig. 7. Normalized (a) switch voltage and (b) switch current waveforms versus different values of external capacitance with step of 0.2 nF.

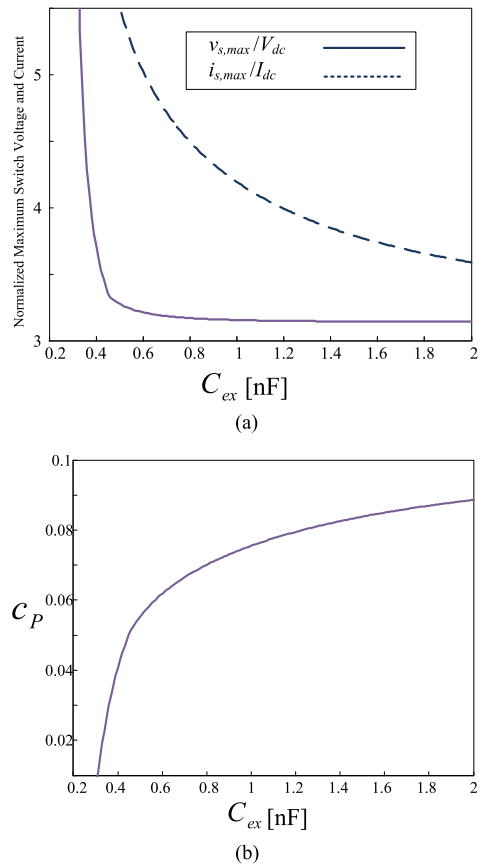

Fig. 8. (a) Maximum values of the normalized switch waveforms and (b) the output power capability, versus different values of external capacitance.

approximately constant versus different values of the dc supply voltage.

A comparison between obtained parameters of the presented structure and related approaches are presented in Table II. According to this table, switch voltage reduction is achieved, while the output voltage is stayed pure sinusoidal. The other advantage of the presented amplifier is that desirable shapes of the switch voltage waveform can be obtained by changing the values of circuit elements. However, the disadvantage of the presented structure is higher maximum switch current, compared with the conventional class E amplifier. The maximum switch voltage reduction in this table is calculated, compared to the maximum switch voltage of conventional class E amplifier $4\,V_{\rm dc}$, according to the nonlinearity of drain-to-source capacitance. This value is calculated using simulation of the conventional class E amplifier, which will be described in the next sections.

V. Efficiency of the Presented Structure

The dissipated power should be calculated in order to obtain the efficiency of the presented structure, according to the following equation [10]:

$$\eta = \frac{P_o}{P_o + P_{\rm DS}}. \tag{41}$$

The dissipated power is sum of the loss powers in actual resistance of the applied elements in the circuit. Main dissipated powers in the circuit belong to resistances of dc-feed inductance ($r_{L_{\rm RFC}}$), series resonator ($r_{L_0C_0}$) and the MOSFET ON-resistance ($r_{\rm DS}$). These resistance values should be measured, to calculate efficiency of the circuit. The values of $r_{L_{\rm RFC}}$ and $r_{L_0C_0}$ are measured as 0.6 and 0.7 Ω, respectively.

Also, the value of $r_{\rm DS}$ is chosen as 0.16 Ω, according to the applied power MOSFET IRF530 datasheet and PSpice model. The total dissipated power could be written as

$$P_{\rm DS} = P_{r_{L_0C_0}} + P_{r_{L_{\rm RFC}}} + P_{r_{\rm DS}}. \tag{42}$$

In (42) the terms of $P_{r_{L_0C_0}}$ and $P_{r_{L_{\rm RFC}}}$ could be simplified as follows, because the value of $I_{\rm dc}$ is constant and i_o is pure sinusoidal:

$$P_{r_{L_0C_0}} = \frac{1}{2\pi}\int_0^{2\pi} r_{LC}{i_o}^2 d\theta = \frac{1}{2} r_{LC}{I_m}^2. \tag{43}$$

$$P_{r_{L_{\rm RFC}}} = \frac{1}{2\pi}\int_0^{2\pi} r_{L_{\rm RFC}}{I_{\rm dc}}^2 d\theta = r_{L_{\rm RFC}}{I_{\rm dc}}^2. \tag{44}$$

The value of $P_{r_{\rm DS}}$ could be obtained using

$$P_{r_{\rm DS}} = \frac{1}{2\pi}\int_0^{2\pi} r_{\rm DS}{i_s}^2 d\theta. \tag{45}$$

The integration in (45) could be performed from $\theta = \pi$ to 2π, because the switch current is zero during $\theta = 0$ to π. According to (41)–(45) the efficiency of the presented structure is calculated theoretically. Also, the simulated and measured efficiency are obtained, which are presented in Table III. The simulated efficiency is calculated using equivalent series resistances of each component.

TABLE II
COMPARISON BETWEEN PRESENTED STRUCTURE AND RELATED APPROACHES

	$v_{s,\max}/V_{\rm dc}$	$i_{s,\max}/I_{\rm dc}$	Maximum switch voltage reduction %	Measured efficiency %	Output power	Operating frequency	Output current
Conventional class E PA	3.56–4.5	2.86	0	–	–	–	Pure sinusoidal
The structure in [26]	2.97	2.83	25.7	80.4	2.22 W	1 MHz	Distorted sinusoidal
Proposed structure	3.147	3.91	21.3	90.3	13.12 W	1 MHz	Pure sinusoidal

TABLE III
THEORETICAL, PSPICE SIMULATION, AND EXPERIMENTAL MEASUREMENT RESULTS OF THE PRESENTED DESIGN EXAMPLE

	Theoretical	Simulation	Measured
$V_{\rm in}$	5 V	5 V	5 V
$V_{\rm dc}$	20 V	20 V	20 V
f	1 MHz	1 MHz	1 MHz
R	15.4 Ω	15.4 Ω	15.35 Ω
L	3 μH	3 μH	3 μH
C	940 pF	940 pF	941 pF
L_0	107.8 μH	107.8 μH	107.89 μH
C_0	235 pF	235 pF	235 pF
$C_{\rm ex}$	1220 pF	1220 pF	1220 pF
$L_{\rm RFC}$	100 μH	100 μH	100 μH
$P_{r\,L\,\rm RFC}$	0.225 W	0.29 W	0.32 W
$P_{r\,LC}$	0.555 W	0.62 W	0.6 W
$P_{r\,\rm DS}$	0.177 w	0.26 W	0.49 W
$v_{s,\max}$	62.9 V	61.1 V	60.4 V
V_o	19.5 V	20.5 V	20.1 V
$P_{\rm out}$	12.24 W	13.64 W	13.12 W
η	92.75%	92.1%	90.3%

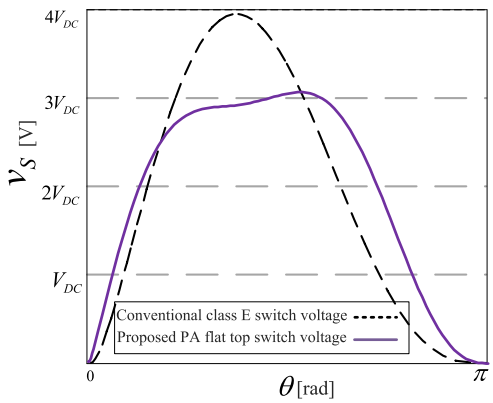

Fig. 9. Simulated flat top switch voltage of the proposed PA, compared to the conventional one.

VI. SIMULATION AND EXPERIMENTAL RESULTS

The simulated switch voltage waveforms of the proposed class E amplifier and the conventional one are shown in Fig. 9. According to this figure, the obtained switch voltage of the proposed amplifier is lower than the conventional structure switch voltage. The MOSFET nonlinear drain-to-source parasitic capacitance is considered in simulation of conventional class E PA, so the peak switch voltage value is obtained more than 3.56 $V_{\rm dc}$. The value of peak switch voltage in simulation of the presented PA is obtained approximately as 3 $V_{\rm dc}$. A design example is presented to verify the results of the proposed circuit, which is explained as follows.

A. Circuit Parameters and Design Procedure

The duty cycle of the input square voltage is considered to be 0.5 and the fundamental frequency of the amplifier is $f =$ 1 MHz. The dc supply voltage is assumed $V_{\rm dc} = 20$ V to provide the desired output power. Using desired value of operating frequency and value of Q, the value of series inductance L_0 can be calculated. Also, the inductance L_0 and capacitance C_0 form an ideal resonator, which resonates at the operating frequency. The value of L_0 is selected in such way that the value of C_0 becomes 235 pF, which can be easily constructed using two series 470 pF capacitors. Therefore, the value of inductance L_0 is selected as 107.8 μH. The value of $C_{\rm ex}$ is an important parameter, which affects all of the amplifier specifications, such as switch voltage, switch current, and output power capability. Therefore, due to the desired specifications, the value of $C_{\rm ex}$ is selected, according to Figs. 7 and 8. So, linear external capacitance of $C_{\rm ex} = 1220$ pF is considered. Value of L and C should satisfy assumption 8 and also should satisfy the flat top shape of amplifier. Therefore, the value of L is chosen 3 μH and the value of C is selected as 940 pF, which can be easily constructed using two parallel 470 pF. From (36), the parameters of φ and R will be obtained, which are 0.81 rad and 15.4 Ω, respectively.

The IRF530 power MOSFET from International Rectifier is used as a switching device. High value of shunt capacitance is considered to mitigate the nonlinearity effects of the drain-to-source capacitance. Value of $C_{\rm ds} = 250$ pF is assumed for the intrinsic MOSFET capacitance, according to the IRF530 MOSFET datasheet. The values of the applied elements and design specifications for the proposed circuit are summarized in Table III. The design example results are also given in this table. Commercial values are considered for choosing the circuit elements. Theoretical, PSpice simulation, and experimental waveforms of the gate-to-source voltage $(v_{\rm gs})$, switch voltage (v_s), and output voltage (v_o) for the proposed PA are depicted in Fig. 10. According to this figure, the flat top switch voltage waveform is achieved. The output power of the designed amplifier is obtained to be 13.12 W. The designed circuit is fabricated and tested, which verifies the simulation and theoretical results.

The prototype is built on a copper-clad fiberglass circuit board, as shown in Fig. 11. According to this figure, types of $L_{\rm RFC}$, L, and L_0 are ferromagnetic core inductors. Mica capacitors are used in the prototype because of their low loss and

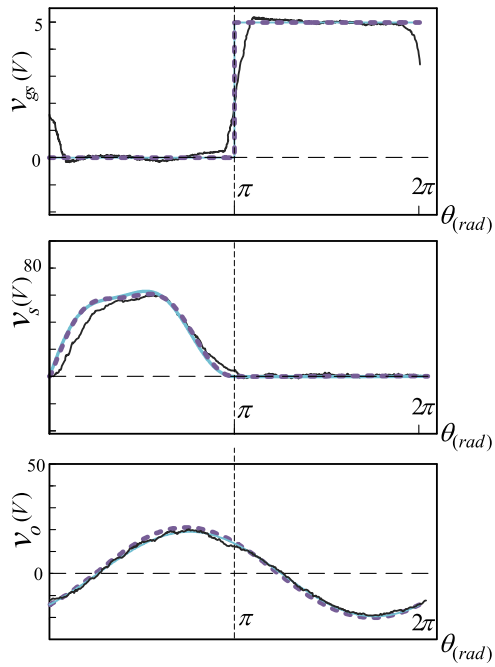

Fig. 10. Theoretical (solid lines), PSpice simulation (dashed lines), and experimental measurement results of the proposed power amplifier.

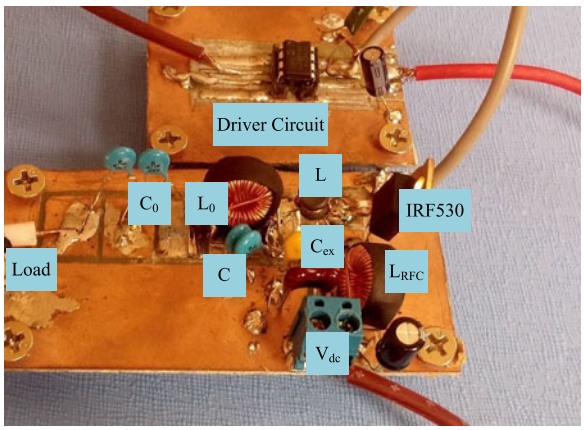

Fig. 11. Photograph of a fabricated power amplifier.

high voltage capability. Two 470 pF series capacitors are used to form 235 pF C_0 capacitor and two 470 pF parallel capacitors are forming 940 pF C capacitor. Also, a 1 nF and a 220 pF capacitors are used in parallel to make 1220 pF $C_{\rm ex}$ capacitor.

VII. Conclusion

A novel structure related to the class E PA has been introduced, analyzed, fabricated, and tested. The results showed approximately 22% reduction in the maximum switch voltage, compared with the conventional class E amplifier. The ZVS and ZDS conditions were satisfied in the presented structure. The simulated and measured results were in good agreement. According to the results, a lower switch voltage stress can be achieved for the presented amplifier, compared to the conventional class E amplifier.

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