Analysis of Main Topologies of Shunt Active Power Filters Applied to Four-Wire Systems

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***Abstract*—This paper presents a complete comparative study about the five most common configurations of shunt active power filter applied to four-wire distribution systems. In order to evaluate the applicability of the studied topologies, two scenarios of four-wire loads are investigated differing by level of zero-sequence harmonic contents. The analysis of simulation steady-state results comprise dc-link capacitor voltage and current stresses, harmonic distortion in grid currents, and semiconductor losses. The results show that structures with fourth inductor generate higher number of levels at output converter voltage. However, when they operate by compensating high levels of zero-sequence harmonics, they can present higher dc-link voltage and lower efficiency. Furthermore, system models, control strategy, and experimental results are presented as well.**

***Index Terms*—Power conversion harmonics, power converter, power filters, power quality.**

I. Introduction

CURRENT harmonics and unbalances may cause huge financial damage in distribution systems. It is well known that the main cause of harmonics is nonlinear loads, such as electronic loads, air-conditioning systems, computer power systems, and drive systems [adjustable speed drive (ASD)]. Among negative effects related with current harmonics, the following can be highlighted: transformer and power cable overheating, premature motor burnouts, and malfunctioning of circuit breakers [1], [2]. In four-wire systems, the most common power quality problem is excessive neutral current, which causes overheating in neutral conductor or even equipment damage. Neutral current is caused by unbalance between single-phase loads (which leads to negative-sequence currents) and single-phase nonlinear loads (which leads to zero-sequence currents) [3].

The most prominent solution for eliminating such effects (caused by nonlinear loads) is the use of shunt active power filters (SAPF) connected at point of common coupling (PCC), located between grid and load [4]–[6]. This device is able to provide all harmonic, reactive and unbalanced contents required by electric loads. In the literature, there are studies about different topologies based on SAPF operating in four-wire systems. The most studied topologies are shown in Fig. 1. They are named here based on their number of converter legs (L) and filter inductors (l), i.e., Fig. 1(a) shows the topology 3L–3l, that is composed of three legs and three inductors, Fig. 1(b) shows 3L–4l, Fig. 1(c) shows 4L–3l, and Fig. 1(d) shows 4L–4l. Finally, Fig. 1(e) shows topology 6L, that is composed of six legs and three isolation transformers.

The topology 3L–3l has been widely studied in the literature [7]–[14]. Most papers discuss about dc-link voltage and current control of three-leg split capacitor converter. Analysis of dc-link voltage control strategies and a proposed method suitable to a startup process of capacitor charging are carried out in [12]. A current control technique based on a modified *dq* frame was proposed in [14], in which comparisons with other techniques in terms of harmonic current mitigation under different conditions of grid voltages and load currents were presented. Hybrid solutions adding *LC* filters to structure 3L–3l were studied in [12] and [14]. These filters can be connected in series [12] or in parallel [14] to reduce ratings of switching devices. The topology 3L–4l was presented and implemented in [15] and [16]. The latter proposes a fault diagnosis algorithm for 3L–4l, in order to locate open-circuit faults. It is worth noting that 3L–4l differs from 3L–3l by an additional inductor in fourth converter conductor. These two topologies require an additional voltage controller in order to balance the dc-link voltages of two capacitors, due to connection of fourth wire conductor at dc-link midpoint [17]. Indeed, this feature can be considered a drawback.

The topology 4L–4l was first presented as solution of SAPF in [18] and [19]. Since then, papers proposing new modulation or control strategies have been presented [20]–[24]. The generalized instantaneous reactive power theory (*p-q* theory) for four-wire systems was presented in [25], in which the topology 4L–3l was used for implementation. In [26], *p-q* theory was also applied to 4L–4l under different field applications (different types of loads, from textile industry to medical drugs distribution warehouse). Same topology was applied with multiple converter modules connected in parallel operation in [27] and [28]. Recently, 4L–4l was applied to microgrids as a multifunction topology [23], in which solar panels were connected

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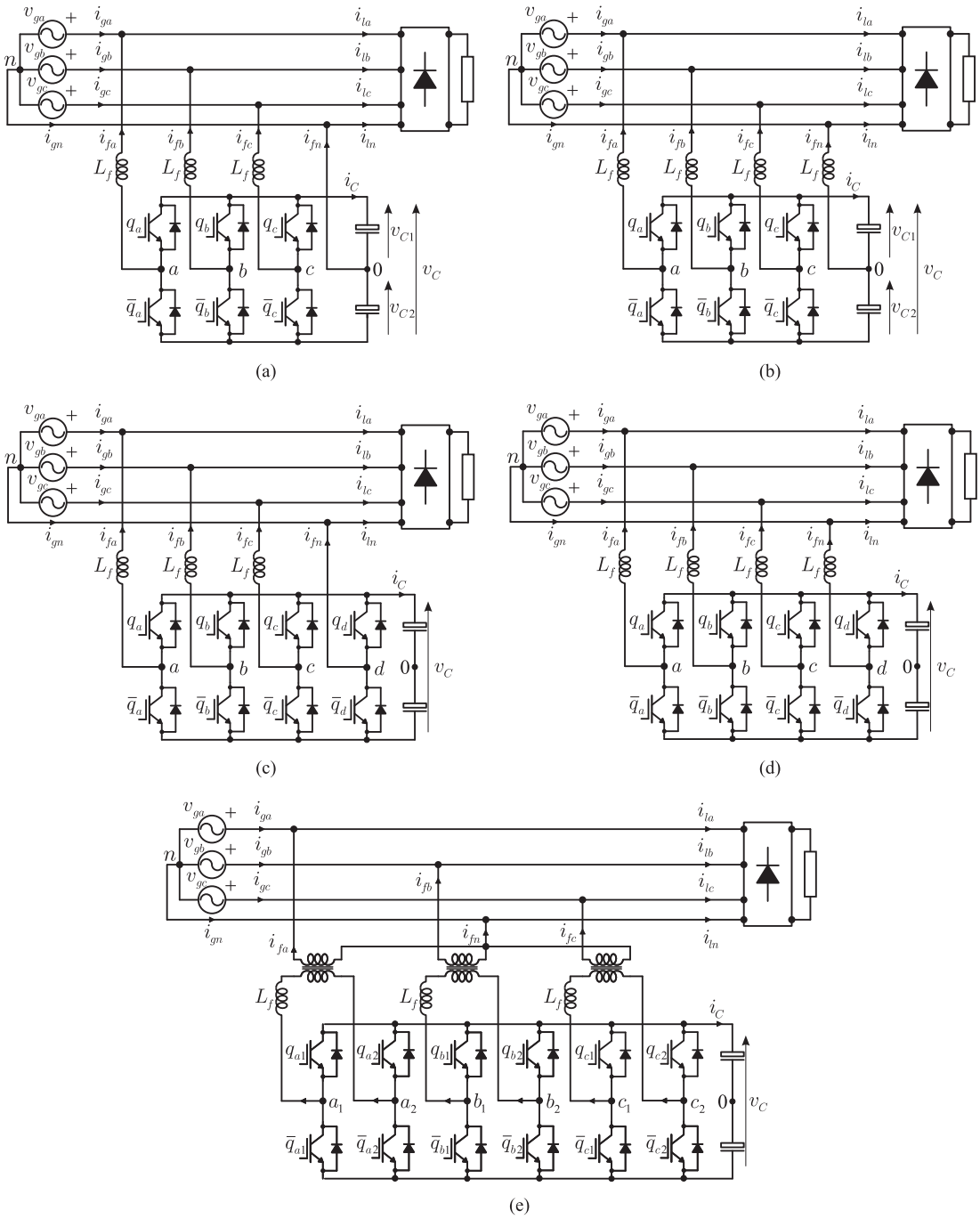


Fig. 1. Main topologies based shunt active filters applied to four-wire systems. (a) Topology 3L–3l. (b) Topology 3L–4l. (c) Topology 4L–3l. (d) Topology 4L–4l. (e) Topology 6L.

to dc-link allowing that active energy, reactive and harmonic contents be supplied to grid, simultaneously. Also for microgrid applications, a conservative power theory implemented in 4L–4l compensating different loads under fixed or variable frequency at PCC was proposed in [24].

Finally, the topology 6L appears as a solution for higher power application [29]. This topology is composed of three isolation transformers, 1 six-leg converter (12 switches), and 1 dc-link capacitor. Its high number of semiconductor devices and the presence of transformers can be considered drawbacks. Alternatively, a 6L structure built from three independent h-bridge converters and three individual dc-link capacitors was studied in [30] and [31]. In this case, isolation transformer are not required, in contrast the topology demands three dc-links and three voltage sensors, increasing control complexity.

Some papers bring approaches involving a group of SAPF topologies [32]–[38]. Comparison between 3L–3l and 3L–4l was carried out in [33], exploring the influence of the fourth inductor in terms of harmonic distortion. *LC* hybrids 3L–3l and 3L–4l were described in [36], in which the minimum dc-link

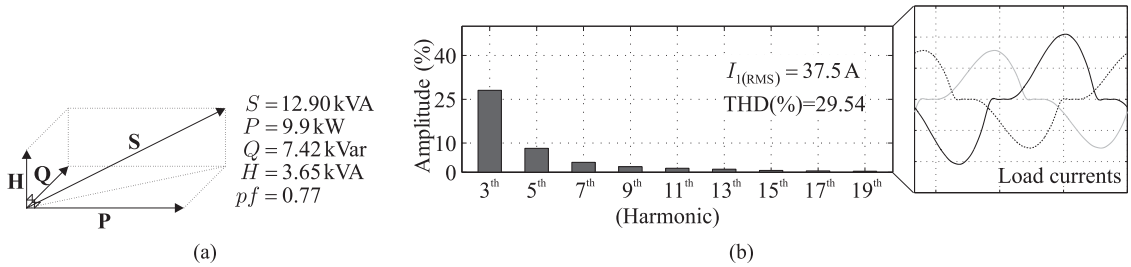


Fig. 2. Characteristics of load 1. (a) 3-D power diagram. (b) Harmonic characteristics.

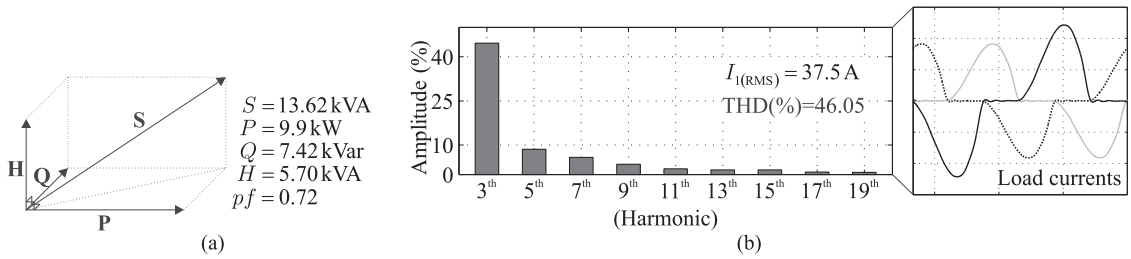


Fig. 3. Characteristics of load 2. (a) 3-D power diagram. (b) Harmonic characteristics.

voltage was investigated. The one-cycle control technique was applied to topologies 3L–3l and 4L–4l in [34]. The topologies 3L–3l, 4L–3l, and 6L were studied with focus on the artificial neural network technique presented in [32]. On the other hand, the topologies 3L–4l, 4L–4l, and 6L were evaluated in terms of harmonic distortion, and general aspects such as dc-link voltage and number of semiconductor devices in [35]. However, literature presents neither an investigation about the impact of the use of a fourth inductor nor a wide comparison of all of topologies under different load conditions.

This paper investigates the five most studied structures of SAPF applied to four-wire systems (see Fig. 1). Analysis will be performed considering two different scenarios of load. Note that some structures have an additional inductor, which can be helpful to reduce the harmonic distortion, but can increase the dc-link voltage, as will be explained here. The topologies are compared taking into account those two load types. These loads present currents with either low or high zero-sequence harmonic contents. The comparisons are carried out in terms of harmonic distortion of grid currents, semiconductor losses, and capacitor dc-link stress (current and voltage). In this way, it is possible to choose the most suitable structure for each type of load, as well as to manage the SAPF to have a good performance. All theoretical analyses are performed in a steady-state simulation. Besides, dynamic modeling, control strategy, definition of minimum dc-link voltage value, and experimental results are presented for all studied topologies.

II. System Configuration

A. Load Specification

The characteristics of first and second load types are shown in Figs. 2 and 3, respectively. These figures show in detail a three-dimensional (3-D) power diagram based on [39] and harmonic

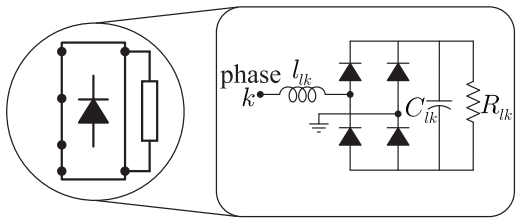


Fig. 4. Load circuit used in simulation analysis.

TABLE I
Parameters Used to Obtain the Patterns of Load

	Load 1	Load 2
l_{lk}	15 mH	15 mH
C_{lk}	1100 μF	1100 μF
R_{lk}	20 Ω	50 Ω

contents of each load. These patterns of harmonic contents (percentage relation between the amplitudes of fundamental and harmonic components) have been obtained from a typical single-phase full-bridge rectifier, shown in Fig. 4, supplied by $V_{gk(\mathrm{rms})}$ of 110 V, whose parameters are detailed in Table I. After that, the power of both loads was adjusted (modifying the fundamental current) in order to increase them, keeping the same active and reactive power for both loads. Note that they differ by the quantity of zero-sequence harmonics only.

From simulation, it is noticed that the larger load power is (lower R_{lk}), the higher the difference between fundamental and zero-sequence harmonics becomes, i.e., lower values of harmonic components. Therefore, a single-phase input ASD system under full-load operation has lower zero-sequence harmonic contents than the same ASD under half-load operation.

However, for an industrial plant, this relation between fundamental and zero-sequence harmonics contents can be changed by the number of linear, three-phase ASD and single-phase ASD loads in operation.

B. System Model

The studied topologies, shown in Fig. 1, are constituted of two-level voltage-source converters associated with filter inductors L_f (inductance l_f and resistance r_f) connected at PCC. For the topology 6L, the leakage inductance of transformer and external interfacing shunt inductance represented by l_f as well as the loss of transformer denoted by r_f have been taken into consideration. For the studied topologies, the following model can be written:

$$v_{gk} = -z_f i_{fk} + v_{fk} \tag{1}$$

where $k = a, b, c$, $z_f = r_f + l_f d/dt$, and output converter voltages v_{fk} for topologies 3L–3l, 3L–4l, 4L–3l, and 4L–4l are given by

$$v_{fk} = v_{k0} - v_{n0} \tag{2}$$

where the voltage v_{n0} is different for each studied topology, i.e.,

1) for 3L–3l

$$v_{n0} = 0 \tag{3}$$

2) for 3L–4l

$$v_{n0} = \frac{v_{a0} + v_{b0} + v_{c0}}{4} \tag{4}$$

3) for 4L–3l

$$v_{n0} = v_{d0} \tag{5}$$

4) for 4L–4l

$$v_{n0} = \frac{v_{a0} + v_{b0} + v_{c0} + v_{d0}}{4}. \tag{6}$$

For topology 6L, v_{fk} are given by

$$v_{fk} = v_{k_1 0} - v_{k_2 0}. \tag{7}$$

The pole voltages of the converters (v_{k0}, $v_{k_1 0}$, and $v_{k_2 0}$) depend on the conduction state of power switches, which generically is given by

$$v_{k0} = (2s_k - 1)\frac{v_C}{2} \tag{8}$$

where v_C is dc-link voltage and s_k are conduction state of the switches, in which $s_k = 1$ indicates a closed switch, whereas $s_k = 0$ indicates a blocked one. The states of switches are defined by comparison between high-frequency triangular and pole reference voltages, which are obtained from model equations and controllers output.

III. Control Strategy

Fig. 5 shows a possible control strategy diagram to ensure sinusoidal currents at grid side, with total compensation of reactive and harmonic contents. From the diagram, v_C is controlled by means of proportional-integral (PI) controller (R_C block), providing I^*_{act} (amplitude of active current). The block $Sync$ represents the synchronization with grid voltages from angle θ, which is acquired from phase-locked loop (PLL). The power-based PLL is implemented in this paper and has been demonstrated in [40]. Reactive and harmonic contents of load currents are found by RH detec. block from synchronous fundamental *dq* frame, which is detailed in [41]. After determination of filter currents i_{fk} (i_{fa}, i_{fb}, and i_{fc}), they are controlled by means of cascaded resonant controllers (R_{ikn} block) [42], [43], ensuring null error at different frequencies. At last, R_{ikn} defines reference converter voltages v^*_{fa}, v^*_{fb}, and v^*_{fc} required by a pulse width modulation (PWM) strategy.

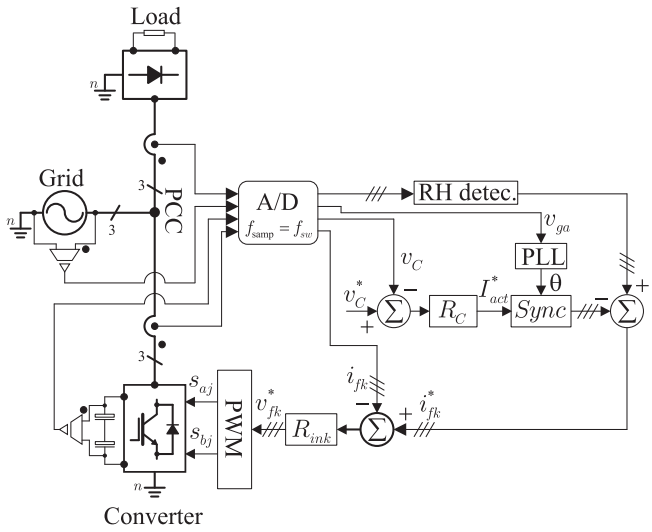


Fig. 5. Overall block diagram control of SAPF.

A. DC-Link Voltage Control

As detailed in [29], the transfer function of dc-link plant has the following form:

$$V_C(s) = \frac{3v_d}{2C_{dc}V_C s} I_{\text{act}}(s) \tag{9}$$

where v_d is the direct input voltage and V_C is the value of v_C at the operation point. The R_C block is used in order to control the dc-link voltage, which is given by

$$R_C = K_{\text{pC}} + \frac{K_{\text{iC}}}{s}. \tag{10}$$

The state-space PI control law for R_C is described as

$$\frac{dx_C}{dt} = K_{\text{iC}}\xi_C \tag{11}$$

$$I^*_{act} = x_C + K_{\text{pC}}\xi_C \tag{12}$$

where x_C is the state variable and $\xi_C = v^*_C - v_C$ is the error of dc-link voltage. The discrete-time equivalent using a zero-order hold method is given by

$$x_C(h) = x_C(h-1) + \frac{1}{f_{\text{samp}}} K_{\text{iC}}\xi_C(h-1) \tag{13}$$

$$I^*_{act}(h) = x_C(h) + K_{\text{pC}}\xi_C(h) \tag{14}$$

in which $h = 0, 1, 2, \ldots$, represents discrete time h/f_{samp} and f_{samp} is the sample frequency.

B. Current Control

From (1) and considering the grid input voltage v_g as a perturbation, the first-order model is given by

$$I_f(s) = \frac{1}{r_f + sl_f} V_f(s). \tag{15}$$

The block R_{ink} is responsible to control filter currents, this block represents resonant controllers for each harmonic frequency, which individually is defined as

$$R_{ink} = 2\frac{K_{pn}s^2 + K_{in}s}{s^2 + (nw_e)^2} \tag{16}$$

accordingly the steady-space control law is given by

$$\frac{dx_{ian}}{dt} = x_{ibn} + 2K_{in}\xi_i \tag{17}$$

$$\frac{dx_{ibn}}{dt} = -(nw_e)^2 x_{ian} - (nw_e)^2 2K_{pn}\xi_i \tag{18}$$

$$v^*_{fkn} = x_{ian} + 2K_{pn}\xi_i \tag{19}$$

where $\xi_i = i^*_f - i_f$ is error of filter current. From [44] and [45], discrete equations of this controller are obtained, as shown in (20)–(22).

$$\begin{aligned} x_{ian}(h) = {} & \cos\left(\frac{nw_e}{f_{\text{samp}}}\right) x_{ian}(h-1) + \frac{\sin\left(\frac{nw_e}{f_{\text{samp}}}\right)}{nw_e} x_{ibn}(h-1) \\ & + \left[\frac{2K_{in}\sin\left(\frac{nw_e}{f_{\text{samp}}}\right)}{nw_e} \right. \\ & \left. - \left(1 - \cos\left(\frac{nw_e}{f_{\text{samp}}}\right)\right) 2K_{pn}\right] \xi_i(h-1) \end{aligned} \tag{20}$$

$$\begin{aligned} x_{ibn}(h) = {} & -nw_e \sin\left(\frac{nw_e}{f_{\text{samp}}}\right) x_{ian}(h-1) \\ & + \cos\left(\frac{nw_e}{f_{\text{samp}}}\right) x_{ibn}(h-1) \\ & + \left[\left(\cos\left(\frac{nw_e}{f_{\text{samp}}}\right) - 1\right) 2K_{in} - nw_e \right. \\ & \left. \times \sin\left(\frac{nw_e}{f_{\text{samp}}}\right) 2K_{pn}\right] \xi_i(h-1) \end{aligned} \tag{21}$$

$$v^*_{fkn}(h) = x_{ian}(h) + 2K_{pn}\xi_i(h). \tag{22}$$

IV. Analysis of Simulation Results

The simulation results are obtained in steady-state open-loop control, in which the used parameters are given in Table II. The topologies are evaluated under two different load operations, shown in Figs. 2 and 3. They are analyzed taking the following figures of merit: definition of minimum dc-link capacitor voltage; dc-link capacitor current stress; harmonic distortion of grid current; and semiconductor losses.

TABLE II
Parameters Used for Simulation Results

Supply voltage	$V_{g\,k\,\text{RMS}}$	110 V
Fundamental frequency	f_1	60 Hz
Filter inductance	l_f	2 mH
Filter resistance	r_f	0.1 Ω
DC-link capacitance	C_{dc}	2200 μF
Switching frequency	f_{sw}	10 kHz

A. DC-Link Capacitor

1) DC-Link Capacitor Voltage Definition: The definition of minimum dc-link voltage ($v^*_{C\,\min}$) of a converter depends on maximum voltage defined by their circuit meshes in order to be able to provide adequate currents. For a converter operating as SAPF, this definition becomes a tough task, due to harmonic contents of filter currents. Additionally, in four-wire systems, the converter should be able to provide unbalanced currents and zero-sequence harmonics. Indeed, the major part of $v^*_{C\,\min}$ is due to fundamental voltage (i.e., grid voltage) but components related to filter impedance voltage ($z_f i_{fk}$) must be taken into account. Note that $v^*_{C\,\min}$ depends on reference output converter voltage (v^*_{fk}) that is defined from (1). These converter voltages are given by the sum of voltages with different frequencies. Then, the maximum value (the worst case) of $\mathbf{v}^*_{\text{fk}\,\max}$ occurs in the alignment of the vectors $\mathbf{v^*_{fk1}}$, $\mathbf{v^*_{fk3}}$, $\mathbf{v^*_{fk5}}$ (see Fig. 6), where $\mathbf{v^*_{fk1}}$ is the parcel of converter voltage in fundamental frequency, $\mathbf{v^*_{fk3}}$ is the parcel in third harmonic frequency, $\mathbf{v^*_{fk5}}$ is the parcel in fifth harmonic frequency. $\mathbf{v}^*_{\mathbf{fn}\,\max}$ is the voltage in fourth filter conductor, comprised of $\mathbf{v^*_{fn1}}$ ($\mathbf{z_f i^*_{fn1}}$) and $\mathbf{v^*_{fn3}}$ ($\mathbf{z_{f3} i^*_{fn3}}$), which exists in topologies with fourth inductor, i.e., 3L–4l and 4L–4l.

Fig. 6 shows voltage diagrams that define $v^*_{C\,\min}$ for the two aforementioned scenarios of load. The first scenario (case 1), shown in Fig. 6(a), presents the converter voltage for a load with low third harmonic content and the second scenario (case 2), shown in Fig. 6(b), for a load with high third harmonic content. In this figure, three variables are defined in order to obtain $v^*_{C\,\min}$, that are $v_{C1\,\min} = |\mathbf{v_{fa}}_{\max} - \mathbf{v_{fb}}_{\max}|$, $v_{C2\,\min} = |\mathbf{v_{fa}}_{\max}|$, and $v_{C3\,\min} = |\mathbf{v_{fa}}_{\max} - \mathbf{v_{fn3}}_{\max}|$. Then, for each topology, $v^*_{C\,\min}$ is defined by one of these three variables ($v_{C1\,\min}$, $v_{C2\,\min}$, and $v_{C3\,\min}$).

Table III shows $v^*_{C\,\min}$ in per unit (p.u.), with base value of 110 V in both scenarios of load. $v^*_{C\,\min}$ of 3L–3l is defined as twice the maximum phase voltage, that is, in both cases of load, equal to $2v_{C2\,\min}$. While, $v^*_{C\,\min}$ of 3L–4l is higher because $\mathbf{v}^*_{\text{fn}\,\max}$ must be taken into account for defining $v^*_{C\,\min}$. Then, its $v^*_{C\,\min}$ is equal to $2v_{C3\,\min}$, for both load cases. For 4L–3l, in both load cases, $v^*_{C\,\min}$ is defined by maximum difference between two phases of converter voltages, that is equal to $v_{C1\,\min}$. On the other hand, the definition of $v^*_{C\,\min}$ for 4L–4l depends on load case, i.e., for case 1, $v^*_{C\,\min}$ is equal to $v_{C1\,\min}$, and for case 2, $v^*_{C\,\min}$ is equal to $v_{C3\,\min}$. At last, topology 6L requires

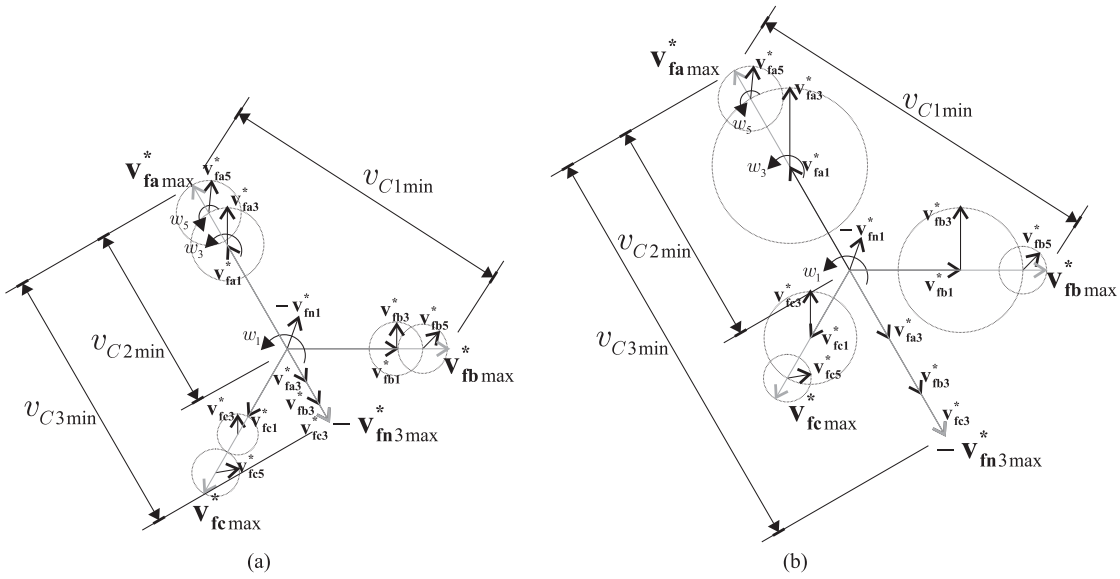


Fig. 6. Minimum dc-link voltage definition. (a) For pattern of load with low third harmonic. (b) For pattern of load with high third harmonic.

TABLE III
DC-LINK CAPACITOR VOLTAGE COMPARISON

Load Type	Topology	Minimum DC-Link Voltage	
Case 1	3L–3l	$2v_{C\,2\,\min}$	3.67 p.u.
	3L–4l	$2v_{C\,3\,\min}$	5.28 p.u.
	4L–3l	$v_{C\,1\,\min}$	2.93 p.u.
	4L–4l	$v_{C\,1\,\min}$	2.93 p.u.
	6L	$v_{C\,2\,\min}$	1.83 p.u.
Case 2	3L–3l	$2v_{C\,2\,\min}$	4.03 p.u.
	3L–4l	$2v_{C\,3\,\min}$	7.69 p.u.
	4L–3l	$v_{C\,1\,\min}$	2.99 p.u.
	4L–4l	$v_{C\,3\,\min}$	3.84 p.u.
	6L	$v_{C\,2\,\min}$	2.01 p.u.

lower $v^*_{C\,\min}$ among all presented topologies, i.e., $v^*_{C\,\min}$ is defined by maximum phase voltage $v_{C2\,\min}$.

From Table III, it is noticed that topologies with inductor in fourth conductor (connected to neutral wire), when compared with topologies without it, may require higher dc-link voltage for compensating loads with high zero-sequence components. In this way, these topologies tend to be less efficient. On the other hand, the fourth inductor has an important role in total harmonic distortion (THD) reduction, as will be shown in this paper.

2) DC-Link Capacitor Current: Stress in dc-link capacitor depends on temperature, RMS capacitor current (I_C^{RMS}) and equivalent series resistance (ESR) [46]. ESR depends on frequency, i.e., ESR reduces with the increase of frequency but becomes constant for frequencies above 3 kHz [47]. The analysis related to dc-link capacitor current is performed concerning the load type 1. Fig. 7 shows dc-link capacitor currents I_C and their spectra for all studied topologies. The amplitudes of harmonic current are represented in p.u value with base value of 37.5 A (fundamental grid current). It is noticed that all topologies present capacitor currents with oscillation at second harmonic (120 Hz) due to compensation of single-phase power. Particularly, topologies 3L–3l and 3L–4l present capacitor currents [see Fig. 7(a) and (b), respectively] with fundamental frequency ($f_1 = 60$ Hz) and triplen frequency ($f_3 = 180$ Hz), due to connection between fourth conductor and center of dc-link capacitor. These components are originated from negative and zero sequence of filter currents, and they are located at frequencies with high values of ESR (low frequencies). In this way, these topologies have the highest stress in dc-link capacitors among all studied topologies. On the other hand, the other topologies do not present f_1 and f_3 components. Capacitor currents of 4L–3l and 4L–4l are shown in Fig. 7(c) and (d), respectively. These topologies present currents with higher amplitude at high frequencies in comparison to the others. The lowest level of capacitor currents is presented by topology 6L due to its lowest level of capacitor voltage.

B. Harmonic Distortion

In this paper, THD is adopted to evaluate grid currents distortion [48]. THD is defined by

$$\text{THD}(p)\% = \frac{100}{Y_1}\sqrt{\sum_{n=2}^{p}(Y_n)^2} \tag{23}$$

where Y_1 is the amplitude of the fundamental component, Y_n is the amplitude of nth component harmonic, and p is the number of harmonics taken in consideration. This study was performed considering the same filter impedance (z_f) in all studied topologies, same modulation index (unitary), same switching frequency (10 kHz), and the converters operating in open-loop control, compensating only reactive power in order to be able to distinguish the levels at output converter voltages. Then, for this analysis, the load type 1 without harmonic contents is used.

Table IV shows the THD of grid currents and the number of levels of output converter voltage (v_{fk}) for all studied topologies. It is noticed that topology 6L presents the lowest THD

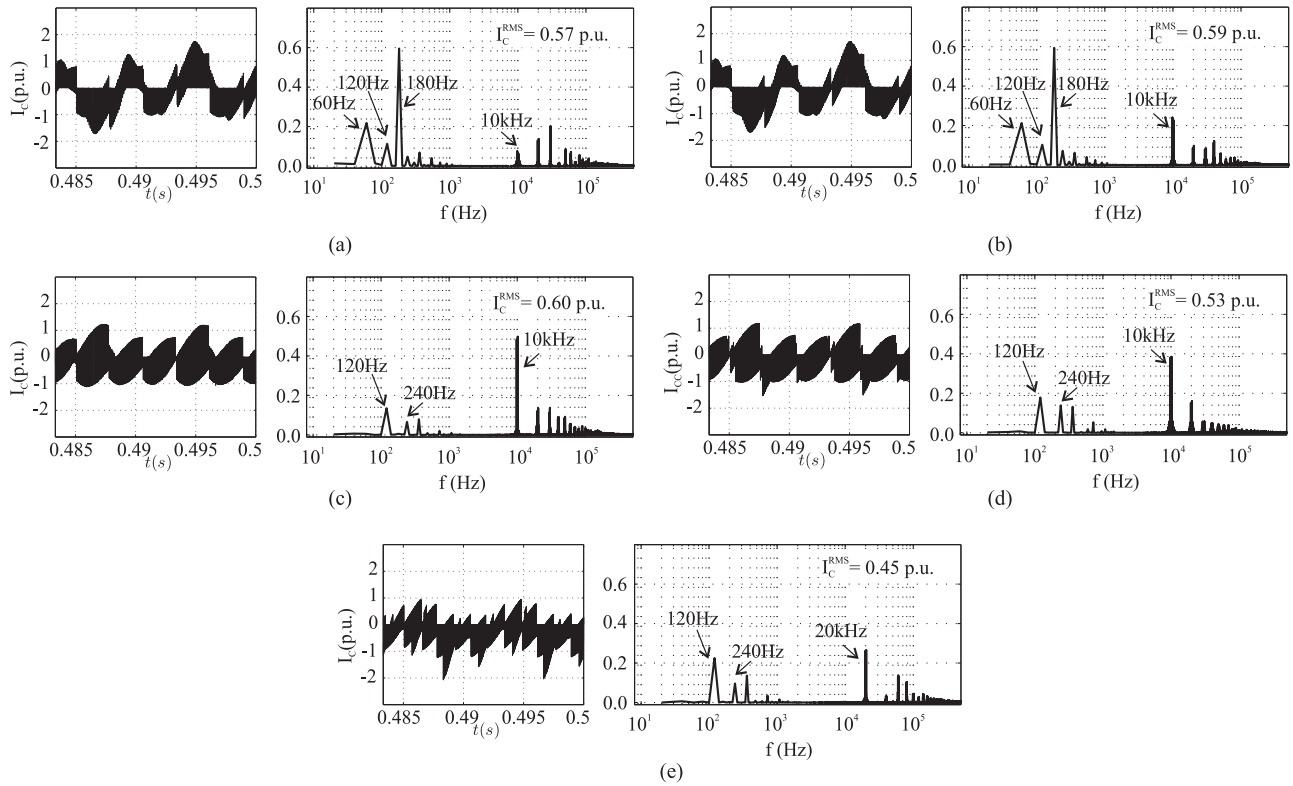


Fig. 7. DC-link capacitor currents and their harmonic spectra. (a) For 3L–$3l$. (b) For 3L–$4l$. (c) For 4L–$3l$. (d) For 4L–$4l$. (e) For 6L.

TABLE IV
THD OF GRID CURRENTS

Topology	THD (%)	Number of Levels
3L–$3l$	3.21	2
3L–$4l$	2.48	6
4L–$3l$	2.13	3
4L–$4l$	1.55	7
6L	0.80	3

value among all topologies since the lowest dc-link voltage value is required by this topology. Topology 6L is followed by topologies 4L (4L–$4l$ and 4L–$3l$, successively). The worst THD results are obtained by topologies 3L (3L–$3l$ and 3L–$4l$). These THD results are justified from the voltage v_{fk}. In (1), it can be noticed that filter currents depend on v_{fk}. Then, the waveform of these voltages as well as the number of levels are determinant factors. It is worth noting that the topologies with additional inductor (X–$4l$) have v_{n0} as a combination of pole voltages [see (4) and (6)] allowing to obtain more levels at v_{fk}. The voltages v_{fk} and its average value v_{fk}^* are shown in Fig. 8. These voltages are presented for a scenario in which the converter compensates only reactive content, in order to distinguish the generated levels. They are presented in p.u. value with base value of 110 V. It is important to know that the advantage obtained for a topology in terms of THD can be turned into switching frequency reduction, i.e., topologies with lower THD can operate with lower switching frequency, as will be shown in the next section.

C. Semiconductor Losses

Semiconductor loss estimation is obtained through PSIM software simulation, using thermal module based on datasheet curves. The semiconductor module used here is Semikron CM100DY-24NF. Semiconductor losses model includes:

1) conduction losses of transistor and antiparallel diode ($P_{cd(\text{diode})}$);
2) transistor turn-on ($P_{sw\text{-ON(trans)}}$) and turn-off ($P_{sw\text{-Off(trans)}}$) losses; and
3) turn-off losses of anti-parallel diode ($P_{sw\text{-OFF(diode)}}$).

For the diode

$$P_{cd(\text{diode})} = v_{\text{drop}} i_d \tag{24}$$

$$P_{sw\text{-OFF(diode)}} = E_{\text{rr}} f \frac{v_r}{v_r^*} \tag{25}$$

where v_{drop}, i_d, E_{rr}, f, v_r, and v_r^* are the diode voltage drop, diode forward current, reverse recovery energy losses, losses calculation frequency, reverse blocking voltage, and reverse blocking voltage in the test conditions, respectively.

For the transistor

$$P_{cd(\text{trans})} = v_{ce(\text{sat})} i_{coll} \tag{26}$$

$$P_{sw\text{-ON(trans)}} = E_{\text{on}} f \frac{v_C}{v_C^*} \tag{27}$$

$$P_{sw\text{-OFF(trans)}} = E_{\text{off}} f \frac{v_C}{v_C^*} \tag{28}$$

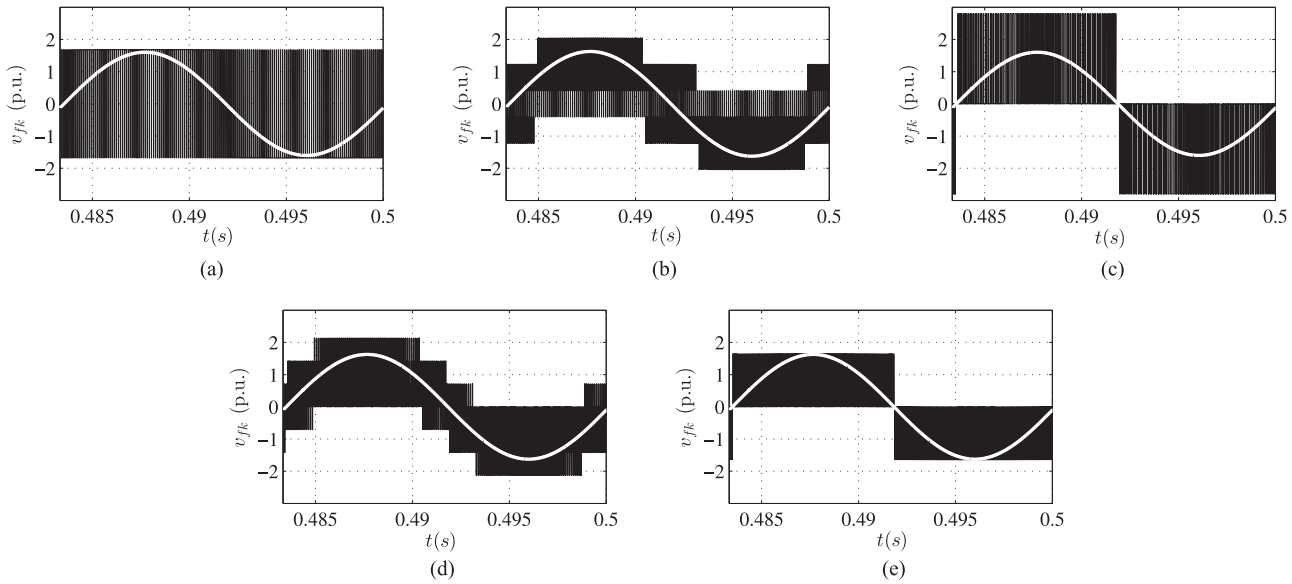
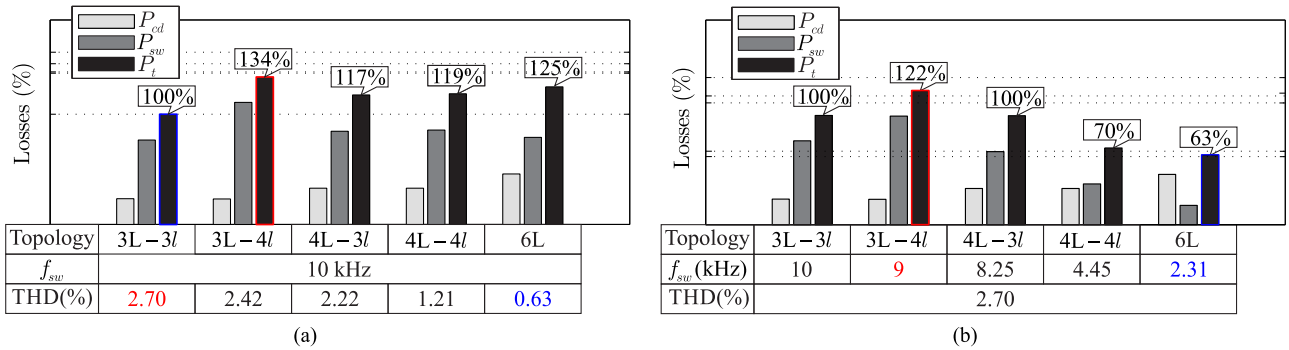


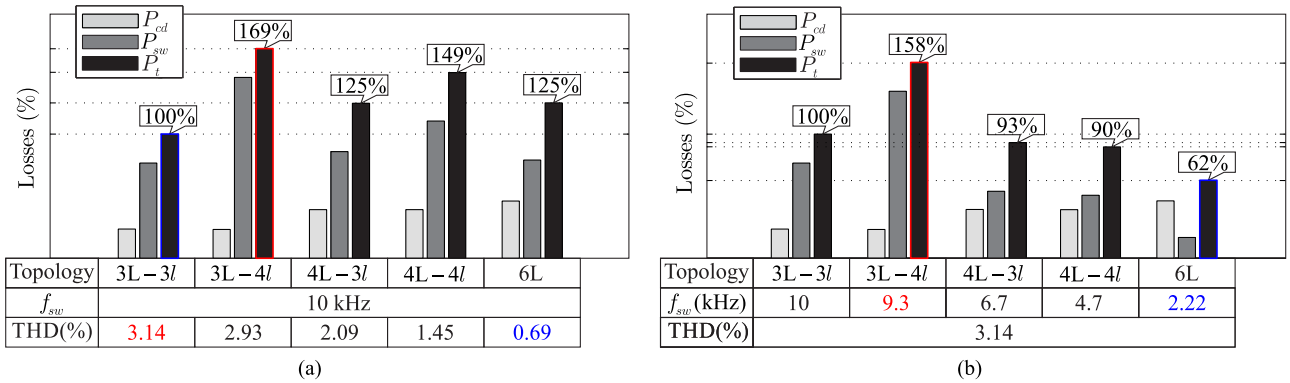
Fig. 8. Output converter voltage v_{fk} for each studied topology. (a) For topology 3L–3l. (b) For topology 3L–4l. (c) For topology 4L–3l. (d) For topology 4L–4l. (e) For topology 6L.



Topology	3L – 3l	3L – 4l	4L – 3l	4L – 4l	6L
f_{sw}	10 kHz				
THD(%)	2.70	2.42	2.22	1.21	0.63

Topology	3L – 3l	3L – 4l	4L – 3l	4L – 4l	6L
f_{sw}(kHz)	10	9	8.25	4.45	2.31
THD(%)	2.70				

Fig. 9. Semiconductor losses for case 1. (a) Same switching frequency scenario. (b) Same THD scenario.



Topology	3L – 3l	3L – 4l	4L – 3l	4L – 4l	6L
f_{sw}	10 kHz				
THD(%)	3.14	2.93	2.09	1.45	0.69

Topology	3L – 3l	3L – 4l	4L – 3l	4L – 4l	6L
f_{sw}(kHz)	10	9.3	6.7	4.7	2.22
THD(%)	3.14				

Fig. 10. Semiconductor losses for case 2. (a) Same switching frequency scenario. (b) Same THD scenario.

where $v_{ce(\text{sat})}$, i_{coll}, E_{on}, v_C, v_C^*, and E_{off} are transistor saturation voltage, the collector current, the turn-on energy losses, the actual dc-link voltage, dc-link voltage in the test conditions, and turn-off energy losses, respectively. This model is an approximation based on datasheet curves; however it is suitable for comparisons among topologies.

In this paper, the losses are divided into conduction (P_{cd}), switching (P_{sw}) and total (P_t), and are given by

TABLE V
SEMICONDUCTOR LOSSES ANALYSIS

Load Type	Topology	Semiconductor Losses					
		Same f_{sw} (10 kHz)			Same THD		
		P_{cd} (%)	P_{sw} (%)	P_t (W)	P_{cd} (%)	P_{sw} (%)	P_t (W)
Case 1	3L–3l	23.35	76.65	442.63	23.35	76.65	442.63
	3L–4l	17.26	82.74	592.71	18.95	81.05	542.00
	4L–3l	28.00	72.00	520.27	33.12	66.88	441.60
	4L–4l	27.78	72.22	525.06	47.04	52.96	310.15
	6L	36.70	63.30	552.94	72.42	27.57	280.37
Case 2	3L–3l	23.37	76.62	497.52	23.37	76.62	497.52
	3L–4l	13.68	86.32	838.97	14.69	85.31	783.91
	4L–3l	31.35	68.65	620.88	42.12	57.87	462.70
	4L–4l	26.10	73.90	743.06	43.53	56.47	445.84
	6L	36.83	63.17	622.12	73.40	26.60	312.34

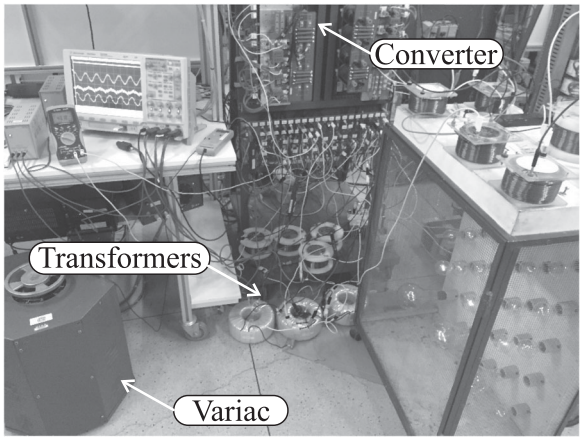


Fig. 11. Experimental platform.

TABLE VI
SETUP USED FOR EXPERIMENTAL RESULTS

Microprocessor	DSP	TMS320F28335
Power switches	Dual module	SKM50GB123D
Driver		SKHI-23
Supply voltage	$V_{\mathrm{g\,k\,(RMS)}}$	63 $\mathrm{V_{(RMS)}}$
Fundamental frequency	f_1	60 Hz
Filter inductance	l_{fk}	2 mH
Filter resistance	r_{fk}	0.5 Ω
DC-link capacitance	C_{dc}	2200 μF
Switching frequency	f_{sw}	10 kHz
Sampling frequency	f_{samp}	10 kHz
Phase a load	l_{la} and r_{la}	18 mH and 8.5 Ω
Phase b load	l_{lb} and r_{lb}	21 mH and 9.5 Ω
Phase c load	l_{lc} and r_{lc}	21 mH and 9.5 Ω

$$P_{cd} = P_{cd(\mathrm{diode})} + P_{cd(\mathrm{trans})} \tag{29}$$

$$P_{sw} = P_{sw\text{-}\mathrm{OFF(diode)}} + P_{sw\text{-}\mathrm{ON(trans)}} + P_{sw\text{-}\mathrm{OFF(trans)}} \tag{30}$$

$$P_t = P_{cd} + P_{sw}. \tag{31}$$

The semiconductor losses analysis is implemented for the two aforementioned types of load (two cases). In case 1, the SAPF compensates a load with lower zero-sequence components (see Fig. 2), and in case 2, SAPF compensates higher zero-sequence components (see Fig. 3). Figs. 9 and 10 show losses of all studied topologies for each case, respectively. Furthermore, two scenarios of comparison have been considered. In the first scenario, all topologies operate with same switching frequency (10 kHz) [see Figs. 9(a) and 10(a)] and, in the second scenario, all topologies operate with different frequencies in order to achieve same THD in grid currents [see Figs. 9(b) and 10(b)]. In other words, the switching frequency of topologies with lower THD is reduced to achieve the THD of 2.7% and 3.14% for case 1 and case 2, respectively.

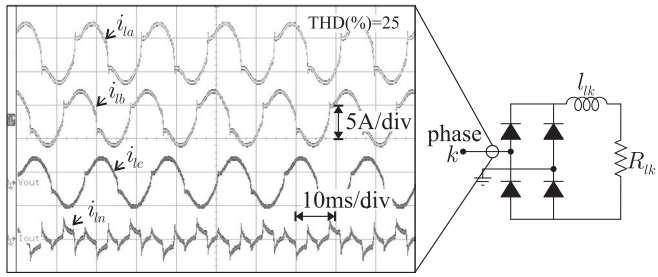


Fig. 12. Experimental load setup, with detailed load circuit and currents.

TABLE VII
EXPERIMENTAL THD AND DC-LINK VOLTAGE

Topology	THD (%)	DC-Link voltage
3L–3l	7	200 V (3.17 p.u.)
3L–4l	6	286 V (4.54 p.u.)
4L–3l	6	170 V (2.70 p.u.)
4L–4l	5.5	170 V (2.70 p.u.)
6L	4.3	100 V (1.59 p.u.)

Figs. 9 and 10 show losses as percentage of topology 3L–3l losses, i.e., 442.63 W (case 1) and 497.52 W (case 2). Table V presents in detail the losses results shown by Figs. 9 and 10. This table presents the values of P_t in watts (W) and, P_{cd} and P_{sw} are detailed in percentage of P_t.

From Figs. 9(a) and 10(a), i.e., scenario with same switching frequency, it is noticeable that losses are directly proportional to number of switching devices and dc-link voltage. It can be seen that losses of 3L–4l and 4L–4l (X–4l) are higher

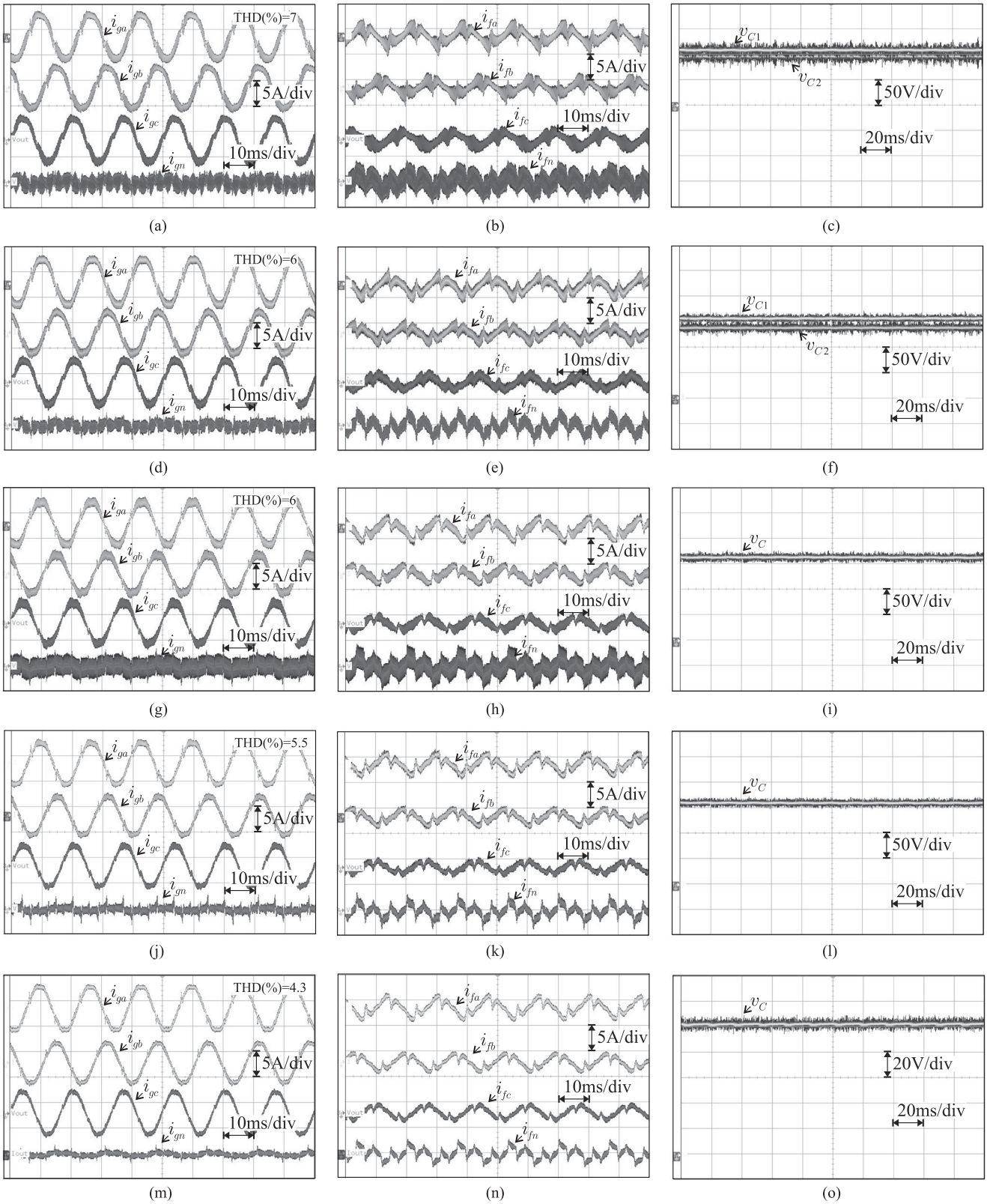


Fig. 13. Experimental results. (a)–(c) For topology 3L–3*l*. (d)–(f) For topology 3L–4*l*. (g)–(i) For topology 4L–3*l*. (j)–(l) For topology 4L–4*l*. (m)–(o) For topology 6L. (a), (d), (g), (j), (m) Grid side currents. (b), (e), (h), (k), (n) Filter currents. (c), (f), (i), (l), (o) dc-link voltages.

than 3L–3l and 4L–3l (X–3l), respectively, due to higher dc-link voltage of topologies X–4l. On the other hand, topology 6L even operating with the lowest dc-link voltage due to its high number of switches presents higher power losses than 3L–3l and X–4l, for case 1, and higher than 3L–3l, for case 2.

For Figs. 9(b) and 10(b), all topologies operate with same THD, i.e., different switching frequencies. The topologies X–4l become more efficient due to switching frequency reduction. However, in both cases the 6L is the most efficient topology. It is worth noting that, in load case 2 [see Fig. 10(b)], the topologies X–4l become less efficient comparing with case 1. This fact occurs due to increase of dc-link voltage caused by higher level of zero-sequence components at filter currents. For instance, in the first case [see Fig. 9(b)], the 3L–4l is 22% less efficient than 3L–3l, while 4L–3l has the same losses as 3L–3l, and 4L–4l is 30% more efficient than 3L–3l. On the other hand, in the case 2 [see Fig. 10(b)], the topologies X–4l become less attractive even with reduction of switching frequency. This fact can be noticed from comparison between Figs. 9(b) and 10(b).

V. Experimental Results

All studied topologies were tested through experimental platform shown in Fig. 11. The experimental setup parameters are presented in Table VI. For these results, the topologies operate compensating harmonic, reactive and unbalance contents from nonlinear loads, whose THD, current waveforms (i_{la}, i_{lb}, i_{lc}, and i_{ln}) and detailed circuit are shown in Fig. 12. These three single-phase nonlinear loads have pattern of low zero-sequence harmonics, i.e., load type 1, with THD of 25% approximately.

Experimental results of grid side currents i_{ga}, i_{gb}, i_{gc}, and i_{gn} [see Figs. 13(a), (d), (g), (j), and (m)], of filter currents i_{fa}, i_{fb}, i_{fc}, and i_{fn} [see Figs. 13(b), (e), (h), (k), and (n)] and of dc-link capacitor voltage v_C [see Figs. 13(c), (f), (i), (l), and (o)] are presented in Fig. 13. Additionally, THD of grid currents and dc-link capacitor voltage are given for each topology in its respective figure, and all experimental setup details are given in Table VII. In which dc-link voltages are normalized in p.u. with base value equal to 63 V.

The results of topology 3L–3l are presented in Fig. 13(a)–(c), whereas topology 3L–4l are presented in Fig. 13(d)–(f). For both topologies, the dc-link midpoint connection of both topologies produces unbalance in dc-link voltages [see Fig. 13(c) and (f)]. The grid current THD of 3L–3l is 7% and of 3L–4l is 6%, and total dc-link capacitor voltages are 200 V and 286 V, respectively. The results of topology 4L–3l are presented in Fig. 13(g)–(i), while the same curves for 4L–4l are presented in Fig. 13(j)–(l). The THD of 4L–3l and 4L–4l are, respectively, 6% and 5.5%, and both operate with dc-link voltage of 170 V. It is noticed that topologies X–4l produce less ripple in grid current (lower THD) than X–3l. Finally, results of topology 6L are presented in Fig. 13(m)–(o). This topology requires the lowest dc-link voltage of 100 V, and its grid currents present lowest ripple (lowest THD), among all topologies presented in this paper.

These results are presented in order to show the feasibility and controllability of all topologies. Additionally, it is possible to evaluate the impact of converter in ripple of grid currents and specification of dc-link voltage.

VI. Conclusion

The five most popular topologies based SAPF applied to four-wire systems has been studied in this paper. These topologies were analyzed in terms of ratings of dc-link voltage and current, quality of output waveforms and efficiency, in which the converters have operated under two different scenarios, i.e., compensating two types of loads, differing by the level of zero-sequence harmonics. In this way, it is possible to make the right decision about which topology should be chosen for any industrial plant. Therefore, system modeling, control strategy (including mathematical modeling of controllers), analysis of simulating results and experimental results has been presented as well. First, dc-link behavior was analyzed including detailed voltage specification and stress of current (verifying the current spectra). Once defined the minimum dc-link for the topologies, they were also analyzed and compared to each other in terms of grid currents THD and semiconductor losses. This last figure of merit has been evaluated for two scenarios: 1) all topologies operating with same switching frequency, and 2) all topologies operating with different frequencies in order to achieve the same THD, this last seems to be the fairer way of comparison.

From analysis, it is possible to conclude that the choice of better topology depends on the type of load to be compensated. Therefore, topologies 3L–4l and 4L–4l (structures with inductor in fourth conductor) present better THD performance than 3L–3l and 4L–3l (structures without inductor in fourth conductor), respectively, but X–4l are less efficient in scenarios with high level of zero-sequence current or high unbalance. Then, they become the best solution for scenarios with low zero-sequence compensation. Topologies 3L–3l and 3L–4l require additional voltage sensor at dc-link capacitor and present low frequency components in dc-link current capacitor, which implies in high capacitor losses. These features appear as important drawbacks to be evaluated. The topology 6L is the most efficient topology among all studied structures, mainly due to lowest level of dc-link voltage. However, this topology requires three isolation transformers and higher number of power switches, which means higher weight, size, and cost. At last, by comparing the experimental THD and dc-link voltages, presented in Table VII, with simulation results, presented in Tables IV and III, this paper has shown results in total accordance.

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