Analysis and Mitigation of Interaction Dynamics in Active DC Distribution Systems With Positive Feedback Islanding Detection Schemes

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***Abstract*—The direct current (DC) technology has gained significant momentum in modern distribution systems due to the high penetration levels of dc loads and dc-based distributed generators (DGs). Unlike conventional ac distribution systems, dc distribution systems have the following distinct features that challenge the system stability. 1) The high penetration level of tightly regulated converters used to interface both DGs and loads yields a destabilizing constant power load (CPL) effect in a considerable range of frequencies. 2) The filtering inductors and capacitors form poorly damped *LC* networks that interact negatively with the CPLs leading to further deterioration of the system stability. 3) Because islanding in a dc system can be hardly detected with passive methods due the absence of the frequency and reactive power terms, DGs are usually equipped with active islanding detection methods to detect the grid disconnection state; however, the islanding detection schemes could negatively impact the distribution system stability. The analysis and mitigation of undesirable interaction dynamics in a dc distribution system considering the aforementioned practical characteristics are not reported in the current literature. In this paper, the interaction dynamics of a dc distribution system characterized by a high penetration level of CPLs, and DGs equipped with positive feedback islanding detection scheme are investigated. The factors affecting the system stability with a single and multiple DGs are thoroughly addressed. Further, a stabilizing compensation loop is proposed to mitigate the stability problems and poor damping capability. Detailed time-domain nonlinear simulations and experimental results validate the analytical results.**

***Index Terms*—Active anti-islanding, constant power loads (CPLs), dc distribution systems, distributed generation (DG), stability.**

NOMENCLATURE

$P_{\rm ref}$	Reference power command of a distributed generator (DG).
P	DG injected power.
$I_{\rm ref}$	Reference current command.
I	DG injected current.
V	Voltage at the point of common coupling (PCC).
I_L	DC-grid load current.
$\sim$	Small-signal perturbation.
$*$	Reference command for voltage and current.
X^o	Steady state quantity of $x(t)$.
ω	Positive feedback high pass filter cut-off frequency.
R_T	Combined filter and ac grid resistance.
L_T	Combined filter and ac grid inductance.
$I^g_{d,q}, U^g_{d,q}, V^g{}_{Fd,Fq}$	dq -current and voltage in ac-grid reference frame.
P_s, Q_s	Injected active and reactive power to the ac grid.
ω_g	AC-grid angular frequency.
$I^g_{cd,cq}, U_{cd,cq}, V_{Fcd,Fcq}$	dq -current and voltage in converter reference frame.
$P_{\rm ext}$	External injected power from the dc distribution network.
$m_{cd,cq}$	Voltage-source converter duty ratios.
RLC load	Resistive-Inductive-Capacitive load

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I. INTRODUCTION

RECENTLY, direct current (DC) power distribution systems have received significant acceptance in power grids because new clean energy resources and loads are intrinsically dc. Furthermore, dc systems offer several advantages over the ac counterparts. For example, a synchronization process is not needed to add a new power component to a dc network, whereas the absence of reactive power improves the overall system efficiency. Furthermore, a dc system facilitates the integration of renewable energy sources with simpler control strategies and at low cost [1], [2].

Fig. 1 shows a schematic diagram of a radial active dc distribution system, in which an ac distribution substation is supplying a radial dc distribution feeder and local ac load when the switch $S_{\rm ac}$ is closed. A bidirectional ac/dc converter at the ac point of common coupling (PCC) is employed to integrate the dc distribution system into the existing ac grid. The dc feeder consists of a number of buses; at each bus, a load or a DG unit or both of them can be connected.

Apparently, the dc feeder can be subjected to islanding events. Islanding is defined as the state at which a DG continues supply-

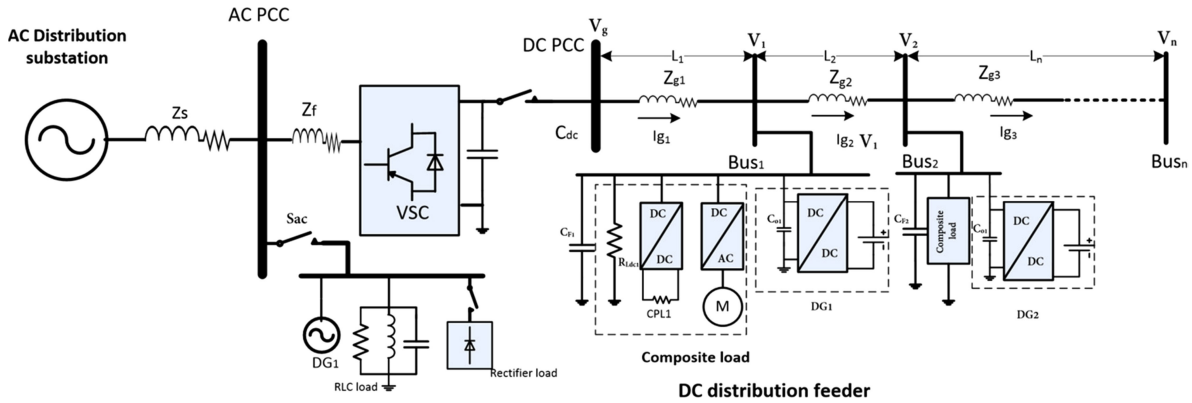


Fig. 1. Radial dc distribution system.

ing power when the distribution system is disconnected either intentionally or unintentionally from the main grid. According to IEEE standards [3], DG units should be equipped with an islanding detection method, and it should be disconnected within 2 s at maximum if the islanded operation is not allowed. The disconnection of DG units is essential for the safety of maintenance personnel and to prevent improper operation of the distribution system. Many passive and active islanding detection techniques were proposed in ac systems. In passive techniques, the voltage and frequency are employed for islanding detection due to the dramatic variations in their values when islanding occurs [4], [5]. In active techniques, small perturbations are injected in the voltage or frequency signals that bring about DG instability in the case of an islanding operation [6]–[8]. However, dc distribution systems do not offer the same monitoring features existing in ac systems, because the available signal to be monitored is only the voltage magnitude. Due to its simplicity and practicality, the positive feedback active islanding technique is usually employed for islanding detection in dc systems [9].

The impact of the positive feedback islanding detection schemes on the stability of multiple grid-connected inverter-based DGs connected to an ac grid was investigated in [10]–[12] using the small-signal modal analysis. It was found that the overall system stability is highly affected by the size and the number of DGs; further, the sensitivity of the power transfer limit to the loading level, load quality factor, and transmission line impedance was addressed. Because dc systems have different characteristics such as the absence of the frequency, reactive power terms, and the tightly regulated nature of the connected loads, the impact of positive feedback scheme on the system stability should be studied considering such important characteristics. The most important feature characterizing the dc distribution system is the high penetration level of tightly regulated point-of-load converters and the low power demand for the resistive loads. The tightly regulated converters and their loads can be viewed by the dc network as constant power loads (CPLs), which insert a negative incremental resistance to the dc network that degrades the system stability [13]. The existence of CPLs is accompanied by the presence of lightly damped *LC* filters that reduce the system stability margin and might lead to the collapse of the network voltage. Therefore, the impact of the positive feedback schemes in a grid-connected dc distribution system becomes a significant concern when the penetration level of CPLs is high, particularly, for a system with multiple DGs and loads distributed along the feeder buses.

Regardless of the positive feedback impact on the system stability, the instability effect caused by CPLs can be compensated by passive or active damping methods. The passive damping methods are realized by inserting passive elements in the network to increase the overall system stability margin; however, these methods increase the cost and yield extra power loss [14], [15]. Hence, the active damping methods have gained large popularity due to their high efficiency because these methods mimic the damping effect of the passive components by modifying the control loops of the converters [16]–[19]. In this paper, a stabilizing method based on the active damping principle is proposed to compensate both the CPL and positive feedback scheme effects on the stability of the dc distribution system. The first objective of this paper is to investigate the interaction dynamics of a typical dc distribution system considering the dynamics of DGs equipped with positive feedback schemes and the high penetration level of CPLs. The second objective is to mitigate the instability associated with the presence of CPLs and DGs equipped with positive feedback islanding detection schemes in the dc distribution system.

This paper is organized as follows. In Section II, the linearized small-signal model of a typical dc distribution system and the positive feedback schemes concept are presented. In Section III, the stability of the proposed system with and without the feedback schemes is assessed. In Section IV, the design guidelines of the proposed stability enhancement method are discussed. In Sections V and VI, time-domain nonlinear simulations and experimental results verifying the analytical results are presented. Finally, the concluding remarks are drawn in Section VII.

II. System Modeling

The equivalent dc network for islanding detection purposes is shown in Fig. 2, where the ac utility and the ac/dc converter can be modeled as a voltage source, plus an *R*-*L* segment (Z_g) representing the short model of the distribution feeder. The load can be modeled as a pure resistive one due to the absence of reactive power in dc systems. Furthermore, a resistive load has

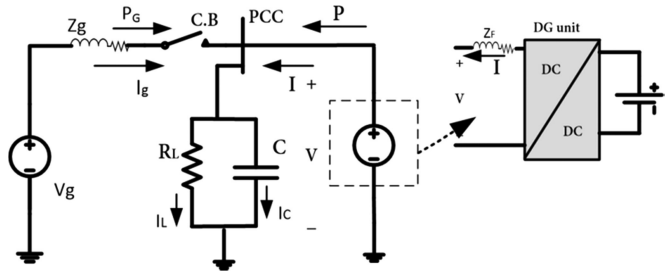


Fig. 2. Islanding detection equivalent circuit in a dc distribution network.

the largest nondetection zone [3]; therefore, it is used in the islanding detection testing model. The DG unit is modeled by a dc voltage-source connected to a dc/dc converter to the PCC. In the grid-connected mode, DGs usually operate to deliver a constant power (*P*), to the network, whereas the function of voltage regulation is performed by the utility side [20], by balancing the load demand with an injected grid power (P_G). The primary objective of the previous model is to study the islanding operating condition, where only the resistive load should be considered to detect the hardest islanding conditions [9]. Therefore, this model cannot be used to study the augmented dc system dynamics.

For the grid-connected operation, details such as ac/dc converter dynamics, the ac grid strength, and dc load characteristics should be considered to accurately investigate the impact of the positive feedback schemes on the entire system dynamics. Fig. 3 shows a detailed schematic diagram of the system depicted in Fig. 2 with one DG and a composite load connected to the DG bus. To study the dynamics of the dc distribution system in details, the switch $S_{\rm ac}$ is assumed to be open for the upcoming analysis, then the impact of the ac bus disturbances dynamics will be investigated. The dc source (V_g) in Fig. 2 is fully represented by a voltage-source converter (VSC) connected to the ac PCC (*U*) via the ac side filter ($R_F - L_F$). The VSC is interfaced to the dc PCC by a dc-link capacitance ($C_{\rm dc}$). The ac side is represented by a stiff voltage source (*E*) and the strength at the PCC is represented by the impedance (Z_s). The VSC is controlled to regulate the dc grid voltage (V_g) and the ac PCC voltage (*U*) to improve the system stability at weak grid conditions [21]. The vector-controlled VSC is synchronized to the ac grid using a standard *dq*-frame three-phase phase locked loop (PLL). The DG unit equipped with a positive-feedback islanding detection scheme, a composite load, and the equivalent bus capacitance (*C*), are connected to the dc PCC through a line with the parameters (R_g, L_g). The modeling details of the system components (VSC, DG, loads, dc feeder) are presented in the next sections. Using the developed models of the system components, the overall system model can be easily derived for any number of buses with DGs and loads. Practical and typical parameters for the cables, converters, and controllers of the system in Fig. 3 are used and given in the Appendix.

A. VSC and AC Grid-Side Dynamics

The dynamics of the interfacing ac/dc VSC and the ac grid can be modeled using the ac grid *d-q* reference frame [22], where the *d*-axis of the reference frame is chosen to align with the ac grid stiff voltage source (*E*). The small-signal model of the ac network dynamics is given by

$$\left(R_T + sL_T\right)\tilde{I}_d^g = \tilde{V}_{Fd}^g + \omega_g L_T \tilde{I}_q^g \tag{1}$$

$$\left(R_T + sL_T\right)\tilde{I}_q^g = \tilde{V}_{Fq}^g - \omega_g L_T \tilde{I}_d^g \tag{2}$$

$$\tilde{U}_d^g = \left(R_s + sL_s\right)\tilde{I}_d^g - \omega_g L_s \tilde{I}_q^g \tag{3}$$

$$\tilde{U}_q^g = \left(R_s + sL_s\right)\tilde{I}_q^g + \omega_g L_s \tilde{I}_d^g \tag{4}$$

$$\tilde{P}_s = 1.5\left(U_d^{go}\tilde{I}_d^g + I_d^o\tilde{U}_d^g + U_q^{go}\tilde{I}_q^g + I_q^o\tilde{U}_q^g\right) \tag{5}$$

$$\tilde{Q}_s = 1.5\left(U_q^o\tilde{I}_d^g - I_d^o\tilde{U}_q^g - U_d^o\tilde{I}_q^g - I_q^o\tilde{U}_d^g\right) \tag{6}$$

$$\tilde{U} = \frac{U^{go}_d}{U^o}\tilde{U}_d^g + \frac{U^{go}_q}{U^o}\tilde{U}_q^g. \tag{7}$$

The dc-link voltage dynamics can be written as [23]

$$s\left(\tilde{V}_g^2\right) = \frac{2}{C}P_{\rm ext} - \frac{2}{C}\left[\tilde{P}_s + T_P\tilde{P}_s S\right] + \frac{2}{C}\left[T_Q\tilde{Q}_s S\right] \tag{8}$$

where $T_P = \frac{2L_F P_s^o}{3U_d^{o\,2}}$ and $T_Q = \frac{2L_F Q_s^o}{3U_d^{o\,2}}$.

The VSC is controlled to regulate the dc grid voltage (V_g) and the PCC of the ac grid (*U*) to their reference value utilizing two PI controllers ($G_{\rm dc}(s)$ and $G_{\rm ac}(s)$, respectively) at the outer control loop of the converter. The output of the outer loop synthesizes the inner loop reference commands. The inner loop is based on vector current control and is realized by two PI controllers ($G_c(s)$) to regulate the converter currents to their reference values generated by the outer loops. The outer and inner loops can be modeled as follows in the converter *d-q* reference frame:

$$\tilde{I}_{cd}^* = \frac{2}{3U_d}\left[-G_{\rm dc}(s)\left(\tilde{V}_g^{2*} - \tilde{V}_g^2\right) + P_{\rm ext}\right] \tag{9}$$

$$\tilde{I}_{cq}^* = -\left[G_{\rm ac}(s)\left(\tilde{U}^* - \tilde{U}\right)\right] \tag{10}$$

$$\tilde{m}_{cd} = G_c(s)\left(\tilde{I}_{cd}^* - \tilde{I}_{cd}\right) \tag{11}$$

$$\tilde{V}_{Fcd} \cong \tilde{V}_{Fcd}^* = \tilde{m}_{cd}\frac{V_g^o}{2} + \tilde{V}_g\frac{M_{cd}^o}{2} + \tilde{U}_{cd} - \omega L_F\tilde{I}_{cq} \tag{12}$$

$$\tilde{m}_{cq} = G_c(s)\left(\tilde{I}_{cq}^* - \tilde{I}_{cq}\right) \tag{13}$$

$$\tilde{V}_{Fcq} \cong \tilde{V}_{Fcq}^* = \tilde{m}_{cq}\frac{V_g^o}{2} + \tilde{V}_g\frac{M_{cq}^o}{2} + \tilde{U}_{cq} + \omega L_F\tilde{I}_{cd}. \tag{14}$$

The VSC is synchronized to the ac grid frame via a three-phase *dq*-PLL that extracts the angle of the voltage at the ac PCC(θ). The angle(θ) relates the voltage and the currents of the converter reference frame to the ac grid reference frame as

$$\left(X^g = X_c e^{j\theta}\right) \tag{15}$$

where X^g is the current or the voltage vector in the ac grid reference frame, and X_c is the current or the voltage vector in the converter reference frame.

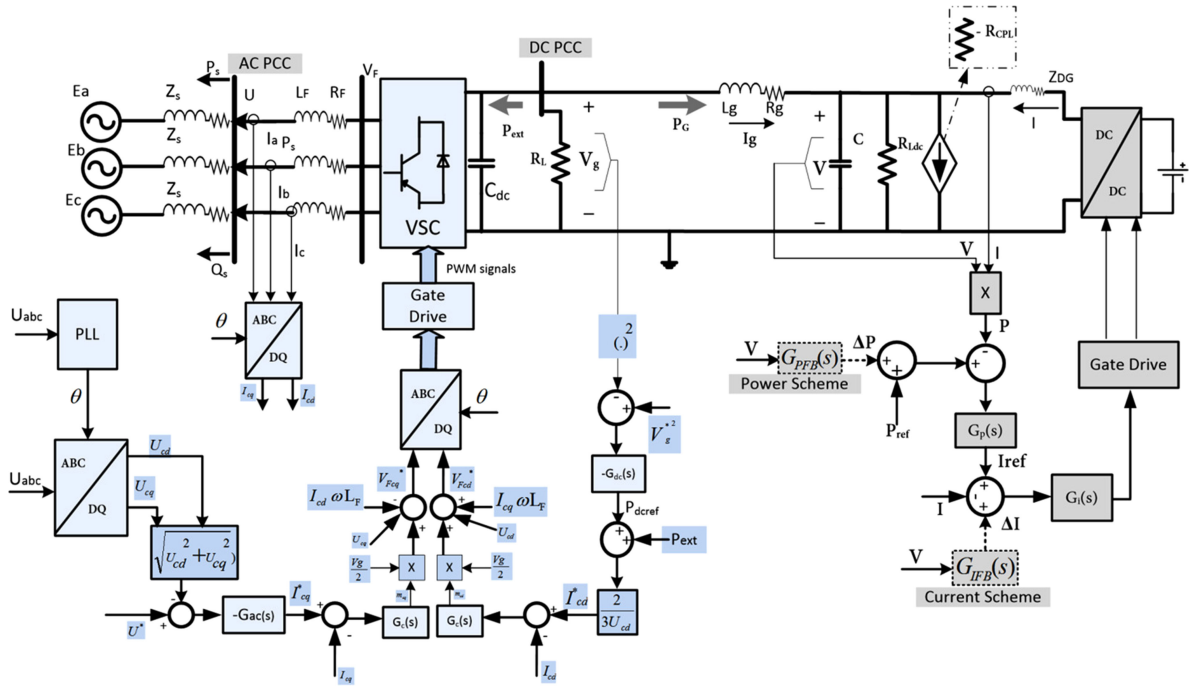


Fig. 3. Detailed dc distribution system.

The transformation of the voltages and currents between the reference frames can be obtained by linearizing (15) into:

$$\begin{bmatrix}\tilde{V}^g_{Fd}\\ \tilde{V}^g_{Fq}\end{bmatrix}=\underbrace{\begin{bmatrix}\cos(\theta_o) & -\sin(\theta_o) & \left(-V^o_{Fcd}\sin(\theta_o)-V^o_{Fcq}\cos(\theta_o)\right)\\ \sin(\theta_o) & \cos(\theta_o) & \left(V^o_{Fcd}\cos(\theta_o)-V^o_{Fcq}\sin(\theta_o)\right)\end{bmatrix}}_{T_1}\times\begin{bmatrix}\tilde{V}^*_{Fcd}\\ \tilde{V}^*_{Fcq}\\ \tilde{\theta}\end{bmatrix} \tag{15a}$$

$$\begin{bmatrix}\tilde{U}_{cd}\\ \tilde{U}_{cq}\end{bmatrix}=\underbrace{\begin{bmatrix}\cos(\theta_o) & \sin(\theta_o) & \left(-U^{g^0}_d\sin(\theta_o)+U^{g^0}_q\cos(\theta_o)\right)\\ -\sin(\theta_o) & \cos(\theta_o) & \left(-U^{g^0}_d\cos(\theta_o)-U^{g^0}_q\sin(\theta_o)\right)\end{bmatrix}}_{T_2}\times\begin{bmatrix}\tilde{U}^g_d\\ \tilde{U}^g_q\\ \tilde{\theta}\end{bmatrix} \tag{15b}$$

$$\begin{bmatrix}\tilde{I}_{cd}\\ \tilde{I}_{cq}\end{bmatrix}=\underbrace{\begin{bmatrix}\cos(\theta_o) & -\sin(\theta_o) & \left(-I^{go}_d\sin(\theta_o)+I^{go}_q\cos(\theta_o)\right)\\ -\sin(\theta_o) & \cos(\theta_o) & \left(-I^{go}_d\cos(\theta_o)-I^{go}_q\sin(\theta_o)\right)\end{bmatrix}}_{T_3}\times\begin{bmatrix}\tilde{I}^g_d\\ \tilde{I}^g_q\\ \tilde{\theta}\end{bmatrix}. \tag{15c}$$

The PLL dynamics can be modeled by [23]

$$\tilde{\theta}=\frac{1}{s}G_{\mathrm{PLL}}(s)\tilde{U}_{cq} \tag{16}$$

where the PLL compensator $G_{\mathrm{PLL}}(s)=K_{p\,\mathrm{PLL}}+\frac{K_{i\,\mathrm{PLL}}}{s}$, $K_{p\,\mathrm{PLL}}$, $K_{i\,\mathrm{PLL}}$ are the compensator constants.

Solving (15) and (16), the phase angle (θ) is related to the PCC voltage (U) in the grid reference frame as follows:

$$\tilde{\theta}=\frac{-G_{\mathrm{PLL}}(s)\sin(\theta_o)}{s+G_{\mathrm{PLL}}(s)x_1}\tilde{U}^g_d+\frac{G_{\mathrm{PLL}}(s)\cos(\theta_o)}{s+G_{\mathrm{PLL}}(s)x_1}\tilde{U}^g_q \tag{17}$$

where $x_1=U^{go}_q\sin(\theta_o)+U^{go}_d\cos(\theta_o)$.

B. DGs and DC Distribution System Dynamics

The DG shown in Fig. 3 is controlled to track a reference power command (P_{ref}) to be injected into the dc distribution system, with two PI compensators ($G_p(s)$ and $G_i(s)$). The outer loop compensator $G_p(s)$ is responsible for regulating the injected power by the DG unit and the inner loop $G_i(s)$ is responsible for regulating the current. Because DGs are interfaced to the dc system by dc/dc and ac/dc converters, the effect of converters output capacitors and the smoothing bus capacitors are denoted in the equivalent model by the equivalent capacitance (C) to accurately consider all the characteristics of emerging dc systems.

In this model, the closed-loop transfer function of the inner current loop is represented by a low-pass filter with a time constant (τ), where $1/\tau$ is the closed-loop current control bandwidth which is selected as 20% of the converter switching frequency [23]. The composite load connected in the investigated system is modeled by a pure resistance ($R_{L\mathrm{dc}}$), and a CPL, represented by its negative incremental resistance ($-R_{\mathrm{CPL}}$) [13], [24], [25].

The resistance (R) is the equivalent composite load resistance. The dc system in Fig. 3, is linearized around a steady state point (V^o, I^o, I_g^o). The load and DG power ratings along with other details and system parameters are provided in the Appendix. The linearized model of the system of Fig. 3 without the positive feedback loops is given by [9]

$$\tilde{V}_g = \tilde{V} + \tilde{I}_g\,(R_g + sL_g) \tag{18}$$

$$\tilde{I} + \tilde{I}_g = \tilde{I}_c + \tilde{I}_L \tag{19}$$

$$\tilde{I}_L = \frac{\tilde{V}}{R}, \qquad \tilde{I}_C = \tilde{V} sC, \text{ and } R = R_{L\mathrm{dc}} // - R_{\mathrm{CPL}} \tag{20}$$

$$\tilde{P} = I^o \tilde{V} + V^o \tilde{I} \tag{21}$$

$$\tilde{I}_{\mathrm{ref}} = G_p(s)\left(\tilde{P}_{\mathrm{ref}} - \tilde{P}\right),\ G_p(s) = K_p + \frac{K_I}{s} \tag{22}$$

$$\tilde{I} = \frac{\tilde{I}_{\mathrm{ref}}}{\tau s + 1} \tag{23}$$

$$\tilde{P}_{\mathrm{ext}} = -\left(V_g^o \tilde{I}_g + I_g^o \tilde{V}_g\right) + \frac{\tilde{V}_g^2}{R_L} \tag{24}$$

where R_L represents the local load at the dc PCC, K_p and K_I are the power compensator constants.

C. Positive Feedback Islanding Detection Schemes

The positive feedback islanding detection schemes are commonly used for islanding detection in ac DGs due to their high accuracy as compared to passive detection schemes, even at the perfect matching between loading and generation. In ac systems, the positive feedback method was applied to the voltage or the frequency signals to inject a disturbance, proportional to the deviation in either the voltage or the frequency signals from their nominal values, to the controller reference command of a DG. In dc systems, the positive feedback concept can be applied only to the voltage signal because the frequency is zero for dc quantities.

In [9], two schemes based on the voltage positive feedback were proposed, the islanding is detected when the stand-alone system consisting of the DG unit and the elements connected to the same bus are driven to an unstable state. To push the system into an unstable state, a disturbing signal is added to the DG unit control loops, which will force the DG to operate unstably or operate at an undesired equilibrium point. This disturbing signal is obtained by applying the voltage deviation of the PCC through a gain to either the outer loop (power scheme) or the inner loop (current scheme) of the DG controller. In each scheme (as shown in Fig. 3), the signal applied to the positive feedback loop is obtained by either processing the measured voltage by a high-pass filter (filter-based methods) or using the deviation of the PCC voltage from the nominal voltage (voltage reference-based method). A detailed comparison study was conducted in [9] to show the advantages and disadvantages of each of the four methods. In this work, the filter-based methods are selected for both schemes due to their operating advantages compared to the voltage reference methods. The latter methods might induce a steady state disturbing signal if the grid voltage is deviated from its nominal value, whereas the filter-based methods mitigate this problem leading to a higher robustness in the system dynamics.

1) Current Loop Disturbance Scheme: The current loop disturbance scheme for islanding detection is based on injecting a current disturbance (ΔI) to the inner control loop of the DG controller. This disturbance is obtained by processing the dc PCC voltage by a high-pass filter ($G_{\mathrm{IFB}}(s)$) as shown in Fig. 3; the deviation is converted into the current disturbance signal applied to the inner control loop of the DG via the current positive feedback gain (K_{IFB}).

For the current scheme, the change in reference current will be modified to

$$\tilde{I}_{\mathrm{ref}} = G_p(s)\left(\tilde{P}_{\mathrm{ref}} - \tilde{P}\right) + G_{\mathrm{IFB}}(s)\tilde{V} \tag{25}$$

where $G_{\mathrm{IFB}}(s) = K_{\mathrm{IFB}}\frac{s}{s+\omega}$ and K_{IFB} is the current feedback gain.

2) Power Loop Disturbance Scheme: The main idea of this scheme is to inject a power disturbance (ΔP) in the outer control loop of the DG controller; this disturbance is directly proportional to the deviation of the PCC voltage.

Similar to the current disturbance scheme, according to Fig. 3, the disturbance is obtained by applying the measured voltage to a high-pass filter ($G_{\mathrm{PFB}}(s)$), and converted into a power signal via power feedback gain (K_{PFB}).

Following the same approach of the previous scheme, the change in the reference current will be modified to

$$\tilde{I}_{\mathrm{ref}} = G_p(s)\left[\left(\tilde{P}_{\mathrm{ref}} - \tilde{P}\right) + G_{\mathrm{PFB}}(s)\tilde{V}\right] \tag{26}$$

where $G_{\mathrm{PFB}}(s) = K_{\mathrm{PFB}}\frac{s}{s+\omega}$ and K_{PFB} is the power feedback gain.

Equations (1)–(26) describe the small-signal dynamics of each subsystem in the s-domain. Using these models, the dynamics of the overall dc system, with any number of buses, DGs, and loads can be easily derived. The overall system dynamics and stability limits can be investigated by transferring the model in (1)–(26) into an augmented state-space model as given in (27). The block diagram in Fig. 4 shows the interlinking between the subsystems,

$$\begin{aligned}\dot{\tilde{\mathrm{X}}} &= \mathrm{A}\tilde{\mathrm{X}} + \mathrm{B}\tilde{U}\\ \tilde{Y} &= C\tilde{X} + D\tilde{U}.\end{aligned} \tag{27}$$

III. Stability Analysis

In this section, the small-signal stability of the system shown in Fig. 3 is investigated. The system parameters affecting the system stability when the DG is equipped with and without the positive feedback islanding detection schemes are presented. The minimum gains required for islanding detection for each scheme are calculated based on the formulas obtained in [9]; however, these gains should ensure the absolute system stability for the grid-connected mode. Therefore, based on the state-space model developed in (27), the maximum feedback gain that drives the system to marginal stability in the grid-connected mode is developed for each scheme. The minimum feedback gain will

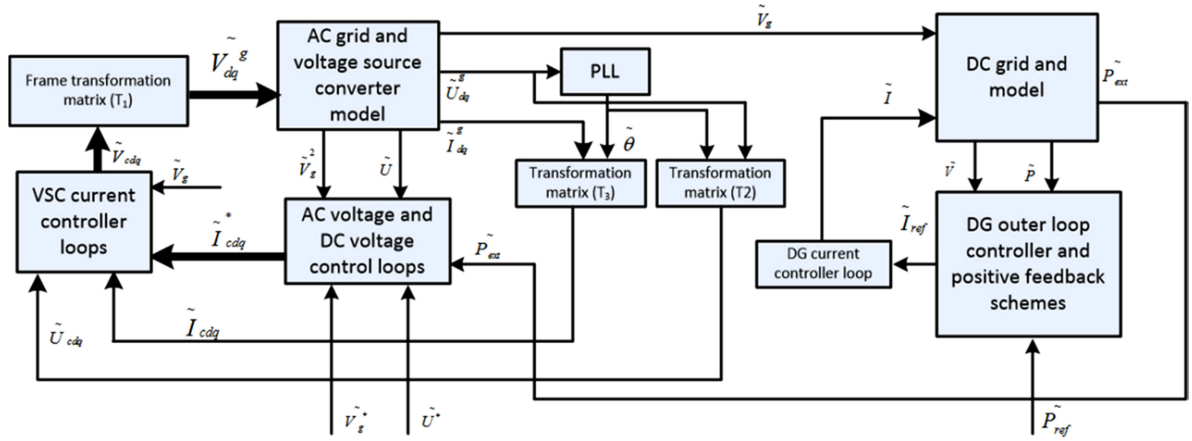
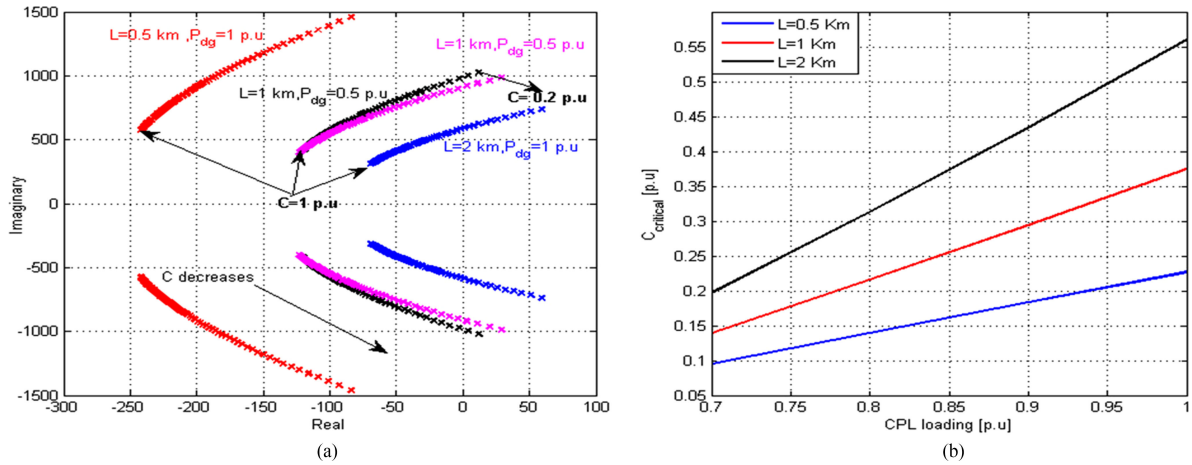


Fig. 4. Overall system block diagram.



(a) (b)

Fig. 5. DC distribution system stability without positive feedback schemes. (a) Dominant eigenvalues for different feeder lengths. (b) Critical capacitance against CPL penetration level at different locations.

be considered as the base value to normalize the results for better comparative analysis. The nominal values of other system parameters are given in the Appendix.

A. System Stability Without Positive Feedback

With the help of the state-space model developed in (27), the dominant eigenvalues are plotted in Fig. 5(a) when the dc bus capacitance is varied from 0.2 to 1 pu at different DG locations (0.5–2 km), and keeping the CPL loading 1 pu. It is clear that the dominant eigenvalues move towards the right-hand side of the *s*-plane as the bus capacitance decreases for a specific DG location. Further, the eigenvalues location moves further to the right of the s-plane as the feeder length increases, leading to unstable states for a low dc bus capacitance. On the same figure, it is clear that the variation of the DG output power does not have the same destabilizing as the DG location and the bus capacitance, resulting in almost the same eigenvalues if the DG power is dropped from 1 to 0.5 pu. The CPL penetration level impact on the system stability is demonstrated in Fig. 5(b) by plotting the critical capacitance required for marginal stability against the CPL loading at different feeder lengths. It is clear that the critical dc bus capacitance varies significantly with the CPL loading and the DG location. The critical capacitance is doubled when the CPL level increases from 0.7 to 1 pu, if the DG is located at 0.5 km from the PCC, whereas this capacitance increases from approximately 0.15 to 0.38 pu, if the DG location is located at 1 km. Accordingly, it is clear that the system stability is significantly affected by the grid strength, bus capacitance, and the CPL penetration level.

B. System Stability With Positive Feedback

The minimum gain $(K_{\min})$ required to detect the islanding event is calculated for the hardest islanding case, i.e., when the power delivered by the DG unit equal to the power absorbed by the connected load (zero power mismatch). It should be noted that the highest stability condition is achieved with a pure resistive load; therefore, to ensure detection at the hardest condition, the minimum gain will be calculated considering 100% resistive loading ($R = R_{L\mathrm{dc}} = 1$ pu) at the DG bus.

To calculate the minimum gain for islanding detection, the islanded network (when the *C.B* opens) shown in Fig. 2 consisting of the DG unit and the load should be driven to an unstable

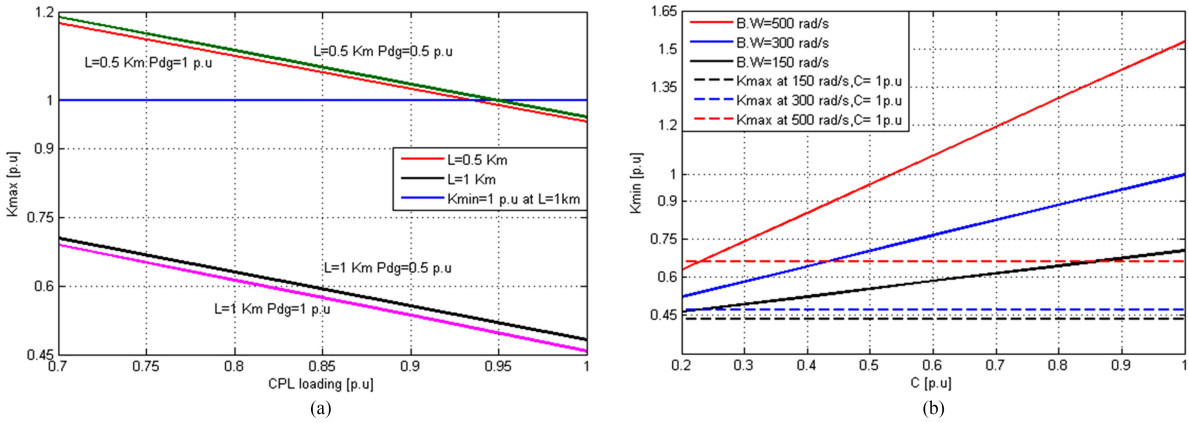


Fig. 6. Current scheme effect on the system stability. (a) Maximum gain against CPL penetration level. (b) Minimum gain against bus capacitance.

state. With each islanding detection scheme, the voltage characteristic equations are derived. Then, the Routh–Hurwitz stability criterion is adopted to find the minimum gain that forces the system eigenvalues into the marginal stability conditions in each scheme.

1) Current Scheme: For the current scheme, the change in the reference power command $\tilde{P}_{\rm ref}$ is set to zero; therefore, the change in the reference current given in (25) is modified into

$$\tilde{I}_{\rm ref} = (-\tilde{P})\left(K_P + \frac{K_I}{s}\right) + \frac{K_{\rm IFB}s}{s+\omega}\tilde{V}. \tag{28}$$

Assuming fast current dynamics with respect to the power loop dynamics [8], and solving (19)–(21), and (28), the voltage characteristic equation is given by

$$a_3 s^3 + a_2 s^2 a_1 s + a_0 = 0 \tag{29}$$

where

$$\begin{aligned} a_3 &= C + CV^o K_p, \quad a_2 = \omega C + \frac{1}{R_{L\rm dc}} + CV^o K_I \\ &\quad + \omega K_P V^o C + \frac{2V^o K_p}{R_{L\rm dc}} - K_{\rm IFB}, \\ a_1 &= \frac{\omega}{R_{L\rm dc}} + \omega K_I V^o C + \frac{2V^o K_I}{R_{L\rm dc}} + \frac{2\omega V^o K_p}{R_{L\rm dc}}, \text{ and} \\ a_0 &= \frac{2\omega V^o K_I}{R_{L\rm dc}}. \end{aligned}$$

Applying the Routh–Hurwitz stability criterion on (29), the minimum gain for islanding detection can be given by

$$K_{\rm min} \cong \frac{I^o}{V^o} + CV^o K_I + 2I^o K_p. \tag{30}$$

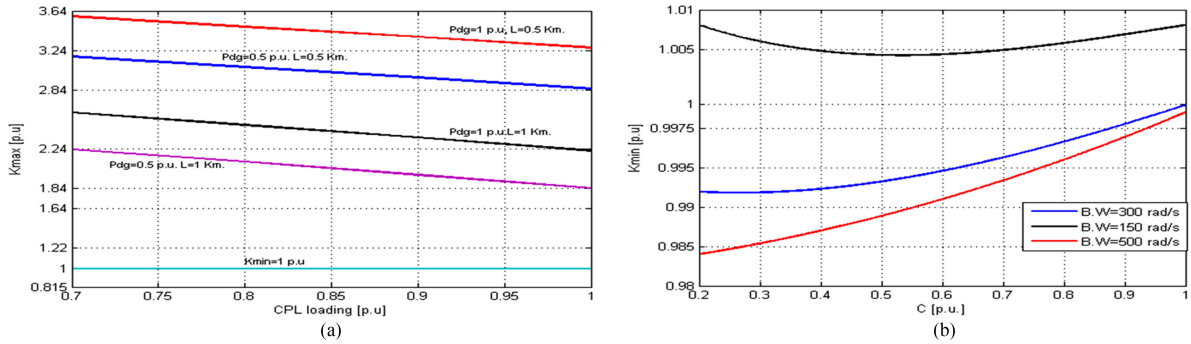
From (30), it is clear that the minimum gain for islanding detection with the current scheme employed is dependent on the system operating point, bus capacitance, and outer loop controller gains.

The impact of the positive feedback schemes on the system stability can be evaluated with the help of the maximum feedback gain satisfying the marginal stability condition. Fig. 6(a) shows the variation of the marginal current feedback gain with the CPL penetration level at different DG locations and operating conditions. At 0.5 km feeder length, it is evident that the maximum gain decreases as the CPL level increases. The maximum gain is 1.2 higher than the minimum value for 0.7 pu CPL, whereas the minimum and maximum gains are equal when the CPL is approximately 0.95 pu. The marginal gain is less than the minimum gain if the CPL is 1.0 pu; this indicates an unstable system for this loading condition.

If the DG is located at 1 km away from the PCC, the marginal gain is less than the minimum for all CPL penetration levels. It should be noted that the DG operating power has a slight effect on the marginal gain; on the other hand, the DG location and the CPL penetration level have the most significant effect on the system stability. To mitigate the previous problem, the power loop bandwidth and the bus capacitance can be varied to modify the minimum detection gain (1 pu CPL and $L = 1.0$ km) as depicted in Fig. 6(b). It is clear that the minimum islanding gain decreases with the reduction of the bus capacitance; however, this will be associated with a reduction in the system stability as indicated in Fig. 5(a). Similarly, it can be observed that decreasing the bandwidth will reduce the minimum detection gain; however, the maximum gain will decrease with the power loop bandwidth showing about (0.45 pu) with (1 pu) bus capacitance. From the previous analysis, it is clear that the employing the positive feedback current scheme of exhibits stability problems with the DG location and CPL penetration level.

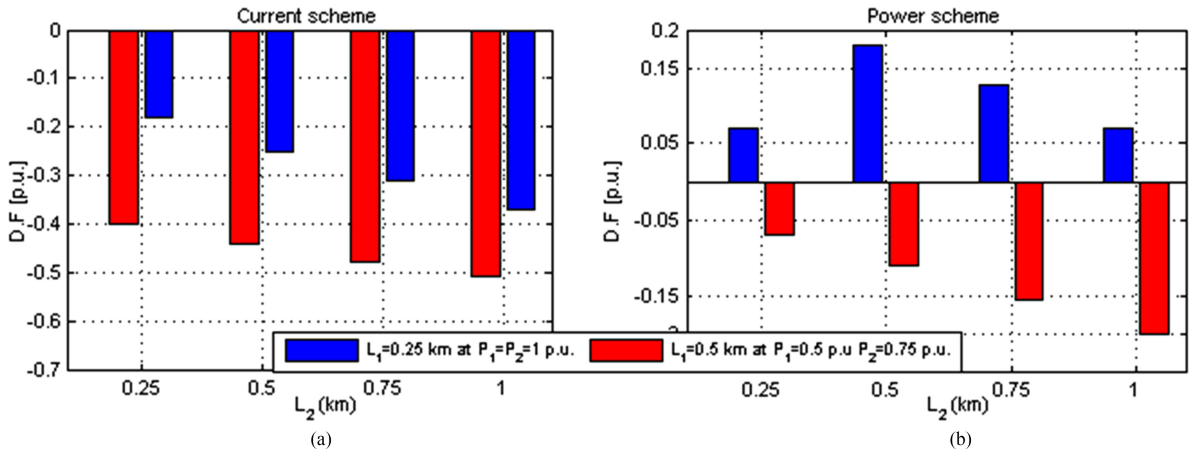
2) Power Scheme: Similarly, the minimum gain $(K_{\rm min})$ required to detect islanding for the power scheme should be calculated at the hardest operating conditions, where the load is 100% pure resistance and the DG unit is supplying its rated power. Under islanding conditions, the voltage characteristic equation can be obtained in (31) by solving (19)–(21), and (26), [8]:

$$\begin{aligned} &a_3 s^3 + a_2 s^2 a_1 s + a_0 = 0 \\ &a_3 = C + CV^o K_p,\ a_2 = \omega C + \frac{1}{R_{L\rm dc}} + CV^o K_I \\ &\quad + \omega K_P V^o C + \frac{2V^o K_p}{R_{L\rm dc}} - K_{\rm PFB} K_p \\ &a_1 = \frac{\omega}{R_{L\rm dc}} + \omega K_I V^o C + \frac{2V^o K_I}{R_{L\rm dc}} + \frac{2\omega V^o K_p}{R_{L\rm dc}} - K_{\rm PFB} K_I \\ &a_0 = \frac{2\omega V^o K_I}{R_{L\rm dc}}. \end{aligned} \tag{31}$$



(a) (b)

Fig. 7. Power scheme effect on the system stability. (a) Minimum gain against bus capacitance. (b) Maximum gain against CPL penetration level.



(a) (b)

Fig. 8. Damping factor for two-DG system at different locations and operating points. (a) Current scheme. (b) Power scheme.

Applying the Routh–Hurwitz stability criterion on (31), the minimum gain for islanding detection can be given by

$$K_{\min} \cong \frac{2V^o}{R_L} + \phi \approx 2I^o \tag{32}$$

where ϕ has a negligible effect on the minimum gain value, and is a function of the bus capacitance, and outer loop controller bandwidth.

Unlike the current scheme, the power scheme shows higher stability margins even with high CPL penetration level (1 pu). As shown in Fig. 7(a), it can be seen that the lowest marginal gain is approximately 1.84 pu for 0.5 pu DG output power and feeder length 1.0 km. It can be noted that the marginal stability of the system is significantly affected by the DG power as the feeder length and the CPL penetration level increase. On the other hand, the power loop controller bandwidth and the dc bus capacitance have a negligible effect on the minimum gain of the power scheme as indicated in Fig. 7(b), which also agrees with (32).

C. System Expandability

Extending the system capacity is one of the most concerns that could affect the overall system performance when the DGs are equipped with positive feedback islanding detection schemes. Therefore, the performance of a multi-DG system is investigated to show the impact of the islanding schemes on the overall system stability. The DGs can be connected at the same PCC or at different locations of the distribution feeder (radial distribution configuration) as shown in Fig. 1. The radial configuration has shown more stability problems than the other configuration; therefore, a two-DG radial distribution system is studied to assess the system dynamics. With the help of the schematic in Fig. 1, the single DG model given in (18)–(24) can be modified to include the second bus (V_2) with another DG and composite load and separated from the first DG bus via a line with the parameters (R_{g2}, L_{g2}). The network current and voltages can be modified to

$$\tilde{V}_g = \tilde{V}_1 + \tilde{I}_{g_q}\left(R_{g1} + sL_{g1}\right) \tag{18a}$$

$$\tilde{V}_2 = \tilde{V}_2 + \tilde{I}_{g_2}\left(R_{g2} + sL_{g2}\right) \tag{18b}$$

$$\tilde{I}_1 + \tilde{I}_{g1} = \tilde{I}_{c1} + \tilde{I}_{L1} \tag{19a}$$

$$\tilde{I}_2 + \tilde{I}_{g2} = \tilde{I}_{c2} + \tilde{I}_{L2}. \tag{19b}$$

Using the developed DG and load models, adding the second bus with a DG and composite load along with the feeder section to obtain the overall small-signal model is straightforward.

The impact of equipping two DGs in a radial system with both schemes for islanding detection can be assessed by the overall system damping factor. The damping factor of two-DG units located at different locations of the distribution feeder is shown in Fig. 8, it is evident that the system damping factors are negative for all operating points and DG units' locations, indicating system instability with the current scheme. Similarly, for the power scheme, extending the system capacity by adding

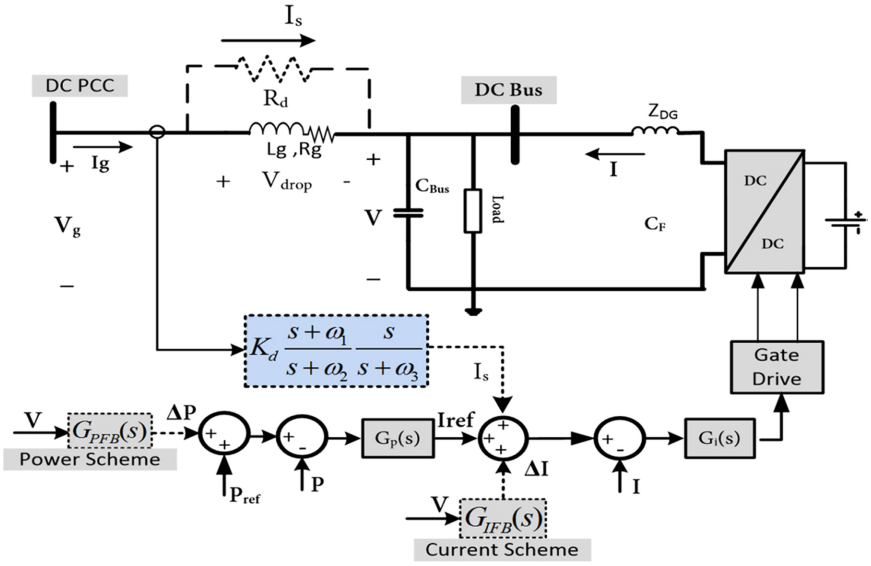


Fig. 9. Proposed stabilizing loop for a DG equipped with islanding detection schemes.

a DG unit would decrease the overall system stability. Although the power scheme shows better damping capability over the current scheme, the system damping capability is very poor even with the DGs operating at their full capacities. Further, the system loses its stability if the DGs operating point moves to lower values.

IV. Stability Enhancement

From the previous analysis, it is clear that a dc distribution system with CPLs and DGs equipped with positive feedback islanding detection techniques will exhibit stability problems, particularly with the current scheme, where the application of this scheme is limited to short feeder lengths and specific CPL penetration level. The first source of instability is the negative incremental resistance inserted by the CPL effect, and the interaction between the feeder inductor and the bus capacitance, which behaves as *LC* network adding further degradation to the system stability. The second source of instability is employing the positive feedback islanding detection schemes, which have an increased destabilizing effect as the feeder length increases. Further, the overall system stability degrades when the system capacity is increased by adding another DG unit due to the negative interaction dynamics among DG units. Hence, a stabilizer is required to mitigate the instability caused by the positive feedback schemes and the CPL effect.

A. Overview of Previous Works

Many stabilizing techniques were proposed to alleviate the degradation in the system stability caused by CPLs; those methods are based on the active damping principle. The active stabilizing methods inject a stabilizing (damping) current either to the CPL side inner loops, or the source-side converter. Adding a stabilizing current to the load-side converter may affect the load performance; therefore, employing the stabilizing current to the source-side converter is preferred to avoid distorting the load performance. One way of improving the system stability is utilizing the bus capacitance of the unstable network; for example, a virtual resistor can be connected across the bus capacitance [26], or in series with bus capacitance [27]. Another method is to insert a virtual capacitor across the filter bus capacitance [28]. Another approach is to utilize the feeder inductor (CPL input filter); for instance, a virtual resistor can be inserted in series with the inductor of the CPL input filter. The output current of the source side converter is converted into a stabilizing reference voltage signal through the virtual resistance; this signal is then added to the source side converter voltage control loop [25]. The virtual resistor can also be inserted across the impedance tying the CPL and the dc source [29], where the injected stabilizing current is proportional to the voltage drop across the line impedance. The main disadvantage of this approach is the difficulty of measuring the dc source voltage. Therefore, a state estimator is used to obtain the source voltage; however, the system complexity increased.

B. Proposed Stabilizing Loop Concept

Because the primary objective of damping methods is to stabilize the network voltage, whereas the positive feedback scheme tends to destabilize the system during islanding condition to facilitate islanding detection, the system should offer a high stability margin in the grid-connected mode and facilitate accurate and fast islanding detection in the islanding events. Therefore, the primary objective of the proposed stabilizing compensator is to inject a stabilizing current component to the converter current (inner) loop. This component is derived from the grid current signal (input current to the PCC) so that the stabilizing loop is only activated in the grid-connected mode. The reason behind selecting the grid current, not the bus voltage, is avoiding the conflict between the positive feedback loop and the stabilizing loop; the grid current will diminish for islanding operation, and hence the stabilizing loop will be idle.

The proposed stabilizing loop, shown in Fig. 9, is mimicking a virtual resistor connected across the terminals of the impedance of the line connecting the dc PCC and the DG unit. Adding a

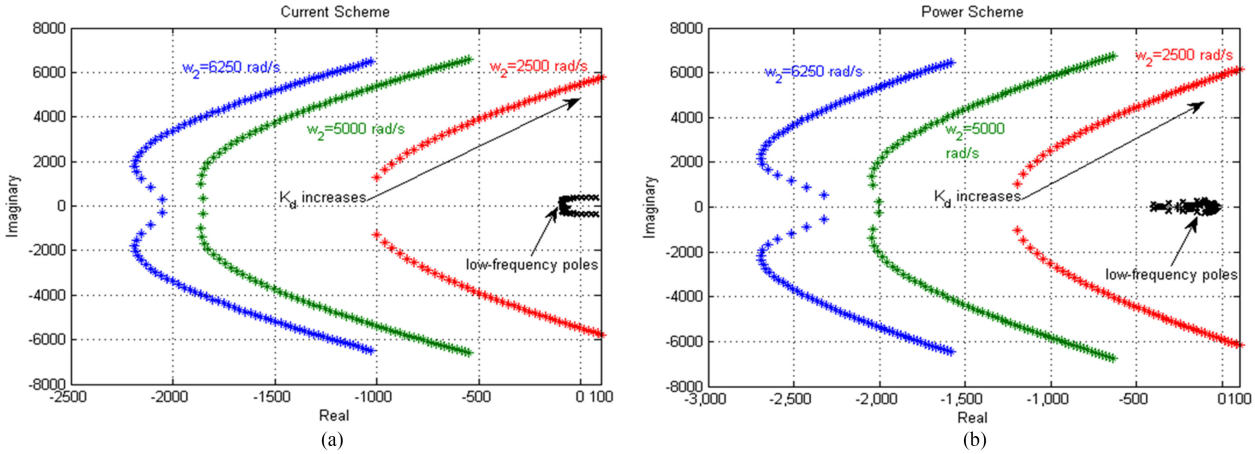


Fig. 10. Dominant eigenvalues with the stabilizing loop used. (a) Current scheme. (b) Power scheme.

resistance to the system increases the positive damping capabilities and improves the overall system stability. The stabilizing component (I_s) can be obtained by dividing the voltage drop across the line ($V_{\rm drop}$) by a resistor R_d as given:

$$I_s = \frac{V_{\rm drop}}{R_d} = \frac{V_g - V}{R_d}. \tag{33}$$

Due to the difficulties associated with 1) measuring the voltage drop across the line, 2) using communication to obtain the remote VSC output voltage, or 3) estimating the grid voltage, the voltage drop ($V_{\rm drop}$) is obtained using the grid current (I_g) as given:

$$V_{\rm drop} = I_g\left(R_g + sL_g\right) \tag{34}$$

$$I_s = \frac{V_{\rm drop}}{R_d} = \frac{I_g\left(R_g + sL_g\right)}{R_d} = \frac{L_g}{R_d}\left(s + \frac{R_g}{L_g}\right) I_g. \tag{35}$$

Equation (35) includes a differentiator term; this term can interact negatively with the system noise, such as the noise resulting from the converter switching nature. To avoid the differentiator problems, a low-pass filter with a cutoff frequency $\omega_2$is employed to the stabilizer transfer function, as given:

$$I_s = \frac{L_g}{R_d}(s+\omega_1)\frac{\omega_2}{s+\omega_2} I_g \tag{36}$$

where $\omega_1 = \frac{R_g}{L_g}$, ω_2 is the cutoff frequency of the low-pass filter.

Rearranging the previous equation

$$I_s = K_d \frac{s+\omega_1}{s+\omega_2} I_g \tag{37}$$

where $K_d = \frac{\omega_2 L_g}{R_d}$ is the stabilizing gain.

To allow the stabilizer to be activated only during transients, a high-pass filter is added to the stabilizer transfer function; then, the stabilizing current I_s is given:

$$I_s = K_d \frac{s+\omega_1}{s+\omega_2}\frac{s}{s+\omega_3} I_g = G_s(s) I_g \tag{38}$$

where ω_3 is the cutoff frequency of the high-pass filter.

Accordingly, the reference current for the current and power schemes given in (25) and (26) are modified to (39) and (40) to include the stabilizing loop dynamics, respectively,

$$\tilde{I}_{\rm ref} = G_p(s)\left(\tilde{P}_{\rm ref} - \tilde{P}\right) + G_{\rm IFB}(s)\tilde{V} + G_s(s)\tilde{I}_g \tag{39}$$

$$\tilde{I}_{\rm ref} = G_p(s)\left[\left(\tilde{P}_{\rm ref} - \tilde{P}\right) + G_{\rm PFB}(s)\tilde{V}\right] + G_s(s)\tilde{I}_g. \tag{40}$$

C. Design Guidelines

The capability of the stabilizer to effectively mitigate the system instability caused by the positive feedback schemes and CPLs depends on the proper selection of the compensator parameters $\omega_1, \omega_2, \omega_3$, and K_d. The following procedure is applied to a single-DG system for better understanding, and hence the two-DG case is investigated.

The first design parameter ω_1 can be easily obtained as given in (36) because the ratio between the line resistance and inductance is fixed and readily known to the designer through the line characteristics offered by the manufacturer. Because the line resistance and inductance are given per unit length, ω_1 can be considered constant for a particular system under study, as long as the same cable is used. The second parameter ω_2 is selected based on the bandwidth of the low-pass filter added in (37) to overcome the differentiator problem existing in (36). Because the low-pass filter is measuring the grid current, it has to pass the resonance frequency of the *LC* network formed by the bus capacitance and the line inductor [13]. A typical value of ω_1 can be selected to be 10 times the resonance frequency of the *LC* network as recommended in [13]. Because the inductance is obtained based on the line length and the bus filter capacitance is predefined to the system designer, the value of ω_2 can be easily obtained. It should be mentioned that the design of ω_1 in this study is based on a line length of 1.0 km. The cutoff frequency ω_3 of the high-pass filter is chosen such that it does not affect the effective range of the low-pass filter; therefore, the cutoff frequency of the high-pass filter is selected to be as small as possible (few hertz). Finally, with the help of the state-space model developed, the stabilizing gain K_d could be chosen such that all the system poles are located in the left-hand side of the s-plane. For optimum performance, this gain could be chosen to maximize the damping factors of the dominant eigenvalues.

The variation of the system eigenvalues with the stabilization gain is shown in Fig. 10(a) and (b) for the current and power

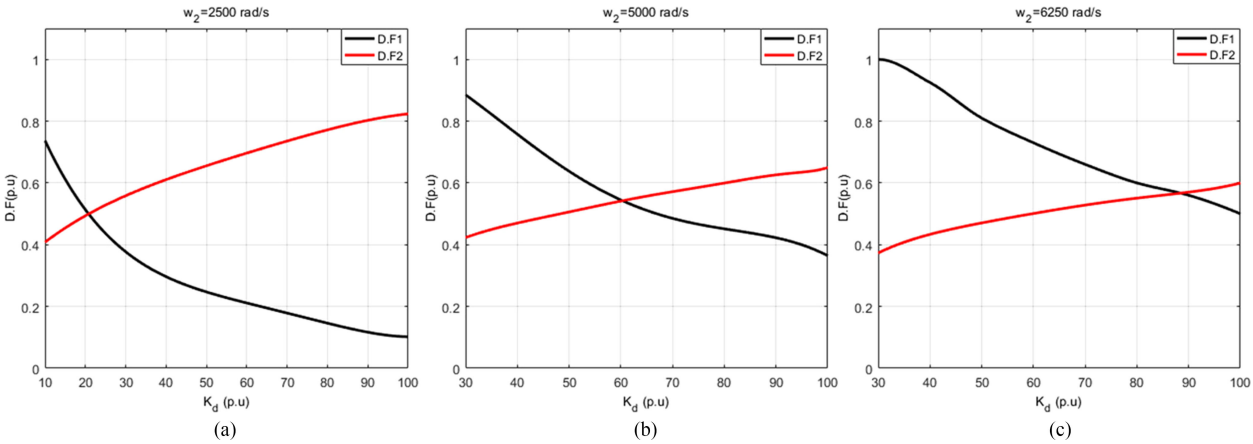


Fig. 11. Current scheme: damping factor variation against stabilizing gain at different cutoff frequencies.

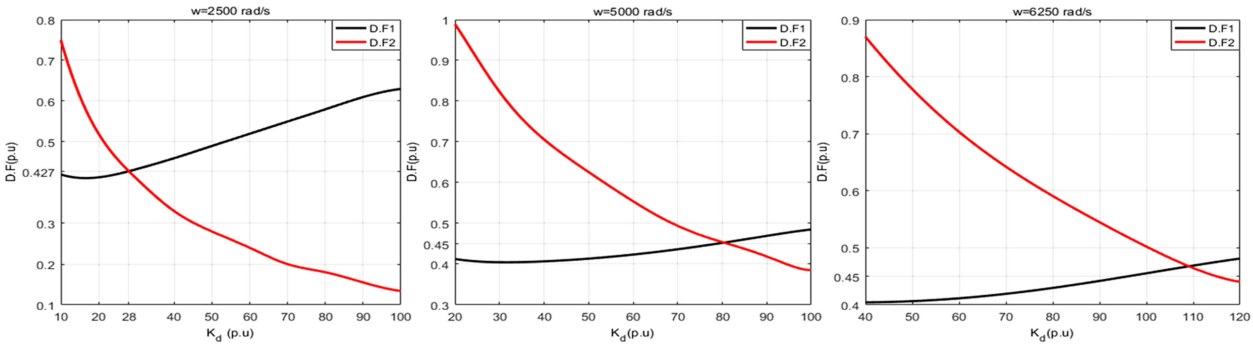


Fig. 12. Power scheme: damping factor variation against stabilizing gain at different cutoff frequencies.

schemes, respectively. The gain is varied from 0 to 300 pu, and the eigenvalues are obtained for three different low-pass filter frequencies (ω_2). The value of ω_2 is designed to be ten times higher than the *LC* network resonance frequency ($\omega_2 =$ 5000 rad/s) and is set to 2500 and 6250 rad/s to account for the variation of the equivalent dc bus capacitance that might result from converters connections and disconnections. It is evident that the low- and medium-frequency eigenvalues are affected by varying the stabilizing gain K_d, the low-frequency eigenvalues responsible for system stability are the same for different values of ω_2; however, the higher frequency poles move further to the left of the *s*-plane as the cutoff frequency increases. It is also evident that increasing the gain K_d does not guarantee the system stability as indicated when $\omega_2 = 2500$ rad/s, where the eigenvalues moved to the right-hand side of the *s*-plane for $K_d = 300$ pu.

For optimum damping capability, the damping factors of the dominant eigenvalues of a system equipped with the current scheme for islanding detection, are plotted against the stabilizing gain (K_d) at different cutoff frequencies as shown in Fig. 11. The optimum stabilizing gain is located at the intersection point of the two damping factor curves so that the damping factors of the dominant eigenvalues are the same. It is clear that the optimum stabilizing gain and the damping factor increase as the cutoff frequency increases, where the damping factor increases from 0.5 to 0.5636 pu when ω_2 varies from 2500 to 6250 rad/s. Similarly, for the power scheme, both the optimum stabilizing gain and the damping factor increase as the low-pass filter cutoff frequency increases as depicted in Fig. 12, improving the damping factor from 0.427 to 0.4678 pu, when ω_2 varies from 2500 to 6250 rad/s. It should be noted the optimum damping factor obtained in the current scheme is higher than the improved damping factor of the power scheme, assuming the equal damping factor criterion is used to find the optimum gain and damping factor.

The previous analysis was conducted with the DG operating at its rated power (1 pu) and feeder length of 1.0 km. The impact of varying the operating point and the DG location was considered to investigate the capability of the stabilizing loop to operate efficiently at different conditions. For the current scheme, Fig. 13(a) shows the damping factor and stabilizing gain variation against the feeder length at various operating conditions. It is clear that damping factor is slightly affected by the DG operating point when the DG power drops from 1 to 0.5 pu for different DG locations. Further, the damping capability increases as the feeder length increases, as it reaches to about 0.6 pu if the DG is located at 1.5 km away from the PCC. On the contrary, the optimum stabilizing gain varies significantly as the DG moves away from the dc PCC; however, this gain almost does not change with the DG operating point to achieve the optimum damping factor.

On the other hand, in the power scheme performance shown in Fig. 13(b), at the rated power operation, the damping factor is almost the same (0.45 pu.) along the dc distribution feeder, except when the DG is only 0.25 km away from the PCC, the

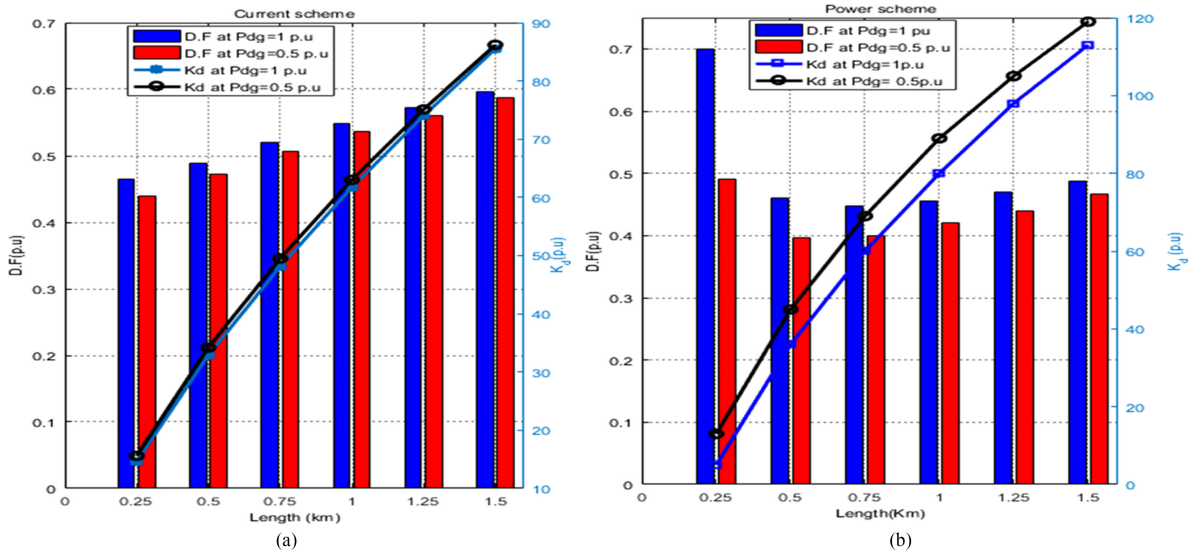


Fig. 13. Damping factor and stabilizing gain variation against feeder length at different operating conditions. (a) Current scheme. (b) Power scheme.

damping factor rises to 0.7 pu. Although the operating point does have a significant effect on the system stability of the power scheme, the reduction in the DG power has a slight effect on the system when the stabilizing loop is used. Similar to the current scheme, the optimum stabilizing gain increases as the DG location changes to obtain the optimum damping factor; however, this gain needs to be slightly modified to achieve the optimum damping if the DG output is dropped from 1 to 0.5 pu.

D. Impact of Converters Filter Structure and DC System Uncertainties

In this section, the impact of the converters filter structure, and variation of system parameters such as the inner loop bandwidth and the bus capacitance, are investigated to assess their effect on the overall system dynamics and proposed stabilizing method functionality.

1) Inductor-Capacitor-Inductor (LCL) Filter Configuration: LCL filters have been widely used as ac-side filters in grid-connected VSC systems, as they effectively attenuate switching harmonics injected by the converters that facilitate high bandwidth current controller and allow proper mitigation of the distorted injected grid current. The LCL network can be connected at the dc bus to filter out the injected current to the dc system. The impact of using LCL network as an output filter for the DG converter is addressed as follows.

Fig. 14 shows the proposed system considering an LCL network as an output filter of the dc/dc converter. The resonance frequency (2 kHz) of the LCL filter is selected to be sufficiently lower than the switching frequency to obtain adequate attenuation of the third-order network, the values of the filter parameters are outlined in the Appendix. A simple active damping loop is used within the DG control structure to suppress the instabilities resulted from the LCL filter resonance and facilitate high bandwidth for the current controller. The damping loop injects a damping voltage to the most inner loop of the converter con-

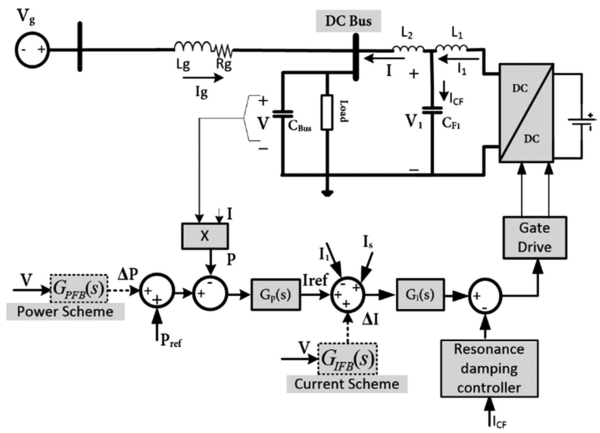


Fig. 14. DG converter with LCL output filter.

troller, and this voltage is proportional to the filter capacitor current. The employed resonance damping controller was proposed for ac systems; this method is extended and adopted for dc systems. Further details on the LCL filter design and resonance damping controller can be found in [30] and [31].

The impact of the LCL filter on the proposed system performance can be illustrated by comparing the system dominant eigenvalues with *LC* filter configuration, as shown in Fig. 15 for both islanding detection methods. It is clear that the low-frequency eigenvalues are almost identical regardless of the output filters configurations, for both islanding detection methods. However, with the resonance damping controller disabled and the stabilizing loop enabled, the effect of the LCL filter resonance can be seen in the two conjugate eigenvalues at a frequency very close to the LCL resonance frequency. The system damping factor is improved in a remarkable way when the resonance damping controller and the stabilizing loop operate simultaneously, by moving the high-frequency poles towards the left-hand side of the *s*-plane. It should be noted that the overall damping factor for the system equipped with the current

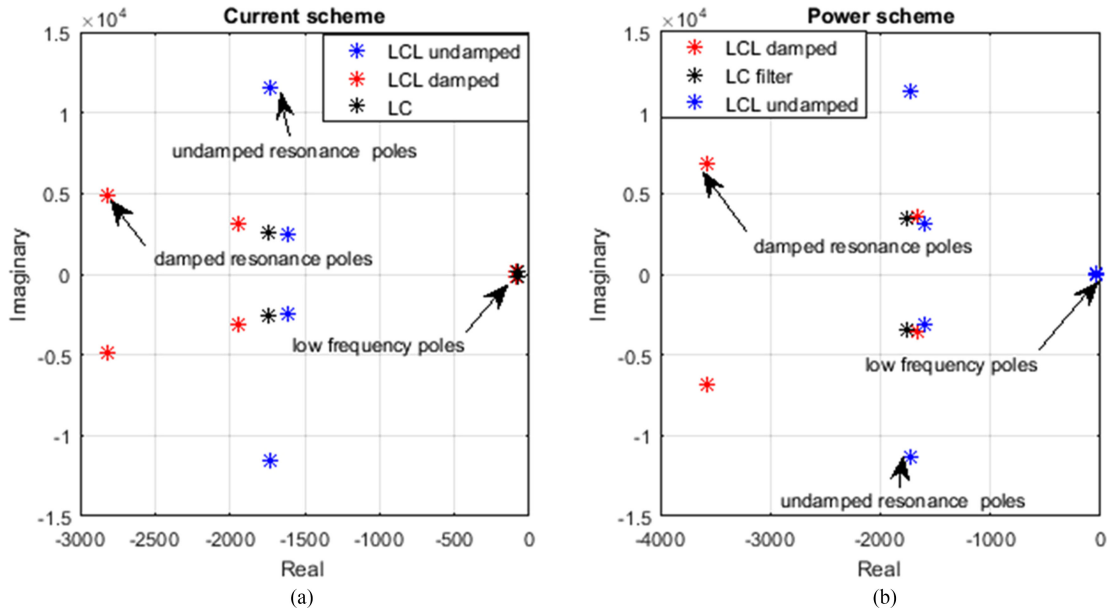


Fig. 15. Impact of LCL filter on the system eigenvalues. (a) Current scheme. (b) Power scheme.

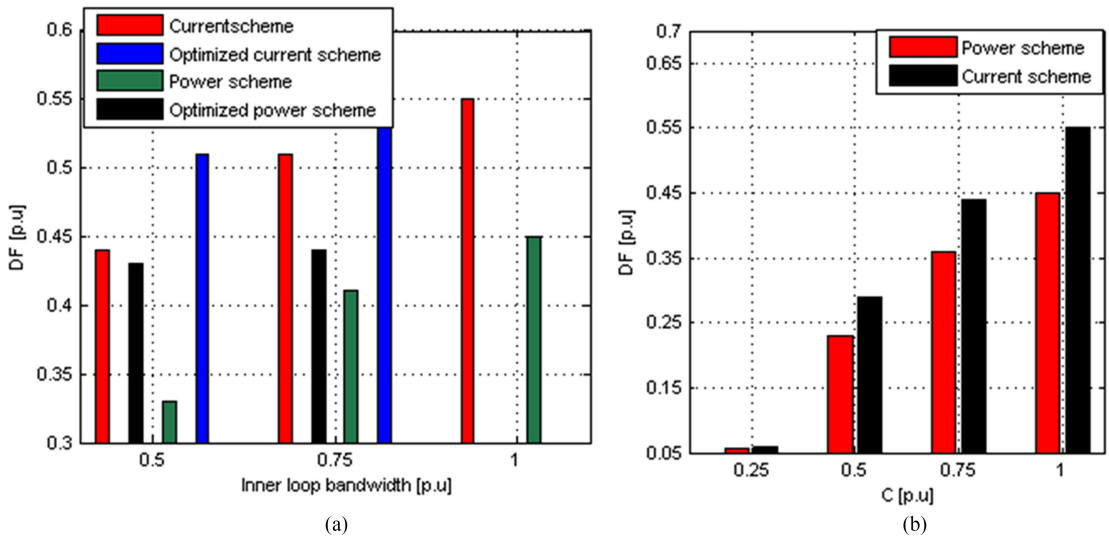


Fig. 16. Variation of system damping factor against (a) inner loop bandwidth and (b) bus capacitance.

scheme is reduced from 0.55 to 0.5 pu, when the LCL filter configuration is employed, with modifying the stabilizing gain K_d (from 60 to 50 pu). On the other hand, the stabilizing gain has to be modified (from 80 to 58 pu) for the power scheme to obtain the best damping factor, which is slightly reduced from 0.45 to 0.427 pu, with the LCL filter used.

2) Inner Loop Bandwidth and Bus Capacitance Uncertainties: The impact of varying the current controller bandwidth and the bus capacitance is shown in Fig. 16. It is clear that overall system damping decreases for both islanding detection schemes if the inner loop current controller is reduced to by 25% and 50%, with the same stabilizing loop design obtained in the previous sections, as shown in Fig. 16(a). The system damping is improved for both schemes if the stabilizing gain (K_d) is retuned for optimal operation. However, the highest damping factors are only obtained with 100% inner loop bandwidth. The variation of bus capacitance shows the remarkable impact on the overall system damping capability as depicted in Fig. 16(b), it is evident that the system damping decreases dramatically with the bus capacitance variation for both islanding detection schemes, and the system has very poor damping capability if the bus capacitance is reduced to 0.25 pu for both schemes. Similarly, the stabilizing gain can be adjusted to obtain the optimum system damping capability; however, the overall system damping will decrease with bus capacitance reduction. It should be noted that the current scheme shows higher damping factor than the power scheme for all bus capacitance values, which can be considered as an advantage for the current scheme.

E. Impact of AC Side Dynamics

The proposed dc distribution system is investigated considering a more detailed model for the ac grid. As shown in Fig. 1, by

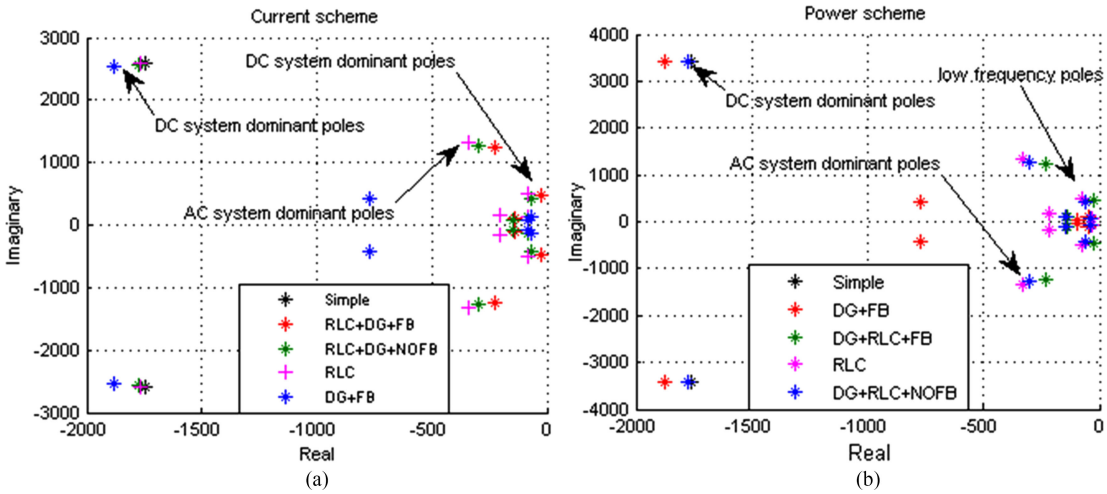


Fig. 17. Hybrid ac/dc system dominant eigenvalues with (a) current scheme and (b) power scheme.

closing $S_{\rm ac}$, the following components are added to the ac PCC and the small-signal model of the hybrid system is developed.

1) A DG unit supplying constant active and reactive power to the ac grid; this DG is equipped with the current scheme for islanding detection. The design of the outer and inner loop controller parameters can be found in [8] and [23].
2) An RLC load with overall 0.95 lagging power factor.

The dominant eigenvalues affecting the overall system for a dc system equipped with the current islanding detection scheme is shown in Fig. 17(a), where the simple ac grid configuration previously discussed is compared with the detailed system for different loading conditions and connections. The parameters of the new RLC load and the DG unit are outlined in the Appendix. It is clear that the dominant eigenvalues of the dc distribution system are slightly affected by the added components on the ac side, keeping the low and high-frequency poles almost at the same location regardless the ac system configuration. However, the ac side dynamics can be observed through their dominant eigenvalues, it is clear that the overall system stability can be highly affected if the DG unit on the ac side is equipped with positive feedback islanding detection scheme and the RLC load drawing its full power, where two conjugate eigenvalues are close to the $j\omega$ -axis. It can be noted that positive feedback scheme on the ac side has its negative impact only if the RLC load is connected, where the interaction between them increases. On the other hand, the system stability has been improved when the DG unit is only connected at the ac PCC; even with the positive feedback is enabled. Similarly, the impact of the detailed ac system on the overall system dynamics when the dc system is equipped with the power islanding detection scheme is illustrated in Fig. 17(b). The system dominant eigenvalues are plotted for different ac system configurations. It is clear that the lowest stability margin can be obtained when the RLC load and the DG unit is equipped with the islanding detection scheme, are both connected on the ac side, and that the overall system dynamics are improved when the RLC load is disconnected.

F. Multi-DG System

The system expandability to include multiple DGs with positive feedback schemes was investigated in Section III-C. It has been shown that the system is exhibiting absolute instability if the current scheme is employed, whereas it shows poor damping capability and instability at low power operation for the power scheme. Therefore, the stabilizing loop proposed for the single-DG system is adopted to stabilize the expanded system. Following the same approach in the single DG analysis, it is assumed that the first DG is already connected to the dc distribution feeder with its positive feedback and stabilizing loop settings, with their gain adjusted as previously explained; and a second DG will be added at different locations of the distribution feeder.

The optimum stabilizing gain for the second DG equipped with the current scheme is plotted against its location, at different operating points, and for two different locations of the first DG ($L_1 = 0.25$ km and 0.5 km). For $L_1 = 0.25$ km, it is evident that the optimum gain increases as the DG moves away from the first DG, keeping the same behavior as for the single DG case, as shown in Fig. 18(a). It is also apparent that the variation of the DGs output power has a small effect on the optimum value of the stabilizing gain. Further, it can be noted that the location of the first DG affects the optimum gain of the second DG slightly. Similarly, for the power scheme, the optimum stabilizing gain of the second DG unit increases with its location, when it moves away from the first DG, as shown in Fig. 18(b). It should be noted that the stabilizing gains are slightly affected by the DGs operating points and the first DG locations. This indicates that very little modifications are required in the stabilizing gain to cope with power variations. Similar to the current scheme, the overall system stability was improved in a significant way when the stabilizing loop was used.

The system stability has been remarkably improved when the stabilizing loop is used for both DGs if the current scheme is employed, as depicted in Fig. 19(a). It can be seen that the damping factor of the stabilized system is approximately 0.4 pu, if the second DG is located at 1.0 km away from the first DG, regardless of the location of the first DG. However, this damping ratio drops to approximately 0.25 pu, if the second DG is located close to the first unit ($L_2 = 0.25$ km), this is because the cutoff frequency (ω_2) is designed to mitigate the instabilities when the DGs are located far away from the PCC. This means that the damping capability for DGs located near the PCC can

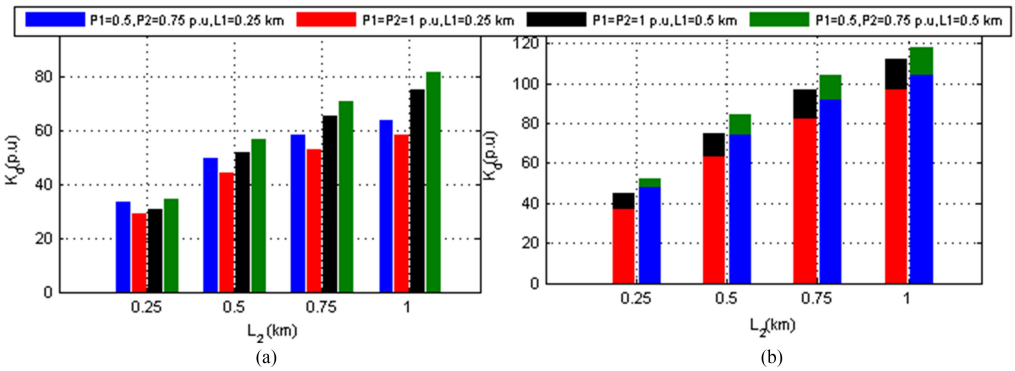


Fig. 18. Variation of the optimum stabilizing gain of the second DG against feeder length. (a) Current scheme. (b) Power scheme.

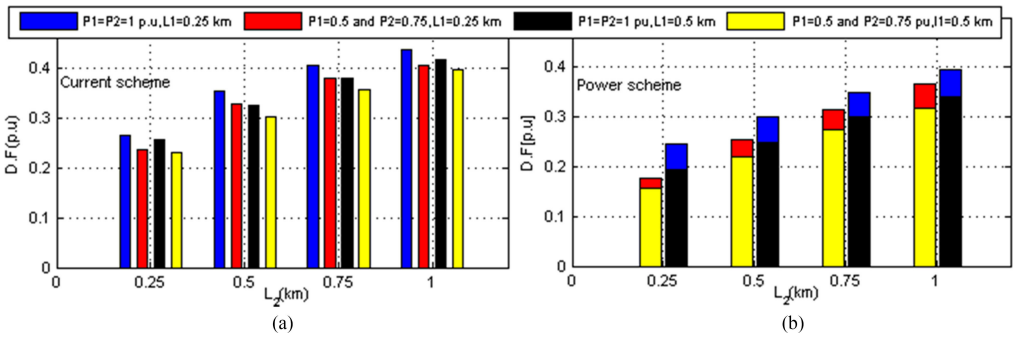


Fig. 19. Variation of the multi-DG system damping factor against feeder length. (a) Current scheme. (b) Power scheme.

be improved by modifying the value of (ω_2). It can be also noted that the system damping is slightly affected by the first DG location and the DG output power, maintaining the system damping factor at relatively high values. For the power scheme, Fig. 19(b) shows the damping factor of the dominant eigenvalues for different DGs operating points and locations. It can be seen that the lowest damping factor (0.15 pu) is obtained when the first DG is located at 0.5 km from the PCC and the second DG is located at 0.25 km away from the first unit; on the other hand the highest damping factor is obtained if the second DG is located at 1.0 km, regardless of the first DG locations.

V. Simulation Results

Time-domain simulation studies, using the detailed nonlinear models of the system components under the MATLAB/Simulink environment, are conducted to evaluate the performance of the typical dc distribution system shown in Fig. 3 in the grid-connected mode. Furthermore, the performance of the proposed stability enhancement method is assessed. Also, an islanding test is conducted to examine the system performance with the DG equipped with both the positive feedback schemes and the stabilizing loop. Finally, the two-DG system performance is examined at different operating conditions. The positive feedback gains are set to 1.2 pu for the current and the power schemes. The system parameters are given in the Appendix

A. System Performance Without Stabilization Loop

Fig. 20(a) and (b) shows the responses of the voltage and the injected power at the PCC of the DG equipped with the current scheme for islanding detection. The DG is located at 0.5 km apart from the PCC and feeding 0.75-pu CPL and 0.25-pu pure resistive load. The system shows unstable response when the CPL penetration level is increased to 1.0 pu at $t = 4$ s, although the positive feedback gain is set to only 1.0 pu. The resulted instability agrees with the analysis presented in Fig. 6, where the marginal gain preserving the system stability in the grid-connected mode is less than the minimum gain to detect islanding for 1.0 pu CPL penetration level. On the other hand, with 1.0 pu CPL, the power scheme succeeded to track the reference power variation applied at $t = 4$ s, where the reference power is reduced to 0.5 pu and retained back to 1 pu at $t = 7$ s. Fig. 20(c) and (d) shows the voltage and power responses at the PCC of the DG equipped with the power scheme. It can be noted that the voltage is dropped to 0.8 pu for a very short time in response to the reference power reduction; the waveform shows an overshoot of 0.1 pu when the power is retained to 1.0 pu. Similarly, the DG output power shows a 0.25 pu overshoot during the reference power variation event. The overshoots in the voltage and power waveforms are generated due to the power perturbation injected to the reference power loop by the positive feedback islanding detection loop.

B. System Performance With Stabilization Loop

The effect of the stabilizing loop on a DG equipped with the positive feedback detection schemes is shown in Fig. 21, where the reference power command is dropped to 0.5 pu at time $t = 4$ s and retained to 1.0 pu at $t = 6$ s. The DG is located at 1.0 km away from the VSC; the load is 1.0 pu CPL; the positive

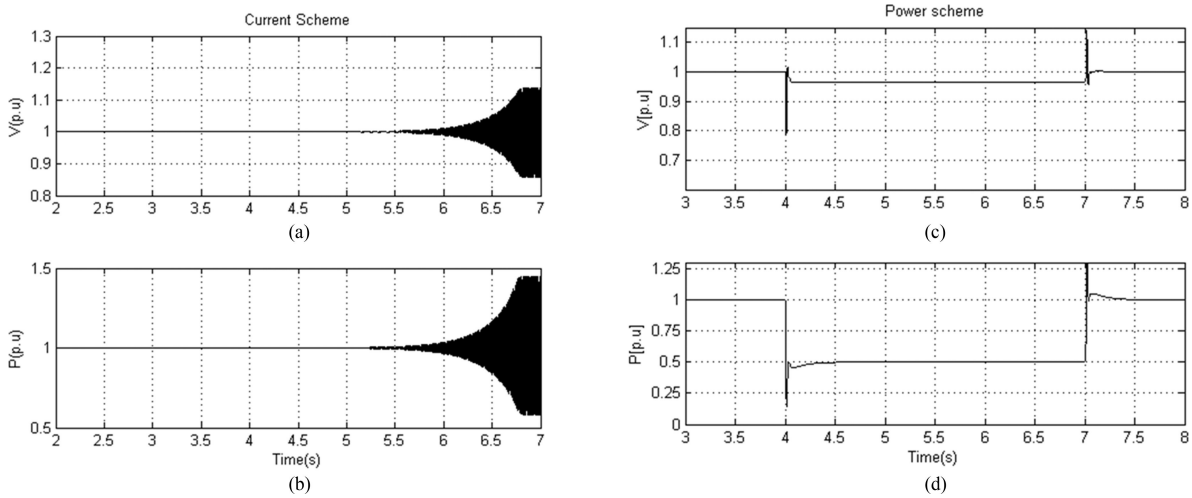


Fig. 20. System response without stabilizing loop for the current and power schemes, respectively. (a), (c) Voltage at the PCC. (b), (d) DG output power.

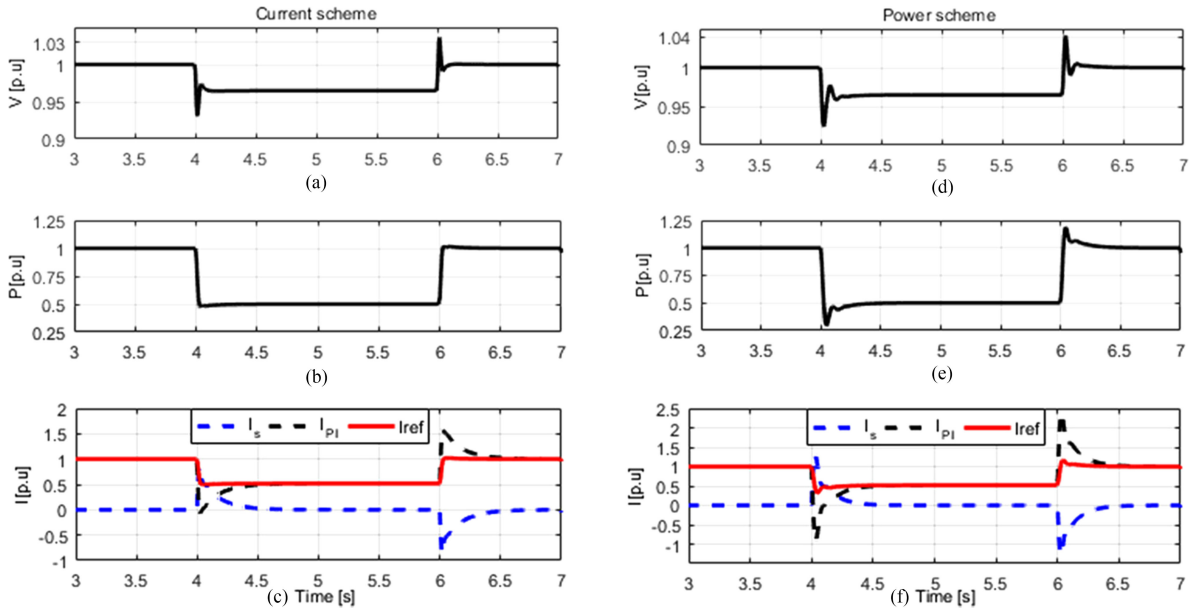


Fig. 21. System response with stabilizing loop applied to the current and power schemes, respectively. (a), (d) Voltage at the PCC. (b), (e) DG output power. (c), (f) Inner loop output currents.

feedback gain is 1.2 pu; the low-pass filter cutoff frequency is selected to be 5000 rad/s; and the stabilizing gain is set to its optimum value for each scheme. For the current scheme, the DG voltage and output power show a stable and well-damped performance as depicted in Fig. 21(a) and (b), respectively. The voltage waveform shows a minor overshoot of 0.03 pu when the reference power changes suddenly by 0.5 pu, whereas the output power waveform shows smooth tracking to the reference power with neglected overshoots. These results prove the effectiveness of the stabilizing loop to stabilize the system. The reference current ($I_{\rm ref}$), the output of the power loop compensator (I_{PI}), and the stabilizing current (I_s) are shown in Fig. 21(c). It is clear that stabilizing current loop injects its component (I_s) only during transient periods; this current is added to the output of the power loop compensator (I_{PI}) to generate the reference current ($I_{\rm ref}$), which is then applied to the current controller inner loop. It can be noted that the reference current ($I_{\rm ref}$) shows a damped response with neglected overshoots, proving the effectiveness of the stabilizing loop.

The impact of the stabilizing loop on the DG equipped with the power scheme for islanding detection can be demonstrated in Fig. 21(d)–(f), where the same variation scenario is applied to the DG reference power command. The DG voltage waveform shows remarkable improvement during the transient periods as compared to the case where the stabilizing loop is not applied. It can be noted that the maximum overshoot is reduced to only 0.04 pu compared to 0.1 pu without the stabilizer as depicted in Fig. 21(d). The output power, shown in Fig. 20(e), shows better response with the stabilizing loop, leading to a reduction in the overshoots compared to the uncompensated case. Similar to the current scheme, Fig. 21(f) shows the stabilizing loop current component that is injected during the transient periods

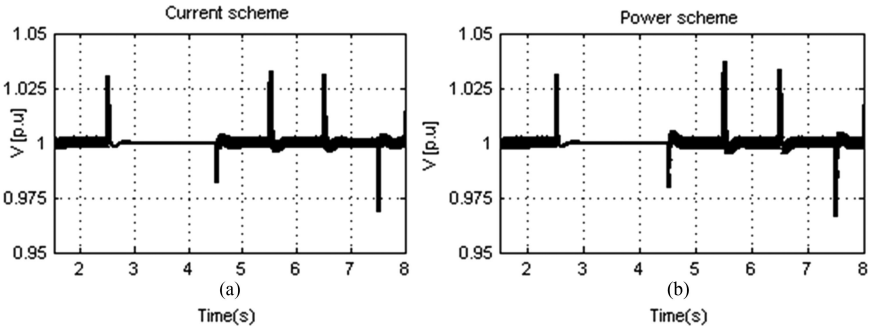


Fig. 22. DC system voltage response to AC system disturbances. (a) Current scheme. (b) Power scheme.

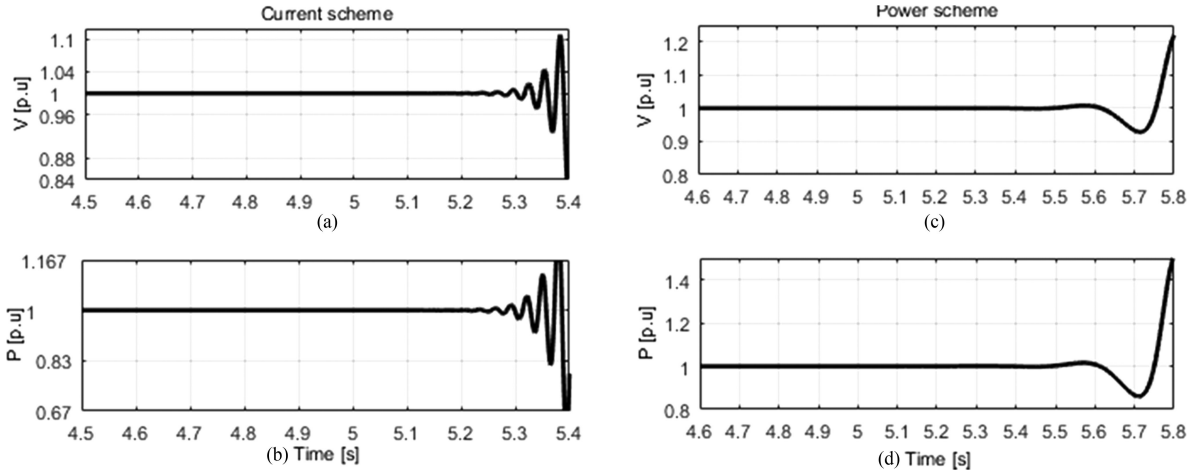


Fig. 23. System response for islanding detection with stabilizing loop of the current and power schemes, respectively. (a), (c) Voltage at the PCC. (b), (d) DG output power.

only; this current is added to the power loop compensator output to generate a damped reference current to improve the overall system stability and response.

C. AC System Dynamics

The system response of the dc distribution system due to the disturbances on the ac side resulting from connection and disconnection of different loads is investigated (the per-unit values used are calculated according to the dc system base power). Initially, the RLC load and the DG unit on the ac side are absorbing and delivering their rated power (outlined in Appendix). Fig. 22 shows the dc bus voltage response for the current and power schemes when a rectifier load is connected at the ac PCC. The rectifier load (0.5 pu) is switched OFF between time $t = 2.5$–4.5 s, resulting in 2.5% minor overshot at the bus voltage; at time $t = 5.5$ s, the RLC load is increased by 0.5 pu resulting in a similar magnitude overshoot in the bus voltage. The effect of the DG unit power variation is examined through increasing the reference power command by 0.5 pu ($t = 6.5$–7.5 s), resulting in minor overshot at the bus voltage. It should be noted also that the harmonics injected by the rectifier load to the ac grid have been superimposed to the VSC output voltage; however, these harmonic content did not affect the operation of the dc distribution system. The overshoots seen at the dc bus are a result of the variation of the voltage at the ac PCC, which is mirrored on the dc output voltage of the VSC, and hence the voltage of dc distribution system is affected. Generally speaking, the interactions between the ac and dc sides are obvious when the ac grid strength is not high (i.e., in weak ac grids); however, these interactions can be mitigated by modifying the VSC controller to increase the overall system robustness and disturbance rejection against system parameter variations.

D. Islanding Test

To facilitate islanding detection, the positive feedback methods cause a destabilizing effect in the DG upon the occurrence of an islanding event. On the other hand, the stabilizing loop is designed to mitigate this destabilizing effect in the grid-connected mode; therefore, it is important to examine the capability of the islanding detection schemes in the compensated system. An islanding event time occurs at $t = 5$ s whereas the DG unit and the load operate at their rated power so that perfect power matching is satisfied at this condition (worst loading case for the islanding detection). Following the IEEE standards for ac systems [3], the protection devices are set to operate from 0.88 to 1.1 pu. This means that the detection will be successful if the voltage is forced to be outside of this operating range to allow the protection devices to operate. The system responses of the current and power schemes are shown in Fig. 23. It can be seen that the voltage and the output power are driven to an un-

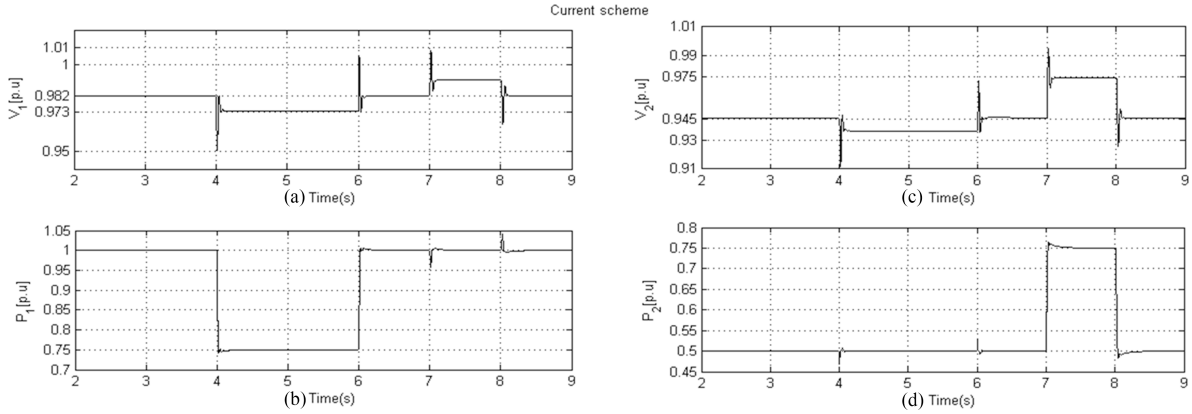


Fig. 24. System response of two DG operation equipped with the current scheme and the stabilizing loop. (a) Voltage at DG1. (b) Output power of DG1. (c) Voltage at DG2. (d) Output power of DG2.

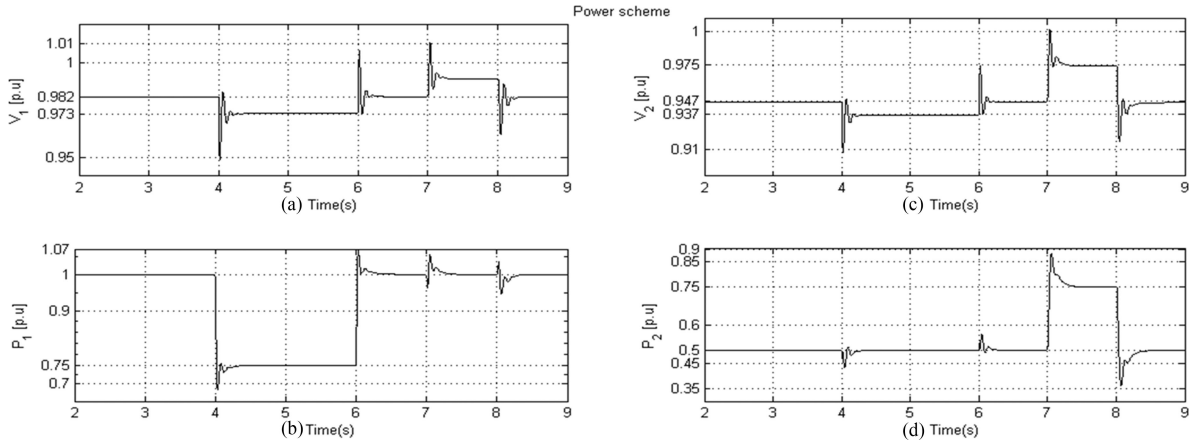


Fig. 25. System response of two DG operation equipped with the power scheme and the stabilizing loop. (a) Voltage at DG1, (b) Output power of DG1, (c) Voltage at DG2, and (d) Output power of DG2.

stable state in both schemes once islanding occurs. Apparently, the current scheme can detect the islanding condition in approximately 400 ms with an oscillatory response [see Fig. 23(a) and (b)]. The power scheme succeeded to detect the islanding event within 800 ms with a damped response [see Fig. 23(c) and (d)]. The short detection time can be considered as an advantage for the current scheme with respect to the detection speed, whereas the damped response is considered as an advantage for the power scheme with respect to the system response during islanding. It should be mentioned that the stabilizing loop is automatically deactivated once the islanding occurs, because the grid current (I_g) vanishes, and hence the stabilizing current is switched to the idle mode.

E. Multiple DG Operation

The performance of the two-DG system is evaluated when both DGs are equipped with the positive feedback islanding detection schemes and the proposed stabilizing loop. Both islanding detection schemes are evaluated for the following scenario: initially, the output power of the first DG is 1 pu, and it is 0.5 pu for the second DG. The reference power command for the first DG is dropped by 0.25 pu at time $t = 4$ s, then the DG is retained to its rated power at time $t = 6$ s. The reference command of the second DG is increased to 0.75 pu for one second, and then, it is returned to 0.5 pu. The positive feedback gains are set to 1.2 pu for both schemes, whereas the stabilizing gains are set to the optimum gains developed in Section IV. The first DG is located at 0.5 km from the VSC and the second DG is located 1.0 km away from the first one.

The system response of the current scheme is shown in Fig. 24. The voltage at Bus1 shows a minor overshoot of magnitude 0.03 pu when the power of DG1 is dropped to 0.75 pu, whereas the output power of DG1 tracks the reference power smoothly with a negligible overshoot, showing response close to that of a single DG operation. Similarly, for the second DG, the voltage shows less than 0.015 pu overshoot when its reference power is suddenly increased by 0.25 pu, whereas the output power maintains a highly damped response with negligible overshoots. The power variation of each DG unit can be considered as an external disturbance to the neighboring DG unit; both DGs succeed to reject the external disturbances caused by power variation with minor overshoots less than 0.05 pu. These results prove the capability of the stabilizer to reject external disturbances successfully.

The performance of the system if both DGs are equipped with the power scheme is shown in Fig. 25, where the same power variation scenario is applied to investigate the system dy-

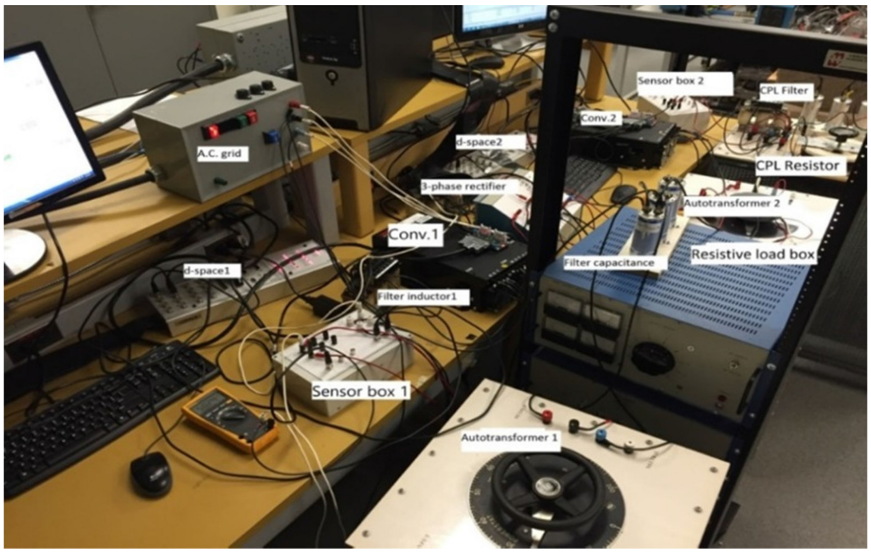


Fig. 26. Experimental setup view.

namics. Similar to the current scheme, the voltage response of DG1 shows a minor overshoot of 0.03 pu, whereas the voltage of DG2 shows an overshoot of 0.025 pu in the transient period accompanying its power variation. The output powers of both DGs succeeded to track their reference commands with approximately 0.07 pu overshoot for DG1, and approximately 0.1 pu overshoot for DG2. Similar to a single DG operation with the power scheme, these overshoots are considered as disadvantages for this scheme in the grid-connected mode. Finally, the stabilizer showed an excellent performance in rejecting the external disturbances caused by power variation of the neighboring DGs (with overshoots approximately 0.05 pu for both DGs).

VI. Experimental Results

To validate the presented analysis and proposed control design, a laboratory-scale dc distribution system, based on the system shown in Fig. 3, is used. A view of the system setup is shown in Fig. 26. A Semistack-IGBT H-bridge-based VSC is used to implement a dc/dc converter interfacing the DG unit to a variable resistive load box and a fixed dc source through an *LC* filter. The CPL is implemented by connecting a tightly regulated voltage-controlled dc/dc buck converter to the dc grid. The buck converter is supplying a pure resistive load. The line is represented by an *R-L* segment, which connects the dc grid source to the DG PCC. The parameters of the experimental setup are given in the Appendix. The dSPACE1104 control system is used to implement the proposed control scheme in real time. The pulse width modulation algorithm is implemented on the slave processor (TMS320F240-DSP) of the dSPACE controller. The dSpace1104 interfacing board is equipped with eight digital-to-analog channels and eight analog-to-digital channels to interface the measured signals to/from the control system. The software code is generated by the Real-Time Workshop under the MATLAB/Simulink environment. The sampling/switching frequency is 10 kHz. The current and voltage sensors used are HASS 50-S and LEM V 25-400, respectively.

The system without the proposed stabilization loop is first examined in two cases. The DG is supplying 0.75 pu constant power to the dc grid and the DG is supplying a composite load of 85% CPL penetration level. Fig. 27 shows the system response when the DG is equipped with the current and power islanding detection schemes. For the current scheme, it is obvious that the system is stable until the positive feedback loop is activated at time $t = 8$ s, then, the voltage, current, and power start to lose their stability by oscillating between upper and lower boundaries due to the controller protection limits (i.e., a limit cycle behavior), as depicted in Fig. 27(a)–(d). Similarly, the response of the system with the power scheme for islanding detection is shown in Fig. 27(e)–(h); the system loses its stability once the positive feedback loop is activated at time $t = 4$ s.

The effect of using the stabilizing loop is presented in Fig. 28 for a system equipped with the current and power islanding detection schemes. The stabilizing loop succeeded to preserve the system stability when the positive feedback loop is activated at time $t = 6$ s, as indicated in Fig. 28(a)–(d). Similarly, the stabilizing loop succeeded to mitigate the stability problem caused by the positive feedback loop and the CPL, maintaining the system stability when the power scheme loop is activated at time $t = 4$ s, as depicted in Fig. 28(e)–(h).

Finally, the islanding detection test was conducted to ensure the proper operation of the islanding detection schemes during the islanding events. The test is performed by setting the load and the DG power to 1.0 pu to achieve perfect power matching; further, the connected load is a pure resistance to consider the worst case scenario for islanding detection [3]. The current scheme results are shown in Fig. 29(a)–(c), where the system loses its stability when the islanding event occurs at $t = 11$ s. Similarly, the power scheme method succeeded to detect the islanding event occurring at $t = 10$ s, as depicted in Fig. 29(d)–(f). The islanding test proved that both islanding detection schemes are working properly when the grid is dis-

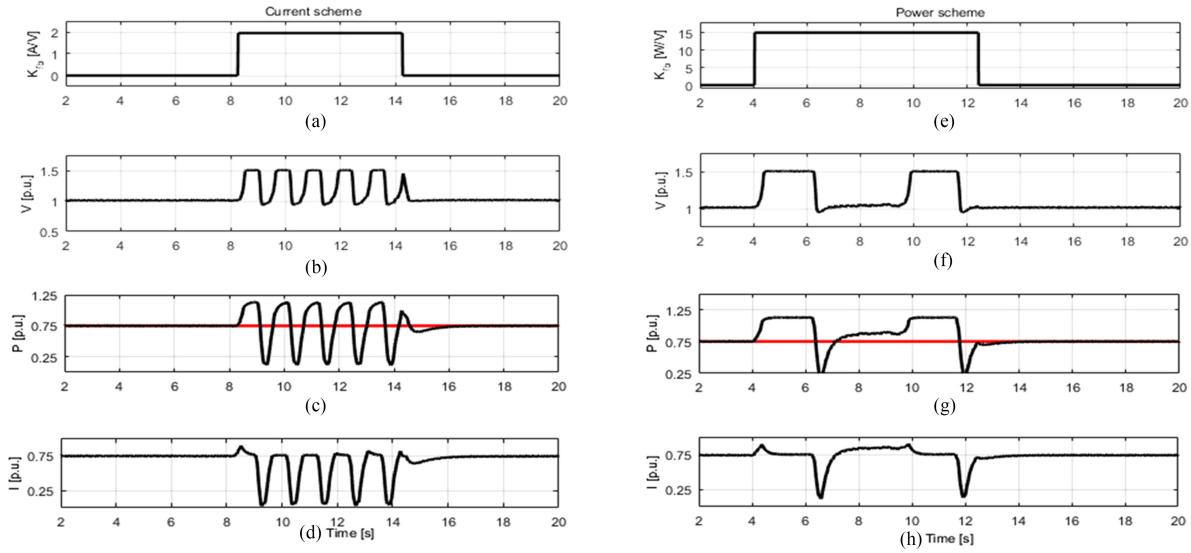


Fig. 27. Experimental results without stabilizing loop for DG equipped with current and power schemes, respectively. (a), (e) Feedback gain. (b), (f) Voltage. (c), (g) DG output power. (d), (h) DG current.

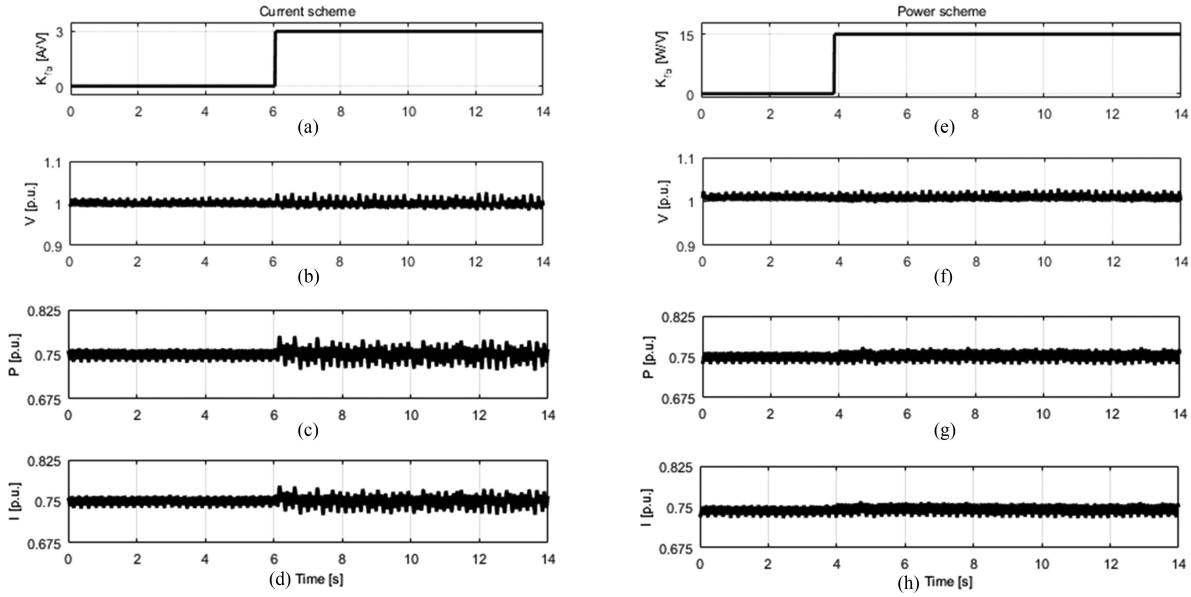


Fig. 28. Experimental results with stabilizing loop for DG equipped with current and power schemes, respectively. (a), (e) Feedback gain. (b), (f) Voltage. (c), (g) DG output power. (d), (h) DG current.

connected, whereas the stabilizing loop is effective only when the grid is connected. These results show that there is no conflict between both loops and validate the selection of the grid current to stabilize the system.

For further justification of the proposed stabilizing loop, the system is examined when the DG is delivering 50% of its rated power. Fig. 30 shows the system response for both schemes when a $\pm 4\%$ step change in the VSC reference voltage command and step load changes are applied at $t = t_o$, $t = t_1$, and $t = t_2$, respectively. It is clear that the bus voltage responds smoothly to the VSC output variation, keeping the system stability. Similarly, the voltage shows negligible variation when the load switches from very lightly loading condition to almost 150% full loading, indicating the robustness of the system under different loading conditions. Further, the performance of islanding detection is examined at different operating points. Fig. 31 shows the system response of both schemes when an islanding event occurs at $t = t_o$ for both islanding detection schemes at 65% power rating and with perfect power matching between the DG and the load. It is clear that the stabilizing loop current component (I_s) vanishes when the grid is disconnected, because it is proportional to the grid current as indicated in (38), and hence the islanding can be detected successfully during islanding operation.

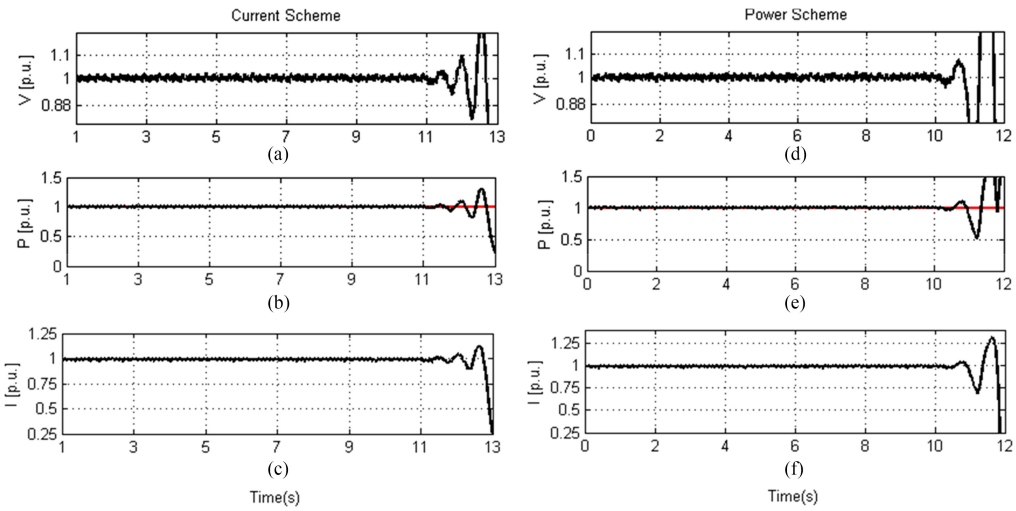


Fig. 29. Experimental results for islanding condition detection with the stabilizing loop applied, for DG equipped with current and power schemes, respectively. (a), (d) Voltage. (b), (e) DG output power. (c), (f) DG current.

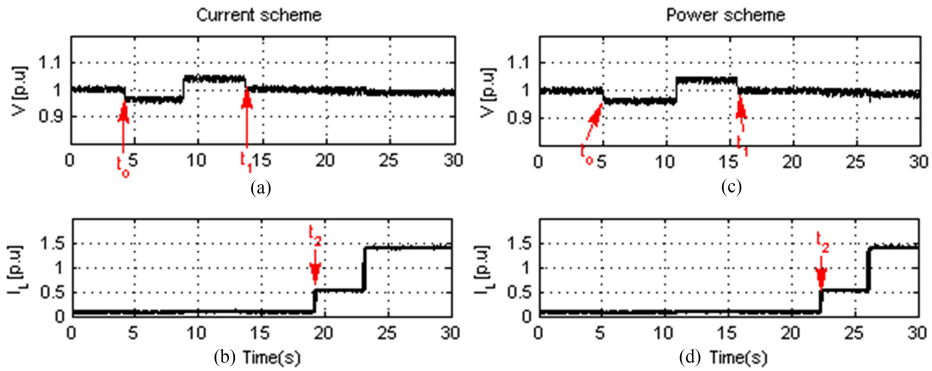


Fig. 30. Experimental results for dc grid voltage and load variations high switching at low power conditions, for DG equipped with current and power schemes, respectively. (a), (c) Voltage. (b), (d) Load current.

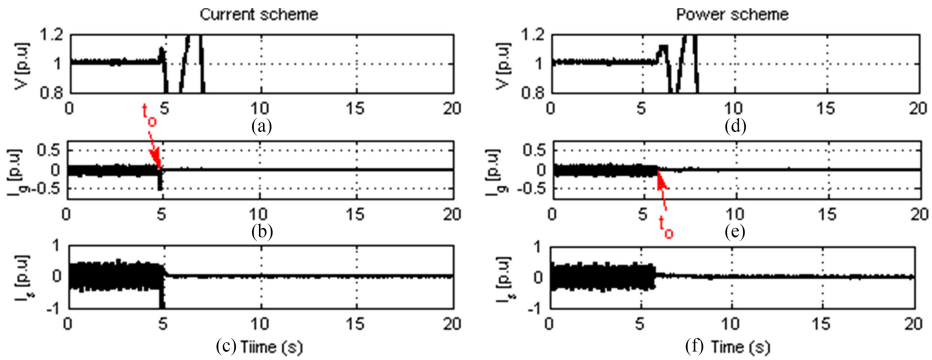


Fig. 31. Experimental results for islanding condition detection at 65% power matching, for DG equipped with current and power schemes, respectively. (a), (d) Voltage. (b), (e) dc grid current. (c), (f) stabilizing current.

VII. Conclusion

This paper investigated the dynamics of a grid-connected dc distribution system considering the practical characteristics of such emerging systems, such as the high penetration level of CPLs, the positive feedback islanding dynamics of DGs, and distribution feeder and dc source dynamics. A detailed small-signal model considering the characteristics above was developed. The augmented small-signal system dynamics was thoroughly investigated to determine the factors affecting the system stability with and without positive feedback detection schemes. Without the positive feedback schemes, it was found that

1) the penetration level of CPLs degrades the system stability, 2) the stability margin is significantly reduced as the feeder length increases, 3) the bus capacitance has a significant effect on preserving the system stability, and 4) the DG operating power has a small effect on the overall system stability.

With the positive feedback schemes, It was found that

1) the current positive feedback scheme affects the system stability significantly;
2) the CPL penetration level reduces the system stability margin in a remarkable way, and the negative effect of the CPL increases as the DG is located away from the dc PCC, leading to impossible application of the current scheme for many conditions;
3) the power scheme gives a better stability margin with longer feeder lengths and high CPL penetration levels;
4) both schemes exhibit instability problems and poor damping capabilities when applied to a multi-DG system.

The instability problem was mitigated by a proposed stabilizing loop applied to the current controller inner loop of the DG to improve the damping capabilities in a single-DG system, and to stabilize the multi-DG system as well. The theoretical results were verified using detailed nonlinear simulations and experimental results using a laboratory-scale setup.

APPENDIX

A. Simulation System Parameters

DC distribution system: System Rating: 500 V, 300 kW, $R_g = 0.0283\ \Omega$/km, $L_g = 0.249$ mH/km, Power control loop bandwidth: 300 rad/s, $C = 10$ mF, Converter switching frequency:10 kHz, $\omega = 2\pi$ rad/s, $\omega_3 = 2\pi$ rad/s, $L_1 = 0.5$ mH, $C_{F1} = 20\,\mu$F, $L_2 = 350\ \mu$H.

AC grid and VSC: System Rating: 5 MVA, 208 V, 60 Hz, $G_{\rm dc}(s) = 0.875 + \frac{50}{s}$, $G_{\rm ac}(s) = \frac{33366}{s}$, $G_{\rm PLL}(s) = 1.2 + \frac{1.2}{s}$, DG unit rating:1.5 MVA/208 V, Rectifier load rating: 150 kW, RLC load rating: 2 MVA, 0.95 lagging PF.

B. Experimental Setup Parameters

System rating: 50 V, $R_L = 12.5\ \Omega$, CPL parameters: 35 V, 9.6 Ω, dc/dc converter built-in capacitance = 2040 μF, $G_p(s) = 0.1 + 0.2$/s, filter capacitance = 20 μF, filter inductance = 0.5 mH, Converter switching frequency = 10 kHz, $R_g = 0.048\ \Omega$, $L_g = 3.6$ mH, $K_d = 25$ p.u.

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