An Isolated High-Frequency Link Microinverter Operated with Secondary-Side Modulation for Efficiency Improvement

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***Abstract*—This paper discusses the operation of a single-stage, isolated, high-frequency ac-link-based single-phase dc–ac converter, suitable for photovoltaic microinverter applications, controlled using phase modulation of the secondary-side cycloconverter devices. A detailed analysis is presented explaining the impact of prominent circuit nonidealities such as device capacitance and transformer leakage inductance on circuit behavior. The proposed extended-dead-time based modulation scheme helps in achieving zero-voltage-switching of the primary devices over the entire line cycle of the ac output and also offers the benefit of reduced transformer rms current due to absence of circulating current in the zero state. A flyback-based regenerative clamp circuit is used for mitigating voltage spikes on the secondary devices arising due to leakage inductance induced oscillations. A generic commutation strategy is also discussed, which makes operation with nonunity power factor loads also possible. Experimental results on a 260-W laboratory prototype under different load conditions are presented to illustrate the discussed principles and highlight the performance improvements.**

***Index Terms*—Cycloconverter, dc–ac power converters, microinverter, snubbers, zero current switching (ZCS), zero voltage switching (ZVS).**

I. Introduction

In recent years, microinverters have emerged as an increasingly popular choice for low-power commercial and residential photovoltaic (PV) installations because of their benefits of module level maximum power extraction, plug-and-play flexibility, increased reliability, and reduced safety hazard. An overview of such module-integrated single-phase PV inverter solutions can be found in [2]–[6].

Popular single-stage high-frequency-isolated microinverter topologies are broadly of two types: flyback based or high-frequency-link based. Though flyback-based solutions [7]– [12] offer benefits of low device count and reduced cost, they also pose certain challenges. Operation in the continuous conduction mode [9] may lead to output distortion on account of presence of right-half zero in the control-to-output transfer function [10], while discontinuous conduction mode leads to high rms currents and also turn-off losses [10]. Boundary conduction mode can be employed to address these issues at the cost of variable switching frequency operation. An added practical consideration with some modified forms of the flyback topology is the extremely low duty-ratio operation of some of the MOSFETS [11], [12], which makes high switching frequency operation challenging, owing to the requirement of an accurate high-speed gate drive.

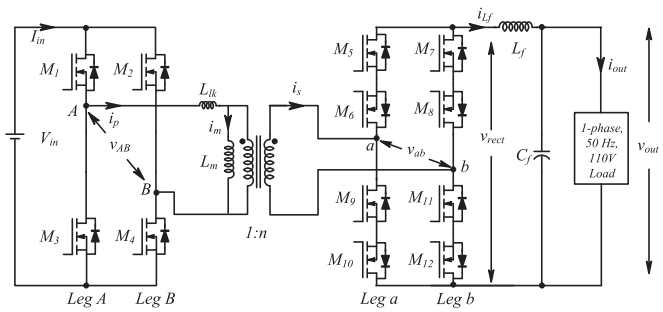

Fig. 1. Single-stage high-frequency link-isolated microinverter topology.

High-frequency ac-link-based architectures represent another category of isolated topologies with single-stage power conversion and these may be further divided into two subcategories. Topologies such as those reported in [13]and [14] are based on the series resonant dc–ac dual active bridge (DAB) converter, wherein a high-frequency resonant inverter is used to synthesize a high-frequency current waveform with its amplitude modulated at line frequency. A half-bridge or full-bridge cycloconverter is then used to down-convert this current to obtain the desired line frequency output. Though such an approach can ensure zero-voltage-switching (ZVS) operation of switches by keeping the switching frequency above the resonant frequency, it suffers from the well-known problem of high reactive power flow inherent in any DAB-based architecture [15]. The other subcategory, which can be conceptually thought to be derived from the popular phase-modulated dc–dc converter [16] is the focus of this paper. This topology, depicted in Fig. 1, consists of a high-frequency inverter, a high-frequency transformer,

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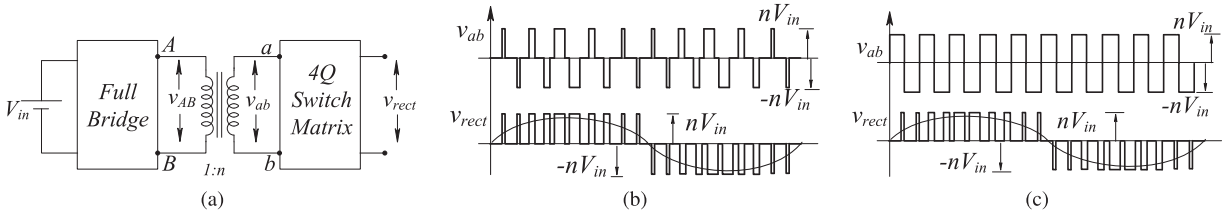

Fig. 2. Illustrating the basic idea behind the two types of modulation strategies. (a) Block diagram of the circuit. (b) PSM (c) SSM. SSM is the focus of this paper.

and a cycloconverter followed by an inductive output filter. The basic principle of operation of the converter is to render a line-frequency sinusoidal profile to the output inductor current (i_L) by controlling the low-frequency average of the output voltage ($v_{\rm rect}$). Fundamentally, this can be achieved in two ways, as Fig. 2 illustrates. One method is to use the primary-side full-bridge to synthesize a high-frequency quasi-square wave voltage with sinusoidally modulated zero-dwell duration and use the secondary-side switch matrix to synthesize the desired low-frequency sinusoidal profile of $v_{\rm rect}$. This strategy, referred to as primary-side modulation (PSM) in this paper has been widely reported in the literature in different forms [17]–[21].

Another strategy, referred to as secondary-side modulation (SSM) in this paper, consists of generating a square wave voltage on the primary side and using the secondary switch network to synthesize the same low-frequency profile of $v_{\rm rect}$ by introducing a zero state of sinusoidally varying duration. This modulation scheme, which has been previously reported for dc–dc [22] and dc–ac [23]–[25] Buck applications, offers advantages of absence of circulating current on the primary side and extended ZVS operation of the primary devices compared to the PSM. The aim of this paper is to explore in detail the working of the SSM scheme when applied to the high-frequency-link inverter of Fig. 1, used for dc–ac boost applications such as PV microinverter. Specifically, the impact of circuit nonidealities such as transformer leakage inductance and device output capacitance, which become pronounced due to the high-transformer turns-ratio necessary for voltage boosting, is analyzed in depth.

The paper is organized into the following sections. In Section II, different ways in which SSM can be implemented are compared and switching logic generation of the adopted method is explained. A comprehensive analysis of circuit operation for resistive load, considering the effects of circuit parasitics is presented in Section III. Necessary modifications to the commutation strategy are also discussed in Section III, which caters to operation with nonunity power factor loads in general. Finally, in Section IV, experimental results on a 260-W laboratory prototype under different load conditions and in grid connected mode are presented to validate the performance of the converter.

II. Secondary-Side Modulation

A. Choice of the Switching Sequence

As explained earlier, the basic idea behind SSM is to create a high-frequency square wave on the primary side and use the secondary switch network to synthesize the voltage $v_{\rm rect}$, such that its switching period average follows a low-frequency sinusoidal profile. As Fig. 3 illustrates, this can be done in five different ways, which differ from one another in the sequence in which powering ("1") and free-wheeling ("0") states appear. The relative merits and demerits of these different implementation strategies are detailed in Table I, from which it is clear that only in the "0101" scheme, commutation of all four primary devices occur following a powering state, helping them achieve possible ZVS turn-on. Moreover the "0101" scheme has other advantages such as reduced filter requirement and higher output voltage compared to some other implementation strategies. Hence among all possible options, the "0101" switching sequence is chosen for implementation of the SSM strategy.

B. Generation of Switching Signals

Fig. 4(a) shows the simplified schematic of circuit with the secondary-side switches replaced by four-quadrant (4Q) equivalents and the output inductor modeled as a current sink (i_{L_f}). Switch-pair M_5, M_6 is depicted by $4Q_1$, switch-pair M_9, M_{10} is depicted by $4Q_2$ and so on. Assuming all the 4Q switches are driven by 50% duty-ratio pulses, it is evident that the top and bottom pair of 4Q switches should have complementary switching functions (with a small overlap) in order to prevent open circuiting of i_{L_f}. The output voltage $v_{\rm rect}$ can be expressed in terms of the switching functions as

$$v_{\rm rect} = v_{\rm ab}(4Q_1 - 4Q_2). \tag{1}$$

The desired profiles of $v_{\rm rect}$ for positive and negative portions of the output ac line cycle are shown in Fig. 4(b) and (c), respectively. The switching period average of $v_{\rm rect}$ is given by

$$< v_{\rm rect} >= \pm nV_{\rm in}m(t) \tag{2}$$

where $m(t)T_s/2$ denotes the duration of the nonzero state of $v_{\rm rect}$ and the plus and minus signs correspond to the positive and negative ac line cycle, respectively. Thus, in order that this switching period average of $v_{\rm rect}$ follows the desired sinusoidal profile of $V_m \sin\omega t$, it is evident that $m(t)$ should be varied over a line cycle as

$$m(t) = (V_m/nV_{\rm in})\,|\sin\omega t|. \tag{3}$$

The desired high-frequency profile of $v_{\rm rect}$ can be synthesized by varying the phase overlap $m(t)T_s/2$ between the switching functions $4Q_1$ and $4Q_2$. For the positive output half-cycle, $4Q_1$ is synchronized with the switching function of M_1, while the

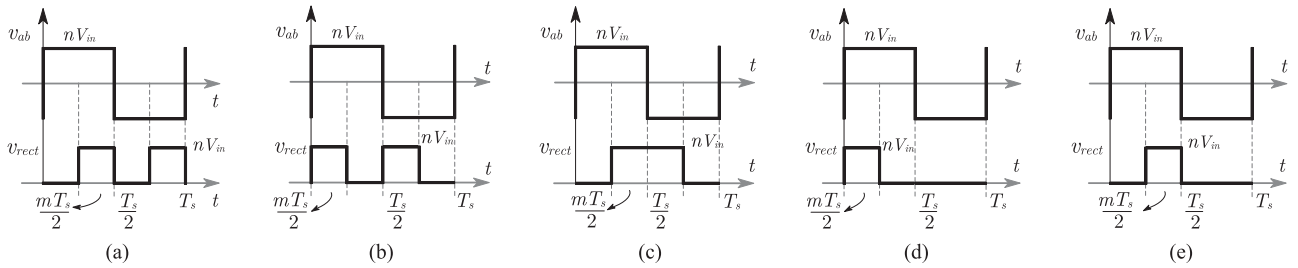

Fig. 3. Illustrating the different ways in which SSM can be implemented. Each strategy is denominated by the respective sequence of powering/high ("1") and free-wheeling/zero ("0") states. (a) 0101 (b) 1010 (c) 0110 (d) 1000, and (e) 0100. Switching strategy "0101" is selected for implementation on account of its advantages.

TABLE I
COMPARISON OF THE DIFFERENT IMPLEMENTATION METHODS OF SSM

0101	1010	0110/1001	1000	0100
Load current is present on primary side at commutation instant of all four primary devices, which helps them in achieving ZVS turn-on.	Primary-side current is zero at commutation instant of all four primary devices, hence they undergo ZCS turn-off.	One leg undergoes ZVS turn-on, while other has ZCS turn-off. Compared to the first two strategies, output filter size is more as effective frequency is half.	Voltage conversion ratio is half compared to the first three strategies. Filter size requirement is more compared to the first two strategies. Primary devices undergo ZCS turn-off.	Voltage conversion ratio is half compared to the first three strategies. Filter size requirement is more compared to the first two strategies. ZCS at one transition, ZVS at another.

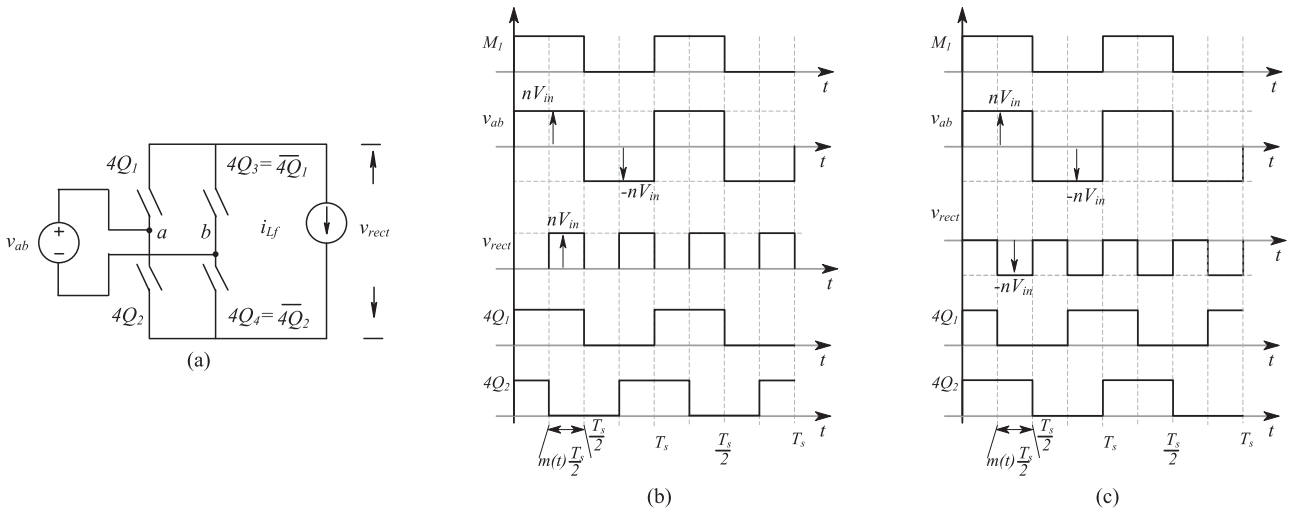

Fig. 4. Explaining generation of switching signals for the adopted SSM switching sequence (0101). (a) Simplified circuit schematic showing the 4Q switches on the secondary. (b) Switching signals for positive output half-cycle. (c) Switching signals for negative output half-cycle. The phase overlap between $4Q_1$ and $4Q_2$ is varied sinusoidally.

phase lead of $4Q_2$ with respect to $4Q_1$ is varied sinusoidally. The reverse is true for the negative output half-cycle.

III. CIRCUIT OPERATION

A. Detailed Operation Considering Nonidealities

In this section, detailed analysis of circuit operation in one high-frequency switching cycle is presented, considering the effect of both transformer leakage inductance and MOSFET output capacitance. For ease of analysis, the output filter inductor L_f is assumed to be large enough so that the switching ripple in $i_{\rm Lf}$ can be ignored and it can be treated as a constant current sink over a given switching period. Also, it should be noted that the following discussion is applicable for resistive loads only, i.e., when instantaneous power flow is always from the dc side to the ac side ($i_{\rm Lf} > 0$ for $v_{\rm rect} \geq 0$). A generic commutation strategy considering nonunity power factor loads is described in a later section. Circuit operation proceeds through several modes (see Fig. 8) as described below.

1) Mode I ($t_0 - t_1$): This mode corresponds to the first zero state of a high-frequency switching cycle. On the primary side, one diagonal pair (M_1 and M_4) is on, while on the secondary side, all four devices (M_5, M_6, M_9, M_{10}) of one leg are on with the other four turned off. Thus, $v_{\rm rect}$ is zero and $i_{\rm Lf}$ freewheels

through the shorted leg. The reflected voltage ($nV_{\rm in}$) from the primary side is blocked by the outer devices (M_7, M_{12}) of the nonconducting secondary-side leg, with the body diodes of the inner devices (M_8, M_{11}) being forward-biased. Just before the end of this mode, gate signal of M_9 is withdrawn, when current through it shifts to its body diode.

2) Mode IIa ($t_1 - t_2$): This mode represents the first of two transition modes from the zero state to the positive powering state and begins when gate signals of M_{11} and M_{12} are applied. Since the output capacitor of M_{11} was previously completely discharged, it turns on with ZVS. Also, as the reflected leakage inductance ($n^2 L_{\rm lk}$) on the transformer secondary is substantial, the current i_s does not change instantaneously and remains zero. When the gate voltage of M_{12} rises above the threshold value, its output capacitor starts discharging quickly into its own channel, at a rate limited by its small on-resistance. Since the output capacitor of M_{12} appears in parallel with the series combination of the output capacitors of M_7 and M_8 (since $v_{\rm rect}$ is zero), they too must discharge and charge, respectively, meaning that current in the shorted leg (leg "a") has a transient dip. However, since M_7 was initially blocking voltage and M_8 was discharged, output capacitance of M_7 is much smaller than that of M_8, due to the nonlinear dependance of MOSFET capacitance on voltage [28]. Thus, the rate of voltage rise across M_8 is many times smaller compared to the rate of voltage fall across M_7. The mode ends when capacitors of M_7 and M_{12} have fully discharged into the channel of M_{12} and current through leg "a" is restored to $i_{\rm Lf}$.

3) Mode IIb ($t_2 - t_3$): Transition from the zero state to the positive powering state continues in this mode, in which current slowly shifts from the body diode of M_9 to the channel of M_{12}. Since the transformer secondary-side reflected leakage inductance appears in series with M_{12}, the secondary current rises from zero and is given by

$$i_s(t) = \frac{nV_{\rm in}}{n^2 L_{\rm lk}} \cdot t. \tag{4}$$

The mode ends when i_s reaches $i_{\rm Lf}$ and current through M_{10} and body diode of M_9 has fallen to zero. For a given load current $i_{\rm Lf} = {I_m}' \sin \omega t$, this duration is given by

$$\Delta t_{2b} = \frac{n^2 L_{\rm lk} |{I_m}' \sin \omega t|}{nV_{\rm in}}. \tag{5}$$

Since $v_{\rm rect} = 0$ during this mode, it is evident that it corresponds to the familiar duty-cycle loss period of phase-modulated dc–dc pulse width modulation converters [16]. The switching-period average of the rectified voltage is given by

$$\langle v_{\rm rect} \rangle = \frac{1}{T_s/2} \left[nV_{\rm in} (mT_s/2 - \Delta t_{2b}) \right]. \tag{6}$$

Ignoring the drop in the filter inductor L_f and using (3), (5), and (6), the output voltage can be expressed as

$$v_{\rm out} = \left[V_m - (2f_s) n^2 L_{\rm lk} {I_m}' \right] \sin \omega t = {V_m}' \sin \omega t. \tag{7}$$

It is thus evident that the finite duration current commutation due to leakage inductance leads to a reduction in the filtered output voltage, corresponding to the impedance drop across

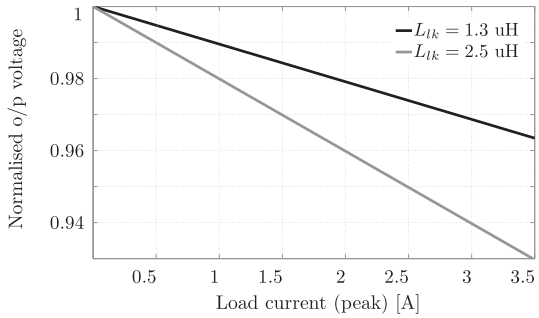

Fig. 5. Plot illustrating reduction of output ac voltage (normalized to the ideal value) due to the effect of duty-cycle loss. The parameter values are $V_m = 110\sqrt{2}$ V, $f_s = 25$ KHz, $n = 5$.

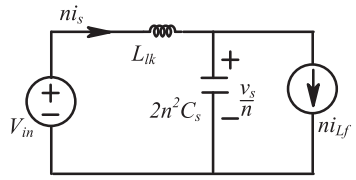

Fig. 6. Simplified equivalent circuit during mode III.

$L_{\rm lk}$. A plot of the variation of output voltage with load current, considering duty-cycle loss, for two values of $L_{\rm lk}$ is depicted in Fig. 5. Corresponding to the value of 1.3 μH for the experimental prototype (cf. Table III), the maximum voltage drop is observed to be close to 4%.

4) Mode III ($t_3 - t_4$): At $t = t_3$, the positive powering state begins as the current through the body diode of M_9 tries to reverse direction thereby beginning to charge its output capacitance. Since M_9 and M_7 are in parallel (as M_5, M_6, M_{10}, M_{11}, and M_{12} were already conducting previously and voltage across M_8 is zero), the simplified equivalent circuit during this mode is given by Fig. 6, which can be solved with the initial conditions of $i_s(t_3) = i_{\rm Lf}$, $v_s(t_3) = 0$ to obtain the relevant equations as

$$v_s = v_{\rm ds9}(t) = v_{\rm ds7}(t) = \ nV_{\rm in}(1 - \cos \omega_1 t) \tag{8}$$

$$i_s(t) = \ i_{\rm Lf} + (nV_{\rm in}/Z_1) \sin \omega_1 t \tag{9}$$

where $\omega_1 = 1/(\sqrt{2n^2 L_{\rm lk} C_s})$, $Z_1 = \sqrt{n^2 L_{\rm lk}/2C_s}$. The voltage spike appearing across the secondary devices due to this resonant ringing, if not arrested, may lead to device failure. In the present converter, this is addressed by employing a regenerative flyback snubber placed across the transformer's secondary terminals, as shown in Fig. 7. The snubber module consists of two identical flyback converters used to separately clamp the positive and negative spikes of the transformer secondary voltage. Details regarding analysis and design of the clamp circuit can be found in [1]. In a practical circuit, due to presence of stray loss elements, the oscillations quickly die out after some time when the voltages across M_9, M_7 (hence $v_{\rm rect}$ also) become steady at $nV_{\rm in}$, while the transformer secondary current settles to i_{L_f}.

5) Mode IV ($t_4 - t_5$): This mode is essentially continuation of the positive powering state and starts after oscillations from the previous mode have damped out. The mode proceeds with M_5, M_6, M_{11}, and M_{12} conducting on the secondary side, while

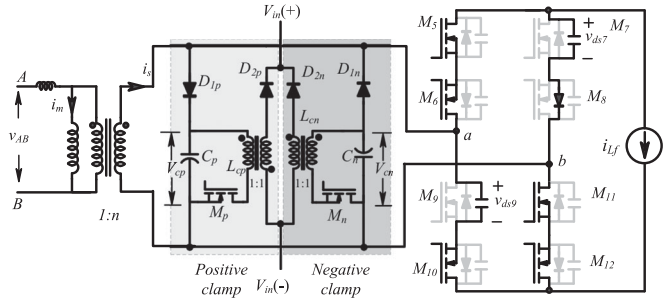

Fig. 7. Schematic of the regenerative flyback snubber circuit used to clamp voltage spikes across the secondary devices in mode III.

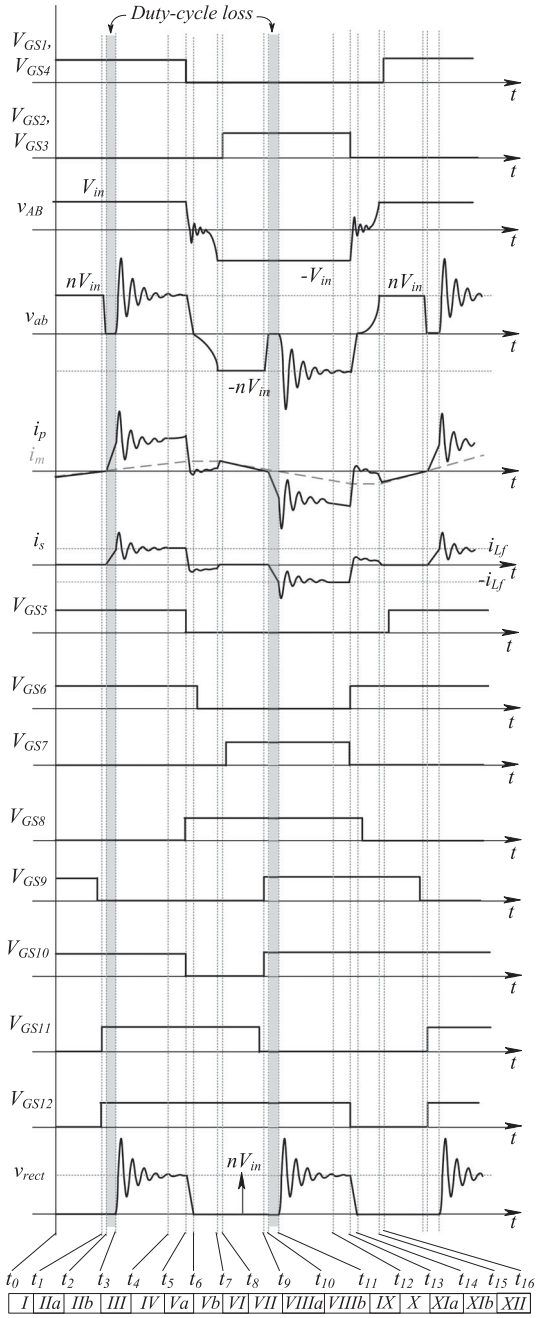

Fig. 8. Detailed waveforms explaining circuit operation during a high-frequency switching cycle (for positive half of the output ac voltage).

on the primary side, M_1 and M_4 continue to conduct, as before. At the end of this mode, gate signal of M_8 is applied while gate signals of M_1, M_4 on the primary side and M_5, M_{10} on the secondary side are withdrawn simultaneously.

6) Mode Va ($t_5 - t_6$): This mode corresponds to start of transition from the positive powering state to the second zero state. Circuit operation during this mode proceeds through four possible submodes, whose equivalent circuits are represented in Fig. 9. Conditions for transitions between these submodes are explained through the state diagram of Fig. 11. Circuit operation starts in mode Va1 with the application of gate pulse of M_8, which results in its ZVS turn-on, since its output capacitor was already discharged. On the primary side, removal of gate pulses of M_1, M_4 causes voltage across these devices to rise gradually while on the secondary side, capacitors of M_9 and M_7 start discharging. Similar to mode IIa, the discharging current of M_9 causes minimal rise in the voltage across M_{10}, since capacitance of M_{10} (which was initially at zero voltage) is much higher compared to that of M_9. Also, till $v_{\rm ab} > 0$, the body diode of M_5 remains forward-biased. Thus, the equivalent circuit during this mode is represented by the multiresonant circuit of Fig. 9(a). From the initial conditions $i_p(t_5) = i_m + ni_{\rm Lf}$, $v_p(t_5) = 0$, and $v_s(t_5) = nV_{\rm in}$ and using the general equations of the multiresonant circuit [29], the relevant equations describing this mode can be obtained as

$$v_p(t) = \left(\frac{i_T.n^2 C_s}{2\omega_2 C_p C_T}\right)\sin\omega_2 t + \left(\frac{i_T}{2C_T}\right)t \qquad (10)$$

$$v_s(t)/n = V_{\rm in} + \left(\frac{i_T}{2\omega_2 C_T}\right)\sin\omega_2 t - \left(\frac{i_T}{2C_T}\right)t \qquad (11)$$

$$i_p(t) = i_T\cos\omega_2 t + \frac{i_T C_p}{C_T}\left(1-\cos\omega_2 t\right) \qquad (12)$$

where $i_T = (i_m + ni_{\rm Lf})$, $C_T = (C_p + n^2 C_s)$, $C_{\rm eq} = (2C_p n^2 C_s)/C_T$, $\omega_2 = 1/(\sqrt{L_{\rm lk} C_{\rm eq}})$.

For higher values of load current, the initial stored energy in $L_{\rm lk}$ may be adequate to completely discharge the capacitors of the incoming primary devices and forward-bias their body diodes. $v_{\rm AB}$ is now clamped to $-V_{\rm in}$ and circuit operation proceeds according to the single-resonant equivalent circuit of Fig. 9(b). Operation in mode Va2 continues provided i_p remains positive.

If i_p reaches zero and tries to become negative, the diodes of the incoming devices once again become reverse-biased and the circuit reverts to the multiresonant circuit of Fig. 9(a). This mode with the same equivalent circuit as mode Va1 but with a negative value of i_p is designated as mode Va3. If the value of i_p is sufficiently negative, the capacitors of the outgoing devices are fully discharged and $v_{\rm AB}$ is clamped to $V_{\rm in}$. The circuit now operates in mode Va4, with the equivalent circuit shown in Fig. 9(c).

If the load current is low, circuit operation proceeds along the inner loop of the state diagram. During operation in mode Va1, i_p falls to zero before $v_{\rm AB}$ falls to $-V_{\rm in}$ and the circuit enters mode Va3. Since i_p is negative, $v_{\rm AB}$ starts increasing again. But if i_p is not sufficiently negative, i_p reaches zero before $v_{\rm AB}$ rises to $V_{\rm in}$ and the circuit enters mode Va1 again.

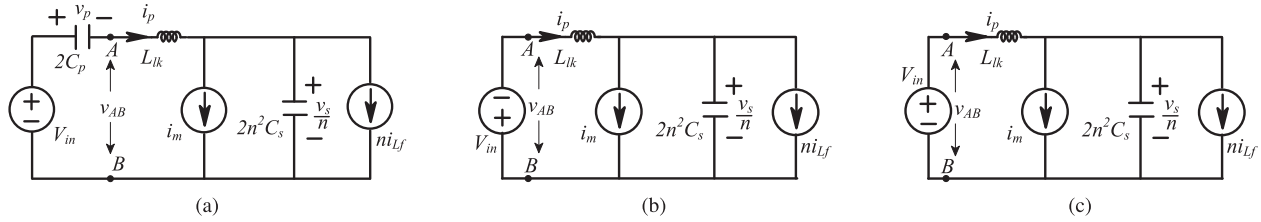

Fig. 9. Simplified equivalent circuits during various possible submodes of mode Va. (a) mode Va1 (b) mode Va2 (c) mode Va4. Mode Va3 has the same equivalent circuit as mode Va1.

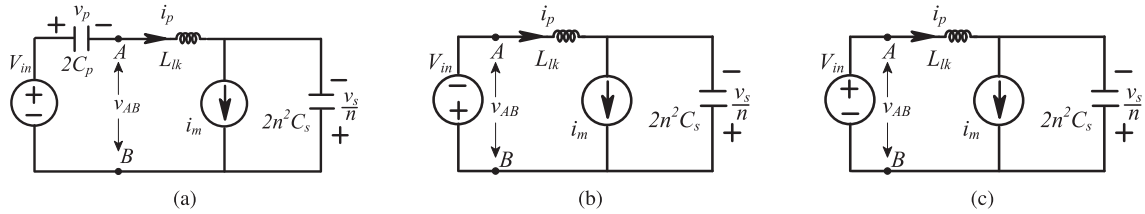

Fig. 10. Simplified equivalent circuits during various possible submodes of mode Vb. (a) Mode Vb1 (b) Mode Vb2 (c) Mode Vb4. Mode Vb3 has the same equivalent circuit as mode Vb1.

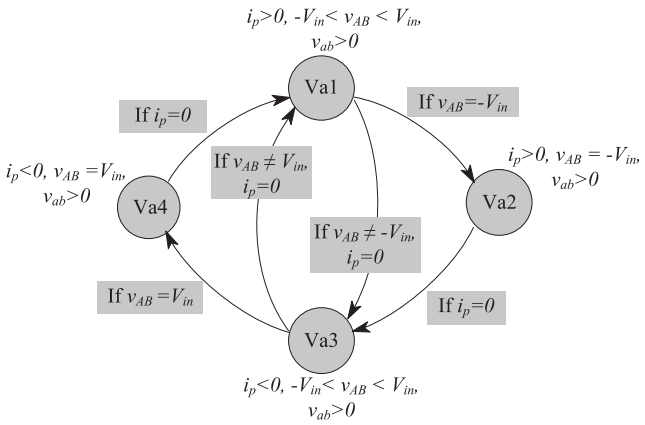

Fig. 11. State diagram explaining evolution of the various submodes of mode Va. Circuit operation proceeds along the outer and inner loops for higher and lower values of load current, respectively. Circuit exits from mode Va from any of the nodes and enters mode Vb when transformer secondary terminal voltage ($v_{\rm ab}$) reaches zero.

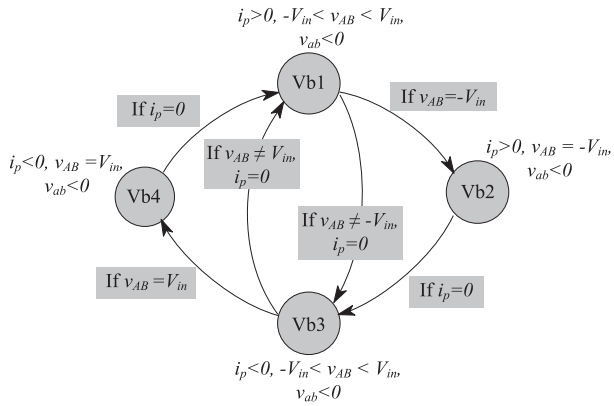

Fig. 12. State diagram explaining evolution of the various submodes of mode Vb. Depending on the conditions at the end of mode Va, circuit operation commences from any one of the nodes. Circuit exits from mode Vb from any of the nodes and enters mode VI when $v_{\rm AB}$ reaches $-V_{\rm in}$ and transformer secondary current (i_s) becomes zero.

Circuit operation continues on any of the nodes depicted on the state diagram of Fig. 11, till $v_{\rm ab}$ reaches zero, when operation in mode Vb starts.

7) Mode Vb ($t_6 - t_7$): As in mode Va, circuit operation in this mode can proceed through four submodes, whose equivalent circuits are depicted in Fig. 10. Depending on the initial conditions at the end of mode Va, circuit operation can commence from any one of these possible submodes. As $v_{\rm ab}$ goes negative at the start of these submodes, capacitors of M_5 and M_{10} begin charging, while the body diode of M_7 remains forward-biased, resulting in shorting of leg "b," through which $i_{\rm Lf}$ freewheels. Thus in the equivalent circuits representing the submodes, the current source $i_{\rm Lf}$ is absent. Circuit transitions between the several submodes continue according to the logic depicted in the state diagram of Fig. 12 with $v_{\rm AB}$ and $v_{\rm ab}$ approaching $-V_{\rm in}$ and $-nV_{\rm in}$, respectively.

The mode ends when the primary-side devices have just completed their voltage commutation process. This means on the secondary side too, M_5 and M_{10} have undergone full voltage commutation and are each blocking a voltage of $nV_{\rm in}$. The transformer secondary current falls to zero and the primary current is equal to i_m.

8) Mode VI ($t_7 - t_8$): This mode corresponds to the small duration between the end of mode Vb and the start of the second zero state when the diodes of the incoming primary devices are conducting. At the end of this mode, gate pulses to M_2 and M_3 are applied, resulting in their ZVS turn-on. The remaining eight modes corresponding to the next half-switching period proceed in identical fashion as the first six.

B. Extended Dead-Time Approach for Primary Switches' ZVS

From the preceding discussion, it is clear that the total time taken for the voltage across the incoming primary devices to

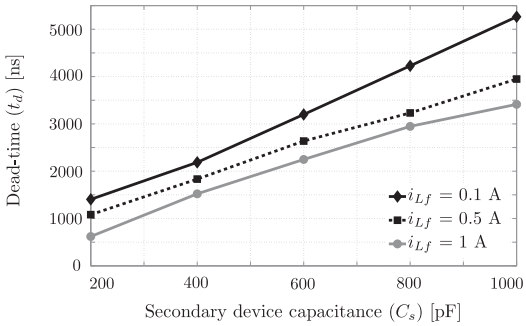

Fig. 13. Dead-time required between complementary primary switches to ensure their ZVS turn-on versus secondary device capacitance. $V_{\rm in} = 48$ V, $L_{\rm lk(pri)} = 1.3\ \mu$H, $C_p = 1.2$ nF, $i_{m\,(\rm peak)} = 0.8$ A.

fall to zero equals the sum of durations of modes Va and Vb. The maximum duration of mode Va occurs for zero load current and can be found from (11) by setting $i_{\rm Lf} = 0$ and solving for $v_s = 0$. This yields

$$0 = V_{\rm in} + \left(\frac{i_m}{2\omega_2 C_T}\right)\sin(\omega_2 \Delta t_{5a(\max)}) - \left(\frac{i_m}{2C_T}\right)\Delta t_{5a(\max)}.$$

It can be shown that the second term in the above equation is much smaller in magnitude compared to the third and hence an approximate solution for $\Delta t_{5a(\max)}$ may be obtained as

$$\Delta t_{5a(\max)} \approx 2V_{\rm in}C_T/i_m. \tag{13}$$

As discussed earlier, only the magnetizing inductor's energy is available in mode Vb to cause the transition of $v_{\rm ab}$ from 0 to $-nV_{\rm in}$ and thus achieve ZVS of the primary switches. Thus, similar to (13), the approximate duration for completion of this mode may be obtained as

$$\Delta t_{5b} \approx 2V_{\rm in}C_T/i_m. \tag{14}$$

Thus, the dead-time required between gate pulses of complementary primary switches in order to ensure their ZVS turn-on even at near-zero load current is given by

$$t_{d(\max)} = \Delta t_{5a(\max)} + \Delta t_{5b} = 4V_{\rm in}C_T/i_m. \tag{15}$$

A plot of dead-time (t_d) required to ensure ZVS of primary devices for different values of secondary-side device capacitance with the load current as a parameter is shown in Fig. 13. The value of t_d needed at a given load current is obtained by first calculating duration of mode Va by exact numerical solution of all occurring submodes. This is then added to the load-independent duration of mode Vb, predicted by (14) to obtain total value of t_d. It is clear from (15) and Fig. 13 that higher value of secondary-side device capacitance increases the dead-time requirement.

From (15) it is clear that it is possible to reduce the required minimum dead-time by adopting a fairly low-magnetizing inductance-based design leading to higher value of i_m. But this would lead to increased transformer rms currents and hence conduction losses. Another technique, which is used in the present work, involves setting a prolonged dead-time between primary-side gate pulses, such that ZVS can be achieved in mode Vb, even with a reasonably low value of i_m. Since for the SSM

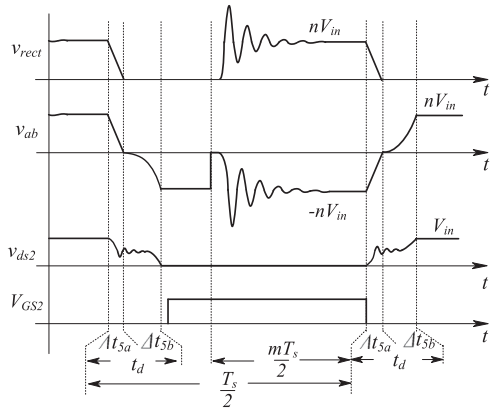

Fig. 14. Explaining limits of the extended dead-time approach. The maximum dead-time required (corresponding to zero load current) should be less than the minimum duration of the cycloconverter's zero state.

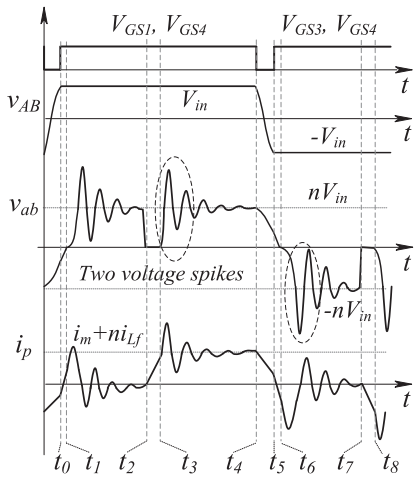

Fig. 15. Explaining occurrence of the additional voltage and current spikes for the low-dead-time SSM scheme.

scheme, the primary-side switching instant coincides with the start of the zero state of the cycloconverter, it is clear that even a slow rail-to-rail voltage commutation on the primary side will not impact the average volt-seconds developed at the output, provided the voltage transition duration does not exceed the minimum zero-dwell duration of $v_{\rm rect}$. Thus, the design limits for the extended dead-time approach can be mathematically expressed as

$$\begin{aligned} &t_{d(\max)} < \min(1 - mT_s/2) \\ &\Rightarrow 4V_{\rm in}C_T/i_m < \big(1 - (V_m/nV_{\rm in})T_s/2\big). \end{aligned} \tag{16}$$

It may be noted that, as discussed earlier, for higher values of load current, the initial stored energy in $L_{\rm lk}$ may be sufficient to completely discharge the capacitors of the incoming primary devices in mode Va itself. In such cases, it is not mandatory to adopt the described extended dead-time scheme to achieve ZVS of these devices. However, such an approach leads to another problem, which Fig. 15 illustrates. As shown, at the beginning of mode Va ($t = t_4$), transformer primary voltage $v_{\rm AB}$ quickly falls to $-V_{\rm in}$ and the circuit enters mode Va2 (cf. Fig. 11). If

TABLE II
SUMMARY OF SOFT-SWITCHING CHARACTERISTICS OF DEVICES FOR THE THREE MODULATION STRATEGIES

Switch	PSM	Low-dead-time SSM	High-dead-time SSM
M_1	Partial ZVS	Partial ZVS	ZVS
M_2	Partial ZVS	Partial ZVS	ZVS
M_3	Partial ZVS	Partial ZVS	ZVS
M_4	Partial ZVS	Partial ZVS	ZVS
M_5	ZVS	ZVS or ZCS	ZVS or ZCS
M_6	ZVS	ZVS	ZVS
M_7	ZVS	ZVS or ZCS	ZVS or ZCS
M_8	ZVS	ZVS	ZVS
M_9	ZVS	ZVS	ZVS
M_{10}	ZVS	ZCS or ZVS	ZCS or ZVS
M_{11}	ZVS	ZVS	ZVS
M_{12}	ZVS	ZCS or ZVS	ZCS or ZVS

TABLE III
DETAILS OF COMPONENTS USED

Component	Symbol	Description
Primary switches	$M_1 - M_4$	FDP075N15A (150 V, 7.5 mΩ)
Secondary switches	$M_5 - M_{12}$	IPA50R140CP (550 V, 140 mΩ)
Transformer	–	Turns-ratio (pr : s) = 10:50, made using 44 standard wire gauge copper foil, L_m (pr) = 450 μH, L_{lk} (pr) = 1.3 μH R_{ac} (pr) = 55 mΩ
Filter inductor	L_f	4 mH, 3 A rms (0.03 p.u)
Filter capacitor	C_f	1 μF, 450 V
Clamp capacitor	C_p, C_n	1 μF, 875 V
Coupled inductor	L_{cp}, L_{cn}	180 μH, 1:1

the gate pulses of the incoming devices (M_2, M_3) are applied next, they turn-on with ZVS and $v_{\rm AB}$ gets clamped to $-V_{\rm in}$. The crucial difference with the extended dead-time approach is when i_p becomes negative afterward, circuit operation continues with the single-resonant equivalent circuit of mode Va2 and thereafter with that of mode Vb2 when $v_{\rm ab}$ becomes negative. This resonant operation subsequently leads to another voltage and current spike in addition to the one encountered at the zero state to powering state transition. The current spike increases the transformer rms current while the voltage spike degrades efficiency by increasing the energy to be processed by the clamp circuit.

C. Summary of Comparison with Other Modulation Schemes

In this section, advantages of the proposed extended-dead-time SSM scheme compared to the PSM scheme and the low-dead-time SSM strategy are highlighted. The soft-switching characteristics of the devices are compared in Table II, which shows that for the PSM and low-dead-time schemes, the primary devices undergo ZVS operation only over a limited range of the output ac line cycle. As is well known from the literature of phase-modulated converters [16], the primary-side leg undergoing commutation following a zero state (leading leg) is likely to miss ZVS. ZVS of the other leg is load dependent and hence its ZVS status varies over the ac line cycle [20]. Magnetizing current can be utilized to extend the ZVS range for PSM, but the continuous modulation of the primary-side voltage in PSM changes the peak magnetizing current level available for ZVS. In contrast, the constant peak value of the magnetizing current in SSM makes it easier to achieve ZVS of the primary devices over the entire line cycle. This idea has been used in the present converter along with the extended-dead-time approach to achieve ZVS of the primary devices over the ac cycle. On the secondary side, all devices undergo ZVS turn-on for PSM. For the SSM schemes, the four inner secondary devices always undergo ZVS while alternate pair of outer devices undergo ZVS and zero current switching (ZCS) over alternate half-cycles of the output. Another key advantage of the high-deadtime SSM scheme compared to PSM is the lower rms value of the transformer current, since unlike the PSM case there is no circulating current in the transformer during the zero state of $v_{\rm rect}$. As mentioned earlier, the transformer rms current for the low-dead-time SSM scheme is also higher because of the additional current spike.

D. Commutation Strategy for Nonunity Power Factor Loads

As mentioned earlier, the commutation strategy described in Section III-A is applicable for resistive loads only. Adopting the same commutation sequence for nonunity power factor loads leads to circuit maloperation during the duration when instantaneous power flow is from the ac side to the dc side. This is explained through Fig. 16, which illustrates circuit commutation at the freewheeling to powering (F2P) and powering to freewheeling (P2F) transitions when $v_{\rm rect} \geq 0$ and $i_{\rm Lf} < 0$. As can be seen from Fig. 16(a) and (c), following the same commutation sequence as described before results in abrupt interruption of the current source $i_{\rm Lf}$ at both transitions.

For instance, removal of the gate pulse of M_9 first at the F2P transition clearly leads to opening of $i_{\rm Lf}$. Modified strategies that lead to safe commutation of the devices are shown in Fig. 16(b) and (d). As Fig. 16(b) illustrates, for the F2P transition, removal of gate pulse of M_{10} (and not M_9) first creates no such open-circuiting problem as the current shifts to the body diode of M_{10}. The remaining part of the commutation sequence (not shown in Fig. 16) involves application of gate-pulse of M_{11} next followed by removal of that of M_9, when capacitors of M_9 and M_{12} begin to be charged and discharged, respectively, by $i_{\rm Lf}$. The F2P commutation sequence ends with the application of gate pulse of M_{12} after its capacitor has been discharged completely, resulting in its ZVS turn-on. Similar considerations dictate choice of the switching sequence at the P2F transition.

In summary, the appropriate commutation sequence to be selected at a particular transition depends on knowledge of the direction of the filter inductor current, as is required for the four-step commutation process outlined in [26], [27]. The complete overview of a generic commutation sequence (for $v_{\rm rect} \geq 0$) is depicted in Fig. 17.

It may be noted that the modified strategy for reactive loads does not fundamentally alter the requirement for voltage clamping of the secondary devices. For the just-described F2P transition, after M_{12} is turned on, resonant oscillations start between the secondary-side leakage inductance and the output capacitances of M_9 and M_7, as in mode III of Section III-A. The clamp

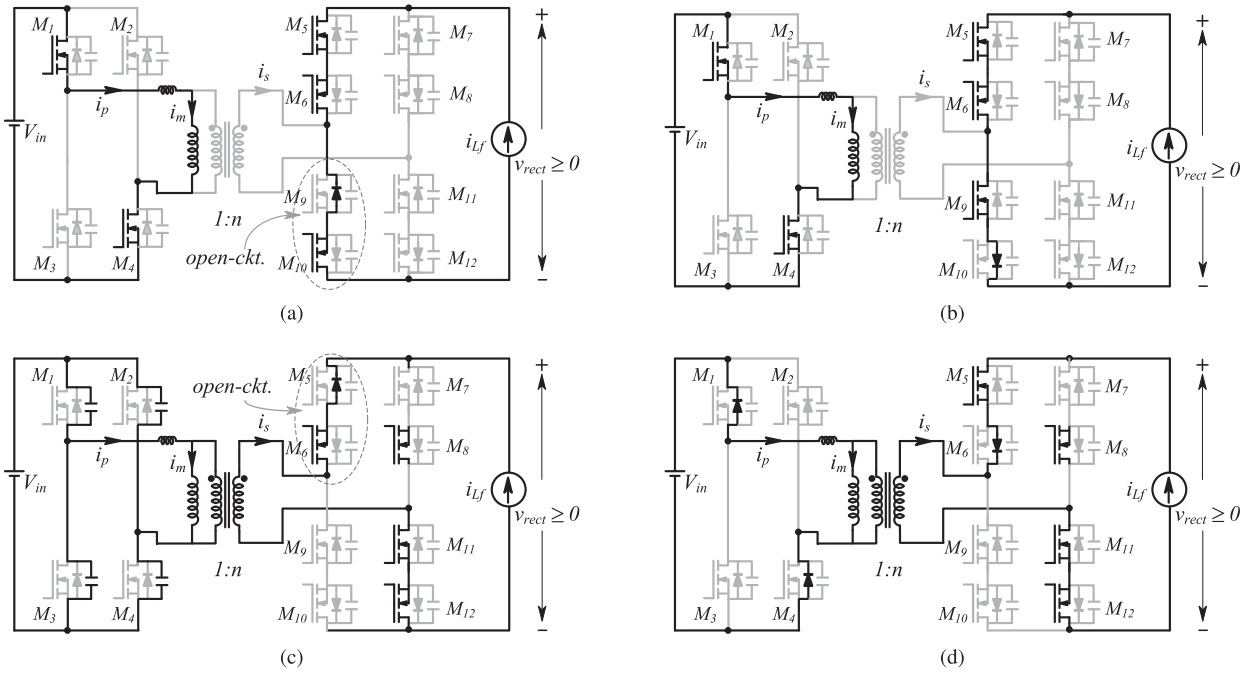

Fig. 16. Illustrating the modifications required to the commutation strategy when instantaneous power flow is from the ac side to the dc side ($v_{\rm rect} \geq 0, i_{\rm Lf} < 0$). (a) Zero state to powering transition. Adopting the same commutation sequence as for resistive loads leads to abrupt opening of the current source $i_{\rm Lf}$. (b) Modified zero state to powering transition. Unlike the $i_{\rm Lf} > 0$ case, gate pulse of M_{10} is removed first (not M_9). This leads to safe commutation. (c) Powering to zero state transition. Adopting the same commutation sequence as for resistive loads again leads to abrupt opening of the current source $i_{\rm Lf}$. (d) Modified powering to zero state transition. Unlike the $i_{\rm Lf} > 0$ case, gate pulse of M_6 is removed first (not M_5). This leads to safe commutation.

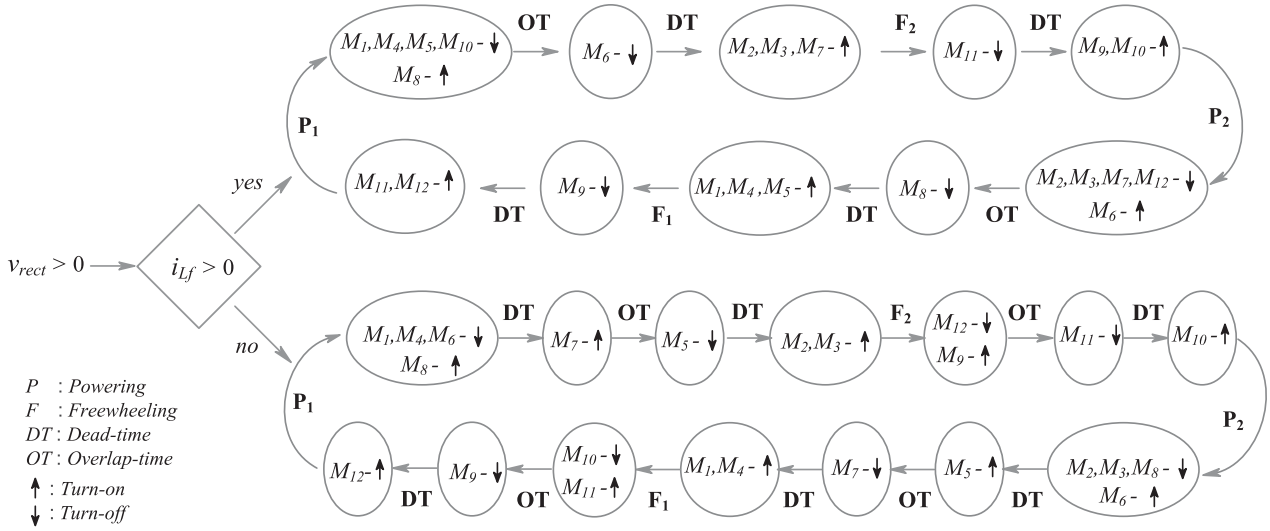

Fig. 17. Diagram summarising the generic commutation sequence for $v_{\rm rect} > 0$. Upward directed arrows denote switches turning on, while downward directed arrows denote switches turning off.

circuit performs the function of arresting the voltage spikes across the devices as before.

IV. Experimental Results

A 260 W, 35–50 V input, 110-V rms, 50-Hz output prototype (see Fig. 18) of the converter, with component specifications listed in Table III has been built and tested. The switching frequencies of the main circuit and auxiliary clamp circuit are 25 and 1.56 KHz, respectively. Gate pulses are given to the converter using a Xilinx XC3S200 FPGA-based control board. A single-ended transformer-coupled gate drive circuit with a dc restore circuit [30] is used to drive each switch.

In order to start the converter without incurring the risk of high inrush currents and/or overvoltage spikes, the following sequence needs to be followed. Initially, gate pulses of only the primary-side devices are to be applied. Further, during the startup process the primary full-bridge can be operated in quasi-square wave mode with gradually increasing pulse width [15] in order to mitigate the overcurrent problem. Once the positive

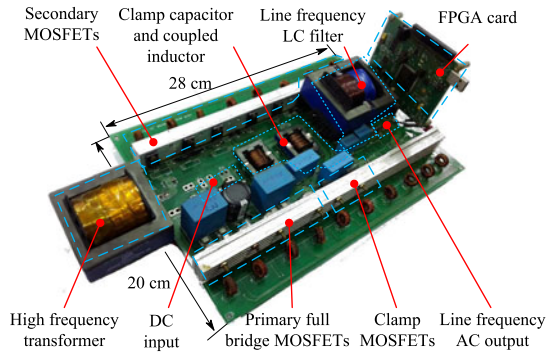

Fig. 18. Photograph of the hardware prototype.

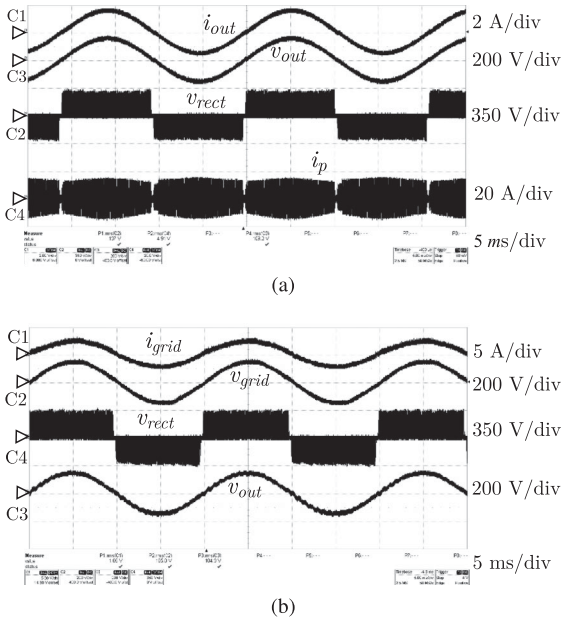

Fig. 19. (a) Waveforms for standalone operation with resistive load - output current ($i_{\rm out}$), output 50-Hz ac voltage ($v_{\rm out}$), rectified voltage ($v_{\rm rect}$) and transformer primary current (i_p). (b) Grid connected operation under unity power factor condition—grid current (i_{grid}), grid voltage (v_{grid}), rectified voltage ($v_{\rm rect}$) and output 50-Hz ac voltage ($v_{\rm out}$) of converter.

and negative clamp capacitors are charged to $nV_{\rm in}$ and $-nV_{\rm in}$, respectively, gate pulses of the secondary devices and the clamp circuit switches can be applied. For grid-connected operation, after the output voltage ($v_{\rm out}$) has been phase synchronized with the grid voltage, the converter can be interfaced with the utility mains.

Relevant steady-state experimental results for unity power factor operation are shown in Figs. 19–25. Low-frequency waveforms of the converter including the final line frequency ac output voltage for standalone resistive load and grid-interactive operation under unity power factor condition are shown in Fig. 19.

Fig. 20 compares important high-frequency waveforms for the SSM and PSM schemes, from which the absence of circulating current during the zero state for the SSM strategy can be clearly observed. Mitigation of secondary voltage spikes due to the clamping action of the snubber circuit can also be noted.

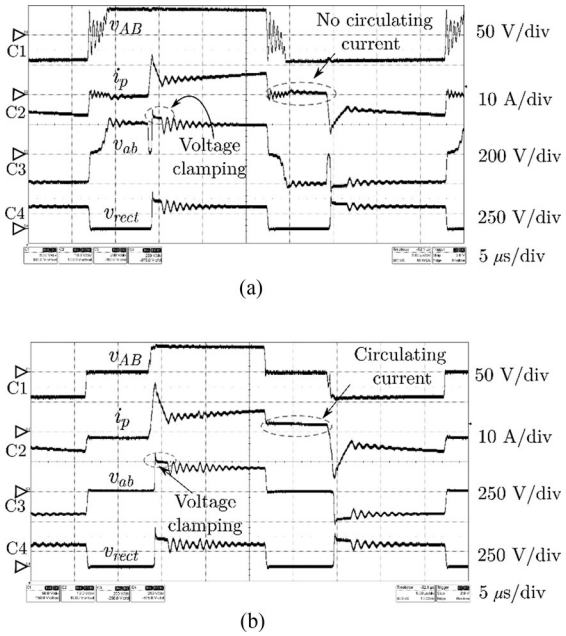

Fig. 20. Illustrating absence of circulating current on the primary side for SSM. (a) SSM (b) PSM.

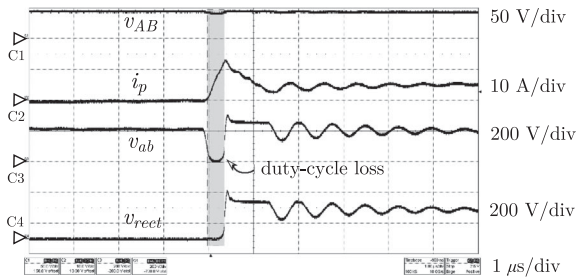

Fig. 21. Illustrating operation of the circuit at the zero state to positive powering state transition.

Fig. 21 shows the close-up of these waveforms for the SSM strategy around the zero state to powering transition, from which the small duty-cycle loss duration, when the voltage $v_{\rm ab}$ collapses to zero, can be identified.

Operation of the circuit at the positive powering to zero-state transition can be explained through the waveforms of Fig. 22. Waveforms corresponding to mode Va for high and low values of load current are shown in Fig. 22(a) and (b), respectively. It can be observed that, the voltage of the secondary-side device (M_7) and the primary-side current quickly collapse to zero at the beginning of this transition, on account of the loading effect of the secondary switches' parasitic output capacitance. Operation in mode Vb is depicted in Fig. 22(c), which shows charging of the secondary-side device capacitor (of M_5) and also the resonant oscillations in the transformer current i_s along with the transformer terminal voltages. The relatively slow rate of charging of the secondary-side device capacitor can be attributed to the fact that this capacitance is comparatively larger as the voltage across it is initially zero. In all three cases, the extended-dead-time-based approach is adopted to affect ZVS turn-on of the incoming primary devices.

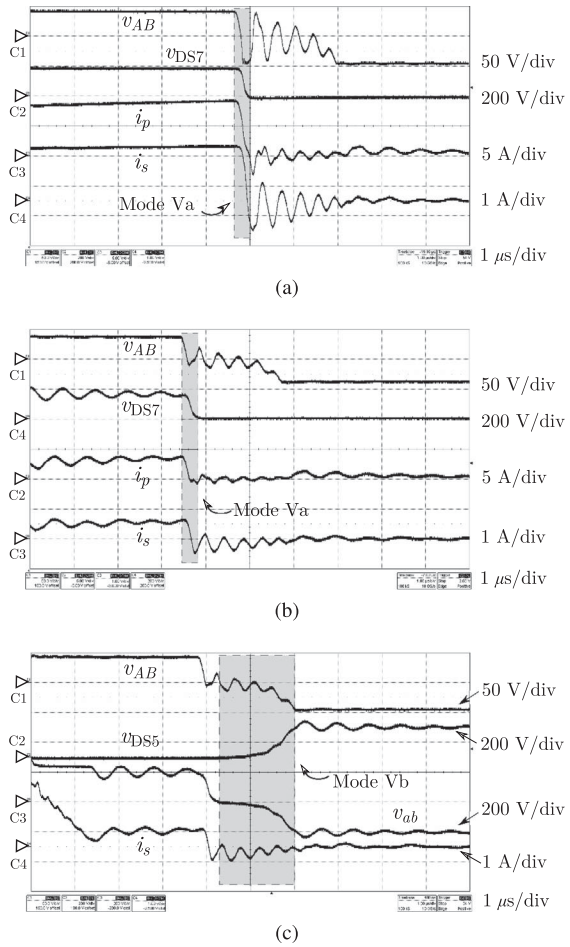

Fig. 22. Illustrating operation of the circuit at the positive powering state to zero state transition. (a) Mode Va for high value of load current. (b) Mode Va for low value of load current. (c) Mode Vb.

The additional voltage and current spikes occurring at the powering to zero state transition for the low-dead-time SSM scheme are highlighted in Fig. 23. Soft-switching operation of the different switches for the extended-dead-time SSM scheme are depicted in Fig. 24. It can be seen that three of the four switches of a secondary leg undergo ZVS turn-on while the other has ZCS turn-off. All four primary devices undergo ZVS turn-on in contrast to the PSM and low-dead-time schemes, where one of the two legs may miss ZVS, as Fig. 25 illustrates.

Waveforms pertaining to operation with nonunity power factor loads are depicted in Figs. 26 and 27. Fig. 26 shows key waveforms over a high-frequency switching period for which power is instantaneously fed back to the input side, which is evident from the opposite polarities of i_{Lf} and $<v_{\mathrm{rect}}>$. The modified commutation sequence ensures safe operation of the devices, as can be inferred from waveforms of v_{ab} and v_{rect}. Low-frequency waveforms corresponding to operation in standalone mode with an *R-L* load are shown in Fig. 27(a). Grid-interactive operation of the converter under different power-factor conditions has also been successfully tested on the prototype. Fig. 27(b) shows waveforms for one such operation, with the converter delivering reactive power to the grid.

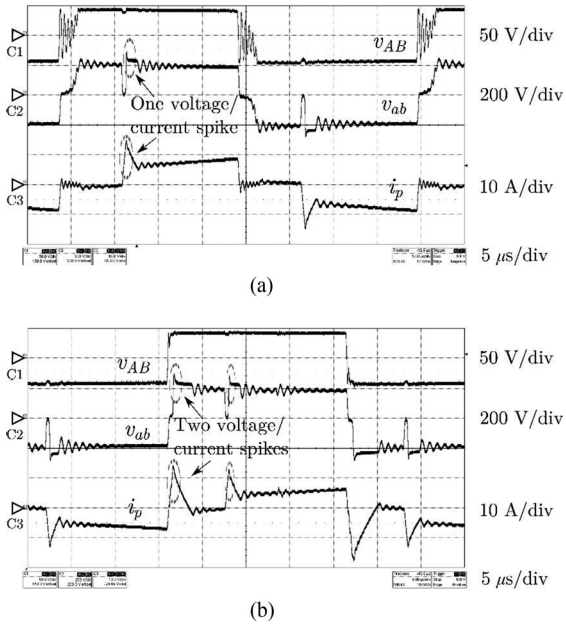

Fig. 23. Illustrating occurrence of second voltage and current spike for SSM with low dead-time. (a) With high dead-time. (b) With low dead-time.

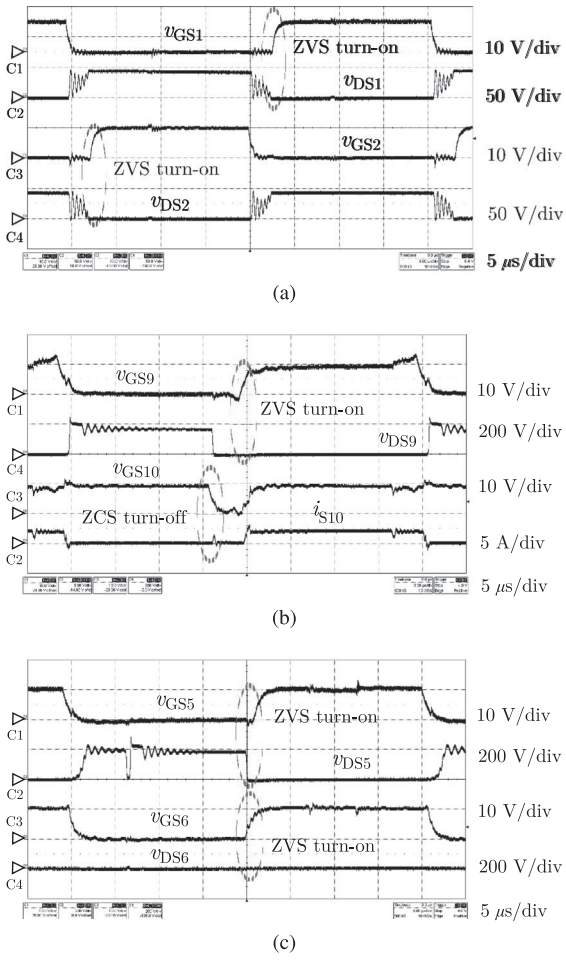

Fig. 24. Illustrating soft-switching operation of the devices for SSM. (a) ZVS turn-on of both primary switches. (b) ZVS turn-on and ZCS turn-off of switches of one 4Q pair of a secondary leg. (c) ZVS turn-on of both switches of another 4Q pair of the same leg.

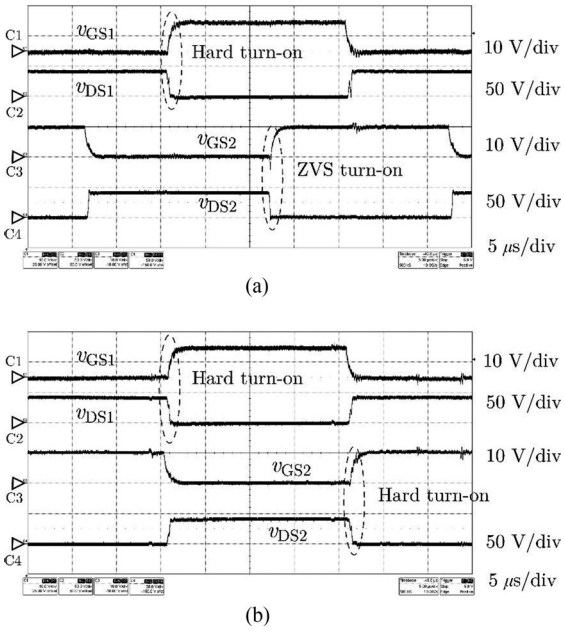

Fig. 25. Illustrating hard-switching operation of the primary devices for (a) PSM and (b) low-dead-time SSM.

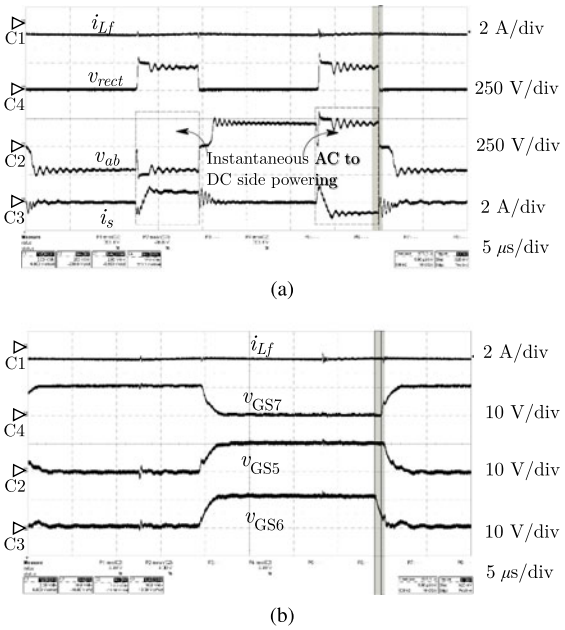

Fig. 26. High-frequency waveforms for nonunity power factor load (a) key waveforms illustrating instantaneous power flow from ac side to dc side (b) sequence of gate pulses at the powering to zero state transition.

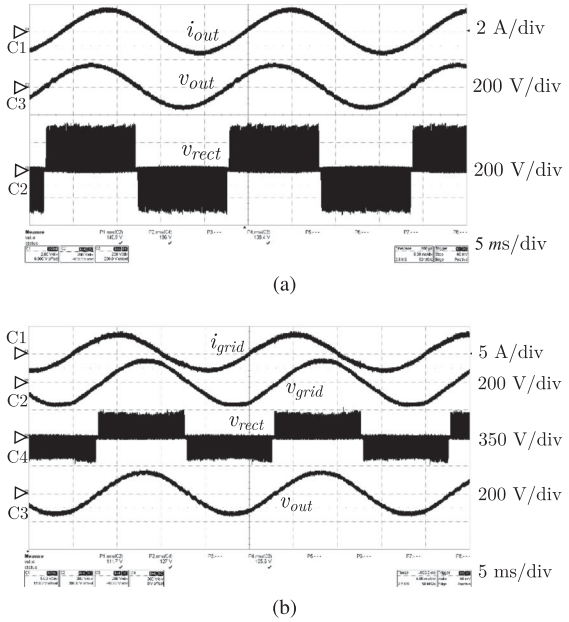

Fig. 27. Low-frequency waveforms for nonunity power factor load (a) standalone operation with R-L load (b) grid-connected operation with reactive power fed to the grid.

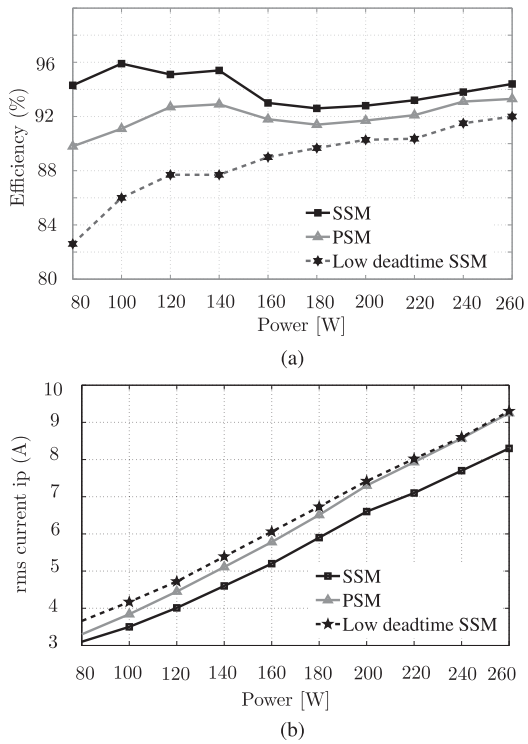

Fig. 28. Comparison of experimentally obtained values of efficiency and transformer primary current rms for the SSM, PSM, and low-dead-time SSM schemes (a) efficiency (b) primary rms current.

Fig. 28 compares the experimentally measured values of efficiency and transformer primary rms current of the converter when it is operated with PSM and low-dead-time SSM with that of the extended dead-time SSM scheme. It is observed that the latter scheme results in efficiency improvements over the entire power range, particularly at low loads.

A detailed breakdown of the losses incurred for the three schemes (excluding clamp circuit losses) at 200-W output power is shown in Fig. 29, from which it can be inferred that the efficiency improvement due to the extended dead-time SSM scheme can be mainly attributed to reduced switching loss and lower high-frequency conduction loss. The losses in the clamp circuit are significant and measured to be 7.1, 8.1, and 9.8 W at 200-W output power for the high-dead-time SSM, PSM and

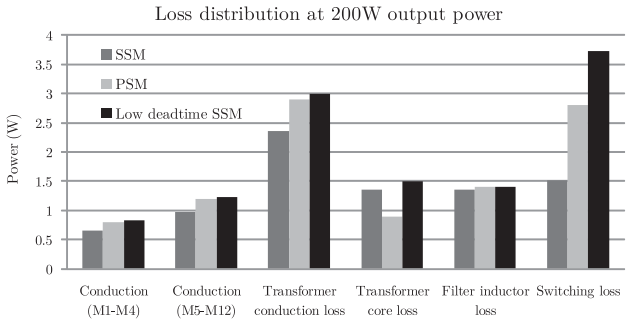

Fig. 29. Comparison of experimentally obtained loss distribution for the three schemes at output power of 200 W (without clamp circuit losses).

low-dead-time SSM schemes, respectively. Hence, design of a more efficient clamp circuit can lead to further efficiency improvements.

V. Conclusion

This paper has presented a strategy for operating the single-stage, isolated, high-frequency link converter, operated as a high-gain boost inverter, based on sinusoidal phase modulation of the secondary legs. A comprehensive circuit analysis with the proposed SSM scheme is presented considering prominent practical nonidealities such as transformer leakage inductance and secondary-side device capacitance. The analysis reveals key insights about influence of the parasitics on the primary-side switches ZVS operation and on generating voltage spikes across the secondary devices. An extended-dead-time-based approach is proposed, which utilizes magnetizing energy to achieve ZVS of the primary devices across the line cycle of the ac output. The proposed scheme has the further advantage of reduced transformer rms current due to the absence of circulating current during the zero state, unlike the conventional PSM scheme. An unified commutation strategy applicable for nonunity power factor loads is also proposed. Experimental tests performed on a 260-W laboratory prototype validate the analysis and exhibit efficiency improvements with the extended-dead-time approach.

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