An Analytical Method to Evaluate and Design Hybrid Switched-Capacitor and Multilevel Converters

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***Abstract*—This paper investigates the use of multilevel conversion in dc–dc applications that require a large voltage conversion ratio. A quantitative method that can serve as a guide to compare and design multilevel topologies for large conversion ratio applications is presented. The proposed method keeps the conduction loss and switching loss constant across the different converters and employs the passive component volume as the single performance metric. As examples, flying capacitor multilevel converters and hybrid switched-capacitor (SC) converters are compared to conventional two-level buck converters, and are shown analytically to have significantly reduced passive component size. Three converter prototypes are implemented, based on the presented methodology to experimentally validate the method as well as demonstrate the advantages of multilevel and hybrid SC converters.**

***Index Terms*—Hybrid switched-capacitor, large conversion ratio, multilevel, passive component volume, switched-capacitor, flying-capacitor multilevel.**

I. Introduction

LARGE voltage step-down/step-up ratio is a common occurrence in power conversion applications. For instance, 380 V to 12 or 48 V conversions are required to deliver power to servers in data centers. Likewise, in offline applications, PFC front-ends generate near 400 VDC that is often stepped down to 12–24 V. High step-up boost converters are used to interface PV panels with the grid [1]. At lower voltage levels, microprocessors are powered by voltage regulation modules which convert the 12 V dc bus to 1–1.6 V. In these applications, the magnetic elements typically dominate the size of the converter. Therefore, in order to reduce the overall volumetric footprint, it is desirable to further reduce the inductor size without sacrificing the conversion efficiency.

Flying capacitor multilevel converters (FCMC) have received attention in medium-voltage dc–ac applications due to their low device voltage ratings and increased pulse frequency seen by the inductor[2]–[4]. Recently, it has also been shown that the FCMC converter is able to achieve excellent power density and efficiency at low voltages (e.g., 400 V) [5]. While there has been extensive research on FCMC converters in the dc–ac domain, the use of such converters in dc–dc applications has been relatively limited. A three-level step-down FCMC, also called three-level buck converter, is used in [6] for envelope tracking power amplifier and shown to be superior to conventional two-level interleaved buck converters. A four-level step-up FCMC for plug-in hybrid electric vehicles is presented in [7], but with only fixed conversion ratios (i.e., no output voltage regulation). A variant of the five-level FCMC is implemented as a bidirectional high-voltage dc–dc converter in [8]. Flying capacitors can also be added to multiphase buck converters [9], [10] to reduce the device voltage stress, and a recent implementation shows significant efficiency improvement over conventional buck converters in high-frequency operation at 3 MHz [11].

Another type of converters that has potential in large step-up/down ratio applications is switched-capacitor (SC) converters [12], [13]. It has been shown that the switch utilization in SC converters is higher compared to buck or boost converters [14]. However, conventional SC converters have charge redistribution loss as well as poor output voltage regulation and, therefore, are typically best suited for low-power applications. The charge redistribution loss can be eliminated in multilevel and hybrid SC converters, which have one or more inductors added to the SC topology [15]–[23]. In addition, lossless output voltage regulation can be achieved through a second-stage magnetic converter [24], [25] or employing the switching techniques presented in [26] and [27] for the hybrid converters. These converters are shown to have higher efficiency and power density compared to conventional SC converters, but comparisons against conventional buck converters are nonexistent to date.

The hybrid SC converters can be regarded as multilevel converters since there are multiple intermediate voltage domains, generated by the flying capacitors. On the other hand, the FCMC can also be seen as a type of hybrid SC converter, since it combines an SC cell with an inductor. Therefore, these topologies are closely related and the term multilevel and hybrid SC are used interchangeably in this paper. Due to the use of flying capacitors and multiple switches, a large number of topological variations are possible for the hybrid SC converters, with some better than others. This paper presents a quantitative method to compare these hybrid converters, from the perspective of the fundamental utilization of the active and passive devices. In particular, this paper explores the applications of FCMC converters and hybrid SC converters in dc–dc conversion, with an emphasis on a large voltage conversion ratio. Unlike previous

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three-level buck converter analysis [6], a formal comparison method is given, and the volume of the flying capacitors is taken into account. It will be shown that multilevel and hybrid SC converters have significantly reduced passive component size compared to buck converters. This paper analytically shows the advantages of the multilevel converters and serves as a guide for designing these converters.

This paper is based on our previous conference paper [28] and is organized as follows. Section II outlines the comparison methodology and the motivation and assumptions behind it. Section III analyzes the FCMC and compares it against the buck converter using the proposed methodology. Section IV generalizes the methodology to hybrid SC converters and use the Dickson hybrid SC converter as an example. Experimental verification is given in Section V. Section VI presents some of the practical challenges of the multilevel converters, and finally conclusions are given in Section VII.

II. Proposed Comparison Methodology

The scope of the comparison is focused on the power stage, which in most cases determine the size and efficiency of a converter. While many additional gate driving and level-shifting circuitries can be required by the multilevel types of converters, their contribution to the size of the circuit can be small when high-power applications are considered. On the other hand, in low-voltage applications, these auxiliary circuits can be further miniaturized by IC integration.

When comparing topologies, a dilemma often faced is the tradeoff between the complexity of the model and the accuracy of the result. Comprehensive loss and size calculations can be carried out, which may yield accurate results, but the resultant expressions are often too complicated to provide any intuitive understanding. On the other hand, simple expressions are easily comprehensible, but the theoretical results may differ significantly from reality. A compromise is drawn in this paper, with an emphasis on obtaining tractable expressions. The rationale is that the converter design is a multidimensional problem, which involves the tradeoff between semiconductor conduction loss, semiconductor switching loss, inductor dc and ac loss, inductor volume, capacitor volume, etc. Each of the components (switch, inductor, capacitor) has multiple parameters that influence both the efficiency and size. There are many second-order effects that are not easily captured in equations with reasonable accuracy. An attempt to compare topologies aiming for high accuracy will likely end up designing and optimizing every topology in detail using real components, which involves a considerable amount of work and loses generality and usefulness of the method along the way. Therefore, this paper on topology comparison serves as the first pass in identifying the advantageous candidates among the applicable topologies. The merits and demerits of each topology can be easily spotted analytically and intuitively. It should then be followed with design methods such as the pareto-front optimization [29], which can be used to determine the final converter and design choice for an application.

In order to yield comprehensible expressions that allow sensible comparison among topologies, the following assumptions are made.

1) The losses considered are only the conduction and switching losses of the semiconductor switches, as well as the conduction loss in inductors.
2) The volume is calculated based on only the volume of the capacitors and inductors. The volume of the active devices and auxiliary circuits is neglected.

These assumptions are based on the observations that the passive components—the inductors and capacitors—usually dominate the size of a converter. On the other hand, the active switching devices usually dominate the losses in hard-switching converters, especially in continuous conduction mode operation where the inductor current ripple is small. While the core loss and ac winding loss of the inductor can also make significant contribution to the power loss, the comparison is valid as long as it does not favor any particular topology by omitting this loss. Ceramic and film capacitors are known to have very small ESR (a few milliohms) in the frequency range of hundreds of kilohertz, and thus, the power loss due to the ESR can often be neglected, as is done in this paper. These losses should certainly be considered in the later design stage.

Another difficulty in comparing different topologies is that there is a tradeoff between the efficiency and size of a converter. As a result, it is not enough just to compare the efficiencies of two converters, without taking into account the size of a converter, and vice versa. In order to carry out a fair comparison among topologies, in this paper, the switch and inductor conduction losses are designed to be the same across the topologies, as well as the device switching losses, by choosing the appropriate switch conductance and switching frequency. With these parameters established, the required inductance or capacitance values can be obtained. This results in a single metric (passive components volume) that reflects the performance of the converter. An advantage of the proposed approach is that it is free from the effect of design tradeoff for each type of converters. By scaling the design parameters such that the switching loss and conduction loss are the same for all converters, the passive component size becomes the only variable and, thus, the comparison can focus on the fundamental difference between the topologies. It should be noted here that size and efficiency are the two facets of the fundamental tradeoff in converters. The choice in this paper is to compare size while keeping efficiency the same, while it is certainly possible to compare the efficiency while keeping the size the same.

Following the preceding rationale, the comparison procedure is proposed as follows.

1) Determine the conductance needed for the switches in order to make the equivalent resistance of each topology the same, so that the conduction losses are the same.
2) Given the conductance and voltage rating of each switch, determine the switching frequency such that the switching losses of all the converters are the same.
3) Determine the inductance required by each topology based on the allowed inductor current ripple, the switching frequency, and duty ratio.
4) Determine the capacitance required by the multilevel topologies from the allowed capacitor voltage ripple.

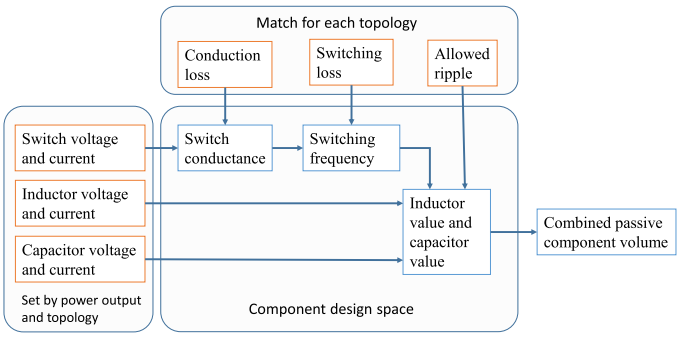

Fig. 1. Flowchart of the proposed comparison methodology.

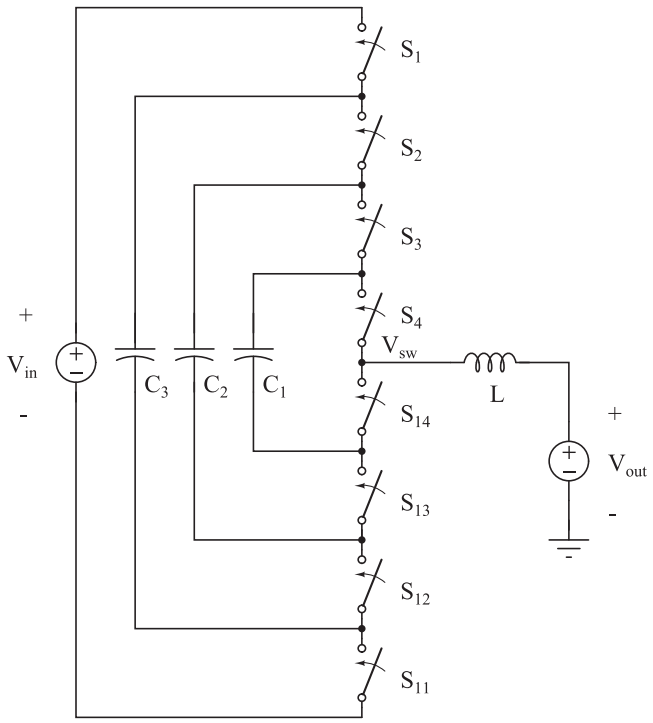

Fig. 2. Schematic drawing of a five-level flying capacitor multilevel converter.

5) Combine the inductance and capacitance into a single passive component volume metric.

An overview of the above procedure is shown as a flowchart in Fig. 1. Since the buck converter is the most basic pulse width modulation (PWM) step-down converter, it is used as a reference to which all topologies are compared to.

III. Flying Capacitor Multilevel Converters

In this section, the details of the comparison method are presented, using the FCMC converters as examples. The schematic drawing of a five-level FCMC converter is shown in Fig. 2. The switching node voltage $V_{\rm sw}$ can have five values ($V_{\rm in}$, $3/4V_{\rm in}$, $2/4V_{\rm in}$, $1/4V_{\rm in}$, and 0), depending on the circuit states. For each switching node voltage, there are more than one circuit states that result in the corresponding voltage. In this paper, since the FCMC is used in large voltage step-down applications, it is assumed that the desired output voltage is between 0 and $\frac{1}{N-1}V_{\rm in}$, where N is the number of levels. The corresponding switch

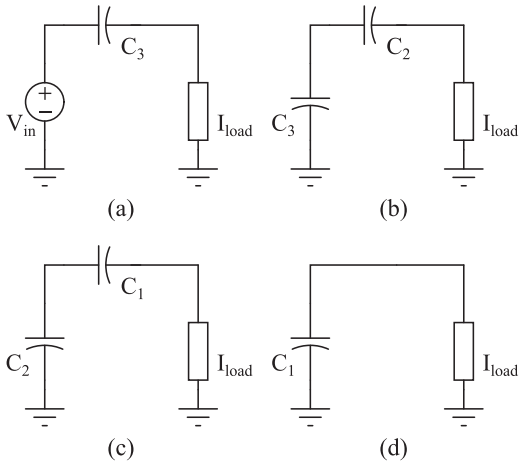

Fig. 3. Equivalent circuits for $V_{\rm sw} = \frac{1}{4}V_{\rm in}$. (a) State 1a. (b) State 1b. (c) State 1c. (d) State 1d.

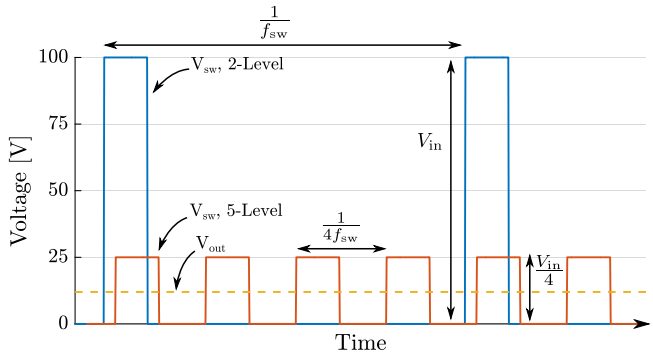

Fig. 4. Switching node voltages $V_{\rm sw}$ and the output voltage of a two-level and five-level converter for 100 to 12 V conversion.

states are shown in Table I, where "1" represents ON and "0" represents OFF. The circuit states to achieve a switching node voltage of $\frac{1}{N-1}V_{\rm in}$ are shown in Fig. 3. A typical switching sequence is $1a \rightarrow 0 \rightarrow 1b \rightarrow 0 \rightarrow 1c \rightarrow 0 \rightarrow 1d \rightarrow 0$, and then back to $1a$. By observing Table I and Figs. 3 and 4, it can be seen that in one complete switching sequence, all the switches only make one set of transitions, yet four voltage pulses at the switching node are produced. In general, the switching node frequency is $(N-1)$ times the transistor switching frequency, for an N-level FCMC. This is known as the "multiplication" effect of the FCMC converter [2]. In addition, it should also be noted that a buck converter can be viewed as a two-level FCMC, and therefore, two-level and buck are used interchangeably in the rest of this paper.

A. Conduction Loss

Following the comparison procedure proposed in Section II, the first step is to make the conduction losses of the converters the same, by selecting the conductance of the switches. Since the switch pairs (S_x and S_{1x}) in Fig. 2 operate in a complimentary fashion, for an N-level FCMC, there are always $(N-1)$ switches that are closed and connected in series with the load. On the other hand, a buck converter (for which $N=2$) always has one switch conducting the load current. Thus, if

TABLE I
SWITCH STATES AND CAPACITOR STATES CORRESPONDING TO SWITCHING NODE VOLTAGES OF $\frac{V_{\rm in}}{N-1}$ AND 0

State	$V_{\rm sw}$	S_1	S_2	S_3	S_4	S_{11}	S_{12}	S_{13}	S_{14}	C_1	C_2	C_3
1a	$V_{\rm in}/(N-1)$	1	0	0	0	0	1	1	1			+
1b	$V_{\rm in}/(N-1)$	0	1	0	0	1	0	1	1		+	−
1c	$V_{\rm in}/(N-1)$	0	0	1	0	1	1	0	1	+	−	
1d	$V_{\rm in}/(N-1)$	0	0	0	1	1	1	1	0	−		
0	0	0	0	0	0	1	1	1	1			

For switches, "1" denotes ON state and "0" denotes OFF state. For capacitors, "+" denotes charging state and "−" denotes discharging state.

the conductance of the switches of a buck converter is $G_{\rm buck}$, the switch conductance of an N-level FCMC $G_{\rm FCMC}$ needs to satisfy (1), in order to result in the same conduction loss.

$$\frac{G_{\rm FCMC}}{G_{\rm buck}} = N-1. \tag{1}$$

It should be noted that the calculation assumes that all the switches in a converter have the same conductance. While, in practice, the low-side switch of the buck converter is usually chosen to have a higher conductance than the high-side switch to maximize the efficiency in a large voltage step-down scenario, the same optimization can be performed on the multilevel converters, and would yield a similar benefit in terms of efficiency improvement. In general, for each different topology, the switches can be optimized so that their conductance corresponds to the rms current through them. For simplicity, this asymmetric switch sizing is omitted from the examples used here, but can be easily included if desired.

B. Switching Loss

The next step is to make the switching losses the same by choosing the switching frequency, based on the previously selected switching conductance and the switch voltage ratings. Assuming the same switch technology, the switch size as well as the switching loss are often approximately proportional to the GV^2 product of the switch, where G is the conductance and V is the blocking voltage of the switch [14]. A justification for the use of the GV^2 product is provided in Appendix A, which presents an empirical analysis of GaN transistors that support this particular device scaling parameter. Moreover, it is recognized here that other metric can be used in place to represent the switching loss, in order to reflect the scaling or limitation of a particular switch technology.

In order to achieve the same switching losses for the buck converter and FCMC converter, the following needs to be satisfied:

$$\sum_{\rm switches} (GV^2)_{\rm FCMC} \times f_{\rm FCMC} = \sum_{\rm switches} (GV^2)_{\rm buck} \times f_{\rm buck}. \tag{2}$$

The FCMC converter has $2(N-1)$ switches, each with a voltage rating of $\frac{1}{N-1}V_{\rm in}$, while the two-level or buck converter has two switches, each with a rating of $V_{\rm in}$. Rearranging (2) and substituting into (1), the sums of the GV^2 products for the two converters are obtained as

$$\frac{\sum (GV^2)_{\rm FCMC}}{\sum (GV^2)_{\rm buck}} = \frac{G_{\rm FCMC}}{G_{\rm buck}} \times \frac{2(N-1)\times\left(\frac{1}{N-1}V_{\rm in}\right)^2}{2\times V_{\rm in}^2} = 1. \tag{3}$$

As can be seen, the sum of the GV^2 turns out to be the same for both converters. This means that the FCMC converters can switch at the same transistor switching frequency as the buck converter for the same conduction loss and switching loss:

$$f_{\rm FCMC} = f_{\rm buck}. \tag{4}$$

In existing literature, the advantage of the FCMC is often stated to be reduced inductor current ripple compared to a buck converter, while it is implicitly assumed that the switching frequency is the same as that of the buck converter. The above analysis provides a basis for such an assumption.

C. Inductor

For efficiency reasons, the inductance value of PWM converters is usually chosen based on a certain inductor current ripple: A larger ripple allows for a smaller inductance, but results in higher ac conduction loss and magnetic core loss. The inductor current ripple in turn depends on the terminal voltages the inductor experiences during a switching cycle. As an illustration, the switching node voltages of a two-level converter and a five-level converter are shown in Fig. 4, for the case of 100 to 12 V conversion. Using periodic steady-state constraint, the inductor value of a buck converter is given by

$$L_{\rm buck} = \frac{\left(1-\frac{V_{\rm out}}{V_{\rm in}}\right)V_{\rm out}}{\Delta I_L f_{\rm buck}} \tag{5}$$

where ΔI_L is the peak-to-peak inductor current ripple.

For the FCMC, the required inductance can be calculated in the same way. For large-step-down voltage conversion ratios that satisfy $\frac{V_{\rm in}}{V_{\rm out}} > N-1$, the inductance is given by

$$L_{\rm FCMC} = \frac{\left(1-\frac{V_{\rm out}(N-1)}{V_{\rm in}}\right)V_{\rm out}}{\Delta I_L f_{\rm FCMC}(N-1)} \tag{6}$$

for a specified inductor current ripple ΔI_L. As a quick check, the inductance required by the buck converter can be obtained by setting N to 2. By taking the ratio of (6) and (5), the inductance of the FCMC normalized by the inductance of the buck converter

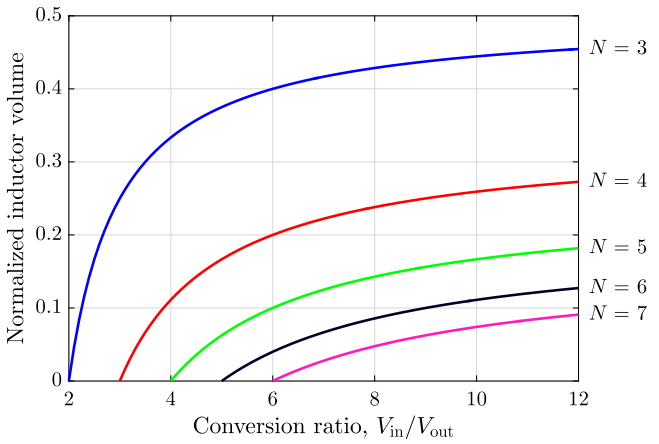

Fig. 5. Inductance required by the FCMC normalized by that required by two-level buck. N is number of levels.

can be obtained as

$$\frac{L_{\text{FCMC}}}{L_{\text{buck}}} = \underbrace{\frac{\left(1 - \frac{V_{\text{out}}(N-1)}{V_{\text{in}}}\right)}{1 - \frac{V_{\text{out}}}{V_{\text{in}}}}}_{K_d} \underbrace{\frac{1}{N-1}}_{K_f}. \tag{7}$$

It can be seen that the reduction in inductor size compared to the buck converter comes from two terms. The term K_d is due to the difference in the duty ratio of the voltage pulse seen by the inductor. The duty ratio of the switching node pulse of the FCMC is $N-1$ higher due to the step-down from the flying capacitors. The second term K_f is due to the fact that for the FCMC, the pulse frequency seen by the inductor is $(N-1)$ times the switching frequency of each switch. To visualize the difference in the required inductance, (7) is plotted in Fig. 5, in which each curve is for an FCMC with a different number of levels. It can be seen that as the conversion ratio $V_{\text{in}}/V_{\text{out}}$ approaches that of the native conversion ratio of the FCMC, $(N-1)$, the inductance required goes to zero, contributed by the term K_d. This is due to the near unity duty ratio of the switching node pulse seen by the inductor. On the other hand, as the conversion ratio increases, the effect of K_d becomes smaller, and the normalized inductance approaches a constant for each level, which is determined by K_f. Overall, the inductance required can be significantly reduced by employing the FCMC, especially if the number of levels is designed to be close to the targeted voltage conversion ratio.

The energy stored by the inductor is also calculated. Using (6) and using the parameter α_I to represent the ripple factor ($\Delta I_L = \alpha_I I_{\text{load}}$), the energy stored by the inductor is

$$\begin{aligned} E_{L,\text{FCMC}} &= \frac{1}{2} L_{\text{FCMC}} I_L^2 \\ &= \frac{1}{2}\left(1 - \frac{V_{\text{out}}(N-1)}{V_{\text{in}}}\right) \frac{P_{\text{out}}}{\alpha_I (N-1) f_{\text{FCMC}}}. \end{aligned} \tag{8}$$

Since the buck converter and the FCMC have the same inductor current magnitude, the ratio of the inductor energy is the same as the ratio of inductor values

$$\frac{E_{L,\text{FCMC}}}{E_{L,\text{buck}}} = \frac{L_{\text{FCMC}}}{L_{\text{buck}}}. \tag{9}$$

The dc conduction losses of the inductors for the FCMC and buck converter are made the same by choosing the same dc resistance for the inductors, since they have the same rms current. It should be noted that core loss and ac loss are neglected in this analysis. In reality, when core loss and ac loss are significant, the multilevel converter losses may differ somewhat, due to the increase in frequency by a factor of $(N-1)$. Appendix D investigates in detail how the core loss changes according to the inductor size and frequency scaling, and can be augmented to the main procedure if desired. In addition, while the presented method fixes conduction and switching losses, and uses the passive component volume as the comparison metric, it is by no means the only performance metric that the FCMC should be designed for. For example, the FCMC converter can be designed to have the same inductor volume and inductor loss with a lower switching frequency than the buck converter, and thus benefit from an overall higher efficiency. Therefore, the fundamental advantages of the FCMC converter is not exaggerated by excluding the ac related losses in the inductor, though the design space may be more limited.

D. Flying Capacitors

The low switch voltage ratings and small inductance are enabled by the multiple voltage levels provided by the flying capacitors. As the number of levels increases, the volume of the flying capacitors increases, and needs to be taken into account. For a multilevel converter, the energy stored by all flying capacitors can be calculated as

$$E_C = \frac{1}{2}\sum_{i}^{m} C_i V_{C,i}^2 \tag{10}$$

where C_i is the capacitance, $V_{C,i}$ is the voltage rating of the ith capacitor, and m is the total number of capacitors. For the FCMC converter, there are $N-2$ flying capacitors, and their voltage ratings are given by

$$V_{C,i} = \frac{i}{N-1} V_{\text{in}} \tag{11}$$

for the ith capacitor as labeled in Fig. 2. With the typical design choice of having equal flying capacitors ($C_i = C_1$), the total energy stored can be obtained by substituting (11) into (10)

$$E_C = \frac{(N-2)(2N-3)}{12(N-1)} C_1 V_{\text{in}}^2. \tag{12}$$

The next step is to determine the capacitor value C_1. While the capacitors have much higher energy density than inductors, it is important that the energy is utilized in the conversion process. The energy utilization of the capacitor is proportional to the voltage ripple across it. Therefore, analogous to sizing the inductor using inductor current ripple, the flying capacitor value can be obtained from the capacitor voltage ripple constraint. The flying capacitor voltages in a switching cycle are shown in Fig. 6. A larger voltage ripple allows for smaller capacitor values, but also adds to the maximum voltage rating of capacitors and switches. In this paper, capacitor voltage ripple is chosen as a fraction of the smallest capacitor voltage rating or the smallest switch voltage rating. Thus, for the FCMC converter, the

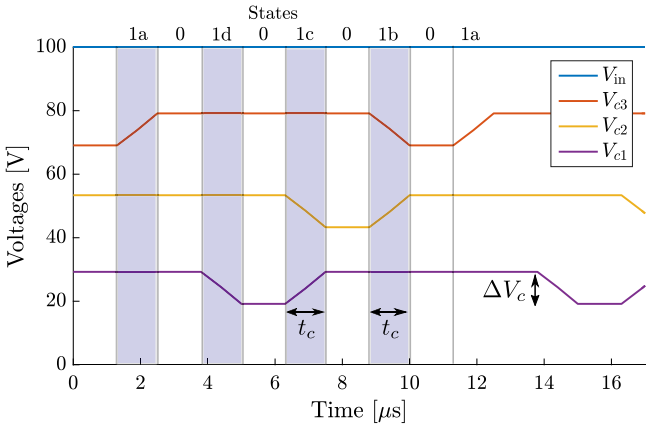

Fig. 6. Flying capacitor voltages for 100 to 12 V conversion.

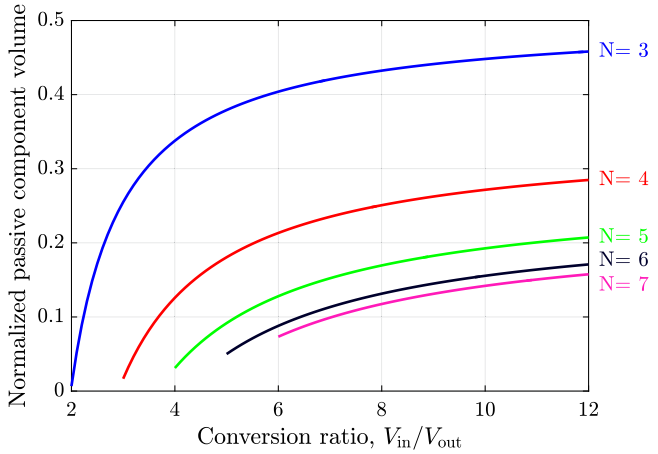

Fig. 7. Passive component volume required by the FCMC normalized by that required by two-level buck converter.

allowed peak-to-peak capacitor voltage ripple is given by

$$\Delta V_C = \alpha_V \frac{V_{\text{in}}}{N-1} \tag{13}$$

where α_V is a relative ripple factor and is less than 1. Then, the capacitance required can be calculated as

$$C_1 = \frac{\Delta Q_C}{\Delta V_C} = \frac{(N-1) I_{\text{load}}\, t_c}{\alpha_V V_{\text{in}}} \tag{14}$$

where ΔQ_C is the charge flowing into the capacitor in a charging period, I_{load} is the load current, and t_c is the duration of one capacitor charging period before it gets discharged, as annotated in Fig. 6. From Figs. 3 and 6, it can be observed that each flying capacitor is only charged in one particular state and discharged in another state. The duration of each state in Fig. 3 is proportional to the duty ratio and inversely proportional to the switching frequency, as given by

$$t_c = \frac{\frac{(N-1)V_{\text{out}}}{V_{\text{in}}}}{(N-1) f_{\text{FCMC}}}. \tag{15}$$

Thus, substituting (15) into (14) and simplifying, the required capacitance is obtained as follows:

$$C_1 = \frac{(N-1) V_{\text{out}} I_{\text{load}}}{\alpha_V V_{\text{in}}^2 f_{\text{FCMC}}}. \tag{16}$$

Substituting (16) into (12) and simplifying, we obtain the energy storage of the capacitors as

$$E_C = \frac{(N-2)(2N-3)}{12} \frac{P_{\text{out}}}{\alpha_V f_{\text{FCMC}}}. \tag{17}$$

It can be seen that the energy stored by the capacitors increases by the square of the number of levels for the FCMC converter. It also should be noted that the analysis here assumes that flying capacitors of their respective voltage rating are used. In practice, however, capacitors with a single voltage rating may be used, due to layout modularity and component availability. In this case, the volume of the capacitors is expected to be larger and the analysis can be easily modified to take into account of practical capacitor selections.

E. Combined Comparison Metric

In this section, the combined volume of passive components is investigated. It is assumed that the inductor volume is proportional to the energy stored ($1/2LI^2$), by the inductor where L is the inductance, and I is the rated (by saturation or thermal limit) current of the inductor. On the other hand, the volume of capacitors is proportional to the energy stored ($1/2CV^2$) by the capacitor, where C is the capacitance and V is the rated voltage of the capacitor. The justifications for these metrics are provided in Appendixes B and C. For simplicity, the nominal inductor current and the capacitor voltage are used in Sections III-C and III-D, which are reasonable assumptions for relatively small current and voltage ripple (α_I and α_V).

For the FCMC, the energy storage requirement for the inductor is given by (8) and the energy storage requirement for the capacitor is given by (17). By comparing (17) and (8), it can be seen that the ratio of the energy stored by the capacitor to that of the inductor only depends on the conversion ratio, the number of levels, and the percentage ripples, and is independent of the output power and switching frequency as

$$\frac{E_{C,\text{FCMC}}}{E_{L,\text{FCMC}}} = \frac{(N-1)(N-2)(2N-3)}{6\left(1-\frac{V_{\text{out}}(N-1)}{V_{\text{in}}}\right)} \times \frac{\alpha_I}{\alpha_V}. \tag{18}$$

The energy stored by the capacitors and inductors cannot be simply added together, since the energy densities of capacitors and inductors can be different by orders of magnitude. In order to compare the volume, the energy needs to be converted into a total volumetric figure of merit, as given by

$$\text{V}_{\text{tot}} = \text{V}_L + \text{V}_C = \frac{\text{E}_L}{\rho_{E,L}} + \frac{\text{E}_C}{\rho_{E,C}} \tag{19}$$

where $\rho_{E,L}$ and $\rho_{E,C}$ are the volumetric energy densities of inductors and capacitors, respectively. Therefore, the volume ratio of the FCMC and buck converters is given by

$$\begin{aligned}\frac{\text{V}_{\text{tot,FCMC}}}{\text{V}_{\text{tot,buck}}} &= \frac{\left(\frac{\text{E}_L}{\rho_{E,L}} + \frac{\text{E}_C}{\rho_{E,C}}\right)_{\text{FCMC}}}{\left(\frac{\text{E}_L}{\rho_{E,L}}\right)_{\text{buck}}} \\ &= \frac{E_{L,\text{FCMC}}}{E_{L,\text{buck}}}\left(1 + \frac{E_{C,\text{FCMC}}}{E_{L,\text{FCMC}}}\frac{\rho_{E,L}}{\rho_{E,C}}\right).\end{aligned} \tag{20}$$

By assuming an appropriate $\frac{\rho_{E,C}}{\rho_{E,L}}$ ratio, one can find the total passive component volume normalized with respect to that required by the two-level buck converter from (18) and (20). An example is provided in Fig. 7, using $\alpha_V = \alpha_I = 0.2$ and a $\frac{\rho_{E,C}}{\rho_{E,L}}$ ratio of 150, which is an average value obtained from a survey of X7R capacitors from TDK and XAL inductors from Coilcraft

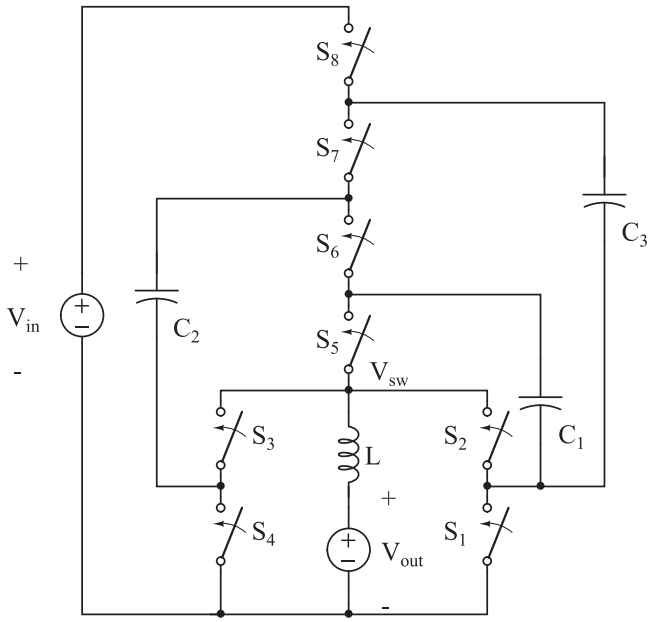

Fig. 8. Schematic drawing of a 4-to-1 soft-charging Dickson converter.

as shown in Appendix C. Comparing Figs. 5 and 7, one can observe that the increase in total volume due to the capacitors is small at lower number of levels, but at high number of levels, the capacitor size start to be comparable to the size of inductors, and further increase in the number of levels will yield minimal benefit. Therefore, the proposed method can also be used to determine the optimal number of levels of an FCMC converter for a particular application. It should be noted that the exact curves in Fig. 7 depend on the parameters used ($\alpha_I, \alpha_V, \rho_{E,L}, \rho_{E,C}$), and will change based on the actual components selected and, thus, will be different for each design. The contribution here is the development of such a general and quantitative method to aid in the evaluation and design of the multilevel converters.

IV. Generalization to Hybrid SC Converters

Another type of converters that utilize both capacitors and inductors for energy transfer is hybrid SC converters. In this section, the proposed analytical method is applied to hybrid SC converters, and a more generalized way to obtain the switch conductance and switching frequency is presented. One example of the hybrid SC converters is the soft-charging Dickson converter [30], whose schematic is shown in Fig. 8. The capacitor voltage ratings for the Dickson converter are the same as the FCMC converters, while the voltage ratings for the switches are $\frac{1}{N-1}V_{\rm in}$ (for S_1, S_2, S_3, S_4, S_5, S_8) and $\frac{2}{N-1}V_{\rm in}$ (for S_6, S_7), where $(N-1)$ is the native conversion ratio of Dickson converter. The output voltage regulation of the Dickson converter can be accomplished by alternating the switching node voltage $V_{\rm sw}$ between $\frac{1}{N-1}V_{\rm in}$ and 0 [27]. For simplicity, the corresponding switch states of a two-phase Dickson converter with regulation are shown in Table II, while the complete elimination of capacitor charge sharing losses can require the use of a four-phase operation [30], [31].

TABLE II
Switch States Corresponding to Switching Node Voltages of $\frac{V_{\rm in}}{N-1}$ and 0

$V_{\rm sw}$	S_1	S_2	S_3	S_4	S_5	S_6	S_7	S_8
$V_{\rm in}/(N-1)$	1	0	1	0	1	0	1	0
$V_{\rm in}/(N-1)$	0	1	0	1	0	1	0	1
0	1	1	1	1	0	0	0	0

An analysis following the method presented in Section II is carried out for the hybrid Dickson converter. The first step is to determine the required switch conductance such that the conduction loss of the Dickson converter is the same as that of a buck converter. The difficulty of analyzing such converters lies in the fact that multiple circuit branches conduct current to the load simultaneously, unlike in the FCMC converter, in which there is only a single current loop. Thus, a general SC analysis approach is taken, by calculating the current through the capacitors using the charge multiplier method presented in [14], with modification to take into account of the regulation operation. It should be noted that while the conduction loss of the FCMC converter can be easily related to the buck converter using the specific analysis in Section III, it can also be formally determined by the general analysis presented in this section.

A charge multiplier vector can be defined for the switches in each phase of the topology as

$$\begin{bmatrix} a_{\rm in,j} & a_{1,j} & a_{2,j} & a_{3,j} & \dots & a_{\rm out,j} \end{bmatrix} \tag{21}$$

where each element is defined as $a_{i,j} = \frac{q_{i,j}}{q_{\rm out}}$, i.e., the charge through the ith switch in the jth phase normalized by the total charge delivered to the load over the entire switching period. The first and last elements correspond to the charge delivered by the input source and the load. The total conduction loss through the switches can be calculated from the mean squared value of the currents, and is then given by

$$P_{\rm cond} = I_{\rm out}^2 \sum_{j}^{\rm phases} \frac{1}{D_j} \sum_{i}^{\rm switches} a_{i,j}^2 R_i \tag{22}$$

where D_j is the duty ratio of the jth phase, and R_i is the on-state resistance of the ith switch.

Each element of the charge multiplier vector in (21) can be found by summing the charges through the appropriate capacitors, which in turn can be found through KCL analysis [14], [17]. The conduction loss of the two-phase Dickson converter is calculated, and is found to approach (23) as N increases.

$$P_{\rm cond} = 2I_{\rm out}^2 R_1. \tag{23}$$

For simplicity, the resistance of each switch is assumed to be the same, and is R_1. Comparing (23) to that of the buck converter, we know that in order to achieve the same conduction loss, the switch conductance of the Dickson converter is given by

$$\frac{G_{\rm Dickson}}{G_{\rm buck}} = 2. \tag{24}$$

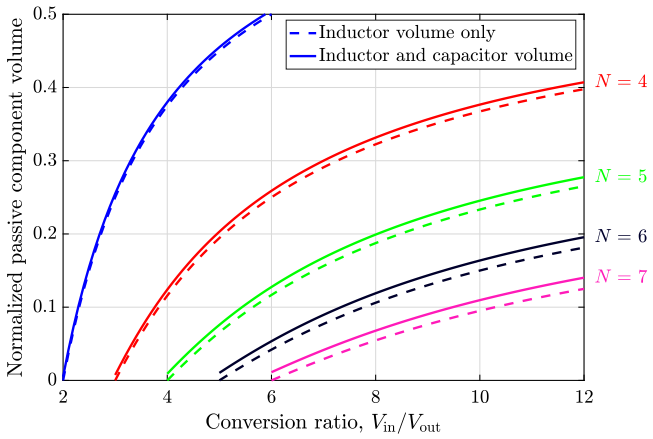

Fig. 9. Passive component volume required by the hybrid Dickson converter normalized by that required by the two-level buck converter. N is the number of levels.

The next step is to determine the switching frequency that satisfies

$$\sum (GV^2)_{\text{Dickson}} \times f_{\text{Dickson}} = \sum (GV^2)_{\text{buck}} \times f_{\text{buck}} \quad (25)$$

which can be rearranged to

$$\frac{f_{\text{Dickson}}}{f_{\text{buck}}} = \frac{G_{\text{buck}}}{G_{\text{Dickson}}} \times \frac{\sum (V^2)_{\text{buck}}}{\sum (V^2)_{\text{Dickson}}}. \quad (26)$$

With known switch conductance and voltage ratings, (26) can then be evaluated as

$$\frac{f_{\text{Dickson}}}{f_{\text{buck}}} = \frac{(N-1)^2}{4(N-1)+6}. \quad (27)$$

The energy stored by the inductors and flying capacitors of the hybrid Dickson converter can then be calculated in the same way as the FCMC converter, and only the final results are presented in this section. The overall passive component volume required by the Dickson converter normalized by that of the two-level buck converter is plotted in Fig. 9. It can be seen that similar to the FCMC converter, the Dickson converter yields significant reduction in passive component volume. However, the volume penalty introduced by the flying capacitance as the number of levels increases is much smaller compared to the FCMC, due to more efficient utilization of the capacitors, by the parallel-connected branches. It can be concluded that the Dickson converter is a better topology when the number of levels and the voltage conversion ratio are large.

It should also be noted that there are other practical aspects that influence the choice of topologies, such as the available switches and capacitors. For example, the Dickson converter has fewer number of switches at higher conversion ratios, thus requiring fewer gate drivers and level shifters. In addition, the control of the Dickson converter is simpler due to fewer number of circuit states, and the balance of flying capacitor voltages is less of an issue. On the other hand, the FCMC can provide a wide range of output (V_{in} to 0), while the Dickson converter only provides an output voltage between $\frac{V_{\text{in}}}{N-1}$ and 0.

TABLE III
COMPONENT LISTINGS

	Buck	Three-level FCMC	Hybrid Dickson
f_{sw}	200 kHz	200 kHz	250 kHz
Switches	EPC2010C × 2	EPC2001C × 4	EPC2007 × 6, EPC2015 × 4
$R_{\text{ds,on}}$	25 mΩ	7 mΩ	30 mΩ, 4 mΩ
V_{ds}	200 V	100 V	100 V, 40 V
Inductor	IHLP-8787MZ-5A	IHLP-6767GZ-11	IHLP-5050CE-01
Inductance	47 μH	22 μH	6.8 μH
I_{sat}	10.0 A	9.5 A	18 A
R_{dc}	17.3 mΩ	20.0 mΩ	19.8 mΩ
Flying capacitor value	-	4.7 μF	1.0 μF
Voltage	-	100 V × 2	250 V × 3, 100 V × 2

V. EXPERIMENTAL VERIFICATION

In order to experimentally validate the proposed analytical method, reference designs are developed, following the principles used in the analytical comparison, subjected to available part selection. Three converter prototypes are implemented: a buck converter, a three-level FCMC, and a seven-level hybrid Dickson SC converter. The detailed operation and design of the hybrid Dickson converter is presented in [30]. The converters are designed with an input voltage of 100 V and an output voltage of 12 V. An output current of 4 A has been tested without external cooling. The component listings for the converter prototypes are shown in Table III. GaN switches are used on all three prototypes for similar switch performance. A voltage rating margin of approximately 2× is chosen for the switches for all three converters. The inductor is chosen to have a dc resistance of approximately 20 mΩ so that the conduction loss is similar to that in the switches, and a current ripple of about 1.1 A. As a result, the inductor has current rating of about 10 A, while the peak load tested is only 4 A. To make a fair comparison, the capacitors are also selected with a voltage that is 2× that of the rated voltage. The converter photos are shown in Fig. 10. It should be noted that while care has been taken in the board layout to reduce the parasitics, the component placement is not optimized for a minimum overall converter size. Therefore, the volumes of individual components are compared (inductors, capacitors, and switches). This also corresponds to the comparison methodology, which does not take into account the influence on the converter size by the PCB layout.

The normalized power losses (defined as $\frac{P_{\text{in}}-P_{\text{out}}}{P_{\text{in}}}$) of the converters at the rated voltages are plotted in Fig. 11. It should be noted that according to the comparison methodology, each converter is to be designed with the same power loss, and therefore, similar power losses should be expected from all three prototypes. From Fig. 11, it can be seen that the power losses for the converters at 4 A load (where conduction loss dominates) are within 25% of each other. It should be noted that while the authors strive to follow the methodology presented here in the design of the converters, the choices in components are oftentimes limited by available parts. This partly explains the lower power loss for the Dickson SC converter at light load. Over-

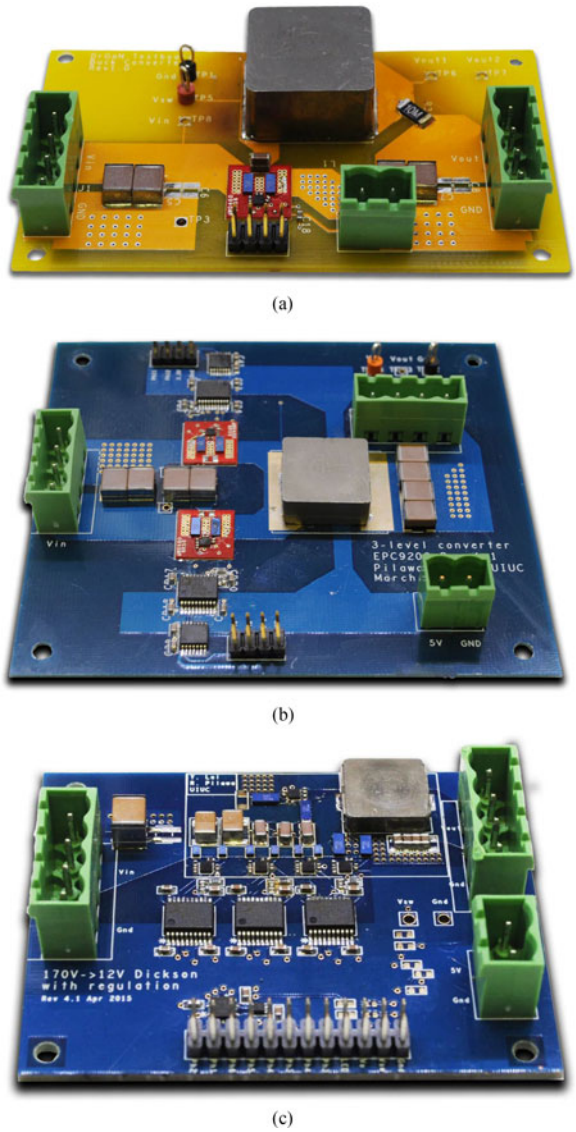

Fig. 10. Photos of converter prototypes. (a) Two-level (buck) converter. (b) Three-level FCMC. (c) Seven-level hybrid Dickson.

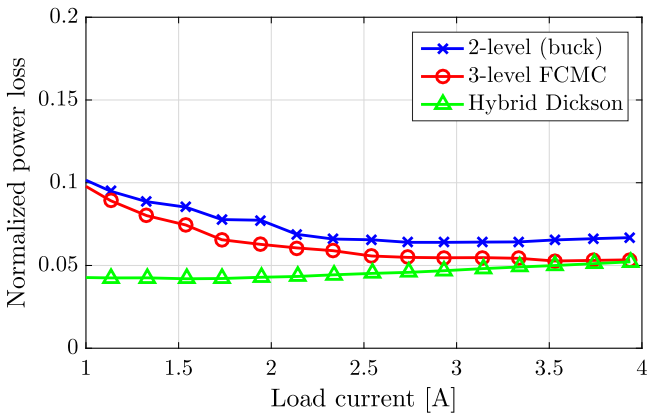

Fig. 11. Normalized power loss comparison between the buck, three-level FCMC, and hybrid Dickson converter.

TABLE IV
VOLUME COMPARISON OF PASSIVE COMPONENTS

	Two-level (buck)	Three-level FCMC	Hybrid Dickson
Inductor	6292 mm^3	2059 mm^3	596 mm^3
Capacitor	-	125 mm^3	115 mm^3
Total	6292 mm^3	2184 mm^3	711 mm^3

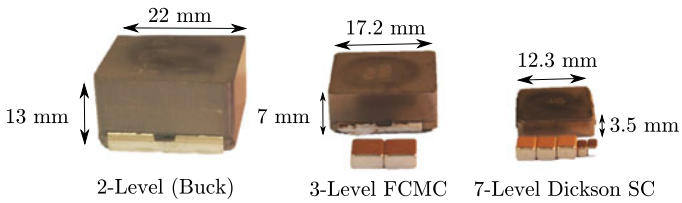

Fig. 12. Photos of inductors and flying capacitors used by the three converter prototypes.

TABLE V
AREA AND OVERALL VOLUME OF THE PROTOTYPES

	Buck	Three-level FCMC	Hybrid Dickson
Passive components (mm^2)	500	350	230
Switches and drivers (mm^2)	25	50	125
Level-shifters	-	100	300
Total area (mm^2)	525	500	655
Maximum height (mm)	13	7	3.5
Overall volume (mm^3)	6800	3500	2300

all, the power losses are close to each other, and the volume comparison can be carried out on a fair ground.

The volumes of the passive component used in the prototypes are compared in Table IV. It can be seen that the inductor size can be reduced considerably by moving to a higher number of levels, while the additional capacitor volume is only a fraction of inductor size. The overall volume is approximately reduced by a factor of three each time, as the number of levels increased from two to three, and then to seven. It should be noted that the goal of the comparison is not to conclude that the Dickson SC converter is a better topology than an FCMC, but rather to show that a topology with a higher number of levels can result in a smaller overall volume than a topology with a lower number of levels. To visualize the difference in the passive component volume, photos of the passive components for the three converters are shown in Fig. 12.

Another advantage associated with reduced inductor size is that the inductor can have a lower height, reducing the overall profile of the design. This has a large impact on the overall volume, since the switches and control circuitry are usually very thin. This advantage can offset the additional footprint of gate drivers and level shifters in the multilevel topologies. The PCB area occupied by the converters are compared in Table V, as well as the final volume of the overall converter. It can be seen that even for a relatively low-power application (50 W),

where the auxiliary circuits can occupy a large portion of the converter area, the overall converter volume can be significantly reduced with multilevel converters.

VI. Practical Issues Associated With Hybrid SC Converters

While this paper focuses on the fundamental comparison of active and passive device utilization between hybrid converters, it should be recognized that there are many practical issues that can influence the choice of topology as well. This section discusses some of the challenges and possible solutions.

A common practical challenge for the multilevel converters is the relatively large commutation loop, resulting in a large loop inductance and forcing a slow switching speed. For some topologies such as the FCMC, the commutation loop can be identified and appropriate decoupling techniques can be used to minimize the loop inductance [32], [33]. For topologies whose commutation loop is inherently large, techniques such as ZCS and ZVS need to be utilized in the resonant variant of these topologies to minimize the overlap loss [17], [34]. If the additional overlap loss is unavoidable, the analysis presented can be modified with a penalty in the switching loss calculation to account for this fact.

In many applications where the input voltage can be ramped up slowly, for example, when the converter is a second stage to a previous step-down stage (e.g., voltage regulator module, intermediate bus architectures), no additional startup circuitry is required. In other cases, however, where the input voltage is not well controlled, start-up circuitry needs to be included for the multilevel converters. One implementation is to use a top switch that is able to withstand the full input voltage while the flying capacitors charge up. The additional switch GV^2 can be included in the analysis if desired. However, the switch loss and size do not necessarily change a lot, since for large step-down applications, the top switch has small rms current and is the smallest switch. In addition, for high number of levels, the top switch is only one of the many switches. Another possible solution is to use a small start-up switch in parallel with a switch that turns on permanently after start-up, as demonstrated in [32] and [35]. This solution can have smaller loss penalty compared to the first, since there is no additional switching loss.

Another challenge is to deliver power to the floating gate drivers. In [36] and [37], modified bootstrap methods are used for FCMC converters, which are both smaller and less costly than the transformer-based isolated power supply. In [38], a monolithically integrated converter is implemented with all the auxiliary circuits on-chip, and successfully demonstrated high efficiencies across a wide operating range.

While the multilevel and hybrid SC converters add design complexity in terms of precharge, level-shifting, and control, these complexity can be addressed by the innovation of circuit designers. Addressing the complexity of multilevel and hybrid converters is an on-going research, and can in many cases be worthwhile, given the potential efficiency and power density improvement.

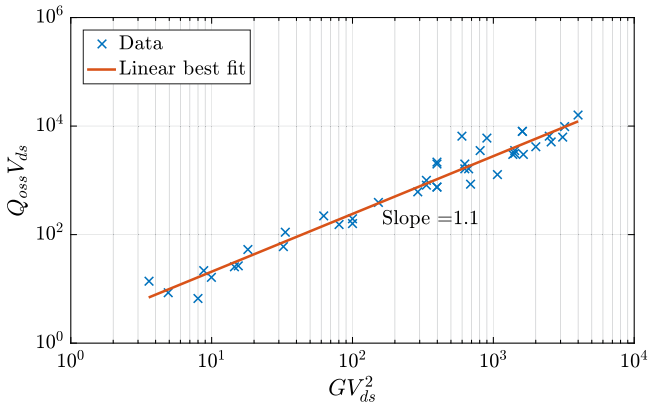

Fig. 13. Plot of capacitance switching loss metric against GV^2 product. Data obtained from EPC GaN switches.

VII. Conclusion

In this paper, an analytical method to compare different multilevel and hybrid SC converters is presented, based on the fundamental active and passive device utilization. The proposed method keep the losses of the converters the same and uses the overall passive device volume as a convenient metric to evaluate these converters. The use of multilevel converters in large step-down dc–dc conversion applications is explored. It is shown that both types of multilevel converters have significantly reduced passive component volumes, compared to two-level buck converters. The hybrid Dickson SC converter is especially suited for designs with a large number of levels due to the efficient use of flying capacitors. Three converter prototypes are implemented to support the proposed methodology. It is shown with both theoretical analysis and hardware that these multilevel converters can achieve a higher efficiency and power density than conventional buck converters.

Appendix

A. Switching Loss of Converters

There are two major sources of switching losses, the capacitance switching loss and the voltage–current overlap loss. These two losses will be investigated separately in this section.

The switching loss of a semiconductor device as a result of the drain–source capacitance is given by

$$\begin{aligned} P_{\mathrm{coss}} &\propto f_{\mathrm{sw}} C_{\mathrm{oss}} V_{\mathrm{ds}}^2 \\ &\propto f_{\mathrm{sw}} Q_{\mathrm{oss}} V_{\mathrm{ds}}. \end{aligned} \tag{28}$$

The related device parameters of GaN switches (Q_{oss}, V_{ds}, R_{ds}) are collected from EPC. The $Q_{\mathrm{oss}}V_{\mathrm{ds}}$ values (capacitance switching loss metric) are plotted against GV_{ds}^2 in Fig. 13, where G is $\frac{1}{R_{\mathrm{ds}}}$. A linear best fit line is also plotted, which has a slope of 1.06 in log–log scale. This means that GV_{ds}^2 is linearly proportional to $Q_{\mathrm{oss}}V_{\mathrm{ds}}$, and that it is a good indication of the switching loss as a result from output capacitance discharge.

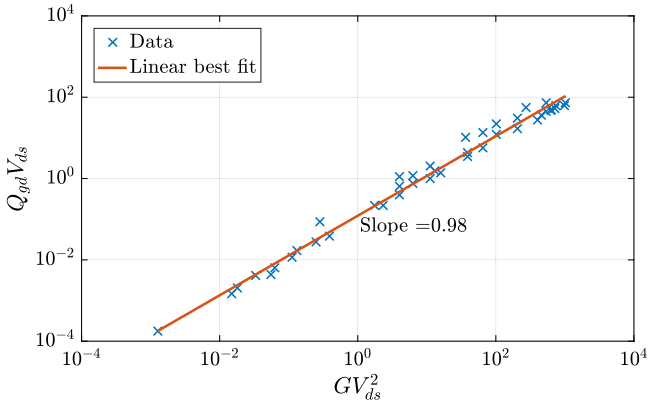

Fig. 14. Plot of overlap switching loss metric against GV^2 product. Data obtained from EPC GaN switches.

The switching loss of a semiconductor switch due to the voltage–current overlap during transition is given by

$$P_{\text{overlap}} \propto \sum^{\text{switches}} f_{\text{sw}} V_{\text{ds}} I_{\text{ds}} t_{\text{tr}} \tag{29}$$

where $V_{\text{ds}} I_{\text{ds}}$ is the power dissipation during the transition and t_{tr} is the duration of the switch transition (commutation). Traditionally, t_{tr} is assumed to be proportional to Q_{gd}, since the gate-to-drain charge determines how fast the switch can be turned ON. Provided that I_{ds} of the switches are the same across the topologies, $Q_{\text{gd}} V_{\text{ds}}$ can be used as metric to compare the overlap switching loss. The $Q_{\text{gd}} V_{\text{ds}}$ values against the GV_{ds}^2 product are plotted in Fig. 14. The linear best fit line has a slope of 0.96 in log scale. This shows that GV_{ds}^2 is linear with respect to $Q_{\text{gd}} V_{\text{ds}}$, and thus a good representation of the overlap switching loss. This assumption that I_{ds} is the same for all switches is true for FCMC, but may not be true for a general hybrid SC topology. Therefore, a more accurate representation of the switching loss is $GV_{\text{ds}}^2 I_{\text{ds}}$, but is omitted in this paper for simplicity.

In practice, especially for the fast GaN devices, the commutation time t_{tr} is likely limited by the allowable voltage ringing during the switch transition, which depends on the parasitic inductance in the commutation loop, but not Q_{gd}. As a result, Q_{gd} may have limited influence on the switching loss. Therefore, in practice, a suitable metric for the switching loss is $V_{\text{ds}} I_{\text{ds}}$, assuming that t_{tr} is a constant value determined by the layout inductance. For the FCMC, there are $2(N-1)$ switches with voltage rating of $\frac{V_{\text{in}}}{N-1}$ and current rating of I_{load}. Thus, we have

$$\frac{\sum (VI)_{\text{FCMC}}}{\sum (VI)_{\text{buck}}} = \frac{2(N-1) \times \frac{V_{\text{in}}}{N-1} I_{\text{load}}}{2 \times V_{\text{in}} I_{\text{load}}} = 1 \tag{30}$$

which is the same result given by (3).

Suitable metrics for switching losses are summarized in Table VI. For simplicity, the sum of GV_{ds}^2 products are used as the overalls switching loss metric since it is a good indication of the capacitance switching loss and also partly reflects the overlap switching loss.

TABLE VI
SUITABLE METRICS FOR SWITCHING LOSSES

Switching loss	Metric
Capacitance loss	GV_{ds}^2
Overlap loss (limited by Q_{gd}, same I_{ds})	GV_{ds}^2
Overlap loss (limited by Q_{gd})	$GV_{\text{ds}}^2 I_{\text{ds}}$
Overlap loss (limited by loop inductance)	$V_{\text{ds}} I_{\text{ds}}$

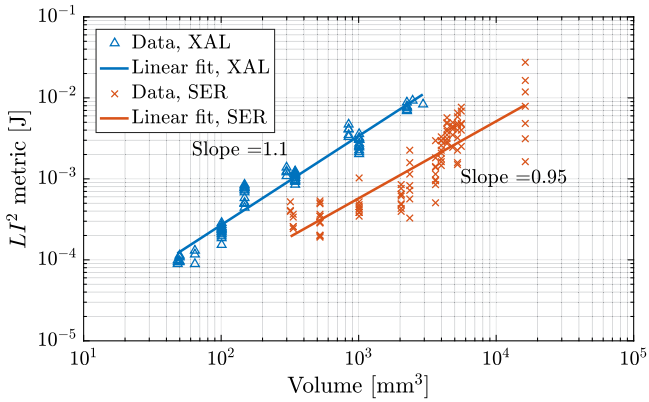

Fig. 15. Plot of LI^2 product against the inductor volumes. Data are obtained from Coilcraft inductors.

B. Inductor Volume Metric

The value of an inductor is given by

$$L = \frac{\mu n^2 A_c}{l_m} \tag{31}$$

where μ is the permeability, n is the number of turns, A_c is the cross-sectional area of the core, and l_m is the mean length of the magnetic path. The saturation current of an inductor is given by

$$I_{\text{sat}} = \frac{B_{\text{sat}} l_m}{\mu n} \tag{32}$$

where B_{sat} is the saturation flux density. From (31) and (32), we obtain the expression for the LI^2 product of the inductor as

$$LI_{\text{sat}}^2 = \frac{B_{\text{sat}}^2 A_c l_m}{\mu}. \tag{33}$$

For a given core material and configuration, B_{sat} and μ are constant, and therefore, the LI^2 product is proportional to the volume of the core $A_c l_m$, which in turn is proportional to the volume of the inductor. It should be noted that here it is assumed that the size of the inductor is constrained by saturation, not by the core loss, which is often the case for the filter inductors used in PWM converters.

In order to validate the expression, the parameters of surface-mount inductors from the Coilcraft XAL and SER families are collected. The volumes of these inductors are plotted against their LI^2 product in Fig. 15, where I is taken as the saturation current. The linear best fit line for the XAL series has a slope of 1.1, while the best fit line for the SER inductors has a slope of

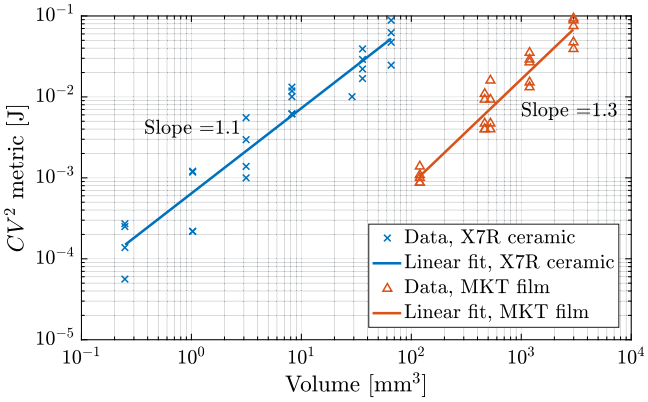

Fig. 16. Plot CV^2 product against the capacitor volumes. Data are obtained from TDK capacitors.

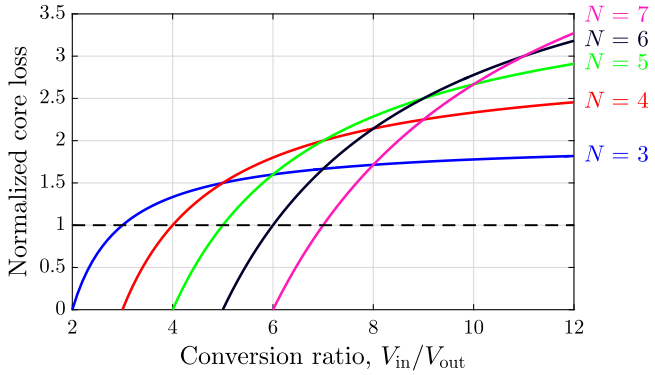

Fig. 17. Core loss of the FCMC inductor normalized by that of the buck converter. $(N-1)$ is the number of levels.

0.95. This suggests that the LI^2 product can be a good indication of the volume of an inductor.

The following series of inductors is used in the plots: Coilcraft XAL4030, XAL4040, XAL5020, XAL5030, XAL5050, XAL7030, XAL7070, XAL1010, XAL1350, XAL1510, XAL1513; Coilcraft SER1360, SER1390, SER1408, SER1410, SER8050, SER8052, SER2915L.

C. Capacitor Volume Metric

The parameters of TDK multilayer ceramic capacitor X7R series as well as its metal film capacitor MKT series are collected. The volumes are plotted against CV^2 product in Fig. 16. The slope of the linear best fit line is 1.1 for the X7R capacitors and the slope for the MKT capacitors is 1.3. Comparing Figs. 15 and 16, it can be seen that the X7R capacitors have on average 150 smaller volume for the same amount of energy stored than the XAL inductors.

The following series of capacitors is used in the plots (not all parts in a series are used). MKT capacitors: TDK B32529, B32520, B32521, B32522, B32523; Ceramic capacitors: TDK X7R capacitors with case size 0402, 0603, 0805, 1206, 1812, 2220, each with voltage ratings at 16, 25, 35, 50, 100, 250, 630, and 1000 V where applicable.

D. Inductor Core Loss Consideration

The proposed analytical framework neglects the core loss and ac loss. This section explores the scaling of these losses as the inductor size changes. A common empirical core loss formula is the Steinmetz equation [39] given by

$$P_{\text{core}} = \alpha f^{\gamma} \Delta B^{\beta} A_c l_m \tag{34}$$

where P_{core} is the core loss, α is a constant for each core material, γ is the exponent that reflects the frequency-dependent behavior, β reflects the flux swing-dependent behavior of the core loss, and $A_c l_m$ is proportional to the volume of the core. β usually has a range of 2–3, while γ has a range of 1–3. For multilevel converters, while the core loss density increases due to the increase in the ripple frequency as in the comparison method, the volume of the core decreases as A_c decreases (due to the reduction in the required inductance). Thus, whether the overall core loss increase or decrease compared to buck converters depends on the exponent γ.

For multilevel converters in general, we have

$$P_{\text{core,ml}} = \alpha f_{ml}^{\gamma} \Delta B^{\beta} A_{c,ml} l_m \tag{35}$$

$$= \alpha \left(\frac{f_{\text{buck}}}{K_f} \right)^{\gamma} \Delta B^{\beta} (K_f K_d A_{c,\text{buck}}) l_m \tag{36}$$

$$= P_{\text{core,buck}} \frac{K_d}{K_f^{\gamma-1}} \tag{37}$$

where K_f and K_d are as defined in (7). For the FCMC, the core loss normalized by that of a buck converter (i.e., $\frac{K_d}{K_f^{\gamma-1}}$) is plotted in Fig. 17, by assuming a γ of 2. It can be seen that when the desired conversion ratio is close to $N-1$, i.e., when K_d factor is dominating, the core loss for the FCMC is smaller. When the desired conversion ratio is much larger than $N-1$, i.e., when K_f factor is dominating, the core loss for the FCMC can be larger than that of the buck converter. It should be noted that the scaling strongly depends on the value of γ. A γ value of 1 means that the core loss for the FCMC is always smaller, and a γ value of 3 can result in a core loss that is much higher than plotted in Fig. 17. It should be noted here that a more accurate core loss frequency scaling can be obtained using the modified Steinmetz equation [40], which takes into account of the triangular inductor current waveform at different duty ratios. The core loss for multilevel converter is expected to be lower than given by the Steinmetz equation, since its duty ratio is closer to 0.5. In addition, a more rigorous inductor loss scaling is given in [41].

The core loss, ac loss, and dc loss of selected inductors from Vishay IHLP family, evaluated at the same current ripple, are obtained from the manufacturer's website and are shown in Table VII. The operating condition is 100 to 12 V conversion with an average load current of 8 A. Smaller inductors are chosen for the FCMC converter with higher number of levels according to Fig. 5. It can be seen that the core loss (and the total loss) actually decreases as the number of levels increases, despite operating at a higher frequency.

Therefore, while including the core loss in the analysis can yield more accurate, omitting core loss does not necessarily yield a biased analysis favoring the multilevel converters.

TABLE VII
LOSS SCALING OF SELECTED VISHAY INDUCTORS

FCMC	Part No.	Inductance	Ripple Frequency	I_{sat}	ΔI_L	Core loss (W)	AC loss	DC loss	Total loss	Volume
Two-level	IHLP-6767GZ-01	22 μH	100 kHz	23 A	4.8 A	1.04 W	2.06 W	1.85 W	4.95 W	2140 mm^3
Three-level	IHLP-6767DZ-01	10 μH	200 kHz	19.5 A	4.6 A	0.80 W	2.28 W	1.80 W	4.89 W	1160 mm^3
Four-level	IHLP-5050CE-01	5.6 μH	300 kHz	19 A	4.6 A	0.76 W	1.56 W	1.26 W	3.58 W	592 mm^3
Five-level	IHLP-4040DZ-01	3.3 μH	400 kHz	18.6 A	4.73 A	0.66 W	1.43 W	0.93 W	3.03 W	474 mm^3
Six-level	IHLP-3232DZ-01	2.2 μH	500 kHz	23 A	4.4 A	0.48 W	0.34 W	1.48 W	2.30 W	290 mm^3

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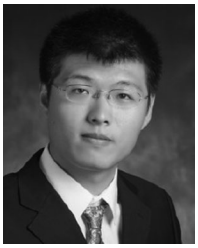

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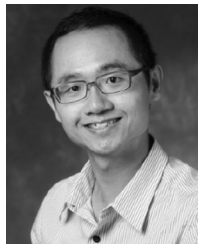

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