Letters

A Modified DPC Switching Technique Based on Optimal Transition Route for of 3L-NPC Converters

Hany A. Hamed, Ahmed F. Abdou, Mohamed Shawky El Moursi, and E. E. EL-Kholy

***Abstract*—This letter presents a modified switching technique for a three-level neutral-point-clamped converters controlled by direct power control (DPC). The proposed switching technique avoids the hard state transition of each phase module as well as reduces the overall switching frequency. For any phase module, it inserts sequence of vectors to avoid the direct transition from positive to negative state and vice versa. The proposed vector sequence is called optimal transition route (OTR). The OTR technique optimizes the route between the present and the next requested vector to avoid the hard transition of any module. The proposed technique not only avoids the risk of damaging the semiconductor switches, but also minimizes the switching frequency resulted in reducing the switching losses. As a result, the reliability and the overall efficiency of the converter is increased. The obtained results confirm its applicability for medium- and high-power grid-connected converters controlled by the DPC method.**

***Index Terms*—Direct power control (DPC), forbidden transitions, switching reduction.**

I. Introduction

THE multilevel converters have been intensively used in grid-connected converters with various control methods such as a vector control (VC), direct power control (DPC), and predictive DPC [1]. The DPC technique has received a wide interest due to its simplicity and very fast power dynamic response. Although the advantages offered by DPC, it has many drawbacks that are addressed in the literature [2], [3]. The disadvantages of DPC have been addressed widely due to its undefined switching frequency. One of the disadvantages of the DPC strategy is the variable switching frequency, which is resolved by introducing a hybrid method DPC-space-vector-modulation (SVM) and model predictive control [4]. However, the proposed techniques alter the genuine of the DPC structure by introducing two PI controllers for inner very current loops as a result, it became analogous to the vector control strategy [5]. Another technique to minimize the switching frequency is called P-DPC has been introduced in [6] and [7]. In this approach, two or three vectors are introduced in time sequence before generating the selected vector via the lookup table based on an objective function for minimizing the power fluctuation [8]. However, the P-DPC control method can be affected by improper selection of the voltage sequence that is tackled by redesigning the lookup table [9]. All former DPC control methods select the required converter vector arbitrarily regardless the present vector position. This could lead to a so-called forbidden vector transition. The forbidden vector transition can be defined as the unsafe transition from present vector to next vector that results in changing the state of any converter phase module directly from "P-state" to "N-state" and vice versa without introducing a zero state or what is called O-state. Changing the phase module state from P-state to N-state and vice versa could lead to power jumps, excessive switching losses and the possibility of catastrophic failure of the semiconductor devices due to a momentary shoot-through short circuit [10], [11]. Yet, as best known by authors, the forbidden transitions have been ignored in most of DPC control strategies [1], [12]. This issue was realized in [13] for two-level pulsewidth modulation (PWM) converters in which a zero vector is forced for one sample before producing the next vector.

In this letter, a novel approach to avoid the forbidden transitions is introduced. The proposed technique also reduces the switching frequency. The letter is organized as follows; Section II introduces the DPC method for the three-level neutral-point-clamped (3L-NPC) converter topology. The proposed control method is introduced in Section III. The validation of the proposed method is introduced in Section IV.

II. Direct Power Control for 3L-NPC Converters

The conventional DPC method depends on a direct selection of the converter vector using a predefined lookup table to instantaneously control the active and reactive powers of the converter while maintaining the dc-link voltage at its target value. The conventional DPC scheme utilizes the grid angle and the error in measured active and reactive powers to produce the switching

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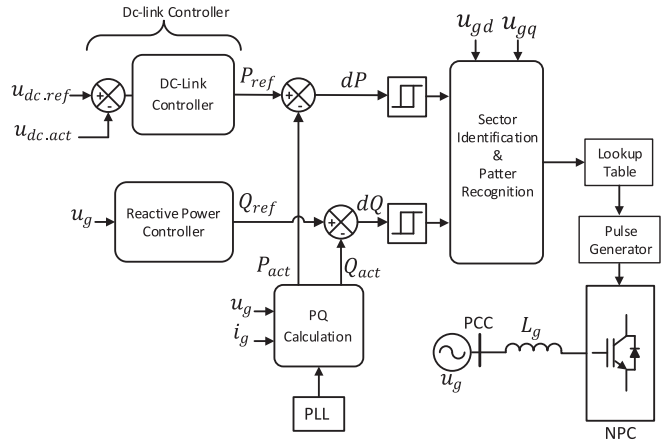

Fig. 1. DPC control scheme for the 3L-NPC converter.

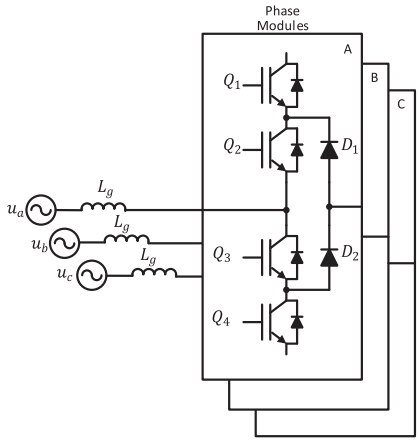

Fig. 2. Phase modules configuration of the 3L-NPC converter.

pulses for the power section module of the 3L-NPC converter as shown in Fig. 1. Mathematically, the instantaneous power is calculated in the synchronous frame as follows:

$$\begin{cases} P_g = \frac{3}{2}(u_d i_d + u_q i_q) \\ Q_g = \frac{3}{2}(u_q i_d - u_d i_q) \end{cases} \tag{1}$$

The DPC controller selects at each control sample of specific converter vector u_k to control the converter power and to regulate the dc-link voltage [14]. The relation between the converter vector, grid vector and converter power change can be expressed as follows:

$$\begin{cases} \frac{dP}{dt} = \frac{1.5}{L_g}\left[u_{gd}^2 - u_{gd}u_k \cos(\theta_g - \theta_k)\right] \\ \frac{dQ}{dt} = \frac{1.5}{L_g} u_{gd} u_k \sin(\theta_g - \theta_k) \end{cases} \tag{2}$$

where L_g is the equivalent upstream inductance, u_{gd} is the d-axis component of grid voltage vector, u_k is the converter voltage vector, and '$\theta_g - \theta_k$' is the relative angle between grid and converter voltage vectors.

According (2), the P and Q rate of change is defined by the amplitude of the converter voltage vector and its angle relative to the grid vector angle. By examining all converter vectors influence, the switching table can be constructed. The selection of the proper converter vector depends on the required active and reactive powers. Using a hysteresis compactor technique to directly produce next vector does not take into consideration the present vector state that could lead to fall into a forbidden transition. This control technique results in variable switching frequency in the worst case equal to the sampling frequency of the control loop. The hysteresis comparators can be presented as follows:

$$h_p = \begin{cases} 1 & dP > H_P \\ -1 & dP < -H_P \end{cases} \tag{3}$$

$$h_q = \begin{cases} 1 & 0 \le dQ < H_Q \\ 2 & dQ \ge H_Q \\ -1 & 0 > dQ \ge -H_Q \\ -2 & dQ < -H_Q \end{cases} \tag{4}$$

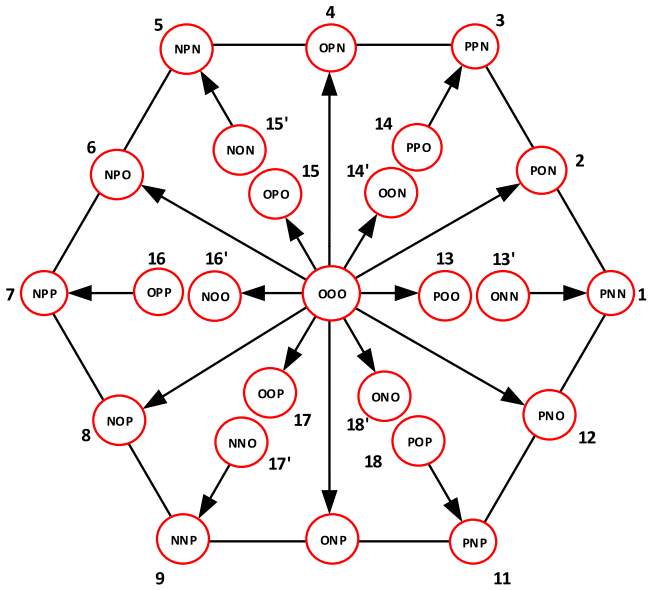

Fig. 3. Space vectors for 3L-NPC.

where H_P and H_Q are the hysteresis bands for the active and reactive power, respectively. The other parameter to select the next vector from the lookup table is the sector of the present voltage vector. The hexagonal space vector is divided to 12 sectors as expressed in the following relation:

$$(n-1) \times \pi/6 \le \theta_n < n \times \pi/6. \tag{5}$$

Depending on the grid vector angle, the corresponding sector can be calculated from

$$\text{Sector} = \text{floor}\left(\theta_g / \frac{\pi}{6}\right) + 1 \tag{6}$$

The 3L-NPC converter can be realized as three identical IGBT phase modules as shown in Fig. 2. The 3L-NPC topology offers a wide degree of freedom for selecting the proper vector as it has 27 vectors as shown in Fig. 3. Depending on the grid vector location and power errors, the suitable converter vector is selected to fulfill the control requirements.

The conventional DPC suffers from several issues such as, uncontrolled switching frequency, high computational load, and complexity introduced by various switching tables [1]. One of

the nonreported drawbacks of the DPC method is the uncontrolled phase module state transition because there is no restriction for selecting the next vector in relation with the current one. This issue is not existing in PWM or SVM methods as a zero vector always inserted in between any two active transitions. Ignoring the forbidden transition could reduce the lifetime of the semiconductor switches and increase the converter losses. To demonstrate one case for a forbidden switching, a transition from u_2 vector to u_9 vector is assumed referring to Fig. 3. This transition requires the three modules to change their states from PON to NNP. This implies that phase module "A" will change its state from P-state to N-state (forbidden), phase "B" module will change its state from O-state to N-state (allowed) and phase "C" module will change its state from N-state to P-state (forbidden). Ideally, transitions will occur instantaneously without a shooting-through problem. However, practically, each switch cannot change its state instantaneously as the IGBT characteristic will not allow for that as in average, the IGBT took longer time to switch OFF than the time taken to switch ON. A typical switching OFF delay time for power IGBT in average could reach to 1.7 μs, while the turn ON delay is much shorter in average of 0.35 μs. In the case of DPC, the next vector is arbitrarily selected. The optimum transition is to select force the next state for each phase module to be "O-state" if a forbidden transition is detected. The optimum transition analysis of each phase module will be introduced and analyzed in next section.

III. Proposed Optimal Transition Routing Concept Based on Forbidden Transition Realization

The proposed approach to safely drive the power modules relies on inserting number of vectors to avoid the forbidden transitions. To illustrate the idea, all allowed transitions are shown in Fig. 4. The proposed control strategy first analyzes the present and the next requested vector, then define the optimum vectors to be inserted in between. This process is called optimum transition route (OTR). The proposed DPC-control-method-based OTR (OTR-DPC) is shown in Fig. 5.

Many routes can be formed for different objectives such as obtaining smooth active and reactive power variations or performing neutral point balancing control. In the proposed design, only the forbidden transition is avoided. The OTR algorithm flow chart is shown in Fig. 6. The proposed algorithm identifies the next vector, and then, optimizes the route by inserting three vectors within the three consecutive samples T_s. The next three vectors are applied for $3xT_s$ samples, and then, the final vector is applied in $1xT_s$ sample. The DPC calculate the next vector with sampling rate equal to $5xT_s$. If no forbidden transition is detected, the OTR algorithm will produce the next vector for $4xT_s$ samples. This will reduce the switching frequency, and consequently, the switching losses. To demonstrate the OTR mechanism, next section will introduce a transition case where the present vector is u_2 and the next requested vector is u_9.

A. Example for OTR With a Forbidden Transition

The following example is given to demonstrate the proposed OTR method. Suppose the present vector is vector u_2 and the

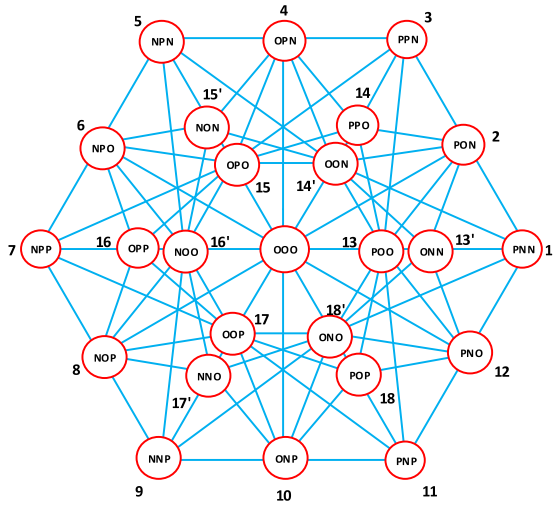

Fig. 4. Allowed vector transitions.

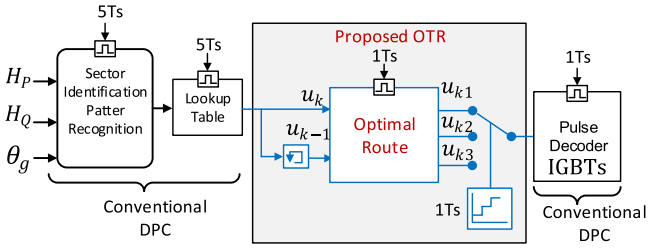

Fig. 5. Proposed OTR-DPC control diagram.

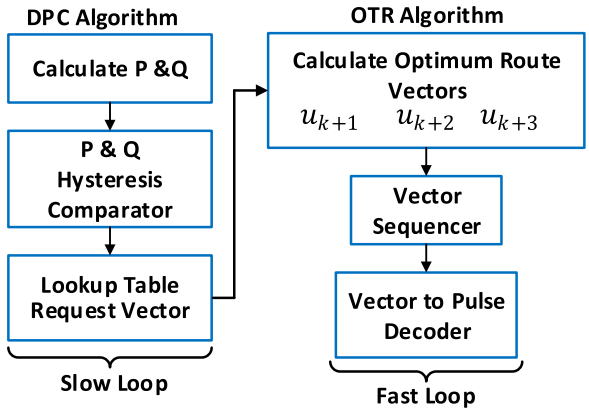

Fig. 6. OTR flow chart.

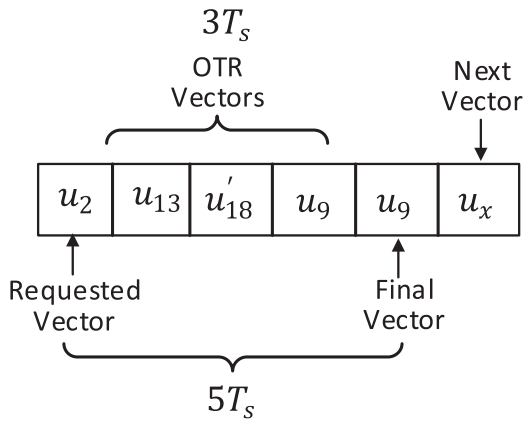

Fig. 7. Optimum transient route from u_2 to u_9.

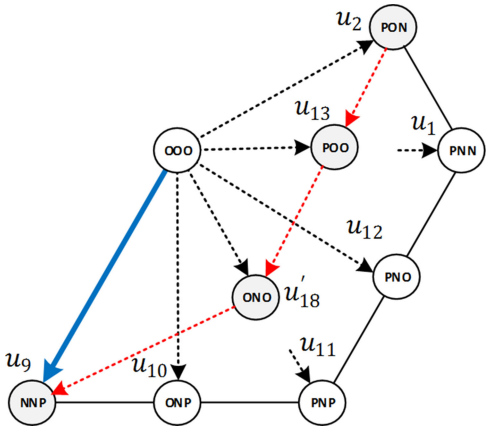

Fig. 8. Optimum transient route from u_2 to u_9.

next vector is u_9. According to the OTR algorithm and refereeing to Fig. 4, the OTR detects a forbidden transition as module A and C has to changes its state from P-state to N-state and vice versa, respectively. The OTR controller optimizes the route from u_2 to u_9 as shown in Fig. 7. The OTR uses three samples to perform the optimum routing. The detailed route transition form u_2 to u_9 is shown in Fig. 8.

IV. Proposed Technique Evaluation

The DPC system shown in Fig. 1 is simulated using MATLAB/Simulink. The objective is to evaluate the effectiveness of the proposed OTR-DPC technique in comparison with the conventional DPC. The system is initially loaded with 80% at constant nominal dc link. The switching counts for each IGBT is taken as a key performance index.

A. Converter Terminal Voltage Evaluation and Switching Counts

The converter terminal phase voltage with the conventional DPC and OTR-DPC is shown in Fig. 9(a) and (b), respectively. The OTR-DPC shows lower switching compared to the other two methods.

The total switching counts of the four IGBTs in phase "A" power module for one fundamental period (20 ms) from $\mathrm{t} = 0.2\,\mathrm{to}\,0.22$ is shown in Fig. 10. In comparison with the conventional DPC and VC-PWM, OTR-DPC has the lowest switching counts. The switching counts is reduced by average of 63% with the proposed OTR-DPC.

B. Active Power and DC-Link Steady-State Evaluation

The OTR-DPC active power and dc-link performances are evaluated as shown in Figs. 11 and 12. The active power response of the conventional DPC is shown in Fig. 11(a). The active power fluctuation is naturally increased due to lowering the switching frequency as shown in Fig. 11(b). The dc-link response is shown in Fig. 12. The dc-link of the conventional DPC is shown in Fig. 12(a). The dc-link fluctuation using the OTR technique is kept within the permissible limit as shown in Fig. 12(b). As the dc link is constant, the delivered power to load behave the same.

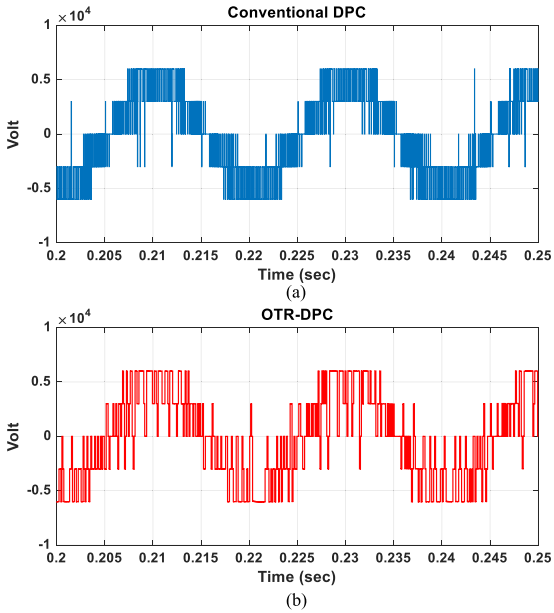

Fig. 9. Converter terminal voltage with different control techniques. (a) Conventional DPC. (b) Proposed OTR-DPC.

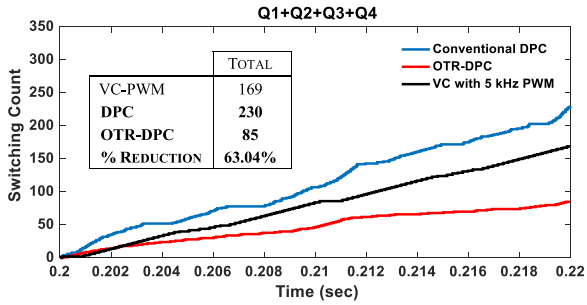

Fig. 10. Switching counts for Phase "*A*" module in one fundamental period.

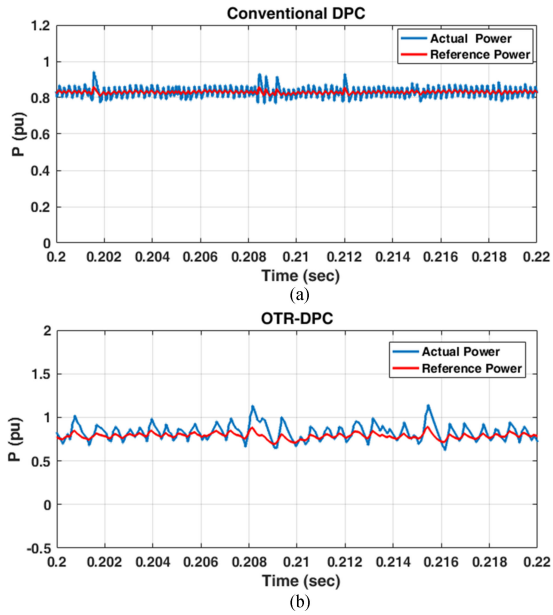

Fig. 11. Active power. (a) Conventional DPC. (b) OTR-DPC.

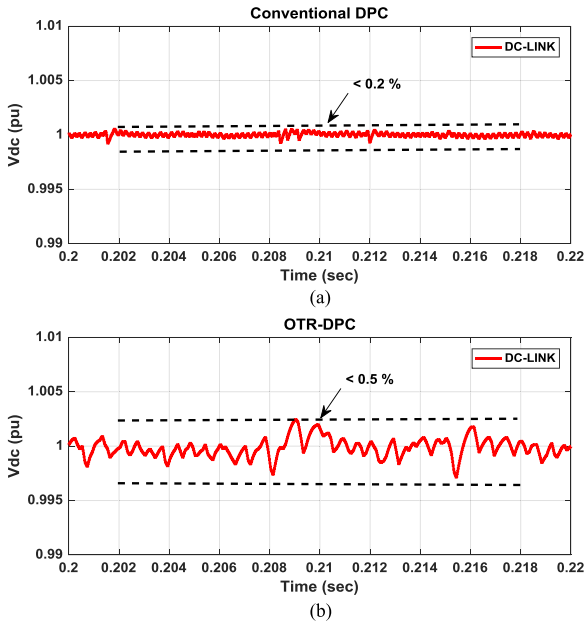

Fig. 12. DC-link regulation. (a) Conventional DPC. (b) OTR-DPC.

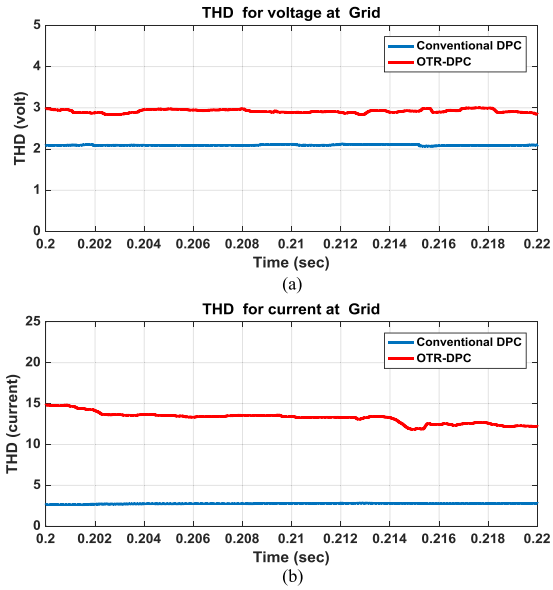

Fig. 13. THD at grid side. (a) Voltage THD. (b) Current THD.

C. Voltage and Current Total Harmonic Distortion (THD)

The THD at grid terminal is shown in Fig. 13(a) and (b), respectively. The voltage THD of OTR-DPC is below 5%, which meet the grid code specified by IEC-61000 standard [15]. Further reduction of THD can be obtained by increasing the line reactor percentage. However, increasing the reactor value will result in reducing the converter terminal voltage that may result in improper operation during sudden loading.

V. Conclusion

In this letter, a new DPC switching strategy is introduced. The proposed OTR-DPC selects the optimum vectors route to avoid the risky forbidden transitions. The OTR technique protects the converter switches from shooting through and also reduces the switching frequency and increases the overall converter efficiency. The OTR technique has effectively introduced a series of well-defined vectors, which resulted in a safe operation of converter semiconductor switches. The proposed OTR-DPC preserves the genuine structure of the conventional DPC that ensures fast response for power control. The reduction in switching frequency increased the voltage and current THD, however, the obtained voltage THD at grid side is still below the permissible limits. The switching frequency can be further reduced by introducing more vectors in the optimum route but at the expense of dc-link and power signals quality. The obtained results highlight the effectiveness of the proposed technique and demonstrate its applicability for medium grid-connected converters driven by the DPC method.

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