A Gate Driver of SiC MOSFET for Suppressing the Negative Voltage Spikes in a Bridge Circuit

Feng Gao, *Member, IEEE*, Qi Zhou, Panrui Wang, and Chenghui Zhang, *Member, IEEE*

***Abstract*—SiC MOSFET has low on-state resistance and can work on high switching frequency, high voltage, and some other tough conditions with less temperature drift, which could provide the significant improvement of power density in power converters. However, for the bridge circuit in an actual converter, high *dv/dt* during fast switching transient of one MOSFET will amplify the negative influence of parasitic components and produce the significant negative voltage spikes on the complementary MOSFET, which will threaten its safe operation. This paper proposes a new gate driver circuit for SiC MOSFET to attenuate the negative voltage spikes in a bridge circuit. The proposed gate driver adopts a simple voltage dividing circuit to generate a negative gate-source voltage as traditional and a passive triggered transistor with a series-connected capacitor to suppress the negative voltage spikes, which could satisfy the stringent requirements of fast switching SiC MOSFETs under the high dc voltage condition with low cost and less complexity. An analysis is presented in this paper based on the simulation and experimental results with the performance comparison evaluated.**

***Index Terms*—Auxiliary transistor, bridge configuration, gate driver, SiC MOSFET.**

I. Introduction

SILICON-BASED technology has to some extent reached its physical limits for power handling and switching frequency capability. To meet the application demands of high power density, high switching frequency, and high operational temperature, wide bandgap devices have become the important alternatives because of their unique characteristics and better performances [1]–[3]. As the promising wide bandgap device, Silicon Carbide (SiC) MOSFET is an excellent alternative of Si IGBT for high power converters [4]–[6]. However, high switching speed may amplify the negative influence of parasitic components and produce the large gate-source voltage spikes during switching transients [7], [8]. Besides, compared to Si MOSFETs, the SiC MOSFETs can withstand the smaller negative gate-source voltage [9], [10], which put forward the strict requirements for gate driver's design. Taking the commercial product of CREE's SiC MOSFET for example, the minimum allowable negative gate-source voltage of the first generation CREE's typical 1.2-kV SiC MOSFET CMF20120D is only –5 V. The second generation CREE's typical 1.2-kV SiC MOSFET C2M0040120D has significant improvement, but its negative gate-source voltage still cannot exceed –10 V [11], [12].

In practice, the bridge configuration is a kind of commonly used converter, where turning-on and turning-off of one switching device will generate the gate-source voltage spikes on its complementary device especially under the high switching speed condition due to the unavoidable crosstalk phenomena. In principle, gate impedance control and gate voltage control are two basic ideas assumed for crosstalk suppression [13]. In specific, gate impedance control is to make the gate impedance of one switch become smaller during the switching transient of its complementary, whose simple realization method is to add a capacitor between gate and source of SiC MOSFET [14], [15]. Such approach is simple and effective but will unavoidably increase the switching losses due to the decreased switching speed. Ishikawa *et al.* [16] proposed to use the actively controlled gate resistance to reduce switching spikes, which however needs to make a feedback control and consequently results in a relative small time delay.

On the other hand, the gate voltage control is to provide a negative gate-source voltage when the positive gate voltage spikes occur. Wang and Chung [17] designed a level-shift circuit without using any extra voltage source, which could generate the negative gate voltage to lower down the positive gate voltage spikes and speed up the switching OFF operation. However, the negative gate voltage brings the risk for damaging the devices when the negative gate-source spikes exceed the minimum allowable negative biased gate voltage. Zushi *et al.* [18] provided another method to eliminate the positive gate voltage spikes by controlling an auxiliary transistor without slowing down the switching speed of SiC JFET, but it cannot eliminate the negative voltage spikes. So it is suitable for SiC JFET because its minimum allowed negative gate-source voltage is –25 V. The combined method proposed in reference [19] can eliminate both positive and negative spikes, which makes the gate impedance become small during the switching transient and uses an additional voltage source to provide the negative gate voltage. However, the auxiliary actively controlled transistors and the

Manuscript received April 6, 2016; revised August 30, 2016 and November 30, 2016; accepted March 21, 2017. Date of publication April 12, 2017; date of current version December 1, 2017. This work was supported by the Tang Scholar Program of Shandong University. This paper was presented in part at the *Applied Power Electronics Conference*, Long Beach, CA, USA, March 20–24, 2016. Recommended for publication by Associate Editor K. Sheng. *(Corresponding author: Qi Zhou.)*

F. Gao and P. Wang are with the Key Lab of Power System Intelligent Dispatch and Control, Shandong University, Jinan 250061, China (e-mail: fgao@sdu.edu.cn; 18366111228@163.com).

Q. Zhou is with the Jiangsu Electric Power Company Research Institute, Nanjing 211103, China (e-mail: dianqizhouqi@163.com).

C. Zhang is with the School of Control Science and Engineering, Shandong University, Jinan 250061, China (e-mail: zchui@sdu.edu.cn).

Color versions of one or more of the figures in this paper are available online at http://ieeexplore.ieee.org.

Digital Object Identifier 10.1109/TPEL.2017.2690938

additional voltage source will unavoidably increase the circuit complexity and cost. Zhou *et al.* [20] assumed the level shift circuit to generate the negative gate-source voltage and added a passively controlled part to eliminate the negative gate-source voltage spikes, which however is still a little bit complex and will decrease the turning-off switching speed. Some resonant gate drivers were also proposed for high switching frequency applications to reduce its power consumption [21], [22], but the topologies are usually complex and the undesired triggering may occur in cases of high-voltage applications. This paper proposes a gate driver of SiC MOSFET for achieving better performance on eliminating the negative gate-source voltage spikes, which adopts a traditional voltage dividing circuit to generate a negative gate-source voltage and a passive triggered transistor with a series capacitor to suppress the negative voltage spikes. The simulations using LTspice and an experimental prototype were carried out to show the performance of the proposed gate driver under different drain-source voltages and different gate resistances with the comparison to other gate circuits.

II. Proposed Gate Driver Circuit and its Operational Principle

Before analyzing the proposed gate driver circuit and its operational principle, this section assumes the synchronous buck converter to simply illustrate the generation mechanism of both positive and negative gate-source voltage spikes. In specific, when the upper switch is turning ON, the voltage between drain and source terminals of the lower switch is suddenly rising up, which induces a current through the parasitic capacitor C_{dg_L} and it will charge up the gate-source capacitor C_{gs_L}, as shown in Fig. 1. Consequently, the gate voltage of lower switch is pushed up and generates a positive spurious triggering pulse [23], [24]. On the other hand, when the upper switch is turning OFF, the negative spurious voltage between the gate-source terminals of the lower switch induced by the load current, as shown in Fig. 2, may also overstress the power device.

The parasitic inductance of L_g and L_s will unavoidably induce the gate voltage oscillation, which can be damped by increasing the gate resistance R_g. However, along with the increase of gate resistance R_g, the spurious triggering voltage will increase when the external parasitic inductance L_s is not added. While according to Wang *et al.* [25], the spurious gate voltage will decrease when L_s is added in the circuit. In general, the spurious triggering pulse induced by the gate impedance of the nonoperating switch depends on the contributions of $C_{dg}dv/dt$ and $L_s di/dt$. Therefore, it can be concluded that the peak value of voltage spikes is determined by the equivalent parameters of switching device itself, the gate loop parasitic components, the power loop parasitic inductances and the maximum value of dc voltage across drain and source terminals.

To attenuate the negative gate voltage spikes, the proposed gate driver neither assumes a large uncontrollable capacitor across gate and source terminals nor implements an actively controlled circuit to achieve the variable gate capacitance. The detailed gate driver circuit is drawn in Fig. 3, where the negative gate voltage is generated by using a voltage level shifter

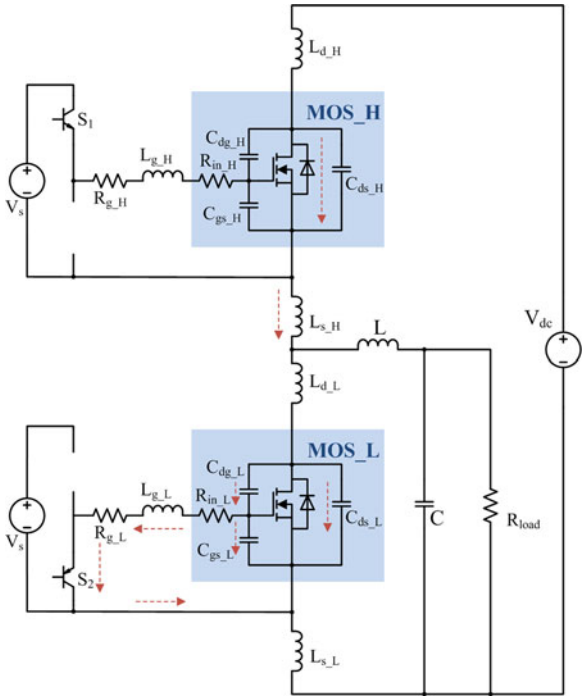


Fig. 1. Illustration of turning-on transient of the upper switch in a bridge circuit.

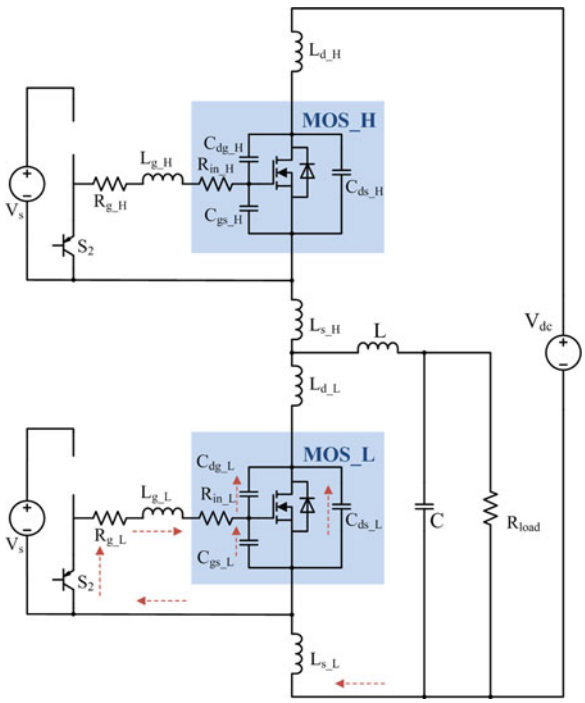


Fig. 2. Illustration of turning-off transient of the upper switch in a bridge circuit.

as traditional. The turning-on speed will not be affected because C_{gs} can be charged by capacitor C_2. Besides, according to the voltage between base and emitter terminals, the passively triggered auxiliary transistor Q in the proposed circuit can connect the capacitor C_2 to the gate terminal of SiC MOSFET when

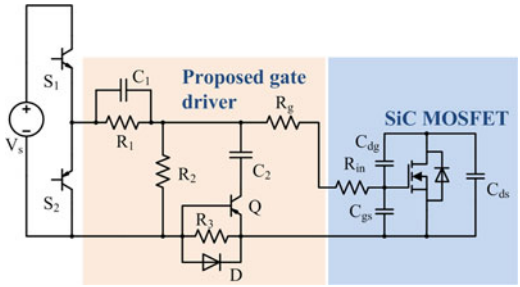


Fig. 3. Proposed gate driver circuit.

the negative gate voltage spikes occur. In addition, R_g is the external gate resistor of the gate driver circuit to mitigate the parasitic ringing.

In detail, this circuit consists of four resistors R_1, R_2, R_3, and R_g, two capacitors C_1 and C_2, one diode D and a p-n-p transistor Q. R_1 and R_2 make up a series voltage divider circuit and can generate various negative gate-source voltages based on the values of R_1 and R_2 without using any extra voltage source. The capacitor C_1 will make the negative gate-source voltage constant. Therefore, C_1 should be large enough to keep the voltage almost constant. Capacitor C_2 in series with a p-n-p transistor Q provides another small impedance loop when the negative gate-source voltage spike occurs. Resistor R_3 is used to turn ON or OFF the transistor Q passively and the diode D can help keep the turning-off speed unchanged because the current goes through D instead of R_3 when the SiC switch turns OFF. The transient operation analysis and the components design of the proposed gate circuit will be discussed below.

A. *Precharging Process*

The main purpose of precharging process is to make sure the voltage across C_1 and C_2 being constant. Before the main circuit begins to work, the gate circuit should be precharged by gate voltage source V_s to guarantee that the capacitors obtain enough energy. Fig. 4 shows the current direction of the precharging process before the main circuit begins to work. During the precharging process, both C_2 and C_{gs} will be charged up. But because there is no voltage across drain and source terminals of SiC MOSFET, the half-bridge circuit will not suffer the shoot-through problem. After the precharging process, the negative voltage of C_1 will clamp the C_{gs} voltage to be negative, while p-n-p transistor Q is OFF and C_2 can keep its voltage to be the positive gate voltage. During the operation of the main circuit, the precharging process is accomplished during the turn-on transient, which will not induce the shoot-through phenomena as well due to the complementary switching characteristics of half-bridge circuit.

There are two main stages of the precharging process: The first stage is to charge the parasitic capacitor C_{gs} and the second stage is to charge the capacitor C_2.

During the first stage, the gate current will first charge the parasitic capacitor C_{gs} of SiC MOSFET. The equivalent circuit is shown in Fig. 5(a). In order to make capacitor C_2 being

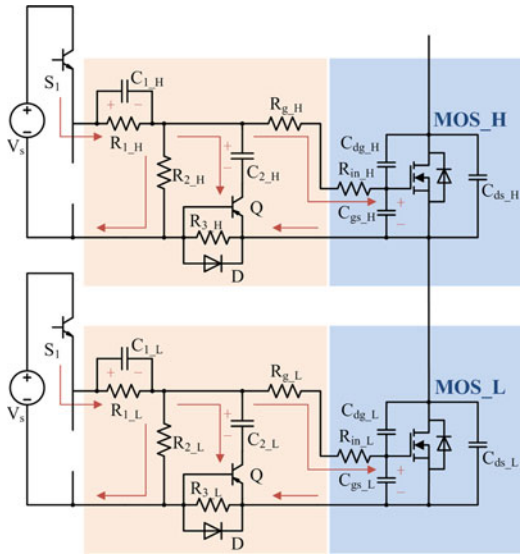


Fig. 4. Current direction of the precharging process.

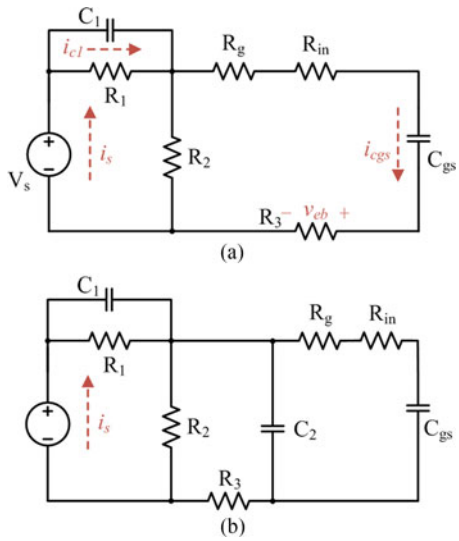


Fig. 5. Equivalent circuits of precharge process under (a) stage 1 and (b) stage 2.

charged, R_3 should be large enough to make V_{R3} being larger than the threshold voltage of the p-n-p transistor Q. And then, the p-n-p transistor Q turns ON and the precharge process turns to the second stage. The capacitor C_2 can be charged up and obtain a steady-state value. The equivalent circuit of the second stage is shown in Fig. 5(b). In general, the gate current will decrease gradually along with the charging duration increase since the voltages of C_2 and C_{gs} will increase gradually. Before the p-n-p transistor Q turns OFF, the voltage of C_2 should be nearly the positive gate voltage in theory, which can be achieved by properly selecting R_3. The components selection will be further introduced in Section II-E in order to ensure the proposed gate driver working well.

After the precharging process, the p-n-p transistors are OFF and the control signals of both upper and lower SiC MOSFETs

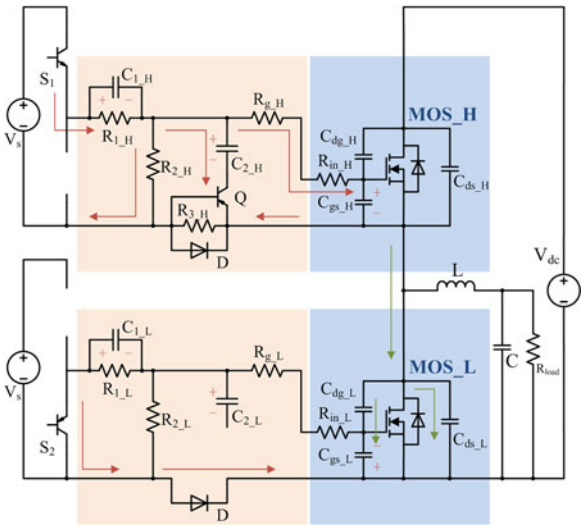


Fig. 6. Illustration of turning-on transient of MOS_H in a bridge circuit.

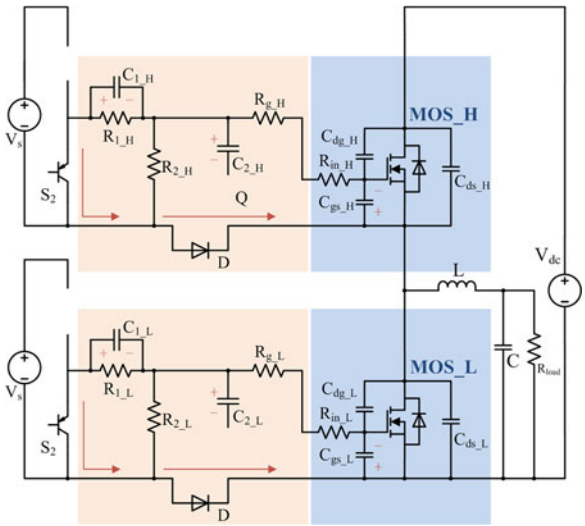


Fig. 7. Illustration of turning-off transient of MOS_H in a bridge circuit.

are switched to be OFF. The capacitor C_1 will provide a negative gate-source voltage for C_{gs}. Then, the main circuit can begin to work as normal.

B. Turning-On Transient

When the MOS_H turns ON and the MOS_L keeps OFF, part of driver current goes through R_{3_H}, which makes the voltage between the emitter and base of Q_H positive. As shown in Fig. 6, the p-n-p transistor Q_H will turn ON and the gate-source capacitor C_{gs_H} of MOS_H is charged by the capacitor C_{2_H}. Therefore, the turning-on speed of MOS_H will not be slowed down in this circuit. When the voltage of capacitor C_{2_H} decreases, the gate source V_s will charge the capacitor C_{2_H} and the gate-source capacitor C_{gs_H} of MOS_H simultaneously. And when the p-n-p transistor Q_H turns OFF along with the decrease of gate current, the gate-source capacitor C_{gs_H} of MOS_H can still be charged by the gate voltage V_s. However, part of inductive load current will charge C_{gs_L} and raise the gate voltage of MOS_L. The unwanted gate voltage rise may trigger the MOS_L to shoot through the main circuit. Therefore, the added negative gate voltage of C_{1_L} can eliminate this risk and prevents the unwanted shoot through in the proposed gate circuit.

C. Turning-Off Transient

Fig. 7 illustrates the equivalent circuit and current directions during the turning-off transients of upper SiC MOSFET. In specific, when the MOS_H turns OFF and the MOS_L still keeps OFF, the voltage across C_1 makes C_{gs_H} of MOS_H get a negative voltage through the diode D_H instead of R_{3_H}. And the capacitance of C_1 should be large enough to keep the negative voltage be almost constant during one switching period. Besides, the voltage between the base and emitter of Q_H is positive. Therefore, the p-n-p transistor Q_H turns OFF and C_2 does not work. The turning-off speed of MOS_H will not be affected. On the contrary, this negative voltage accelerates the discharge of gate-source capacitor C_{gs_H} of MOS_H.

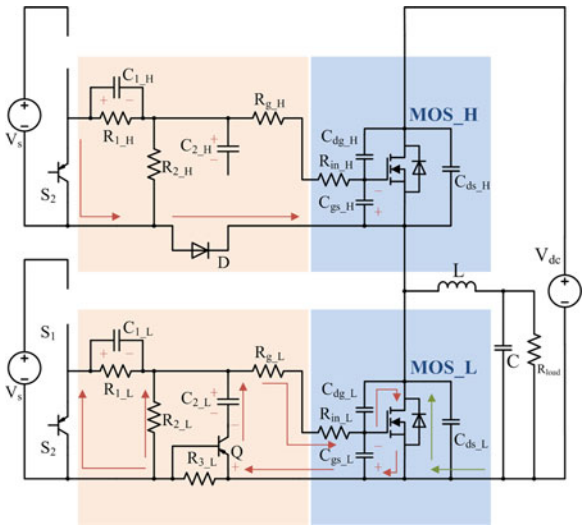


Fig. 8. Current direction of lower switch's gate driver when C_{2_L} is connected to the circuit.

D. Operational Principle of Negative Gate Voltage Spike Suppression

When the MOS_H turns OFF, drain-source voltage of the lower switch MOS_L will suffer a sudden mutation from $V_{\rm dc}$ to 0. The negative gate voltage spike will occur on the MOS_L. Fig. 8 shows the current direction of the proposed gate driver when the negative gate voltage spike occurs. The proposed gate driver circuit will make part of the leakage current go through the resistor R_{3_L}. Actually, this current will increase gradually because of the existence of parasitic inductance L_g. When the voltage across R_3 reaches the threshold voltage of p-n-p transistor, 0.7 V in general, the p-n-p transistor works and the capacitor C_2 connects to the circuit.

Doing so, it could provide another low impedance loop through the p-n-p transistor and C_{2_L} to release the energy stored in the parasitic capacitor C_{dg_L} and suppress the negative gate-source voltage spikes effectively. When the p-n-p transistor Q_L is turning ON, its voltage drop will be $V_{C1\_L} + V_{C2\_L} + V_{R3\_L}$, where V_{R3_L} is the voltage across R_{3_L} from right to left. The commonly used p-n-p transistors, e.g., ZXTP25140BFHTA, could have the large voltage drop when turning on [26], which can keep the connection of C_2. And along with the decrease of leakage current, the p-n-p transistor will turn OFF since V_{R3_L} will not keep triggering the p-n-p transistor. Because the p-n-p transistor only conducts for the short intervals during the whole switching period to suppress the negative gate voltage spikes and charge C_2, the losses of the proposed gate driver indeed will not increase significantly.

It is also noted that the actual voltage across R_g, R_{in} and C_{gs} is $-(V_{C1} + V_{R3})$, but the proposed circuit can still perform better than the traditional gate driver because the voltage across R_3 is small and the accessed C_2 can attenuate the negative voltage spike significantly. On the other hand, when the p-n-p transistor is ON, the voltage across it is large. However, according to p-n-p transistor working principle, the collector current $I_c = \beta I_b$, and the emitter current $I_e = I_b + I_c$, where β is the dc amplifying coefficient of p-n-p transistor. Therefore, the maximum current through C_2 is determined by the characteristics of the assumed p-n-p transistor. When employing the proper p-n-p transistor, most of the leakage current will go through C_2 and does not increase the voltage drop across R_3 significantly.

E. Passive Components Design Criteria

In this section, passive components design criteria are analyzed. First, according to Kirchhoff laws and the Laplace transforms applied to Fig. 5(a), (1) can be obtained

$$\begin{cases} \frac{1}{sC_1} \cdot I_{c1}(s) + R_1 \cdot [I_{c1}(s) - I_s(s)] = 0 \\ R_2 \cdot [I_s(s) - I_{C_{gs}}(s)] - R_1 \cdot [I_{c1}(s) - I_s(s)] = \frac{V_s}{s} \\ \left(R_g + R_{\text{in}} + R_3 + \frac{1}{sC_{gs}}\right) \cdot I_{C_{gs}}(s) + R_2 u \cdot I_{C_{gs}}(s) \\ \qquad = R_2 \cdot I_s(s) \end{cases}. \quad (1)$$

Therefore, the current through C_{gs} can be derived as follows:

$$\begin{aligned} I_{C_{gs}}(s) &= \frac{V_s}{A_{1S} + A_2 + \frac{A_3}{s \cdot C_1 R_1 + 1}} \\ &= \frac{(\frac{1}{A_1} s + \frac{1}{A_1 C_1 R_1}) \cdot V_s}{s^2 + (\frac{1}{C_1 R_1} + \frac{A_2}{A_1}) s + \frac{A_2 + A_3}{A_1 C_1 R_1}} \end{aligned} \quad (2)$$

where

$$\begin{cases} A_1 = R_g + R_{\text{in}} + R_3 \\ A_2 = \frac{1}{C_{gs}} + \frac{R_2 + R_3 + R_g + R_{\text{in}}}{R_2 C_1} \\ A_3 = \frac{1}{C_{gs} R_2} - \frac{R_2 + R_3 + R_g + R_{\text{in}}}{R_2 C_1} \end{cases}.$$

In order to avoid fluctuations on the current of C_{gs}, C_1 and R_3 should meet the following equation:

$$4A_1 A_3 \cdot C_1 R_1 = (A_1 - A_2 \cdot C_1 R_1)^2 \quad (3)$$

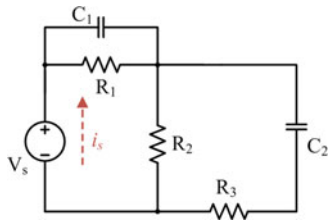


Fig. 9. Simplified circuit of precharge process stage 2.

And the voltage across resistor R_3 can be calculated based on (2)

$$\begin{aligned} v_{R3} = &\frac{R_3 \cdot V_s}{A_1} e^{-(\frac{1}{2C_1 R_1} + \frac{A_2}{2A_1}) \cdot t} \\ &- t \cdot \left(\frac{1}{2A_1 C_1 R_1} - \frac{A_2}{2A_1^2}\right) e^{-(\frac{1}{2C_1 R_1} + \frac{A_2}{2A_1}) \cdot t}. \end{aligned} \quad (4)$$

The selection of R_3 should be large enough to make v_{R3} being larger than the threshold voltage of the p-n-p transistor Q so that the capacitor C_2 can be charged during the precharging process, which means

$$v_{R3}(0^+) = \frac{R_3 \cdot V_s}{R_g + R_{\text{in}} + R_3} > 0.7. \quad (5)$$

Where, the threshold voltage of the p-n-p transistor Q is assumed to be 0.7 V. It is noted that when the gate resistance R_g becomes smaller, (5) can be fulfilled more easily and the voltage of C_2 can be charged to the wanted positive voltage more easily because the p-n-p transistor Q can keep ON longer. Therefore, a relatively small gate resistor is encouraged to be used. According to Wang and Chung [17], capacitor C_2 should be much larger than the parasitic capacitor C_{gs} so that the precharging process is hardly affected and the circuit can be simplified, as shown in Fig. 9.

Conducting Laplace transform, $V_{c1}(s)$ can be solved as

$$V_{c1}(S) \frac{C_2 + \frac{R_3 C_2}{R_2} + \frac{1}{R_{2s}}}{B_1 S^2 + B_2 S + R_0} \cdot V_s \quad (6)$$

where

$$\begin{cases} B_1 = C_1 C_2 R_3 \\ B_2 = C_1 + C_2 + C_2 R_0 R_3 \\ R_0 = \frac{R_1 + R_2}{R_1 \cdot R_2} \end{cases}.$$

Performing the inverse Laplace transform, $v_{C_1}(t)$ can be solved as follows:

$$\begin{aligned} v_{C_1}(t) = &\frac{V_s}{R_2 R_0} \\ &- \frac{2B_1 V_s}{R_2 \sqrt{B_2^2 - 4B_1 R_0}} \left(\frac{1}{B_2 - \sqrt{B_2^2 - 4B_1 R_0}} e^{-\frac{B_2 - \sqrt{B_2^2 - 4B_1 R_0}}{2B_1} t} \right. \end{aligned}$$

$$+\frac{1}{B_2+\sqrt{B_2^2-4B_1R_0}}e^{-\frac{B_2+\sqrt{B_2^2-4B_1R_0}}{2B_1}t}\Bigg)$$
$$+\frac{(C_2+\frac{C_2R_3}{R_2})V_s}{\sqrt{B_2^2-4B_1R_0}}\left(e^{-\frac{B_2-\sqrt{B_2^2-4B_1R_0}}{2B_1}t}-e^{-\frac{B_2+\sqrt{B_2^2-4B_1R_0}}{2B_1}t}\right). \tag{7}$$

From (7), the initial value and the final value of negative gate voltage is $v_{C_1}(0)=\frac{V_s}{R_2R_0}-\frac{2B_1V_s}{R_2\sqrt{B_2^2-4B_1R_0}}$ and $v_{C_1}(\infty)=\frac{R_1}{R_1+R_2}V_s$, respectively. Therefore, the precharging process can be accelerated if $\frac{2B_1V_s}{R_2\sqrt{B_2^2-4B_1R_0}}$ is as small as possible.

And before the p-n-p transistor Q turns OFF, the voltage of capacitor C_2 should approach the positive gate voltage. Therefore, when the voltage of R_3 equals to 0.7 V, the voltage of capacitor C_2 should meet (8), where the margin can be set to 0.2 V

$$|v_{C_2}|>\frac{R_2}{R_1+R_2}V_s-0.2. \tag{8}$$

Further, (9) can be derived by considering above constraints

$$\begin{cases} v_{R_3}=\frac{R_3\cdot V_s}{A_1}e^{-(\frac{1}{2C_1R_1}+\frac{A_2}{2A_1})\cdot t}-t\cdot\left(\frac{1}{2A_1C_1R_1}-\frac{A_2}{2A_1^2}\right) \\ \qquad e^{-(\frac{1}{2C_1R_1}+\frac{A_2}{2A_1})\cdot t}=0.7 \\ v_{C_2}(t)=V-v_{C_1}(t)>\frac{R_2}{R_1+R_2}\cdot V_s-0.2. \end{cases} \tag{9}$$

On the other hand, the negative gate voltage should meet the following inequality to avoid shoot through:

$$|v_{C_1}|>uC_{gs}(\max)-V_{gs(th)}. \tag{10}$$

So, resistors R_1 and R_2 should meet the following operation conditions:

$$\frac{R_1}{R_2}<\frac{V_s}{uC_{gs}(\max)-V_{gs(th)}}-1. \tag{11}$$

Additionally, the values of passive components are related to the turning-off transient process. During turning-off transient, the capacitor C_1 will be discharged through R_1 and R_2. Therefore, in order to neglect the discharging of C_1 through R_1 and R_2, the time constant should be large enough, that is to say $\frac{R_1R_2}{R_1+R_2}\cdot C_1\gg T_s$, and T_s is the switching period. Performing the Laplace transform and the inverse Laplace transform, $v_{C_{gs}}$ can be calculated as

$$v_{C_{gs}}(t)=-\frac{C_1V_{c1}}{C_1+C_{gs}}[1-e^{-(\frac{1}{C_1}+\frac{1}{C_{gs}})(R_{\rm in}+R_3)t}]. \tag{12}$$

Therefore, the capacitor C_1 should be much larger than C_{gs} to make the voltage across C_{gs} reach V_{C1}.

When considering the negative voltage spikes suppression and neglecting the normal negative gate-source voltage, the simplified Laplace transform equivalent circuit is shown in Fig. 10, where R' represents R_1 and R_2 in parallel.

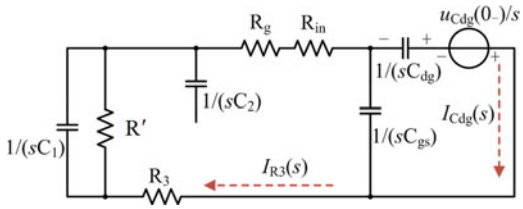


Fig. 10. Simplified Laplace transform equivalent circuit before Q turning ON.

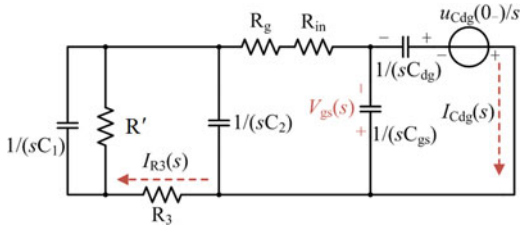


Fig. 11. Simplified Laplace transform equivalent circuit when Q turns ON.

First, in order to make p-n-p transistor Q turn ON when the negative gate-source voltage spikes occur, the emitter-base voltage should be larger than the threshold voltage of the p-n-p transistor. According to Kirchhoff laws, the current through R_3 is presented as by (13) shown at the bottom of this page.

Performing the Laplace inverse transform, and the maximum current through R_3 can be obtained by the following equation:

$$I_{R_3}(\max)=\frac{V_{\rm dc}}{C_{dg}}\cdot\frac{2R_1}{R'\cdot(R_3+R_g+R_{\rm in})}. \tag{14}$$

Therefore, the following equation should make the voltage of R_3 being larger than the threshold voltage of the p-n-p transistor Q:

$$U_{R_3}(\max)=I_{R_3}(\max)\cdot R_3=\frac{V_{\rm dc}}{C_{dg}}\cdot\frac{2R_1\cdot R_3}{R'}\cdot(R_3+R_g+R_{\rm in})>0.7. \tag{15}$$

Then, after the p-n-p transistor Q turns ON, most of the current I_{Cdg} will go through C_2 instead of C_{gs} and R_3, and the corresponding equivalent circuit is shown in Fig. 11. Therefore, the rated voltage across emitter and collector terminals of p-n-p transistor should be larger than V_s. The p-n-p transistor works on amplification region and the rated current should be larger than the initial value of gate current and the current I_{Cdg}. Besides, in order to absorb more I_{Cdg}, the amplifying coefficient of selected p-n-p transistor should also be as large as possible.

$$I_{R_3}(s)=\frac{V_{\rm dc}}{C_{dg}}\cdot\left\{\frac{sC_1R_1+1}{s^2C_1R'(R_3+R_g+R_{\rm in})+s[C_{gs}(R'+R_3+R_g+R_{\rm in})+C_1R_1]+1}\right.$$
$$\left.+\frac{(sC_1R_1+1)C_{dg}}{s^2C_1R'(R_3+R_g+R_{\rm in})+s(R'+R_3+R_g+R_{\rm in})}\right\} \tag{13}$$

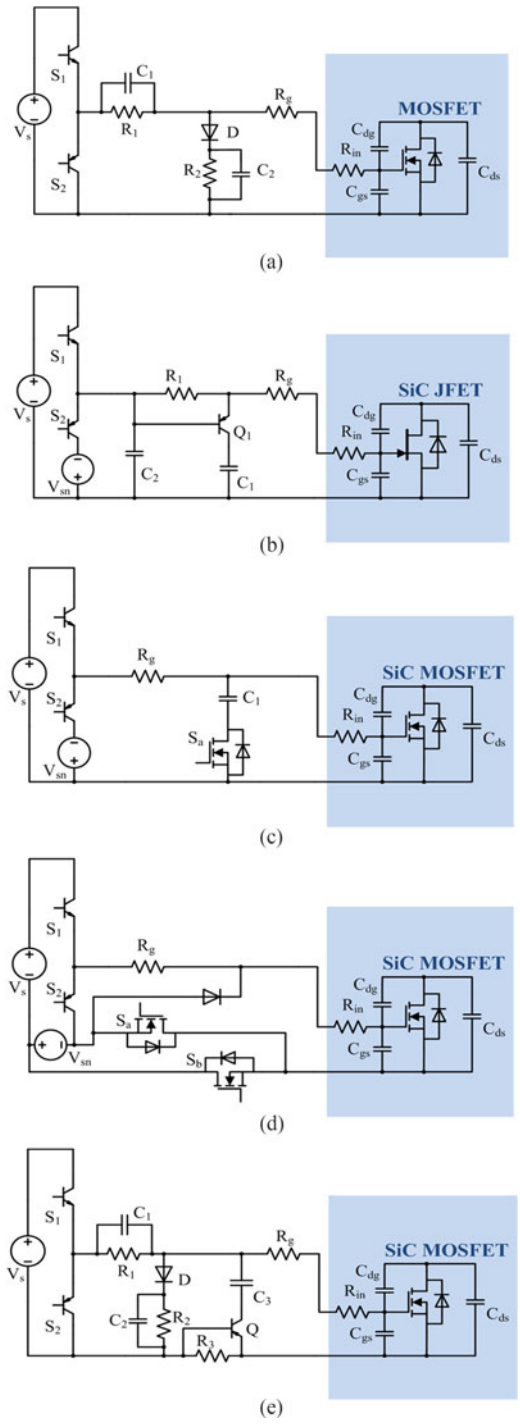


Fig. 12. Topologies of different gate drivers with: (a) Level shifting circuit proposed in [17], (b) positive spikes suppressing circuit in [18], (c) active suppressing circuit GIR in [19], (d) active suppressing circuit GVC in [19], and (e) passive suppressing circuit in [20].

According to p-n-p transistor working principle, the collector current $I_c = \beta I_b$, and the emitter current $I_e = I_b + I_c$, where β is the dc amplifying coefficient of p-n-p transistor. Therefore, the larger dc amplifying coefficient is, the more leakage current can be absorbed, which means most of the leakage current will go through C_2 and does not increase the voltage drop across R_3 significantly.

Being similar to (5), a small gate resistor R_g is also recommended to fulfill (15) to make the proposed gate driver work well, because the large gate current can help the auxiliary transistor Q turn ON for a longer time to suppress the negative voltage spikes effectively.

TABLE I
COMPARISON OF DIFFERENT GATE DRIVERS

Gate driver	Suppressing positive gate-source voltage spikes	Suppressing negative gate-source voltage spikes	Complexity
Proposed gate driver	Yes	Yes	Normal
Fig. 12(a)	Yes	No	Normal
Fig. 12(b)	Yes	No	Normal
Fig. 12(c)	Yes	Yes	Additional control signal
Fig. 12(d)	Yes	Yes	Additional control signal
Fig. 12(e)	Inferior	Yes	Normal

TABLE II
MAIN PARAMETERS OF C2M0040120D

Parameters	Values
Minimum/maximum allowed gate source voltage	–10 V/+ 25 V
Gate threshold voltage	2.8 V
Internal gate resistance	1.8 Ω
Drain-source breakdown voltage	1200 V
Input capacitance	1893 pF
Reverse transfer capacitance	10 pF
Drain-source on-state resistance	40 mΩ

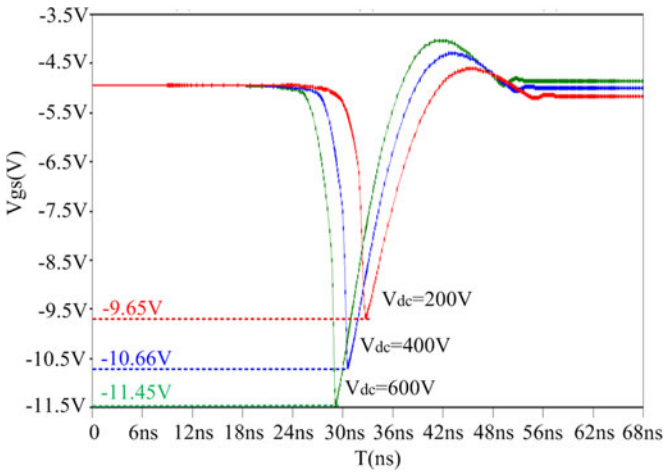


Fig. 13. Gate-source voltage spikes waveform of most basic gate driver under different dc voltages.

F. Comparison of SiC mosfet Gate Drivers

In order to show the advantages of the proposed gate driver, some comparisons with other novel gate drivers are presented in details. Fig. 12 shows five MOSFET gate drivers proposed in [17]–[20]. The circuits in reference [17] and [18], as shown in Fig. 12(a) and (b), can suppress the positive gate-source

TABLE III
PASSIVE ELEMENTS PARAMETERS OF DIFFERENT GATE DRIVERS

Gate drivers	R_1	R_2	R_3	C_1	C_2	C_3
Proposed gate driver	2.5 kΩ	9.5 kΩ	2 Ω	0.2 *u*F	0.1 *u*F	/
Fig. 12(a)	2.5 kΩ	9.5 kΩ	/	0.2 *u*F	0.1 *u*F	/
Fig. 12(b)	2 Ω	/	/	0.1 *u*F	6.8 nF	/
Fig. 12(c)	/	/	/	0.1 *u*F	/	/
Fig. 12(d)	/	/	/	/	/	/
Fig. 12(e)	2.5 kΩ	9.5 kΩ	2 Ω	0.2 *u*F	0.1 *u*F	0.1 *u*F

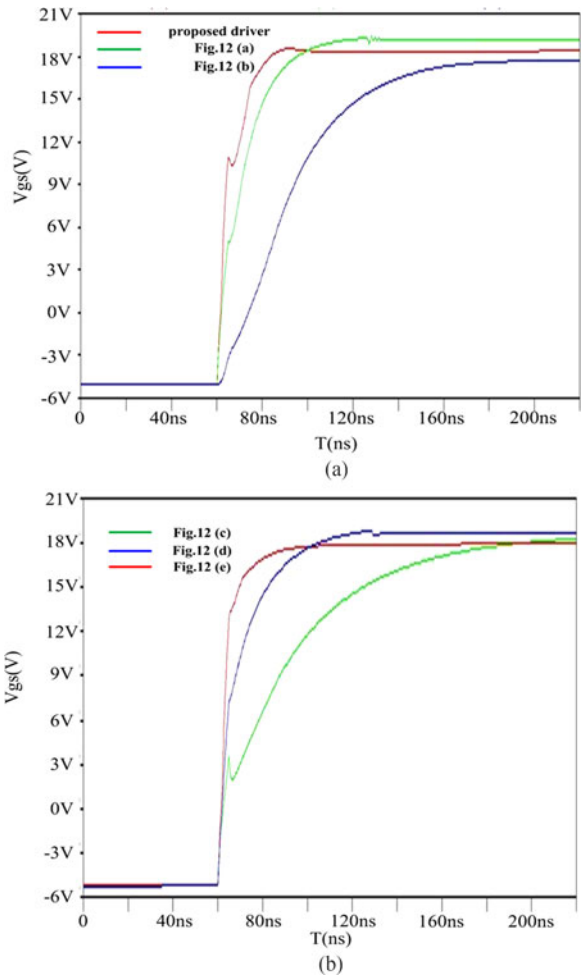


Fig. 14. Turning-on transient of different gate drivers in a bridge circuit.

voltage spikes by providing a negative gate voltage and a low impedance loop, respectively. However, they both play no sense on suppressing the negative gate-source voltage spikes. Fig. 12(a) shows a voltage divided circuit to generate the negative gate-source voltage passively and Fig. 12(b) can eliminate the positive gate-source voltage spikes of switching devices effectively. The approaches proposed in [19], as shown in Fig. 12(c) and (d), can eliminate both positive and negative spikes, and the approach in Fig. 12(d) is more effective for crosstalk suppression, but the auxiliary actively controlled transistors and the implementation of relatively complicated logic signal synthesis will unavoidably increase the circuit

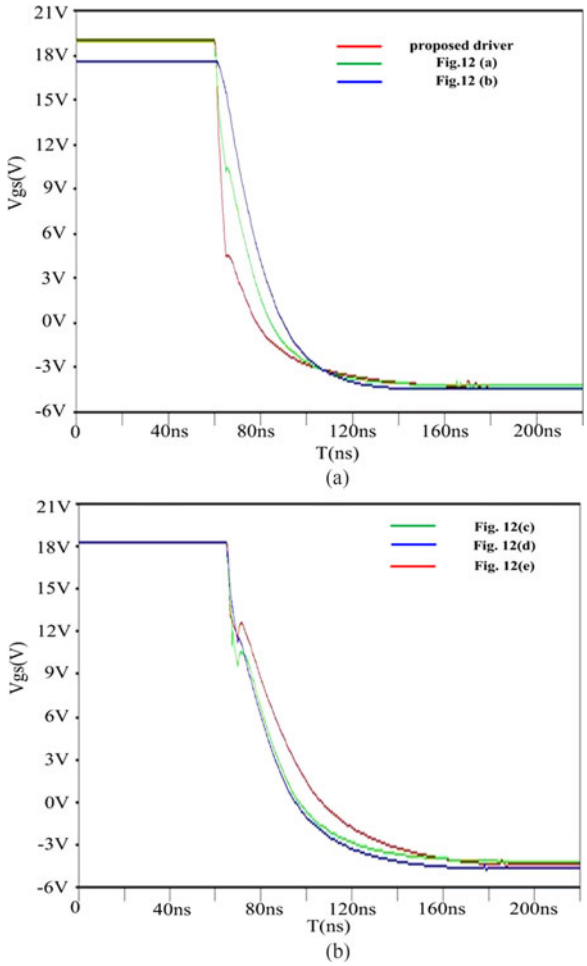


Fig. 15. Turning-off transient of different gate drivers in a bridge circuit.

complexity and cost. And the method in [20], as shown in Fig. 12(e), can suppress the negative gate-source voltage spikes. But comparing the proposed circuit in Fig. 3, Fig. 12(e) will assume one additional capacitor to maintain the voltage across R_2 and decrease the turning-off switching speed because R_3 is connected in series with gate resistor R_g when turning OFF SiC MOSFET.

Table I presents the comparison of different gate drivers' spike-suppressing capability and circuit complexity. The proposed gate driver in this paper has superior characteristics comparing to other gate drivers in terms of the voltage spikes suppression capability and the realization complexity.

III. SIMULATION VERIFICATIONS

A bidirectional buck converter using the C2M0040120D SiC MOSFETs was assumed for simulation and experimental verification. Table II lists the main parameters of C2M0040120D when its operational temperature is 25 °C. Cree, Inc., offers the Spice model of C2M0040120D when using the LTspice. Therefore, LTspice is assumed to simulate the different gate drivers and the proposed one in this paper.

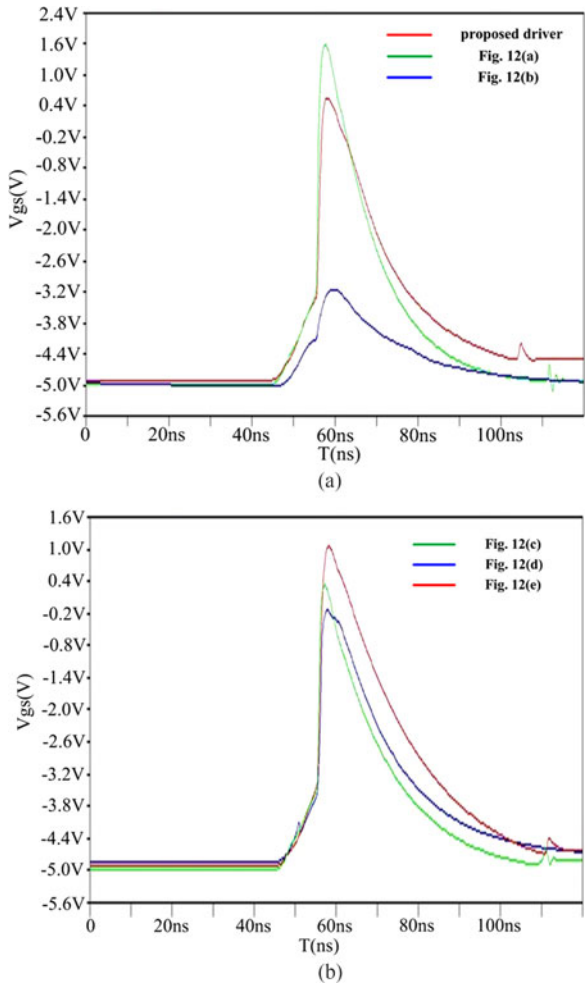


Fig. 16. Positive gate voltage spikes of different gate drivers in a bridge circuit.

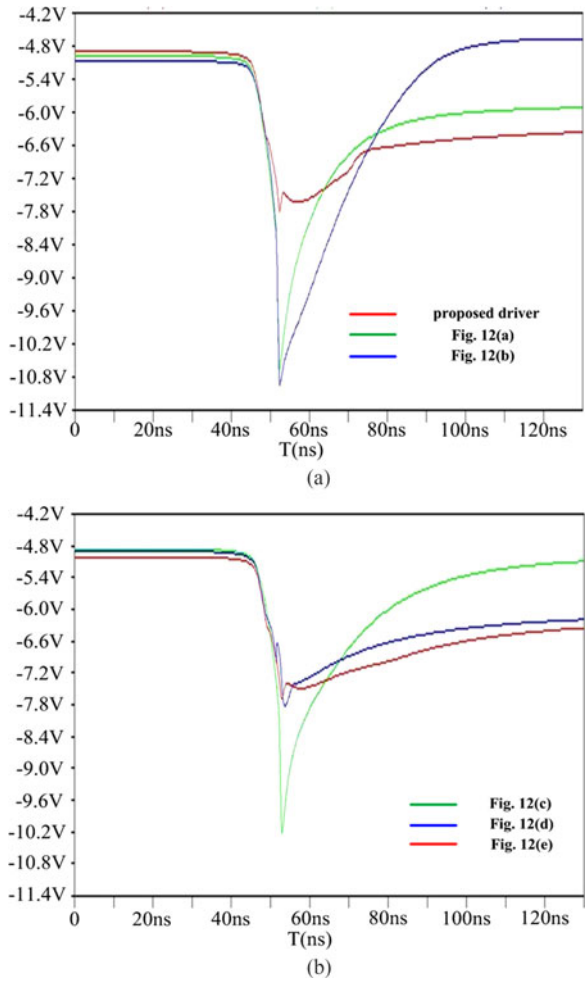


Fig. 17. Negative gate voltage spikes of different gate drivers in a bridge circuit.

TABLE IV
MAXIMUM POSITIVE GATE-SOURCE VOLTAGE SPIKE AND TURNING-ON SWITCHING PERFORMANCES OF DIFFERENT GATE DRIVERS

Gate driver	Maximum positive gate -source voltage spike	Switching time	Switching losses	*dv/dt*
Fig. 12(a)	1.69 V	46 ns	6.9 W	49 V/ns
Fig. 12(b)	–2.85 V	95 ns	14.25 W	45 V/ns
Fig. 12(c)	0.32 V	103 ns	15.45 W	40 V/ns
Fig. 12(d)	–0.15 V	53 ns	7.95 W	49 V/ns
Fig. 12(e)	1.05 V	31 ns	4.65 W	50 V/ns
Proposed	0.74 V	27 ns	4.05 W	50 V/ns

TABLE V
MINIMUM NEGATIVE GATE-SOURCE VOLTAGE SPIKE AND TURING-OFF SWITCHING PERFORMANCES OF DIFFERENT GATE DRIVERS

Gate driver	Minimum negative gate -source voltage spike	Switching time	Switching losses	$\frac{dv}{dt}$
Fig. 12(a)	–10.8 V	53 ns	7.95 W	69 V/ns
Fig. 12(b)	–10.4 V	62 ns	9.3 W	69 V/ns
Fig. 12(c)	–9.13 V	71 ns	10.65 W	72 V/ns
Fig. 12(d)	–7.91 V	72 ns	10.8 W	72 V/ns
Fig. 12(e)	–7.72 V	90 ns	13.5 W	67 V/ns
Proposed	–7.31 V	46 ns	6.9 W	143 V/ns

Compared to Si MOSFETs, SiC MOSFETs have a lower drift region resistance, but a higher channel resistance. At the low gate-source voltages ($V_{\rm GS} < 13$ V), the channel resistance dominates the total on resistance, which has a negative temperature coefficient. In other words, the higher temperature is, the larger on-resistance is if the gate-source voltage is lower than 13 V. Therefore, it is always recommended to turn on SiC MOSFETs with $V_{\rm GS}$ higher than 18 V according to the datasheet. In order to be consistent with the experimental conditions, the input source voltage V_s of gate driver is set to 24 V and the positive gate-source voltage and negative gate-source voltage is set to +19 and –5 V, respectively. The dc voltage of main circuit varies from 200–600 V and the loads set to 100 Ω. A parasitic inductance 5 nH and the external gate resistance 5 Ω are included in all gate drivers in simulations.

Fig. 13 shows the gate-source voltage spikes of the most basic gate driver without any auxiliary circuit added under different dc voltages. It is observed that when the dc voltage is above 400 V, the negative voltage spike exceeds the minimum allowable

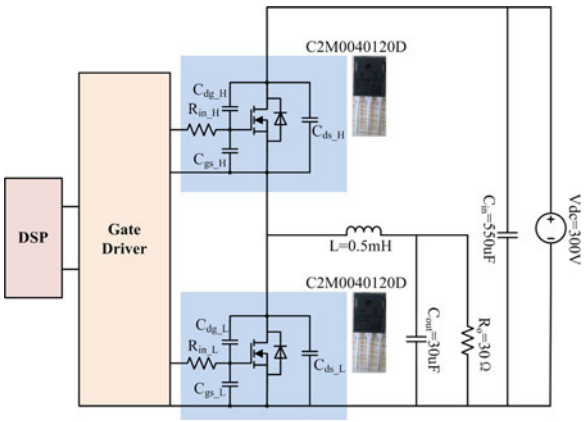


Fig. 18. Schematic of experimental circuit.

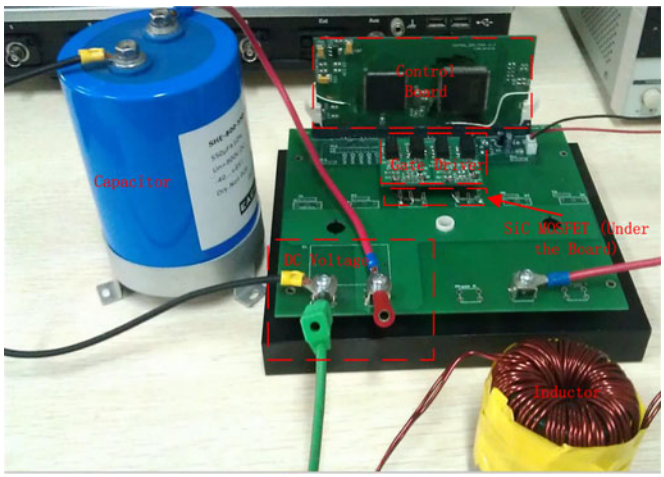


Fig. 19. Prototype of bidirectional buck converter using SiC MOSFETs.

TABLE VI
EXPERIMENT PARAMETERS

Parameters	Values
Carrier frequency	100 kHz
Inductor	550 uH
Capacitor	550 uF
Load	30 Ω
Duty cycle	50%
Dead time	0.3 us

negative biased gate voltage of SiC MOSFET, which will make the SiC MOSFET fail. However, the drain-source breakdown voltage of C2M0040120D is 1200 V. Therefore, the most basic gate driver is unable to exert the full advantages of SiC devices.

In order to show the advantages of the proposed gate driver, the switching speed and the gate voltage spikes are compared among different gate drivers mentioned earlier in Fig. 12(a)–(e) and the proposed gate driver. The input dc voltage is set to 600 V. According to the set positive gate-source voltage and negative gate-source voltage, the values of R_1 and R_2 are selected as 2.5 and 9.5 kΩ in Fig. 12(a) and (d) and the proposed one in

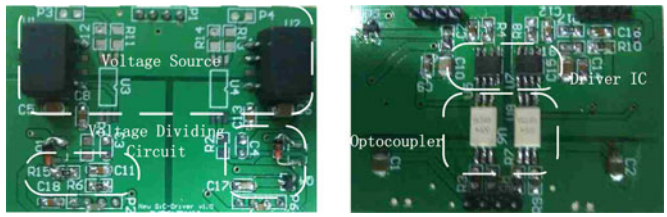


Fig. 20. Picture of the proposed gate driver prototype.

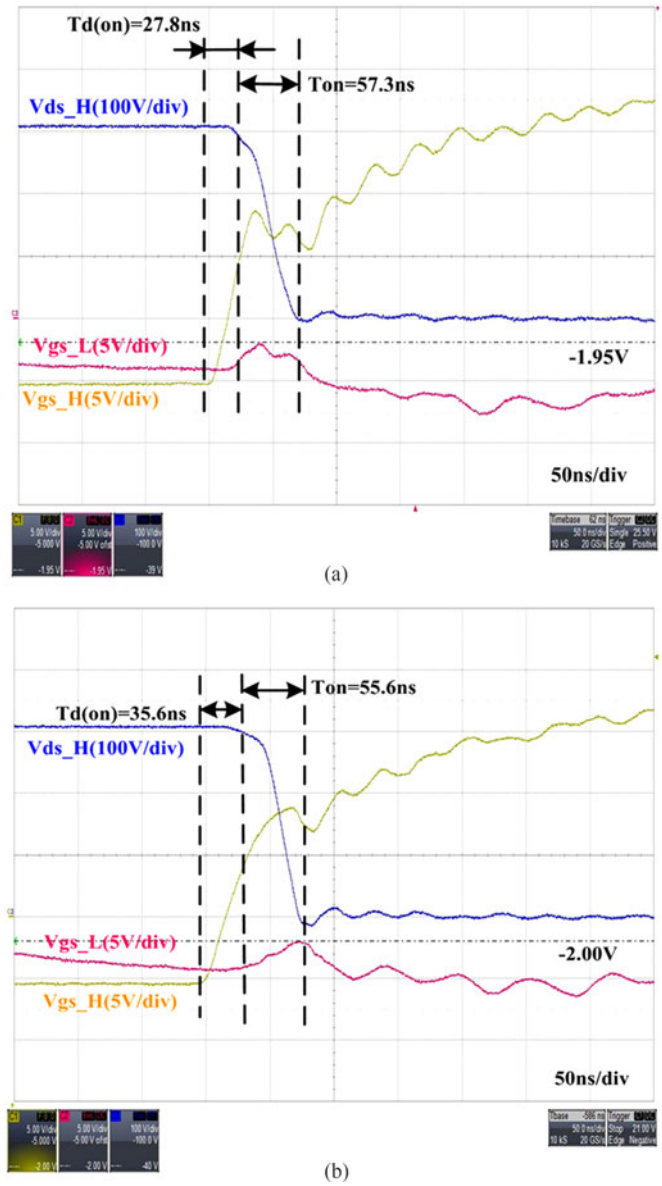


Fig. 21. Captured waveforms of turning-on process of the upper switch in (a) the most basic gate driver and (b) the proposed gate driver.

this paper, respectively. The values of capacitors C_1 and C_2 are selected as 0.2 and 0.1 μF according to (7) and (8). And the value of R_3 is selected as 2 Ω according to (9) and (15). All passive components in the compared gate drivers are listed in Table III.

The turning-on transient and the turning-off transient of these different gate drivers are shown in Figs. 14 and 15, where the

TABLE VII
COMPARISON OF BOTH GATE DRIVERS

Switching time	Most basic gate driver	Proposed gate driver
Turn-on delay time ($t_{d(\mathrm{on})}$)	27.8 ns	35.6 ns
Turn-on time (t_{on})	57.3 ns	55.6 ns
Positive spike (V_p)	–1.95 V	–2.00 V
Turn-off delay time ($t_{d(\mathrm{off})}$)	30.8 ns	29.4 ns
Turn-off time (t_{off})	101.8 ns	93.8 ns
Negative spike (V_n)	–8.20 V	–6.70 V

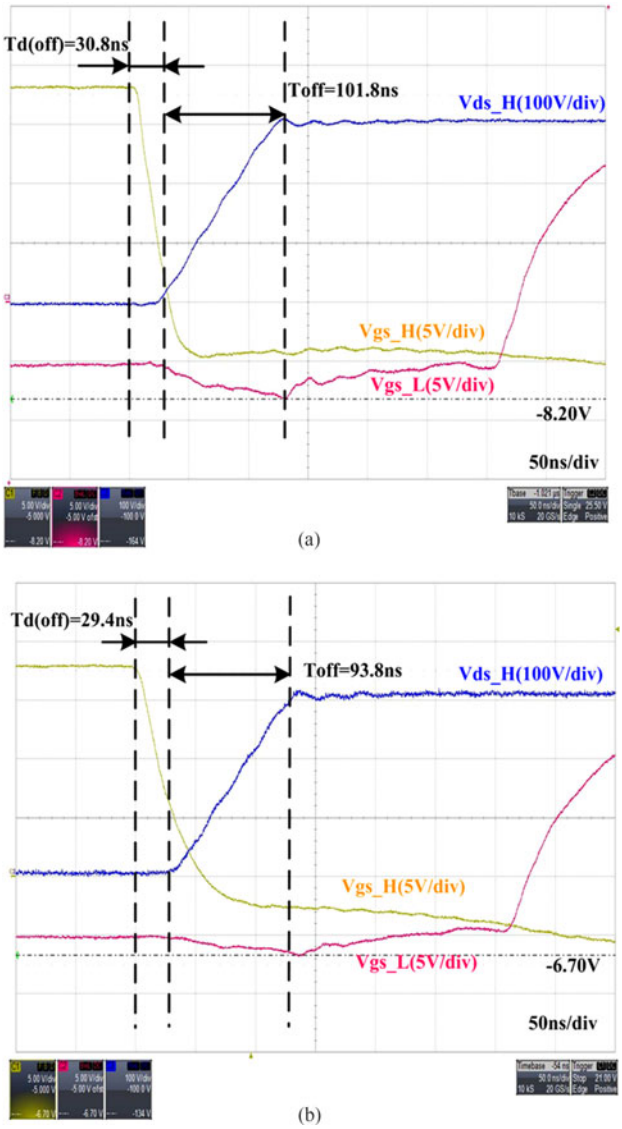


Fig. 22. Captured waveforms of turning-off process of the upper switch in (a) the most basic gate driver and (b) the proposed gate driver.

gate driver circuit in Fig. 12(b) shows the slowest turning-on transient process because capacitor C_2 is always connected in the circuit, which will also increase the switching losses and decrease the operational efficiency. And the turning-on switching time in Fig. 12(e) is almost the same as the proposed one because the gate-source capacitor C_{gs} is mainly charged by C_2. While during the turning-off transient, the gate-source capacitor

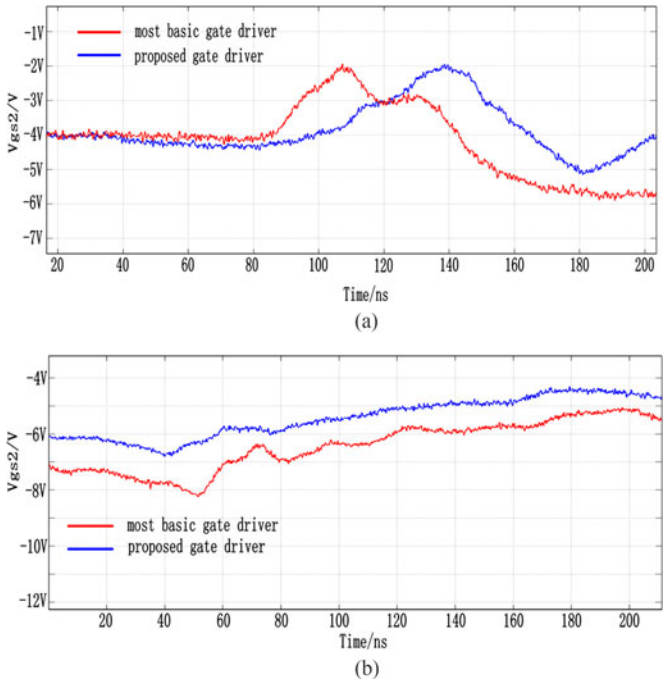


Fig. 23. Part of switching waveforms for illustrating (a) positive spikes and (b) negative spikes of both gate drivers.

C_{gs} is charged by the capacitor C_1 the same as the proposed gate driver, but R_3 becomes part of the turning-off driving resistance in Fig. 12(e). Therefore, the turning-off speed of Fig. 12(e) will decrease, as shown in Fig. 15, and leads to the high switching losses compared to the proposed gate driver. It is noted that the negative gate-source voltage produced by the passive level shifter is slightly larger than –5 V in Fig. 14, mainly because capacitance C_1 has a little voltage drop during its discharging process.

Fig. 16 shows the positive gate-source voltage spikes of lower switch when the upper switch is turning on. Table IV lists the maximum values of the positive gate-source voltage spikes and the turning-on switching performances appeared in these different gate drivers, where the switching time and *dv/dt* are directly measured from the switching waveforms and the listed switching losses are derived by averaging the product of voltage and current during the switching transient. The gate driver in Fig. 12(e) and the proposed gate driver show the minimum switching time and switching losses. The positive gate voltage spikes of all these gate drivers are below the gate threshold voltage of 2.8 V, which means the negative gate voltage can prevent the unwanted shoot through in the phase-leg configuration effectively.

Fig. 17 shows the waveforms of negative gate-source voltage spikes when the complementary switch is turning OFF. Table V lists the minimum values of negative gate voltage spikes and the turning-off switching performances. It is noted that the proposed gate driver can suppress the negative gate voltage spikes effectively, whose suppression performance is slightly superior to the circuits in Fig. 12(d) and (e). Also, the proposed gate

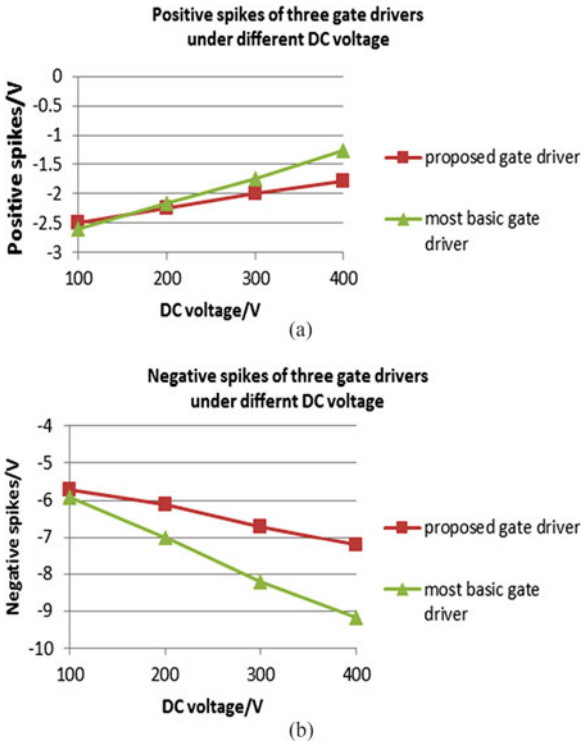


Fig. 24. (a) Positive and (b) negative voltage spikes of both gate drivers under different dc voltages.

driver shows shorter switching time, lower switching losses and larger *dv/dt*.

IV. Experimental Verifications

The performance of the proposed gate driver circuit was verified by an experimental prototype. Fig. 18 shows the schematic of experimental circuit and Fig. 19 is the prototype of bidirectional buck converter using SiC MOSFETs. The main circuit parameters are listed in Table VI. Fig. 20 shows the captured pictures for both sides of the proposed gate driver. In order to comparatively evaluate the performance of the proposed gate driver, the most basic gate driver without any auxiliary circuit added was also constructed in experiment. But to prevent the converter shoot through in experiment, a negative gate-source voltage –5 V was added in the most basic gate driver. Therefore, the most basic gate driver and the proposed gate driver both have the positive gate voltage of +19 V and the negative gate voltage of –5 V in experiment.

The gate-source voltage is generated by MORNSUN's B0524XT-1WR2 and B0505XT-1WR2. The optocoupler is ACPL-W346 from Avago Technologies and the additional p-n-p transistor is ZXTP25140BFHTA manufactured by Zetex Semiconductors. First, the external gate resistors of both gate drivers are 15 Ω, and in order to accelerate the switching-off process, a diode is antiparallel connected to the external gate resistor. When the dc input voltage of buck converter is 300 V, the switching waveforms of two gate driver circuits are shown in Figs. 21 and 22, where it is noted that the proposed gate driver works properly. It is also observed that the proposed gate driver

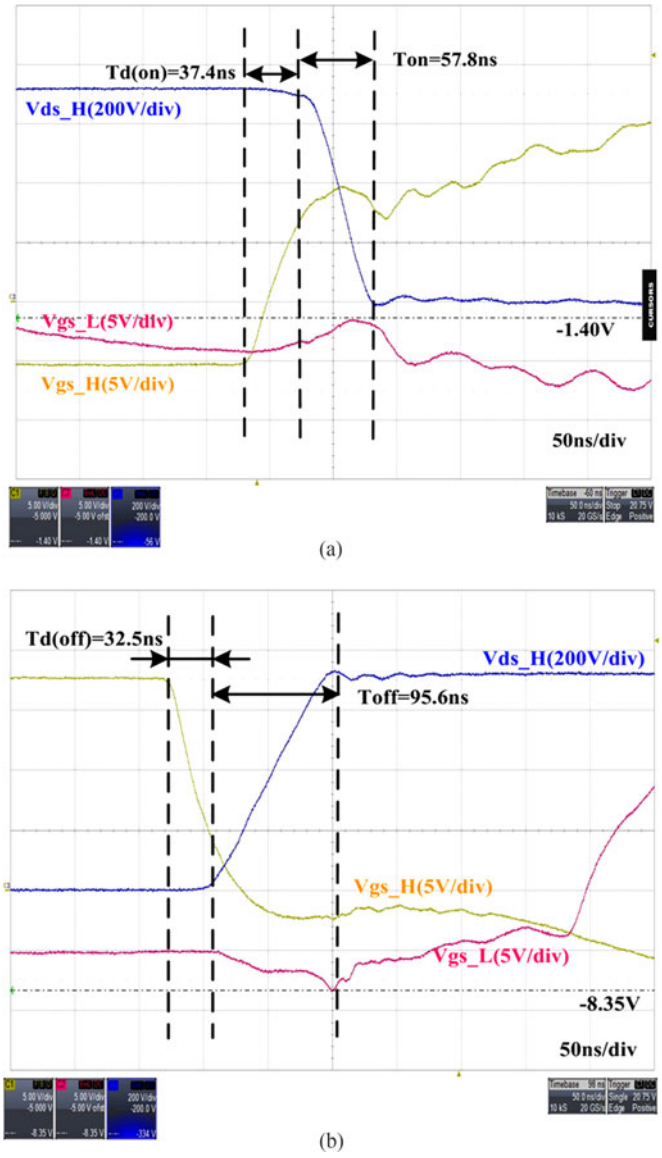


Fig. 25. Captured waveforms of (a) turning-on and (b) turning-off process of the upper switch in the proposed gate driver under 800-V dc voltages.

can attenuate the negative gate-source voltage spikes without slowing down the switching speed as shown in Fig. 22(b). The main performance evaluation parameters of both gate drivers are listed in Table VII. It is observed that the proposed gate driver will not slow down the switching speed but could effectively attenuate the negative gate source voltage spikes. In order to show the advantages of the proposed gate driver, part of switching waveforms have been redrawn in Fig. 23 to clearly demonstrate the positive and negative spikes of both gate drivers, respectively. The switching oscillations are mainly caused by the parasitic inductance of gate drivers.

This paper also compares the positive and negative spikes of the proposed gate driver and the most basic gate driver under different dc voltages, as shown in Fig. 24, where the voltage spikes will increase along with the increase of dc input voltage. But the proposed gate driver can still satisfy the stringent

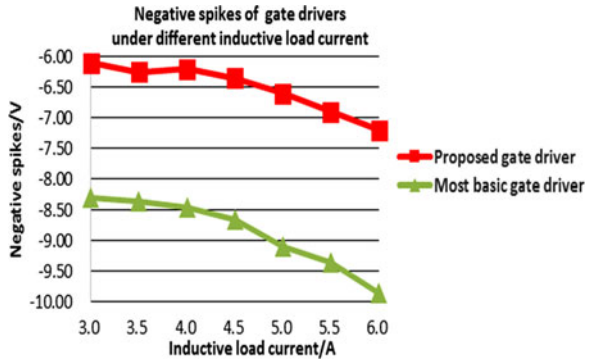


Fig. 26. Negative voltage spikes of both gate drivers under different inductive load current.

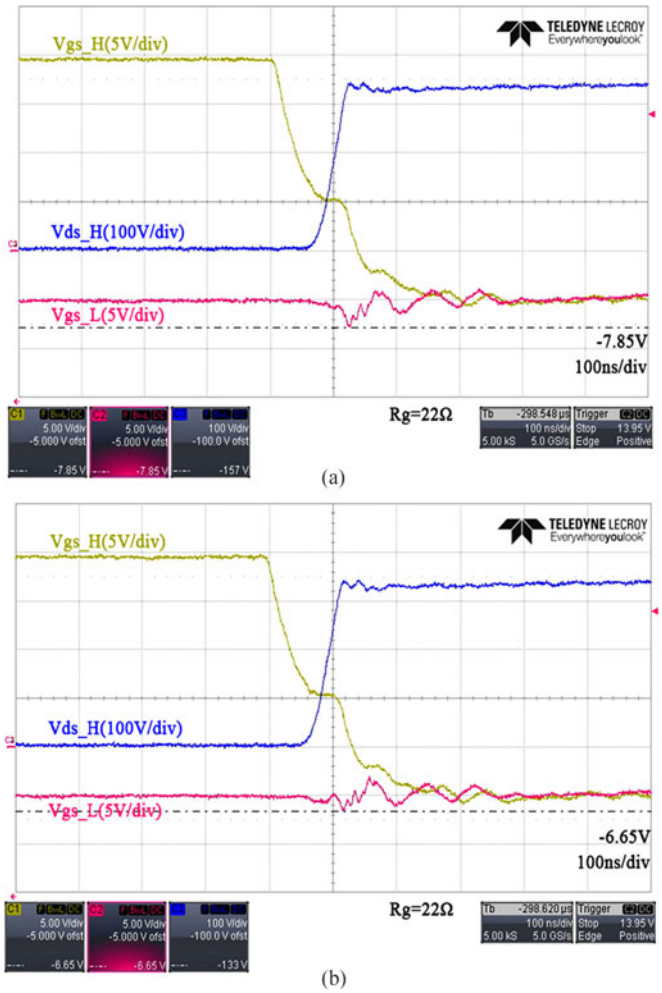


Fig. 27. Captured waveforms of switching-off process of the upper switch with a gate resistor of 22 Ω in (a) the most basic gate driver and (b) the proposed gate driver.

requirement of SiC MOSFET under high-dc input voltage. For illustration, Fig. 25 shows the captured waveforms of turning ON and OFF of the upper switch under dc voltage 800 V by using the proposed gate driver, where both positive and negative gate source voltage spikes are still within the allowed range.

In order to further verify the performance of the proposed gate driver under different inductive loads, a set of experiments were

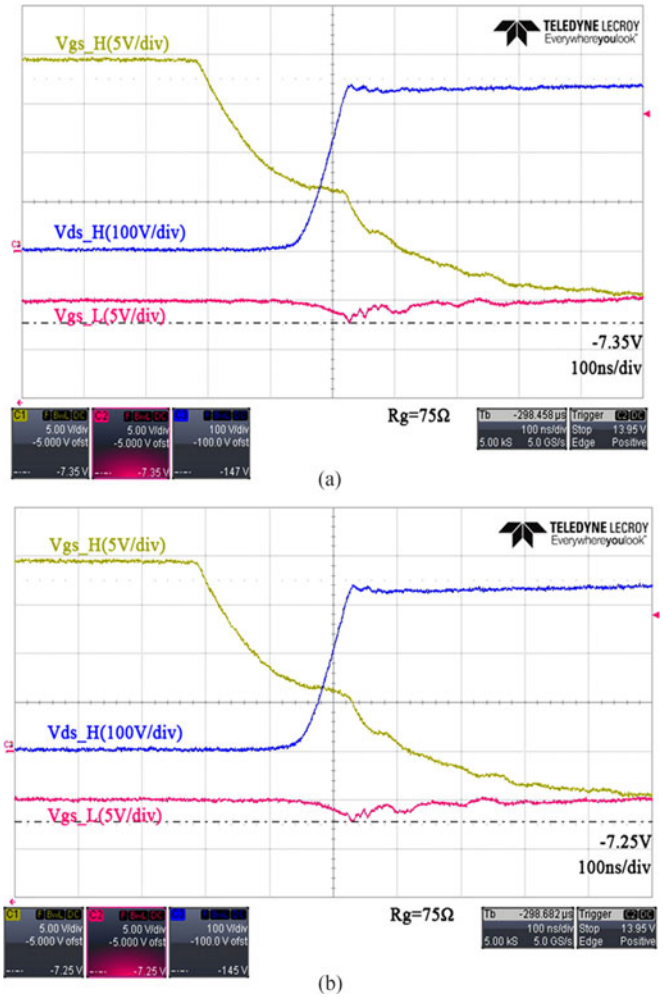


Fig. 28. Captured waveforms of switching-off process of the upper switch with a gate resistor of 75 Ω in (a) the most basic gate driver and (b) the proposed gate driver.

also conducted. The dc voltage was set to be 300 V and the load was varied. A diode is still antiparallel connected to the gate resistor to accelerate the switching-off process. Fig. 26 shows the measured peak value of negative gate voltage spikes under different inductive load currents for both gate drivers. It is noted that the proposed gate driver can still suppress the negative gate voltage spikes effectively even under the large load current.

This paper also verifies the performance of the proposed gate driver under the different gate resistance. The gate resistors of 22, 30, 51, and 75 Ω were assumed for both gate drivers, respectively. In order to find out the relationship between the gate resistor and the negative voltage spike, the antiparallel diode of gate resistor is removed in this set of experiment. Figs. 27 and 28 show the switching-off waveforms of two gate drivers under dc input voltage of 300 V with gate resistance of 22 and 75 Ω, respectively. The measured peak value of negative voltage spikes under different gate resistance are drawn in Fig. 29. It is noted that the negative voltage spikes of the most basic gate driver become small as the gate resistance increases, which is in agreement with the theoretical analysis in Section II. But the proposed gate driver can suppress the negative voltage spikes

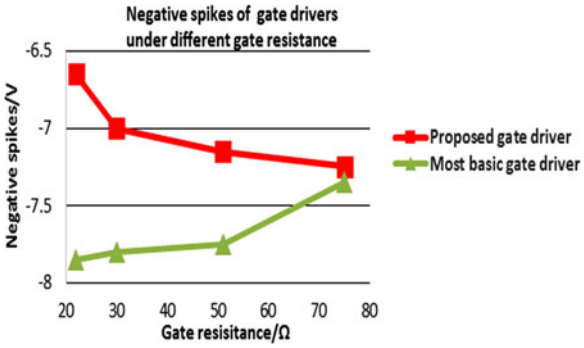


Fig. 29. Negative voltage spikes of both gate drivers under different gate resistance.

more effectively when the gate resistance is small because the small gate resistance will increase the driving current and then prolong the ON duration of passively controlled p-n-p transistor.

V. Conclusion

This paper proposes a novel gate driver of SiC MOSFET with a passive triggered auxiliary transistor. The auxiliary transistor will connect to a series capacitor into the gate circuit to suppress the negative gate voltage spikes upon the complementary switch turns OFF. Since the auxiliary transistor is controlled passively, the circuit configuration is simple. By employing a *RC* level shifter, the proposed gate driver can reduce the magnitude of positive gate voltage spikes and then fully satisfy the stringent driving requirements of SiC MOSFETs with high switching speed. The simulation and experimental results also validated the performance of the proposed gate driver.

References

[1] Z. Chen, Y. Yao, D. Boroyevich, K. D. T. Ngo, P. Mattavelli, and K. Rajashekara, "A 1200-V, 60-A SiC MOSFET multichip phase-leg module for high-temperature, high-frequency applications," *IEEE Trans. Power Electron.*, vol. 29, no. 5, pp. 2307–2320, May 2014.

[2] S. Safari, A. Castellazzi, and P. Wheeler, "Experimental and analytical performance evaluation of SiC power devices in the matrix converter," *IEEE Trans. Power Electron.*, vol. 29, no. 5, pp. 2584–2596, May 2014.

[3] J. A. Carr, D. Hotz, J. C. Balda, H. A. Mantooth, A. Ong, and A. Agarwa,"Assessing the impact of SiC MOSFETs on converter interfaces for distributed energy resourcess," *IEEE Trans. Power Electron.*, vol. 24, no. 1, pp. 260–270, Jan. 2009.

[4] X. Zhong, X. Wu, W. Zhou, and K. Sheng, "An all-SiC high-frequency boost DC-DC converter operating at 320˚C junction temperature," *IEEE Trans. Power Electron.*, vol. 29, no. 10, pp. 5091–5096, Oct. 2014.

[5] J. Biela, M. Schweizer, S. Wafer, and J. W. Kolar, "SiC versus Si evaluation of potentials for performance improvement of inverter and DC–DC converter systems by SiC power semiconductors," *IEEE Trans. Ind. Electron.*, vol. 58, no. 7, pp. 2872–2882, Jul. 2011.

[6] T. Zhao, J. Wang, A. Q. Huang, and A. Agarwal, "Comparisons of SiC MOSFET and Si IGBT based motor drive systems," in *Proc. IEEE Ind. Appl. Conf.*, Sep. 2007, pp. 331–335.

[7] Z. Wang, X. Shi, Y. Xue, L. M. Tolbert, F. Wang, and B. J. Blalock, "Design and performance evaluation of overcurrent protection schemes for silicon carbide (SiC) power MOSFETs," *IEEE Trans. Ind. Electron.*, vol. 61, no. 10, pp. 5570–5581, Oct. 2014.

[8] S. Jahdi, O. Alatise, P. Alexakis, L. Ran, and P. Mawby, "The impact of temperature and switching rate on the dynamic characteristics of silicon carbide schottky barrier diodes and MOSFETs," *IEEE Trans. Ind. Electron.*, vol. 62, no. 1, pp. 163–171, Jan. 2015.

[9] R. Singh and A. R. Hefner, "Reliability in SiC MOS devices," *Solid-State Electron.*, vol. 48, no. 10/11, pp. 1717–20, Oct./Nov. 2004.

[10] M. Kevin, "Challenges in SiC power MOSFET design," *Solid-State Electron.*,vol. 52, no. 9, pp. 1631–1635, Jul. 2008.

[11] "CMF20120D-silicon carbide power MOSFET," 2012. [Online]. Available: http://www.wolfspeed.com/downloads/dl/file/id/585/product/16/cmf20120d.pdf

[12] "C2M0040120D-silicon carbide power MOSFET," 2015. [Online]. Available: http://www.wolfspeed.com/downloads/dl/file/id/165/product/165/product/9/c2m0040120d.pdf

[13] Z. Zhang, F. Wang, L. M. Tolbert, and B. J. Blalock, "A gate assist circuit for cross talk suppression of SiC devices in a phase-leg configuration," in *Proc. IEEE Energy Convers. Congr. Expo.*, 2013, pp. 2536–2543.

[14] Z. Chen, M. Dailovic, D. Boroyevich, and Z. Shen, "Modulized design consideration of a general-purpose, high-speed phase-leg PEBB based on SiC MOSFETs," in *Proc. Eur. Power Electron. Appl. Conf.*, Aug. 2011, pp. 1–10.

[15] "Shoot-through in synchronous buck converters," Apr. 25, 2003. [Online].Available: http://www.fairchildsemi.com/application-notes/AN/AN-6003.pdf

[16] K. Ishikawa, K. Ogawa, S. Yukutake, N. Kameshiro, and Y Kono, "Traction Inverter that applies compact 3.3kV/1200A SiC hybrid module," in *Proc. 2014 Int. Power Electron. Conf.*, 2014, pp. 2140–2144.

[17] J. Wang and H. S. H. Chung, "A novel RCD level shifter for elimination of spurious turn-on in the bridge-leg configuration," *IEEE Trans. Power Electron.*, vol. 30, no. 5, pp. 976–984, Feb. 2015.

[18] Y. Zushi, S. Sato, K. Matsui, Y. Murakami, S. Tanimoto, "A novel gate assist circuit for quick and stable driving of SiC-JFETs in a 3-phase inverter," in *Proc. 27th Annu. IEEE Appl. Power Electron. Conf. Expo.*, 2012, pp. 1734–1739.

[19] Z. Zhang, F. Wang, L.M. Tolbert, and B. J. Blalock, "Active gate driver for crosstalk suppression of SiC devices in a phase-leg configuration," *IEEE Trans. Power Electron.*, vol. 29, no. 4, pp. 1986–1997, Apr. 2014.

[20] Q. Zhou, F. Gao, and T. Jiang, "A gate driver of SiC MOSFET with passive triggered auxiliary transistor in a phase-leg configuration," in *Proc. IEEE Energy Convers. Congr. Expo.*, 2015, pp. 7023–7030.

[21] H. Fujita, "A resonant gate-drive circuit with optically isolated control signal and power supply for fast-switching and high-voltage power semiconductor devices," *IEEE Trans. Power Electron.*, vol. 28, no. 11, pp. 5423–5430, Nov. 2013.

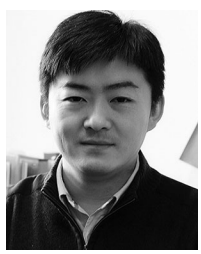
[22] M. Swamy, T. Kume, and N. Takada, "An efficient resonant gate-drive scheme for high-frequency applications," *IEEE Trans. Power Electron.*, vol. 48, no. 4, pp. 1418–1431, Jul. 2012.

[23] Q. Zhao and G. Stojcic, "Characterization of Cdv/dt induced power loss in synchronous buck DC-DC converters," *IEEE Trans. Power Electron.*, vol. 22, no. 4, pp. 1505–1513, Jul. 2007.

[24] M. E. Jacobs, K. J. Timm, and V. J. Thottuvelli, "Appartus and method for generating negative bias for isolated MOSFET gate-driver circuits," *EP Patent 0 693 825*, Jan. 2, 1996.

[25] J. Wang and H. Shu-Hung Chung, "Impact of parasitic elements on the spurious triggering pulse in synchronous buck converter," *IEEE Trans. Power Electron.*, vol. 29, no. 12, pp. 6672–6685, Dec. 2014.

[26] "ZXTP25140BFH PNP medium power transistor," 2006. [Online]. Available: http://www.diodes.com/ files/datasheets/ZXTP25140BFH.pdf



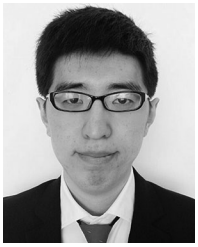
Feng Gao (S'07–M'09) received the B.Eng. and M.Eng. degrees in electrical engineering from Shandong University, Jinan, China, in 2002 and 2005, respectively, and the Ph.D. degree in electrical engineering from the School of Electrical and Electronic Engineering, Nanyang Technological University, Singapore, in 2009.

From September 2006 to February 2007, he was a Visiting Scholar in the Institute of Energy Technology, Aalborg University, Aalborg, Denmark. From 2008 to 2009, he was a Research Fellow in Nanyang Technological University. Since 2010, he has been with the School of Electrical Engineering, Shandong University, where he is currently a Professor and the Vice Dean.

Dr. Gao received the IEEE Industry Applications Society Industrial Power Converter Committee Prize for a paper published in 2006. He is currently an Associate Editor of the IEEE TRANSACTIONS ON POWER ELECTRONICS.

Qi Zhou received the B.Eng. and M.Eng. degrees in electrical engineering from Shandong University, Jinan, China, in 2013 and 2016, respectively.

He is currently at Jiangsu Electric Power Company Research Institute. His research interests include gate drivers of SiC MOSFET, dc–dc converters, and control strategies.



Panrui Wang received the B.Eng. degree in electrical engineering from Shandong University, Jinan, China, in 2016, where he is currently working toward the M.Eng. degree in electrical engineering.

His research interests include semiconductor device modeling and gate driver design of SiC MOSFET.

Chenghui Zhang (M'14) was born in China in 1963. He received the B.S. and M.S. degrees in electrical engineering from Shandong University of Technology, Jinan, China, in 1985 and 1988, respectively, and the Ph.D. degree in electrical engineering from Shandong University, Jinan, China, in 2001.

In 1988, he joined Shandong University, where he is currently a Full Professor in the School of Control Science and Engineering and the Director of the Research Center of Power Electronics Energy-Saving Technology and Equipment of the Chinese Education Ministry. His current research interests include optimal control of engineering, power electronics and motor drives, and energy-saving techniques.

Prof. Zhang was selected as a Changjiang Scholar of the Education Ministry and a Taishan Scholar of Shandong Province in 2009.