# Virtual Direct Power Control Scheme of Dual Active Bridge DC–DC Converters for Fast Dynamic Response

Wensheng Song, *Member, IEEE*, Nie Hou, and Mingyi Wu

***Abstract*—One of the essential requirements for high-performance dual active bridge (DAB) dc–dc converters as the controlled dc voltage sources is to obtain the constant output voltage rapidly and accurately under all working conditions. In order to reach fast dynamic response, combing direct power control with feedforward control strategy, this paper proposes a virtual direct power control (VDPC) scheme with single-phase-shift control for DAB dc–dc converters to face with these following extreme conditions, such as start-up, load step-change, no-load, the input voltage fluctuation, and the desired output voltage step-change. The proposed VDPC scheme of DAB dc–dc converters can achieve no overshoot and fast transient response for the output voltage in load or input voltage disturbances and start-up stage. Dynamic response of the output voltage control has been also improved when the desired value steps up and down. Finally, four control schemes consisting of traditional voltage loop control, load current feed-forward control, model-based phase-shift control, and the proposed VDPC schemes are compared and tested in a scale-down DAB dc–dc converter experimental prototype. Experimental results verify the above excellent performance of the proposed VDPC scheme and the effectiveness of theoretical analysis.**

***Index Terms*—Dual active bridge (DAB) dc–dc converter, fast dynamic response, phase-shift control, virtual direct power control (VDPC).**

## I. Introduction

AT THE beginning of the 1990s, the dual active bridge (DAB) dc–dc converter was first proposed in [1], as shown in Fig. 1. Due to these benefits of high power density, zero-voltage switching, bidirectional power flow capability, and the convenience of cascading and paralleling, DAB dc–dc converters have attracted more and more attention in the modern power systems, energy conversion, and storage application, such as distributed generating systems [2]–[4], automotive applications [5]–[9], energy storage systems [10], [11], and power electronic transformer in railway traction applications [12], [13]. DAB dc–dc converter is now becoming a very popular topology for high-power isolation power conversion application.

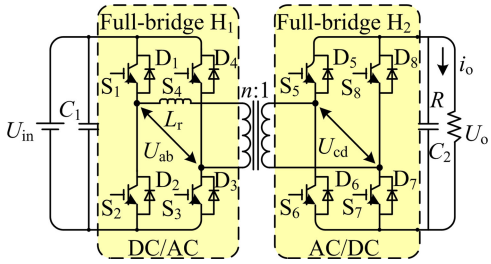


Fig. 1. Topology of DAB dc–dc converters.

Obviously, in the above applications, DAB dc–dc converters may suffer some extreme conditions, such as the input voltage fluctuation, the output load distribution, no-load conditions, and so on. Thus, the robust and fast dynamic response is an essential requirement for DAB dc–dc converters in industry application. Many researchers have focused on searching various advance control schemes to enhance the dynamic response and static performance. For example, in order to analyze the dynamic characteristics, small-signal modeling methods of DAB dc–dc converters [14]–[16] have been described in detail to develop the discrete-time average model. In addition, on the basis of state-space average modeling and small-signal modeling schemes for DAB dc–dc converters, a novel model-based phase-shift (MPS) control has been proposed to improve the dynamic characteristics of DAB dc–dc converters in the load disturbance condition [17], [18].

Meanwhile, by developing a linearized dynamic model of DAB dc–dc converters, [19] presents a feedforward compensation strategy with load current to improve the output transient response of the adopted converters in the load disturbance condition. In [19], the lookup table solution is adopted to realize the feedforward compensation strategy. But it is not easy to be realized in real time and online. A boundary control scheme by using the natural switching surface, is reported in [20] for DAB dc–dc converters, which is an excellent control scheme for dealing with various dynamic change conditions. And these excellent dynamic behaviors can be achieved, such as no overshoot, fast transient response for start-up and load disturbances, and reaching steady state within few switching actions. However, the proposed method belongs to variable frequency control

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The authors are with the School of Electrical Engineering, Southwest Jiaotong University, Chengdu 610031, China (e-mail: songwsh@swjtu.edu.cn; nie_hou@126.com; 1536689170@qq.com).

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schemes and the transformer saturation will occur. Transformer saturation is a critical issue in this control scheme. But in constant frequency control scheme, if the parameter and structure of the high-frequency transformer are designed appropriately, the transformer saturation can be easily avoided [21], [22].

In addition, the load current feed-forward (LCFF) control is an alternative solution [23], [24] to improve dynamic performance for load change. In order to achieve robust dynamic response of DAB dc–dc converters, the direct power control can be an effective approach, which has been widely applied and reported for the front-active rectifiers [25], [26] and grid-side inverters in renewable generation system [27], [28]. How to quickly reach the desired output power is the essential requirement of dynamic control for most converters. Thus, direct power control will be a better choice, compared with the load feedforward control.

In view of the studies mentioned above, focusing on direct power control, this paper presents a simple virtual direct power control (VDPC) scheme, which is easily implemented as constant frequency control for DAB dc–dc converters to improve the dynamic response. Based on the traditional single-phase-shift (SPS) control, the VDPC scheme is analyzed in details. In the executing procedure of the proposed VDPC scheme, three quantities consisting of the output voltage, input voltage and the load current should be measured and sampled. Fortunately, some circuit parameters such as the inductor value, the transformer conversion ratio, and the switching period are not necessary. Then, an experimental comparison of the traditional voltage loop (TVL) control, the LCFF control deriving from the existing current feedforward control [23], [24], the MPS control [17], [18], and the proposed VDPC schemes for DAB dc–dc converters is shown to illustrate the salient features and the superior performance of the proposed VDPC scheme. In addition, the proposed VPDC scheme in the no-load operation condition is tested in the experimental platform.

The paper is organized in the following manner. In Section I, an introduction is stated. In Section II, the SPS control and the MPS control are analyzed in detail. On the basis of the traditional SPS control, the VDPC scheme is proposed and discussed in Section III. The experimental comparison results of four control schemes are shown and discussed to verify the effectiveness of theoretical analysis in Section V, followed by a conclusion in Section VI.

## II. Switching Mode Analysis of SPS Control and the MPS control

The equivalent topology of DAB dc–dc converters with the phase-shift control is shown in Fig. 2, where $L$ represents the total inductance of the transformer leakage inductor and the auxiliary inductor $L_r$; $U_{\rm ab}$ and $U_{\rm cd}$ are the output pulse voltage of H1-bridge and the input pulse voltage of H2-bridge, respectively; $U_L$ and $i_L$ are the voltage and current of inductor $L$, respectively; and $n$ represents turns ratio of the isolated transformer.

The main characteristic waveforms of SPS control for DAB dc–dc converters with different initial values of inductor current $i_{\rm L}(t_0)$ are shown in Fig. 3, where $T_{\rm s}$ represents a switching

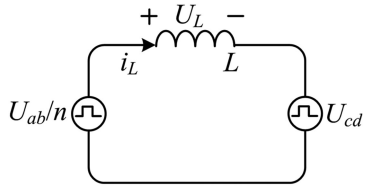


Fig. 2. Equivalent circuit of DAB dc–dc converters with phase-shift control.

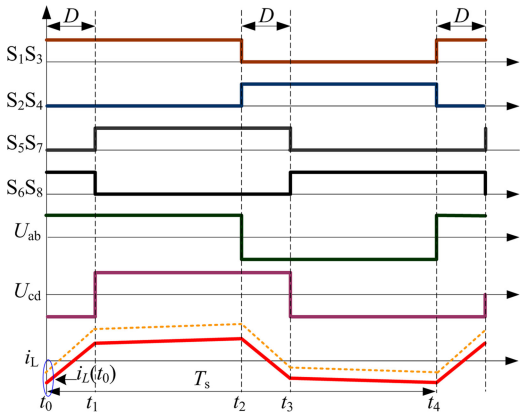


Fig. 3. Main characteristic waveforms of SPS control scheme for DAB dc–dc converters.

interval, $D$ is defined as the phase-shift ratio. The direction and the magnitude of the power flow can be adjustable and relative to phase-shift ratio $D$.

Then, the transmission power can be expressed as

$$P = \frac{1}{T_s}\int_{t_0}^{t_4} U_{\rm ab}(t) i_{\rm L}(t) dt. \tag{1}$$

For different initial values of the inductor current $i_{\rm L}(t_0)$, the transmission power can be expressed as

$$\begin{aligned} P &= \frac{1}{T_s}\int_{t_0}^{t_4} U_{\rm ab}(t)(i'_{\rm L}(t) - I)dt \\ &= \frac{1}{T_s}\int_{t_0}^{t_4} U_{\rm ab}(t) i'_{\rm L}(t) - U_{\rm ab}(t) I dt \end{aligned} \tag{2}$$

where $i'_{\rm L}(t)$ represents the ac component of inductor current $i_L$, and $I$ is the dc component of current $i_L$. Because the wave shape of the output voltage $U_{\rm ab}(t)$ of $\rm H_1$ bridge presents as the symmetrical square-wave during positive and negative half-period, the absolute value of $U_{\rm ab}(t)$ equals the input voltage $U_{\rm in}$. Thus, the integral value of component $U_{\rm ab}(t)$ $I$ in the right-had side of (2) is zero, and the transmission power $P$ is relative to $U_{\rm in}$, $U_o$ and $D$, shown as

$$P = \frac{U_{\rm in} U_o D(1-D) T_s}{2nL}. \tag{3}$$

Obviously, the transmission power $P = U_{\rm o}^2/R$. Thus, combining with (3), the output voltage $U_o$ can be expressed as

$$U_o = \frac{U_{\rm in} D(1-D) T_s R}{2nL}. \tag{4}$$

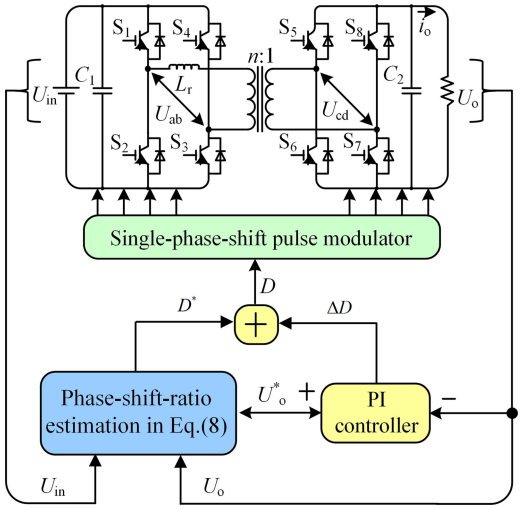


Fig. 4. Block diagram of the MPS control with input voltage feedforward for DAB dc–dc converters.

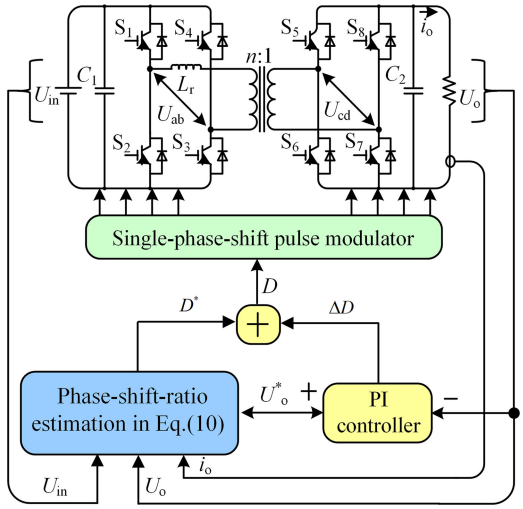


Fig. 5. Block diagram of the MPS control scheme with the output current and input voltage feedforward for DAB dc–dc converters [17], [18].

The desired phase-shift ratio $D^*$ is derived from (4) and expressed as

$$D^* = \frac{1-\sqrt{1-8LU_o^*/nRU_{\rm in}T_s}}{2} \tag{5}$$

where the load resistance $R$ should be estimated online, and is deduced from (5) as

$$R = \frac{2LU_o}{nU_{\rm in}D(1-D)T_s} = \frac{2L}{nT_s}\frac{U_o}{U_{\rm in}D(1-D)}. \tag{6}$$

In addition, in the real power converter system, because of the large supporting capacitor $C_2$, the output voltage does not vary with the changed resistance value, immediately. Thus, this retardation will influence the dynamic performance of load resistance estimation, especially in load step change condition.

In the MPS control [17], [18], it is obvious that these parameters such as inductance $L$, the transformer turn ratio $n$, and the switching cycle $T_{\rm s}$ can be eliminated by combining (5) and (6). Thus, the virtual load resistance $R_{\rm v}$ can be defined and expressed as

$$R_v = \frac{U_o}{U_{\rm in}D(1-D)} = \frac{nT_S}{2L}R. \tag{7}$$

Substituting the resistance $R$ of (7) into (5) yields

$$D^* = \frac{1-\sqrt{1-4U_o^*/R_vU_{\rm in}}}{2}. \tag{8}$$

It is clear from (8) that the desired phase-shift ratio $D*$ is independent of the inductor $L$, the transformer turns ratio $n$, and the switching cycle $T_s$.

The control block diagram of the MPS control scheme with input voltage feedforward [17], [18] is shown in Fig. 4. A proportional-integral (PI) controller is adopted to improve the dynamic response of the output voltage control. And the output of the PI controller $\triangle D$ is added to the desired phase-shift ratio $D*$ as the phase-shift ratio $D$, which is expressed as follows:

$$D = D^* + \Delta D. \tag{9}$$

According to the MPS control, the load resistance can be expressed as $R = U_{\rm o}/i_{\rm o}$. And substituting it into (5), the phase-shift ratio $D^*$ can be expressed as the following equation by gathering the load current $i_o$:

$$D^* = \frac{1-\sqrt{1-8LU_o^*i_o/nU_oU_{\rm in}T_s}}{2}. \tag{10}$$

Moreover, the control block of the MPS control scheme with the load current and input voltage feedforward is shown as Fig. 5.

According to the sampling input voltage $U_{\rm in}$, output voltage $U_o$ and load current $i_o$ and the inductor value $L$, the switching cycle $T_s$ and the transformer turn ratio $n$, the phase-shift ratio $D^*$ can be estimated from (10) to improve the dynamic performance of DAB dc–dc converters. However, in order to obtain the high precise phase-shift ratio $D^*$, these parameters should be very accurate. Otherwise, the dynamic performance will be deteriorated.

## III. Proposed VDPC Scheme

In order to improve the dynamic response of DAB dc–dc converters, the direct power control is one effective solution. According to the principle of direct power control, if the desired output power can be reached immediately, the excellent dynamic performance can be achieved. Thus, in order to meet the desired output power requirement, the relationship between the input transmission power and the output power should be described.

In the actual converter application, power losses of the DAB dc–dc converter cannot be ignored, and there exists a difference between the input power and the output power. So, the required transmission power $P^*$ cannot be simply expressed as the arithmetic product of the desired output voltage $U_o^*$ and current $i_o^*$. Thus, a virtual power control is adopted to compensate this power difference caused by power losses and voltage drops of power switches. Due to the bidirectional power flow operation mode of DAB dc–dc converters, the unified transmission power

reference $p^*$ can be expressed as follows:

$$p^* = |U_v^*|\, i_o^* \tag{11}$$

where $U_v^*$ is named as the virtual desired output voltage, which is the output value of the PI controller. And the desired output current $i_o^*$ can be described as follows:

$$i_o^* = \frac{U_o^*}{U_o} i_o. \tag{12}$$

Substituting (12) into (11) yields

$$p^* = \frac{|U_v^*|\, U_o^* i_o}{U_o}. \tag{13}$$

The control goal is to achieve the transmission power $p$ to reach its reference value $p^*$. According to (3) and considering the regeneration condition, the transmission power $P$ can be unified as $p$ in SPS control mode without these constant parameters, such as $L$, $T_s$, and $n$

$$p = \frac{U_{\text{in}} U_o D(1 - |D|)}{2}. \tag{14}$$

Combining (13) and (14), in order to ensure that the unified transmission power $p$ reaches the unified power reference $p^*$ ($p = p^*$), phase-shift ratio $D$ can be derived as follows:

$$D = \begin{cases} \dfrac{1}{2} - \sqrt{\dfrac{1}{4} - \dfrac{U_o^* U_v^* i_o}{U_o^2 U_{\text{in}}}} & (i_o \geq 0) \\ -\dfrac{1}{2} + \sqrt{\dfrac{1}{4} + \dfrac{U_o^* |U_v^*|\, i_o}{U_o^2 U_{\text{in}}}} & (i_o < 0) \end{cases}. \tag{15}$$

From (15), the virtual desired output voltage $U_v^*$ should satisfy the following range as

$$|U_v^*| \in \left[0, \left|\frac{U_o^2 U_{\text{in}}}{4 U_o^* i_o}\right|\right]. \tag{16}$$

The virtual desired output voltage $U_v^*$ can be generated from a voltage PI controller, which is adopted to adjust the output voltage. According to (15), the control block diagram of the VDPC scheme can be illustrated in Fig. 6. In the VDPC scheme shown as Fig. 6, at the beginning of each sampling or control interval, the control system should sample the output voltage $U_o$, the input voltage $U_{\text{in}}$, and the load current $i_o$. The output value of PI-based voltage controller is set as the virtual desired output voltage $U_v^*$. Then, with respect to the desired output voltage $U_o^*$, the desired virtual output voltage $U_v^*$, the input voltage $U_{\text{in}}$, and the load current $i_o$, the mathematical expression of phase-shift ratio $D$ can be described and shown as (15). Finally, the switching drive signals can be generated from the SPS modulator with the phase-shift ratio $D$. Note that the idea of the proposed VDPC can be also extended to combine with dual-phase-shift [29], extended-phase-shift [4], and triple-phase shift [30] control schemes. Due to the paper length limitation, these expressions of phase-shift ratios will not be deduced and reported in this paper.

Unlike the MPS scheme in Fig. 5, these parameters including the inductance $L$, transformer ratio $n$, and the switching cycle $T_s$ are not necessary in the VDPC scheme. The proposed VDPC method is not sensitive to these parameters. Moreover, even if the proportionalities of these sampling values between the converter and the control system are not accurate, the dynamic performance of the VDPC scheme will not be affected. For example, if there exists an inaccurate proportionality of the sampling input voltage, the virtual desired output voltage will be correspondingly adjusted from the PI controller to obtain the desired output voltage. Thus, the VDPC scheme is also not sensitive to the sampling proportionalities of sensors.

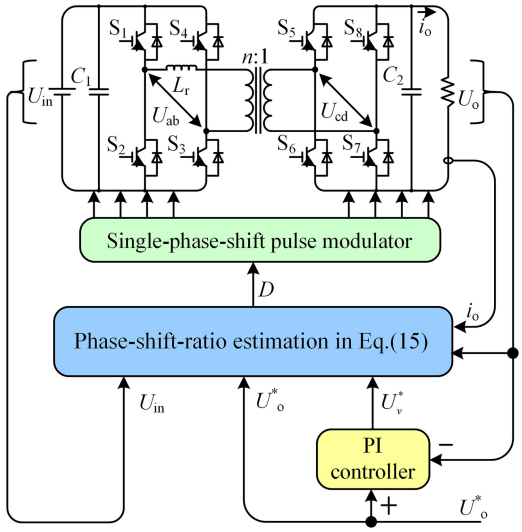


Fig. 6. Block diagram of the proposed VDPC scheme for DAB dc–dc converters.

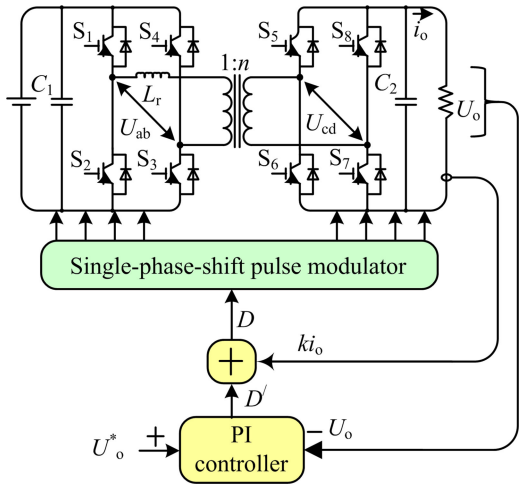


Fig. 7. Block diagram of the LCFF control for DAB converters.

In addition, the TVL control is to adopt the output voltage PI controller to produce the phase-shift ratio directly. Depending on the existing current feedforward control [23], [24] and combing with TVL control idea, the block diagram of the LCFF control is shown in Fig. 7. In the LCFF control scheme, the phase-shift ratio $D$ can be expressed as follows:

$$D = D' + k i_o \tag{17}$$

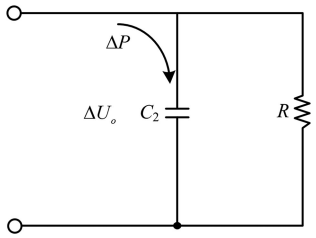


Fig. 8. Equivalent circuit of the output circuit of the DAB system.

where *k* is the feedforward ratio of the load current $i_o$. By using the LCFF, the adopted converter can achieve a better dynamic response under the load change.

## IV. Small-Signal Modeling and Disturbance Analysis of the VDPC Scheme

The phase-shift ratio in the VDPC scheme is directly estimated and free of the PI controller. Thus, the system stability is mainly affected by the sampled output voltage, input voltage, and load current, involved in the calculation rather than the PI controller. The PI controller is used to compensate the difference between the calculation model and physical systems. Thus, in this section, the effect on the output voltage of these disturbances in the sampled output voltage, input voltage, and load current is discussed in steady state by small-signal model analysis. These sampling voltage and current disturbances are caused by those voltage and current sensors and sensor interface circuits.

Assuming the sampled input voltage and load current are accurate and there is a small-signal perturbation $\hat{U}_o$ in the output voltage, because $\hat{U}_o$is small enough, the calculated phase-shift value $D^{/}_{U_o}$ can be expressed as follows:

$$D^{/}_{U_o} = D + \hat{D} = D + \frac{\partial D}{\partial U_o}\hat{U}_o. \tag{18}$$

According to (15), the partial derivative of phase-shift value *D* with respect to the output voltage $U_o$ can be expressed as

$$\frac{\partial D}{\partial U_o} = -\frac{U_o^* U_v^* i_o}{U_o^3 U_{\text{in}}}\left(\frac{1}{4} - \frac{U_o^* U_v^* i_o}{U_o^2 U_{\text{in}}}\right)^{\frac{1}{2}}. \tag{19}$$

In addition, the controlled transmission power can be expressed as

$$P^{/} = P + \Delta P = \frac{U_{\text{in}}(U_o + \hat{U}_o)(D + \hat{D})[1 - (D + \hat{D})]}{2} \tag{20}$$

where $\Delta P$ is the power ripple, neglecting the higher order perturbation, the controlled transmission power can be further expressed as

$$\begin{aligned} P^{/} &= P + \Delta P \\ &\approx \frac{U_{\text{in}} U_o D(1-D)}{2} + \frac{U_{\text{in}}(U_o\hat{D} + D\hat{U}_o - 2U_o D\hat{D} - D^2\hat{U}_o)}{2}. \end{aligned} \tag{21}$$

The secondary of the DAB system can be simplified [31], as shown in Fig. 8. In this equivalent circuit, when the power ripple is delivered to the RC network, the output voltage will be charged from $U_o$ to $U_o'$, and $U_o'$ is the final output voltage value. The output power ripple can be expressed as

$$\begin{aligned} \Delta P &\approx \frac{1}{2}C_2(U_0'^2 - U_0^2) = \frac{1}{2}C_2(U_o' + U_o)(U_o' - U_0) \\ &= \frac{1}{2}C_2(\Delta U_o + U_o + U_o)(\Delta U_o + U_o - U_0) \\ &= \frac{1}{2}C_2(\Delta U_o + 2U_o)\Delta U_o \approx U_o C_2 \Delta U_o \end{aligned} \tag{22}$$

where the $\Delta U_o$ is the output voltage fluctuation, and expressed as

$$\Delta U_o = \frac{\Delta P}{U_o C_2}. \tag{23}$$

Combining (19), (21), and (23), the output voltage fluctuation $\Delta U_o$, which is caused by the perturbation value $\hat{U}_o$, can be further expressed as

$$\begin{aligned} \Delta U_o &= \frac{\Delta P}{C_2 U_o} \\ &= \frac{\left[-\frac{U_o^* U_v^* i_o}{U_o^2 U_{\text{in}}}\left(\frac{1}{4} - \frac{U_o^* U_v^* i_o}{U_o^2 U_{\text{in}}}\right)^{\frac{1}{2}} + D\right] U_{\text{in}}}{2C_2 U_o}\hat{U}_o \\ &\quad + \frac{\left[2\frac{U_o^* U_v^* i_o}{U_o^2 U_{\text{in}}}\left(\frac{1}{4} - \frac{U_o^* U_v^* i_o}{U_o^2 U_{\text{in}}}\right)^{\frac{1}{2}} D - D^2\right] U_{\text{in}}}{2C_2 U_o}\hat{U}_o. \end{aligned} \tag{24}$$

Similarly, assuming the sampling output voltage and load current are accurate and these is a perturbation $\hat{U}_{\text{in}}$ in the input voltage, the partial derivative of phase-shift value *D* with respect to the input voltage $U_{\text{in}}$ can be expressed as

$$\frac{\partial D}{\partial U_{\text{in}}} = -\frac{U_o^* U_v^* i_o}{2U_o^2 U_{\text{in}}^2}\left(\frac{1}{4} - \frac{U_o^* U_v^* i_o}{U_o^2 U_{\text{in}}}\right)^{-\frac{1}{2}}. \tag{25}$$

Then, the output voltage fluctuation caused by the perturbation value $\hat{U}_{\text{in}}$, can be expressed as

$$\begin{aligned} \Delta U_o &= \frac{\left[-\frac{U_o^* U_v^* i_o}{2U_o^2 U_{\text{in}}^2}\left(\frac{1}{4} - \frac{U_o^* U_v^* i_o}{U_o^2 U_{\text{in}}}\right)^{\frac{1}{2}} + D\right]}{2C_2}\hat{U}_{\text{in}} \\ &\quad + \frac{\left[\frac{U_o^* U_v^* i_o}{U_o^2 U_{\text{in}}^2}\left(\frac{1}{4} - \frac{U_o^* U_v^* i_o}{U_o^2 U_{\text{in}}}\right)^{\frac{1}{2}} D - D^2\right]}{2C_2}\hat{U}_{\text{in}}. \end{aligned} \tag{26}$$

Assuming the sampling output voltage and the load current are accurate and these is a perturbation $\widehat{i_o}$ in the load current value, the partial derivative of phase-shift value *D* to the load current $i_{\text{o}}$ can be expressed as

$$\frac{\partial D}{\partial i_o} = \frac{U_o^* U_v^*}{2U_o^2 U_{\text{in}}}\left(\frac{1}{4} - \frac{U_o^* U_v^* i_o}{U_o^2 U_{\text{in}}}\right)^{\frac{1}{2}}. \tag{27}$$

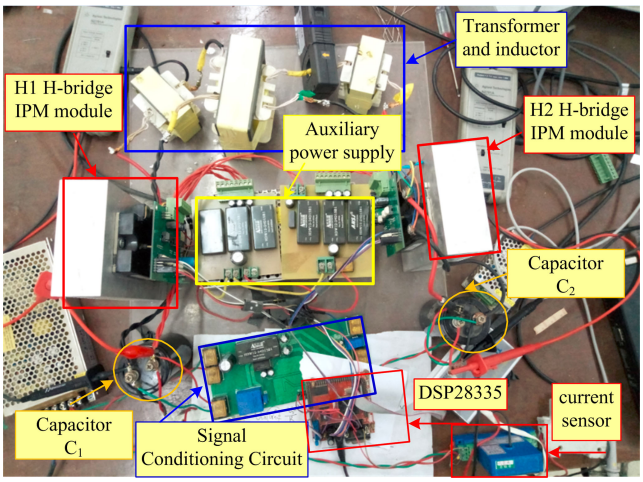


Fig. 9. Photo of the experimental hardware prototype.

Then, the output voltage ripple caused by the perturbation value $\widehat{i}_o$, can be expressed as

$$\Delta U_o = \frac{U_o^* U_v^*}{4C_2 U_o^2}\left(\frac{1}{4} - \frac{U_o^* U_v^* i_o}{U_o^2 U_{\text{in}}}\right)^{\frac{1}{2}}(1-2D)\widehat{i}_o. \tag{28}$$

In the steady state, the output voltage $U_o$ is approximately equal to the desired output voltage $U_o^*$, and combing (24), (26), and (28), and these disturbances in $U_{\text{in}}$, $U_o$, and $i_o$ cannot change the power transmission straightway and influence others. Thus, the output voltage fluctuation $\Delta U_o$ can be further expressed in (29) shown at the bottom of the page.

According to (29), the output voltage ripple $\Delta U_o$ is relative to these perturbation values $\hat{U}_o$, $\hat{U}_{\text{in}}$, and $\hat{i}_o$. Thus, in order to reduce the output voltage ripple of the DAB dc–dc converter, the input voltage $U_{\text{in}}$, the output voltage $U_o$, and load current $i_o$ should be accurately sampled. In addition, it is clear from (29) that the large capacitor $C_2$ can reduce the sampling errors effect on the output voltage ripple, due to these perturbations in the sampling voltage and currents.

## V. Experimental Analysis

In order to verify the aforementioned theoretical analysis, an experimental hardware prototype of the DAB dc–dc converter is designed with TMS320F28335 DSP controller of Texas Instruments. And the photo of experimental prototype [30] is shown in Fig. 9. And electrical parameters of the adopted DAB dc–dc converter are listed in Table I.

The experimental test is described as follows: First, an experimental comparison of the proposed VDPC scheme and the MPS control [17], [18], the LCFF control and the TVL control is carried out. And then, in order to test the parameter sensitiveness of the proposed VDPC scheme, an experimental comparison of the proposed VDPC scheme and the MPS scheme [17], [18], in Fig. 5, is shown and discussed under a parameter mismatch condition. Moreover, the VPDC scheme is tested under no-load operation condition in the experimental platform.

TABLE I
Electrical Parameters of the Experimental Prototype

| Parameters | Values |
|---|---|
| Transformer turn ratio | $n = 1$ |
| Auxiliary inductor | $L_r = 0.2$ mH |
| Switching frequency | $f_s = 10$ kHz |
| Input-side capacitor | $C_1 = 2.2$ mF |
| Output-side capacitor | $C_2 = 2.2$ mF |
| Resistive load | $R = 20\,\Omega$ |

### A. Dynamic Response Comparison of the TLV Control, MPS Control, LCFF Control, and the VDPC Schemes

When the experimental parameters are set as $R = 15\ \Omega$, $U_{\text{in}} = 60$ V, and $U_o^* = 49$ V, Fig. 10 shows the transient experimental results of the DAB dc–dc converter system during start-up process. From Fig. 10(a)–(d), the charging time of the output capacitor during start-up process is 304 ms in TVL control, 416 ms in LCFF control, 440 ms in MPS control, and 100 ms in the proposed VDPC scheme, respectively. It is clear that the proposed VDPC scheme can reach the steady state with the shortest charging time. And the longest charging time exists in the MPS control.

When the experimental parameters are set as $R = 20\ \Omega$ and $U_o^* = 49$ V, Figs. 11 and 12 show the transient experimental results of the DAB dc–dc converter system with the input voltage step-change, where the input voltage $U_{\text{in}}$ steps down from 66 to 58 V in Fig. 11, and conversely in Fig. 12. Form Figs. 11 and 12, the TVL control [see Figs. 11(a) and 12(a)] and the LCFF control [see Figs. 11(b) and 12(b)] take a long settling time over 150 ms in both the input voltage step-down and step-up conditions for the output voltage to reach the desired value. Furthermore, in the MPS scheme [see Figs. 11(c) and 12(c)] and the VDPC scheme [see Figs. 11(d) and 12(d)], the output voltage is almost unchanged when the input voltage steps up and down. Thus, the MPS control and the VDPC scheme can keep the output voltage constant, and achieve excellent dynamic behavior when the input voltage changes.

$$\Delta U_o = \frac{\left[-\frac{U_v^* i_o}{U_o U_{\text{in}}}\left(\frac{1}{4}-\frac{U_v^* i_o}{U_o U_{\text{in}}}\right)^{\frac{1}{2}} + D + 2\frac{U_v^* i_o}{U_o U_{\text{in}}}\left(\frac{1}{4}-\frac{U_v^* i_o}{U_o U_{\text{in}}}\right)^{-\frac{1}{2}} D - D^2\right] U_{\text{in}}}{2C_2 U_o}\hat{U}_o + \frac{U_v^*}{4C_2 U_o}\left(\frac{1}{4}-\frac{U_v^* i_o}{U_o U_{\text{in}}}\right)^{\frac{1}{2}}(1-2D)\widehat{i}_o$$
$$+ \frac{\left[-\frac{U_v^* i_o}{2U_o U_{\text{in}}^2}\left(\frac{1}{4}-\frac{U_v^* i_o}{U_o U_{\text{in}}}\right)^{\frac{1}{2}} + D + \frac{U_v^* i_o}{U_o U_{\text{in}}^2}\left(\frac{1}{4}-\frac{U_v^* i_o}{U_o U_{\text{in}}}\right)^{\frac{1}{2}} D - D^2\right]}{2C_2}\hat{U}_{\text{in}}. \tag{29}$$

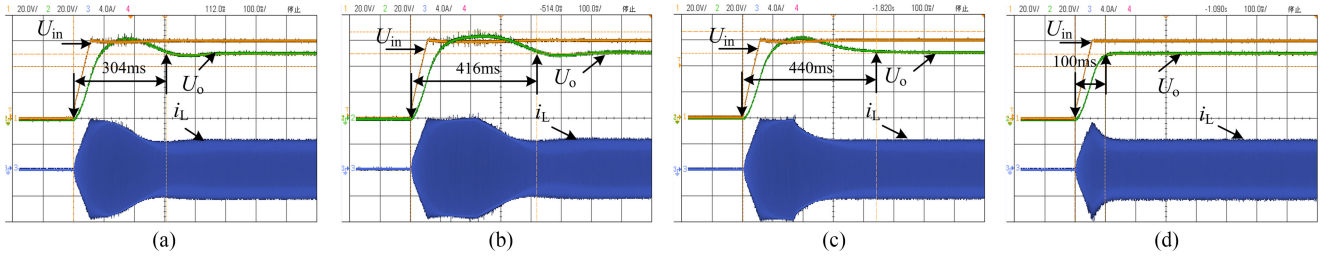


Fig. 10. Experimental results during the start-up process. (a) TVL, (b) LCFF, (c) MPS, (d) VDPC ($U_{\rm in}$ and $U_{\rm o}$: 20 V/div; $i_{\rm L}$: 4 A/div; Time: 100 ms/div).

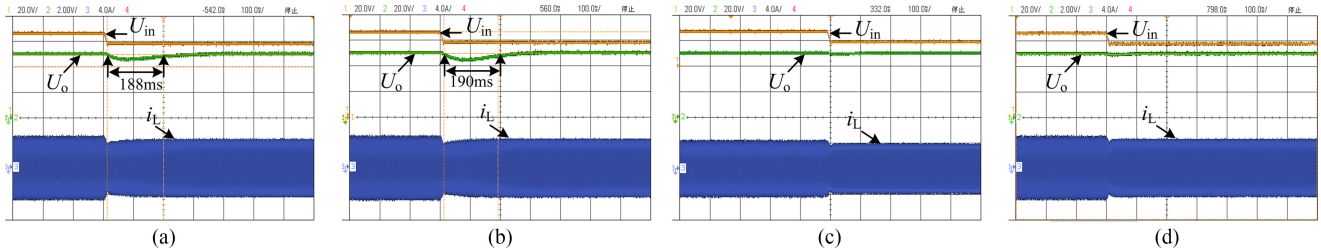


Fig. 11. Experimental results when the input voltage steps down from 66 to 58 V. (a) TVL, (b) LCFF, (c) MPS, (d) VDPC ($U_{\rm in}$ and $U_o$: 20 V/div; $i_L$: 4 A/div; Time: 100 ms/div).

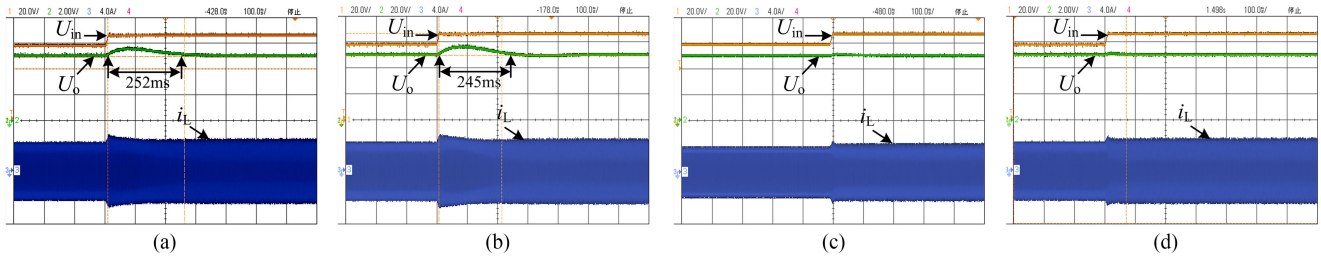


Fig. 12. Experimental results when the input voltage steps up from 58 to 66 V. (a) TVL, (b) LCFF, (c) MPS, (d) VDPC ($U_{\rm in}$ and $U_o$: 20 V/div; $i_L$: 4 A/div; Time: 100 ms/div).

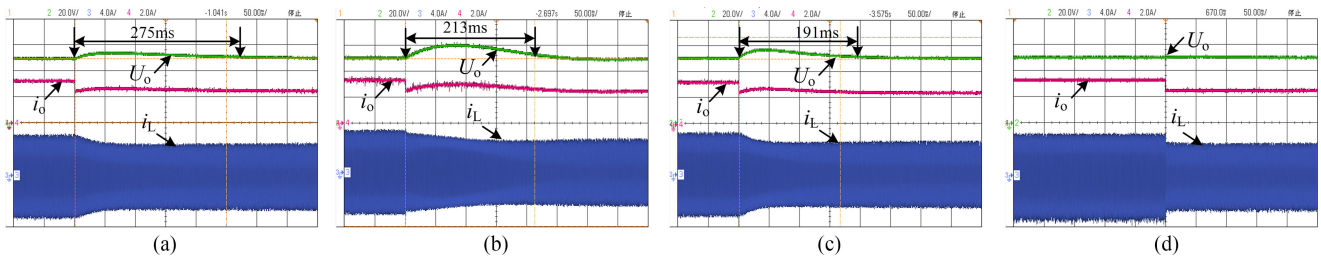


Fig. 13. Experimental results when the load steps from 15 to 20 Ω. (a) TVL, (b) LCFF, (c) MPS, (d) VDPC ($U_o$: 20 V/div; $i_L$: 4 A/div; $i_o$: 2 A/div; Time: 50 ms/div).

When the input voltage and the desired output voltage are set as $U_{\rm in} = 70$ V and $U_o^* = 49$ V, Figs. 13 and 14 show the experimental results of the DAB dc–dc converter with the resistive load step-change, where the load resistance steps from 15 to 20 Ω in Fig. 13, and conversely in Fig. 14. From Figs. 13 and 14, in the TVL control, when the load steps change, the transient response of the output voltage is very slow [see Figs. 13(a) and 14(a)], with a long settling time over 250 ms in both the load step-down and step-up conditions, and the LCFF control [see Figs. 13(b) and 14(b)] and the MPS control [see Figs. 13(c) and 14(c)] can reduce the settling time to be below 220 ms. More importantly, in the VDPC scheme [see Figs. 13(c) and 14(c)], the output voltage is almost unchanged in the load step variation. Thus, the VDPC scheme can keep the output voltage constant, and achieve an excellent dynamic behavior when the load steps up or down.

When the experimental parameters are set as $R = 20$ Ω, $U_{\rm in} = 60$ V, Fig. 16 shows the transient experimental results of the DAB dc–dc converter system under the desired output voltage step-change condition, where the desired output voltage

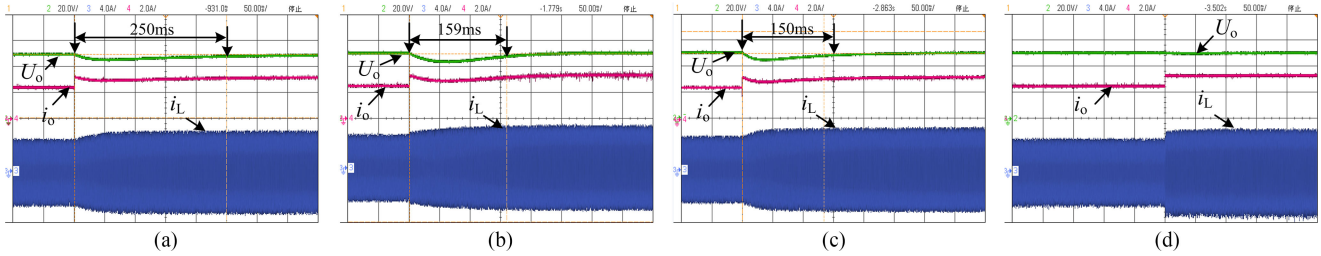


Fig. 14. Experimental results when the load steps from 20 to 15 Ω. (a) TVL, (b) LCFF, (c) MPS, (d) VDPC ($U_o$: 20 V/div; $i_L$: 4 A/div; $i_o$: 2 A/div; Time: 50 ms/div).

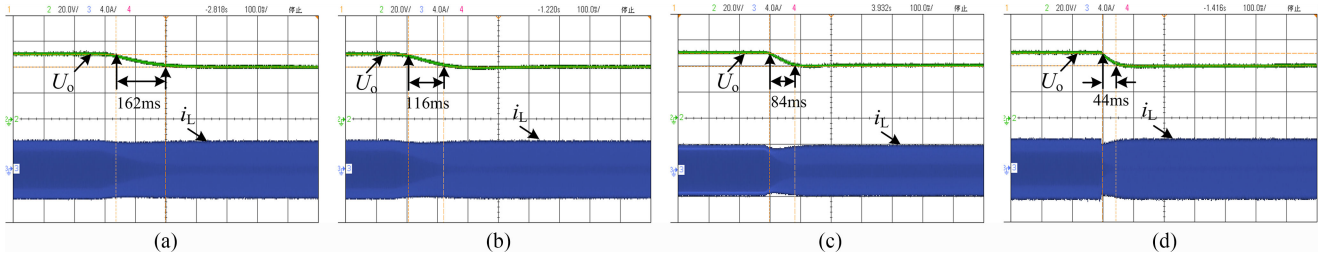


Fig. 15. Experimental results when the desired output voltage steps from 49 V to 40 V. (a) TVL, (b) LCFF, (c) MPS, (d) VDPC. ($U_o$: 20 V/div; $i_o$: 4 A/div; Time: 100 ms/div).

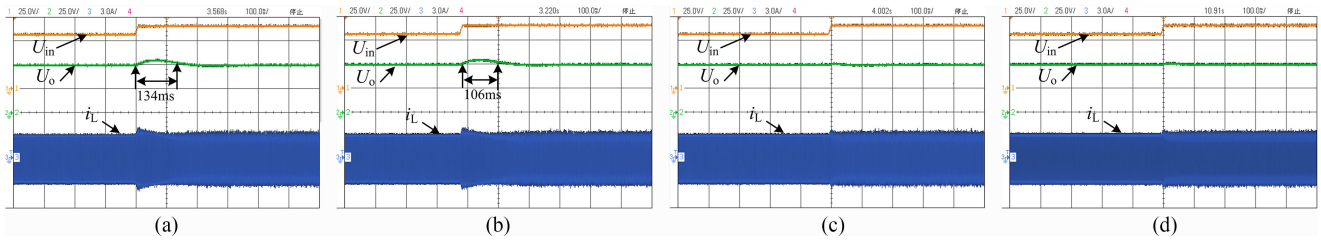


Fig. 16. Experimental results of two control schemes with different parameter mismatch ratio $k$. (a) MPS scheme with $k = 0.5$, (b) MPS scheme with $k = 2$, (c) VDPC scheme with $k = 0.5$, (d) VDPC scheme with $k = 2$ ($U_o$: 25 V/div; $i_o$: 3 A/div; Time: 100 ms/div).

TABLE II
EXPERIMENTAL PERFORMANCE COMPARISON OF THREE CONTROL SCHEMES

| Control schemes | Start-up | Load disturbance | Input voltage disturbance | The desired output voltage step-change |
|---|---|---|---|---|
| TVL control | Slow | Slow | Slow | Slow |
| LCFF control | Slow | Fast | Slow | Fast |
| MPS control | Slow | Fast | Fastest | Faster |
| VDPC scheme | Faster | Fastest | Fastest | Fastest |

$U_o^*$ steps from 49 to 40 V. In the TVL control, when the desired output voltage $U_o^*$ steps down, the transient response of the output voltage is slow [see Fig. 15(a)] with the settling time of 162 ms. In the LCFF control [see Fig. 15(b)], the settling time is 116 and 44 ms. In the MPS control [see Fig. 15(c)] and VDPC [see Fig. 15(d)], the settling time is 84 and 44 ms, respectively. Thus, even if the desired output voltage steps down or up, the proposed VDPC scheme can realize the shortest settling time, compared with the TVL control and MPS control.

According to Figs. 10–15, an experimental performance comparison of TVL control, LCFF control, MPS control, and VDPC scheme can be concluded in Table II.

From Table II, it is easy to find that the proposed VDPC scheme can achieve the best dynamic performance among the four controls, and the MPS control also presents excellent performance under input voltage disturbance.

### *B. Parameter Sensitiveness Comparison of VDPC and MPS Scheme With Input Voltage and LCFF*

As shown in Figs. 5 and 6, the feedforward control with the input voltage and load current is adopted to estimate the phase-shift ratio in both MPS and VDPC schemes. If there exists proportionality mismatch of the sampling input voltage, (10) can be rewritten as

$$\begin{aligned} D^* &= \frac{1-\sqrt{1-8(L/k)U_o^* i_o/nU_oU_{\text{in}}T_s}}{2} \\ &= \frac{1-\sqrt{1-8LU_o^* i_o/(kn)U_oU_{\text{in}}T_s}}{2} \\ &= \frac{1-\sqrt{1-8LU_o^* i_o/nU_o(kU_{\text{in}})T_s}}{2} \\ &= \frac{1-\sqrt{1-8LU_o^*(i_o/k)/nU_oU_{\text{in}}T_s}}{2} \end{aligned} \tag{30}$$

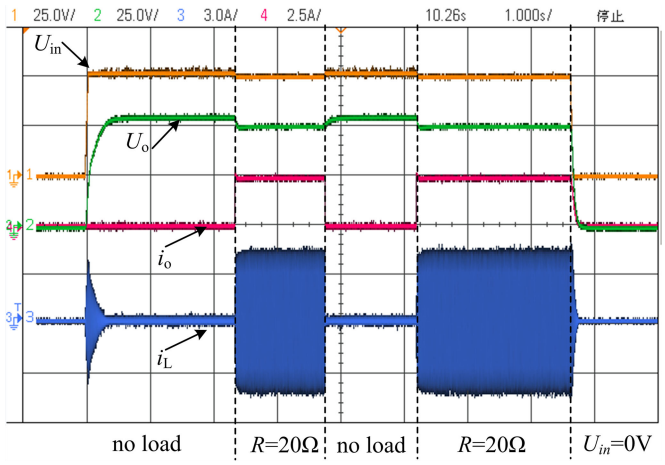


Fig. 17. Experimental results of the proposed VDPC scheme in no-load operation condition ($U_o$: 25 V/div; $i_o$: 2.5 A/div; $i_L$: 3 A/div; Time: 1 s/div).

where $k$ is the parameter mismatch ratio. From (30), the parameter mismatch effect of $L$, $n$, $i_o$ on the estimated phase-shift ratio $D^*$ is the same with that of the sampling input voltage. In a steady-state condition, parameter mismatch effect can be eliminated by the output voltage PI controller in the MPS scheme shown in Fig. 5. But the transient response will be slower when the input voltage or the load current steps change, which relies on the parameter tuning of the PI controller. Actually, there does not exist the proportionality mismatch of the sampling input voltage and load current. But the inductance mismatch exists commonly.

Fortunately, from (15), the estimated phase-shift-ratio $D^*$ in the proposed VDPC scheme is irrelative to parameters $L$ and $n$. Even if there exists proportionality mismatch of the sampling input voltage with its actual value, the VDPC scheme can achieve fast dynamic response even if the input voltage or load steps up and down. Fig. 16 shows transient experimental results of the MPS control and VDPC schemes with different parameter mismatch ratio $k$ value when the input voltage steps up. It is clear that the proposed VDPC can achieve the better transient response than the MPS control scheme with load current and input voltage feedforward, when there exists a parameter mismatch between the control system and the actual converter circuit.

### C. No-Load Operation Testing of the VDPC Scheme

When the experimental parameters are set as $U_{\rm in} = 50$ V, $U_o^* = 49$ V and $R = 20\ \Omega$, Fig. 17 shows experimental results of the proposed VDPC scheme for DAB dc–dc converters in no-load operation condition.

In Fig. 17, at the beginning of this experiment test, there is no load and the phase-shift ratio $D$ is equal to 0, and then adding the load ($R = 20\ \Omega$), the actual output voltage will reach the desired output voltage quickly. During the working status with the load ($R = 20\ \Omega$), if the load step from 20 Ω to no-load, the control system can also response this change immediately. Note that the output voltage in Fig. 17 is a little bit higher than the desired value in the no-load condition. Because the load current is approximate to zero, the proposed VDPC is hard to force the output voltage to reach its reference value absolutely.

## VI. Conclusion

An essential requirement for a high-performance DAB dc–dc converter is to reach the desirable output voltage rapidly and accurately under extreme operation condition, such as start-up, load or input voltage transient variation, no-load, and the desired output voltage change. In order to obtain the fast dynamic response, a VDPC scheme with SPS control has been proposed for DAB dc–dc converters as the controlled voltage source in this paper. On the basis of energy conservation concept, the VDPC scheme is analyzed in detail in an SPS control mode. An experimental scale-down prototype test is adopted to verify the dynamic performance of the VDPC scheme. The conducted studies conclude that the proposed VDPC scheme is characterized as the following.

1) In the load or input voltage disturbance condition, the proposed VDPC scheme shows excellent dynamic behavior, such as no overshoot, fast transient response, and the constant output voltage for the input voltage and load disturbances.
2) In start-up process or the desired output voltage step-change condition, compared with the TVL control and MPS control, the proposed VDPC scheme can significantly achieve fastest dynamic response.
3) Compared with the MPS scheme with input voltage and LCFF, the VDPC scheme is not sensitive to parameters such as the inductance $L$, and does not need to know the precise proportionalities of the input voltage and the load current between the real converter and the control system.
4) When the converter operates at no-load status, the VDPC scheme can respond quickly and make the transmission power be equal to zero. And when the load is connected in the converter, the output voltage can reach the desired output voltage quickly.

Although this paper reports the proposed VDPC scheme combing with SPS control for DAB dc–dc converters as the controlled voltage source, note that the idea of the proposed VDPC scheme can also be extended and applied for the other phase-shift methods. In addition, the VDPC can also be extended for DAB dc–dc converters as the controlled current source, on the basis of replacing the output voltage PI controller with the output current PI controller. The detail description will not be reported in this paper.

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**Wensheng Song** (M'13) received the B.S. degree in electronic and information engineering and the Ph.D. degree in electrical engineering from Southwest Jiaotong University, Chengdu, China, in 2006 and 2011, respectively.

He is currently an Associate Professor in the School of Electrical Engineering, Southwest Jiaotong University. From September 2009 to September 2010, he was a Visiting Scholar in the Department of Electrical Engineering and Computer Science, University of California, Irvine, CA, USA. From July 2015 to December 2015, he was a Visiting Scholar with the University of Alberta, Edmonton, AB, Canada. His current research interests include digital control and modulation methods of electrical ac–dc–ac railway traction drive systems, and multilevel converters.

**Nie Hou** was born in Mianyang, Sichuan, China, in 1990. He received the B.S. degree in electrical engineering in 2014 from Southwest Jiaotong University, Chengdu, China, where he is currently working toward the M.S degree in electrical engineering.

His current research interests include digital control and optimization methods of dc–dc converter, and dc distribution system.

**Mingyi Wu** was born in Xiangyang, Hubei, China, in 1992. He received the B.S. degree in electrical engineering in 2015 from Southwest Jiaotong University, Chengdu, China, where he is currently working toward the M.S degree in electrical engineering.

His current research interests include power electronics and motor drives.