Isolated Boost DC–DC Converter With Three Switches

Minh-Khai Nguyen, *Member, IEEE*, Truong-Duy Duong, Young-Cheol Lim, *Member, IEEE*, and Yong-Jae Kim, *Member, IEEE*

***Abstract*—This paper documents a new three-switch, isolated boost dc–dc converter. The major features of the proposed converter are as follows: 1) continuous input current; 2) reduced one active switch, one additional diode, and one additional capacitor; 3) unchanged primary and secondary voltage waveforms of the transformer when the duty cycle is changed; and 4) removal of the snubber circuit. This paper presents the operating principles, analysis, parameter design guidelines, and simulation results for the proposed converter. To verify the performance of the proposed converter, a 400 W prototype was constructed with a 40–60 V dc input. A PID controller was used to maintain the dc output voltage at 400 V. The simulation and experimental results matched those of the theoretical analysis.**

***Index Terms*—Current-fed full-bridge (CFFB) converter, dc–dc power conversion, galvanic isolation, step-up transformer, voltage double rectifier (VDR).**

I. Introduction

HIGH step-up dc–dc conversion techniques are required in many applications such as fuel cells (FCs), solar photovoltaic systems, and uninterruptible power supplies. For these applications, a high step-up voltage ratio with high conversion efficiency is necessary. Many high step-up dc–dc converters have been proposed and investigated to convert low voltages into a constant dc bus voltage. For isolated topologies that provide galvanic isolation, voltage-fed full-bridge (VFFB) and current-fed full-bridge (CFFB) dc–dc converters are widely used [1]–[14]. Because the voltage source converters have a buck function, the major voltage gain of the VFFB dc–dc converters [1]–[4] is provided by a high-frequency transformer with a large turn ratio. To improve the voltage boost ability, a boost converter [5], [6] or an active-clamped three-level rectifier [7] is attached to the secondary side of the VFFB dc–dc converter. Because the current-fed converters have a boost function, the CFFB dc–dc converters [8]–[14] are suitable for applications with a high step-up voltage gain. In addition, the input current ripple and turn ratio of the high-frequency transformer in CFFB converters are lower than those in VFFB dc–dc converters.

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M.-K. Nguyen and Y.-J. Kim are with the Department of Electrical Engineering, Chosun University, Gwangju 61452, South Korea (e-mail: khaibk@ieee.org; kimyj21@chosun.ac.kr).

T.-D. Duong and Y.-C. Lim are with the Department of Electrical Engineering, Chonnam National University, Gwangju 500-757, South Korea (e-mail: duyduong11141375@gmail.com; yclim@chonnam.ac.kr).

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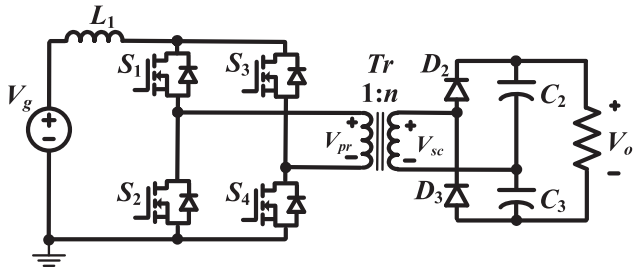

Fig. 1. Conventional current-fed, four-switch, isolated boost dc–dc converter.

CFFB converters, however, the resonance between the leakage inductor of the transformer and the output capacitance of the primary switches causes voltage spikes in devices. To absorb the switch turn-off voltage spike in CFFB converters, a passive snubber is used [15], which causes increased power loss. To recover the energy of the snubber in CFFB converters, active clamping circuits with increasing size and cost have been proposed [16]–[19]. In an attempt to avoid the need to use the active clamping circuits, soft-switching snubberless naturally clamped CFFB converters have been proposed in [8], [9], [20], and [21].

An interleaved CFFB converter was proposed in [10] to reduce the input current ripple. By interleaving two isolated CFFB converters, the size of the magnetic components and the current stress of the devices are reduced. An input-series output-parallel connection for CFFB converter modules was proposed in [11] to increase the voltage-blocking capability at the input and decrease the current ripple at the output. A dual-input CFFB converter based on a distributed multitransformer structure was presented in [12] and [13] for hybrid renewable energy systems. However, the types of CFFB converters proposed in [10]–[13] use a greater number of transformers and switches, which increases the loss and cost of the overall system.

A conventional CFFB converter is shown in Fig. 1, which consists of a boost inductor, a full-bridge inverter with four switches, a high-frequency step-up transformer, a voltage double rectifier (VDR), and a load. When only a pair of switches (S_1 and S_4) or (S_2 and S_3) is turned "ON," the input current decreases and the converter operates in energy-transfer mode. When all switches are turned "ON," the input current increases and the converter operates in boost mode. The output voltage gain and the peak-to-peak inductor L_1 current ripple of the conventional

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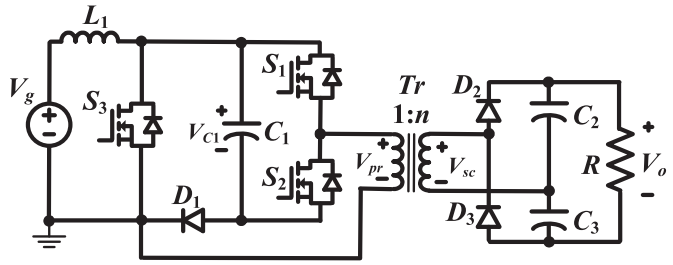

Fig. 2. Proposed three-switch, isolated boost dc–dc converter.

CFFB converter can be expressed as [20]

$$\begin{cases} V_o = \frac{2n}{1-D_c} V_g \\ a\% = \frac{\Delta I_L}{I_L} = \frac{D_c T {V_g}^2}{2 L_1 P_o}, \end{cases} \tag{1}$$

where D_c, T, and n are the duty cycle when all switches are turned "ON," the switching period, and the turn ratio of the transformer, respectively.

The turning "ON" time interval of all switches is used to control the output voltage in conventional CFFB converters. Moreover, the current-fed converter generates a zero voltage at the primary side of the transformer when all switches are turned "ON." Therefore, the primary and secondary voltage waveforms of the high-frequency transformer vary according to when the period occurs for which all switches are "ON."

In this paper, a three-switch isolated boost dc–dc converter is proposed. Compared to the conventional CFFB converter, the proposed converter uses one less active switch, one extra diode, and one extra capacitor. The operating principles, analysis, and parameter design guidelines for the proposed converter are presented. To verify the analysis, results of the simulation and experiment are provided.

II. Proposed Topology

A circuit diagram of the proposed three-switch isolated boost dc–dc converter is shown in Fig. 2. The low-voltage side consists of a boost inductor (L_1), three switches (S_1, S_2 and S_3), a capacitor (C_1), a diode (D_1), and the primary winding of the transformer (*Tr*). The high-voltage side consists of the load (*R*) and the secondary winding of the transformer (*Tr*) connected to the VDR implemented by two diodes (D_2 and D_3) and two capacitors (C_2 and C_3). The main characteristics of the proposed converter are as follows:

1) the input dc current is continuous with low ripple, whereby a decoupling capacitor bank or an *LC* input filter at the front end (typically used to protect the energy source such as the FC) is unnecessary;
2) it uses one less active switch, one extra diode, and one extra capacitor than the conventional isolated boost dc–dc converter;
3) the primary- and secondary-side voltage waveforms of the high-frequency transformer are unchanged when the output voltage is controlled; this facilitates the ease of the design of the high-frequency transformer; and
4) the snubber circuit is not used because the voltage spike is limited by clamping the capacitor C_1 voltage.

As shown in Fig. 2, switch S_2 in the proposed converter is now not connected to the source ground. Thus, three gate drivers with three separate grounds are used in the proposed converter. Compared to the conventional current-fed, four-switch, isolated boost dc–dc converter shown in Fig. 1 (in which four gate drivers with three separate grounds are used), both converters use the same number of separate grounds.

A. Operating Principle

A circuit analysis of the proposed converter is performed under the following conditions:

1) the inverter operates in continuous conduction mode;
2) all devices are ideal and lossless;
3) the high-frequency transformer is modeled by means of a leakage inductor connected to an ideal transformer;
4) the current flow to the windings of the transformer and the inductor increases or decreases linearly;
5) the capacitance of the capacitors is sufficient to maintain a constant capacitor voltage;
6) oscillations between the leakage inductance and parasitic capacitances are ignored; and
7) $D_{\rm A}$ is the minimum value of *D*, where *D* is the duty cycle of switch S_3.

$D_{\rm A}$ is set to 0.3 in order to maintain the ac pulse primary- and secondary-side voltage waveforms of the high-frequency transformer at 30% positive, 20% zero, 30% negative, and 20% zero sequentially, respectively. $D_{\rm A}$ should be in the range of [0.25, 0.5] for the optimal utilization of the high-frequency transformer. The selection of D_A depends on the minimum voltage gain of the converter.

Fig. 3(a) shows the equivalent circuits of the proposed converter, in which the two windings of *Tr* are replaced by a leakage inductor (L_σ) connected to an ideal transformer and a mutual inductance (L_m). Fig. 4 shows the key waveforms of the proposed converter.

Stage 1–[$t_0 - t_1$, Fig. 3(b)]: S_1 is turned "ON," while S_2 and S_3 are turned "OFF." The inductor L_1 is discharged, while the leakage inductor of the transformer and the capacitor are charged. The D_1 and D_2 diodes are forward-biased, while the D_3 diode is reverse-biased. The primary voltage of the transformer is V_{c1}. The secondary side of the transformer generates a positive voltage. The time interval in this stage is t_{01}. We have

$$\begin{cases} L_1 \frac{di_{L1}}{dt} = V_g - V_{C1} \\ L_\sigma \frac{di_{L\sigma}}{dt} = V_{C1} - \frac{V_o}{2n} \\ L_m \frac{di_{\rm Lm}}{dt} = \frac{V_o}{2n}. \end{cases} \tag{2}$$

The secondary current of the transformer increases linearly from zero to the peak value and is calculated by

$$i_{\rm sc} = \frac{1}{2n^2} \left(\frac{2nV_{C1} - V_o}{L_\sigma} - \frac{V_o}{L_m} \right) t. \tag{3}$$

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Stage 2–[$t_1 - t_2$, Fig. 3(c)]: when the primary winding current is charged to the inductor L_1 current, the D_1 diode

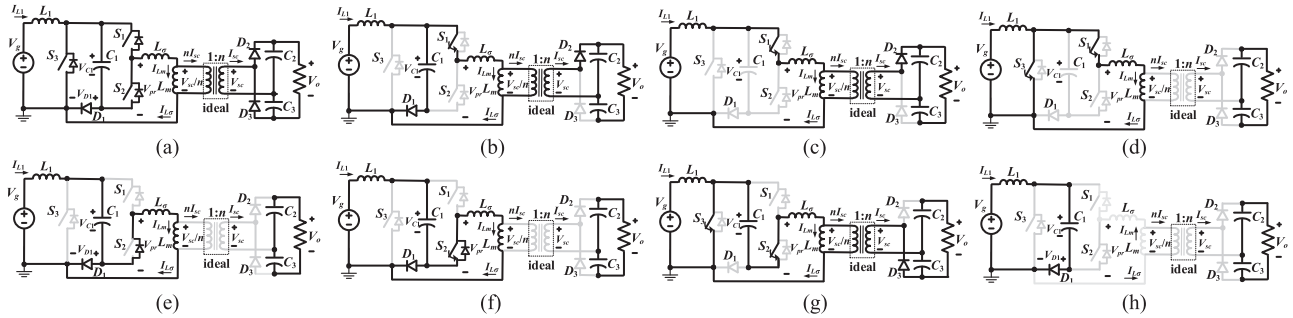

Fig. 3. Proposed converter: (a) equivalent circuit and (b)–(h) operating stages.

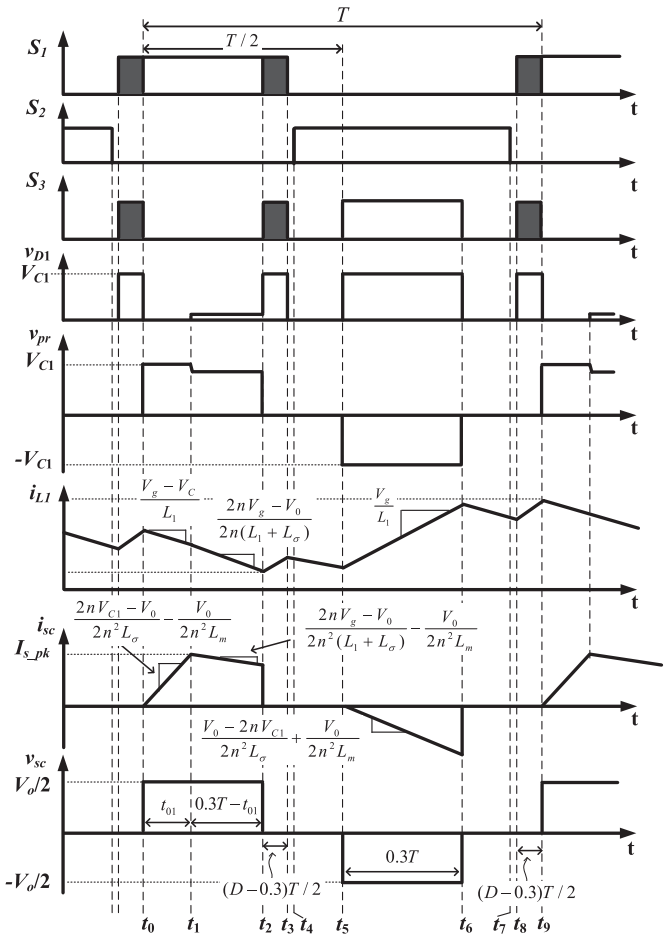

Fig. 4. Key waveforms of the proposed converter.

is reverse-biased. The leakage inductor of the transformer is discharged. Because the leakage inductor of the transformer is changed from the stored energy state in stage 1 to the transferred energy state in stage 2, the primary voltage of the transformer is lower than V_{c1}. The secondary side of the transformer still generates a positive voltage. The time interval in this stage is $(0.3{\cdot}T - t_{01})$, where T is the switching period. The secondary current of the transformer is expressed as

$$i_{\rm sc} = \frac{1}{2n^2}\left(\frac{2nV_g - V_o}{L_1 + L_\sigma} - \frac{V_o}{L_m}\right)t + I_{s\text{-pk}} \qquad (4)$$

where I_{s_pk} is the peak value of the secondary current of the transformer.

Stage 3–[$t_2 - t_3$, Fig. 3(d)]: when the proposed converter requires a higher boost voltage, one further mode, as shown in Fig. 3(d), is applied. This mode is inserted into the zero states, where the winding voltages of the transformer are zero, such that the voltage waveforms of the transformer are unchanged. In this mode, S_1 and S_3 are turned "ON," while S_2 is turned "OFF." The inductor L_1 is charged. The primary winding of the transformer is short-circuited by S_1 and S_3. All diodes are reverse-biased and the secondary voltage of the transformer is zero. The time interval in this stage is $(D - 0.3){\cdot}T$, where D is the duty cycle of switch S_3, and $D \geq 0.3$. We have

$$\begin{cases} L_1 \frac{di_{L1}}{dt} = V_g \\ L_\sigma \frac{di_{L\sigma}}{dt} = L_m \frac{di_{\rm Lm}}{dt} = 0. \end{cases} \qquad (5)$$

Stage 4–[$t_3 - t_4$, Fig. 3(e)]: At t_3, S_1 and S_3 are turned "OFF" and S_2 remains turned "OFF." The inductor L_1 current is freewheeling through D_1, while the primary winding current freewheels through the body diode of S_2. The time interval in this stage is very short.

Stage 5–[$t_4 - t_5$, Fig. 3(f)]: Because the current flows through the body diode of S_2 at t_4, the direction of the current of S_2 reverses and S_2 is turned "ON" with zero-voltage switching (ZVS). The inductor L_1 current freewheels through D_1 and decreases linearly. The primary winding of the transformer is in a short-circuit situation through S_2 and D_1. The secondary voltage of the transformer is zero, the D_2 and D_3 diodes are reverse-biased, and the primary current of the transformer is unchanged. We get

$$\begin{cases} L_1 \frac{di_{L1}}{dt} = V_g - V_{C1} \\ L_\sigma \frac{di_{L\sigma}}{dt} = L_m \frac{di_{\rm Lm}}{dt} = 0. \end{cases} \qquad (6)$$

Stage 6–[$t_5 - t_6$, Fig. 3(g)]: At $t_5 = T/2$, S_3 is turned "ON," while S_1 remains "OFF" and S_2 remains "ON." The inductor L_1 is charged, while the capacitor C_1 is discharged. The primary voltage of the transformer is $-V_{c1}$. Also, the secondary voltage of the transformer is $-nV_{c1}$. The D_1 and D_2 diodes are reverse-biased, while the D_3 diode is forward-biased. The time interval in this stage is

0.3·*T*, and is the sum of the time intervals in stages 1 and 2 to generate symmetrical ac waveforms at the primary side of the transformer. We get

$$\begin{cases} L_1 \frac{di_{L1}}{dt} = V_g \\ L_\sigma \frac{di_{L\sigma}}{dt} = -V_{C1} + \frac{V_o}{2n} \\ L_m \frac{di_{\mathrm{Lm}}}{dt} = \frac{-V_o}{2n}. \end{cases} \tag{7}$$

The secondary current of the transformer is calculated by

$$i_{\mathrm{sc}} = \frac{1}{2n^2}\left(\frac{-2nV_{C1}+V_o}{L_\sigma} + \frac{V_o}{L_m}\right)t. \tag{8}$$

Stage 7–[t_6 – t_7, Fig. 3(f)]: At t_6, S_3 is turned "OFF," while S_1 remains "OFF" and S_2 remains "ON." The converter operates as stage 5. The primary winding of the transformer is in a short-circuit situation through S_2 and D_1, and the primary winding current then reduces to zero. The time intervals in stages 5 and 7 are equal (0.7 – *D*)·*T*/2.

Stage 8–[t_7 – t_8, Fig. 3(h)]: At t_7, the current of S_2 is zero, and S_2 is turned "OFF" with zero-current switching (ZCS). The inductor L_1 current still freewheels through D_1. The drain-source voltage of S_2 increases from zero to V_{C1}, while the drain-source voltage of S_1 decreases from V_{C1} to zero. The time interval in this stage is very short.

Stage 9–[t_8 – t_9, Fig. 3(d)]: At t_8, the drain-source voltage of S_1 is zero and S_1 is turned "ON" with ZVS. In this stage, S_2 is turned "OFF" while S_1 and S_3 are turned "ON." The converter operates as stage 3. The time intervals in stages 3 and 9 are equal (*D* – 0.3)·*T*/2.

As shown in Fig. 4, the transformer currents are not symmetric about their two halves, which are positive and negative. This could result in a deteriorated performance of the transformer in the proposed converter in comparison to that in the conventional full-bridge converters. Further, a small air gap is used to avoid the core saturation caused by the asymmetric transformer currents.

In the proposed converter, a capacitor C_1 is placed between the input inductor and the leakage inductor of the transformer for the removal of the snubber circuit. When the input inductor is changed from the stored energy state to the transferred energy state, the currents of the inductors do not change suddenly because the capacitor C_1 links between the input inductor and the leakage inductor. Therefore, a snubber circuit is not needed in the proposed converter. However, because the S_3 switch is turned OFF with hard-switching, an over-stress voltage appears on S_3. As discussed in [14], the voltage rating of the primary switches in the isolated boost converter is typically rated at two to three times the maximum input voltage. Therefore, an acceptance over-stress on the S_3 switch is less than three times the maximum input voltage. This over-stress depends on the stray inductances of the circuit and the slope of di_{DS3}/dt, where i_{DS3} is the drain–source current of S_3.

B. Voltage Conversion Ratio

Applying the volt-second balance law to the inductor L_1, in a steady state, (2), (5)–(7) yield

$$V_{C1} = \frac{V_g - (0.3 - t_{01}/T)V_{D1}}{1-D} \tag{9}$$

where V_{D1} is the diode D_1 voltage in stage 2. As shown in Fig. 4, V_{D1} in stage 2 is very small in comparison with V_g. Also, the value of $(0.3 - t_{01}/T)$ is small. Therefore, $V_{D1} \cdot (0.3 - t_{01}/T)$ is very small and can be neglected. The capacitor C_1 voltage in (9) can be approximated as

$$V_{C1} \approx \frac{1}{1-D} V_g. \tag{10}$$

Given $t_0 = 0$, from (2), the inductor L_1 current and the primary current of the transformer are calculated using

$$\begin{cases} i_{L1} = \frac{V_g - V_{C1}}{L_1}t + \frac{P_o}{V_g} - \frac{D(D-2D_A)T}{2(1-D)L_1}V_g \\ i_{L\sigma} = \frac{2nV_{C1}-V_o}{2nL_\sigma}t - \frac{DT}{2nL_m}V_o \end{cases} \tag{11}$$

where P_o is the output power.

At t_1, the inductor L_1 current is equal to the primary current of the transformer. Substituting (10) into (11), we have

$$t_{01} = \left(\frac{P_o}{V_g^2 T} - \frac{D(D-0.6)}{2(1-D)L_1} + \frac{DG}{2nL_m}\right) \times \frac{2n(1-D)TL_\sigma L_1}{2n(L_1 + L_\sigma D) - (1-D)L_1 G} \tag{12}$$

where $G = V_o/V_g$ is the output voltage gain. The ratio of the stage-one time interval to the positive-stage time interval is defined by

$$k = \frac{t_{01}}{t_{02}} = \frac{t_{01}}{0.3T} \le 1. \tag{13}$$

Substituting t_{01} in (12) into (3), the peak value of the secondary current of the transformer is

$$I_{s\_\mathrm{pk}} = \frac{1}{2n^2}\left(\frac{2nV_{C1}-V_o}{L_\sigma} - \frac{V_o}{L_m}\right)t_{01}. \tag{14}$$

From (3), (4), and (8), the average secondary current of the transformer is calculated as

$$\bar{i}_{\mathrm{sc}} = \frac{1}{T}\begin{bmatrix} \frac{1}{2n^2}\left(\frac{2nV_{C1}-V_o}{L_\sigma} - \frac{V_o}{L_m}\right)\frac{t_{01}^2}{2} \\ +\frac{1}{2n^2}\left(\frac{2nV_g-V_o}{L_1+L_\sigma} - \frac{V_o}{L_m}\right)\frac{(0.3T-t_{01})^2}{2} \\ +I_{s\_\mathrm{pk}}\frac{0.3T-t_{01}}{T} + \frac{1}{2n^2}\left(\frac{2nV_{C1}-V_o}{L_\sigma} - \frac{V_o}{L_m}\right)\frac{(0.3T)^2}{2} \end{bmatrix}. \tag{15}$$

Substituting I_{s_pk} in (14) into (15), and simplifying it, we get

$$\bar{i}_{\mathrm{sc}} = \frac{T}{4n^2}\begin{bmatrix} \left(\frac{2nV_g-V_o}{L_1+L_\sigma} - \frac{2nV_{C1}-V_o}{L_\sigma} - \frac{2V_o}{L_m}\right)\left(\frac{t_{01}}{T}\right)^2 \\ +0.06\left(\frac{2nV_{C1}-V_o}{L_\sigma} - \frac{2nV_g-V_o}{L_1+L_\sigma}\right)\frac{t_{01}}{T} \\ +0.09\left(\frac{2nV_g-V_o}{L_1+L_\sigma} + \frac{2nV_{C1}-V_o}{L_\sigma} - \frac{2V_o}{L_m}\right) \end{bmatrix}. \tag{16}$$

Because the leakage inductor (L_σ) is very small in comparison with the input inductor (L_1) and the mutual inductance (L_m), the average secondary current of the transformer in (16) is approximated as

$$\bar{i}_{\rm sc} \approx \frac{2nV_{C1} - V_o}{4n^2 L_\sigma}\left(0.09 + 0.06\frac{t_{01}}{T} - \left(\frac{t_{01}}{T}\right)^2\right). \quad (17)$$

Because a VDR is used in the proposed converter, the average secondary current of the transformer is two times the load current ($\bar{i}_{\rm sc} = 2I_o$). Substituting V_{c1} in (10) and $t_{01} = 0.3k \cdot T$ in (13) into (17), we get

$$G = \frac{V_o}{V_g} \approx \frac{2n}{1-D} - \varepsilon \quad (18)$$

where$\varepsilon = \frac{8n^2 L_\sigma I_o}{0.09(1+2k-k^2)TV_g}$.

From (18), it can be observed that the output voltage gain is controlled by *D*. Note that (18) is not a closed-form expression because *G* depends on *k*, but *k* depends on *G* according to (12). However, the effect of *k* on the dc voltage gain in the circuit design is insignificant because ϵ in (18) is very small in comparison to $2n/(1 - D)$.

C. Pulse-Width-Modulation (PWM) Control

Fig. 4 also shows the pulse-width-modulation (PWM) control method for the proposed converter. In this PWM control method, the extra state, where S_1 and S_3 are turned "ON" simultaneously, is inserted into the zero state to extend the period for which S_1 is "ON" continuously. The reference voltage, $V_{\rm ref}$ is compared to a high-frequency triangle waveform, V_{tri} to generate the control signals for the S_3 switch. Another reference voltage with amplitude of $(1 - V_{\rm ref})$ is compared to $V_{\rm tri}$ to generate the control signals for the S_1 and S_2 switches. To generate the extra states, the control voltage, $V_{\rm con}$ is compared to $V_{\rm tri}$. Note that $V_{\rm con}$ is in the range of $[1 - V_{\rm ref}, V_{\rm ref}]$ to ensure that the extra state is only inserted into the zero state. In the proposed converter, $V_{\rm ref}$ is normally kept constant for the unchanging voltage waveforms of the transformer. Therefore, the control voltage of the proposed converter is only $V_{\rm con}$.

D. Voltage and Current Stresses

The capacitor C_1 voltage stress is approximated in (10). The voltage stress of the $S_1 - S_3$ switches, the D_1 diode, and the transformer primary side are equal to the capacitor C_1 voltage stress. The voltage stress of the C_2 and C_3 capacitors are half of the output voltage, while the voltage stress of the D_2 and D_3 diodes are equal to the output voltage.

To easily derive the current stress of the D_1 diode, we ensure that the inductor current is taken as constant with a free ripple. The inductor current is the input current and is equal to P_o/V_g, where P_o is the output power. The diode D_1 current can be

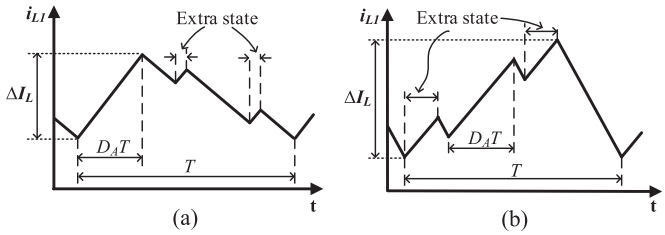

Fig. 5. Inductor L_1 current ripple. (a) $D < 0.5$ and (b) $D > 0.5$.

TABLE I
SIMULATION AND EXPERIMENTAL PARAMETERS OF PROPOSED CONVERTER

Input voltage range (V_g)		40–60 V
Output voltage (V_o)		400 V
Inductor (L_1)		1 mH
Transformer	Turn ratio	1:2.5
	Primary inductance	1.4 mH
	Leakage inductance	11 μH
Capacitors	C_1	220 μF
	$C_2 = C_3$	150 μF
Switching frequency		10 kHz
Resistive load (R)		600 Ω

expressed as

$$i_{D1} = \begin{cases} -\frac{P_o}{V_g t_{01}}t + \frac{P_o}{V_g}, & 0 < t < t_1 \\ P_o/V_g, & t_3 < t < t_5 \text{ and } t_6 < t < t_8 \\ 0, & \text{other time intervals.} \end{cases} \quad (19)$$

The RMS current of the D_1 diode is given by

$$I_{\rm RMS\_D1} = \frac{P_o}{V_g}\sqrt{0.7 - D + t_{01}/(3T)}. \quad (20)$$

From (10) and (20), the stresses on the elements depend on the existence of an extra stage. Because the effect of *k* on the dc voltage gain is insignificant, we can set $k = 0.5$ in the circuit design. Next, the maximum duty cycle ($D_{\max}$) of S_3 is calculated from (18) based on the maximum dc voltage gain. Then, the stresses on the elements are calculated based on $D_{\max}$.

III. Parameter Design of the Inductor and Capacitor

A. Parameter Design of the Inductor

Different PWM control conditions cause varying input current ripples in the proposed converter. The inductor is designed based on the peak-to-peak current ripple passing through to the inductor. Fig. 5 shows the peak-to-peak current ripple of the L_1 inductor using the PWM control method presented in Section II-C. When $D < 0.5$, the peak-to-peak inductor L_1 current is calculated based on stage 6, in which the secondary voltage is negative. When $D \geq 0.5$, the peak-to-peak inductor L_1 current is calculated based on stages 1 and 2, in which the secondary voltage is positive. From (2) and (6), the peak-to-peak

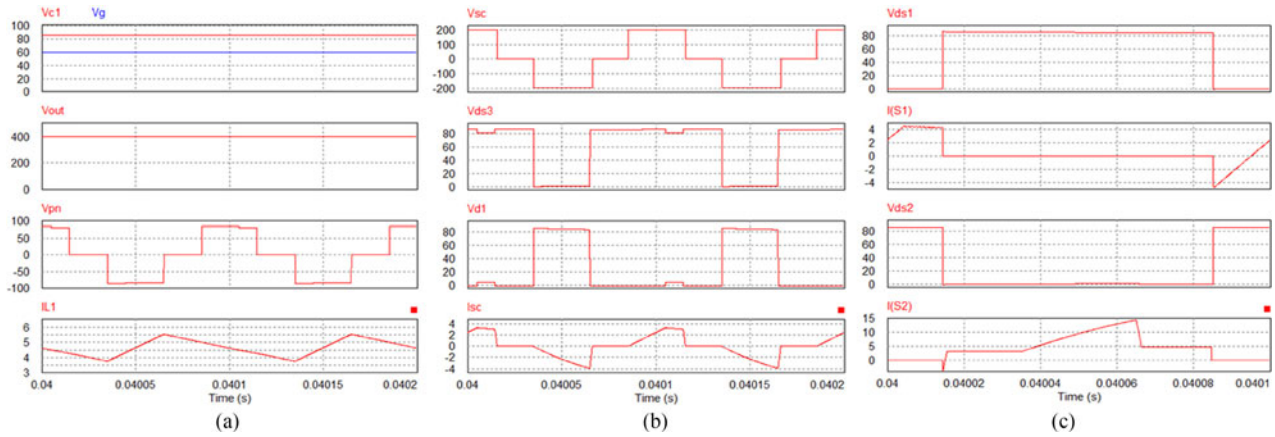

Fig. 6. Simulation results when $V_g = 60$ V. From top to bottom: (a) capacitor and input voltages, output voltage, primary voltage of the transformer, and input current; (b) secondary voltage of the transformer, drain–source voltage of S_3, diode D_1 voltage, and secondary current of the transformer; and (c) drain–source voltage of S_1, drain–source current of S_1, drain–source voltage of S_2, and drain–source current of S_2.

inductor L_1 current is

$$\Delta I_L = \begin{cases} \frac{0.3TV_g}{L_1} & D < 0.5 \\ \frac{0.3DTV_g}{(1-D)L_1} & D \geq 0.5. \end{cases} \tag{21}$$

The input current ripple of the proposed converter is calculated as

$$a\% = \frac{\Delta I_L}{I_L} = \begin{cases} \frac{0.3T{V_g}^2}{L_1 P_o} & D < 0.5 \\ \frac{0.3DT{V_g}^2}{(1-D)L_1 P_o} & D \geq 0.5. \end{cases} \tag{22}$$

Comparing (22) to (1), the input current ripple of the proposed converter is two times higher than that of the conventional converter.

If the inductor current ripple $\Delta I_{\rm L}$ is chosen such that $\Delta I_{\rm L} \leq a\% I_{\rm L}$, the required L_1 inductance should be

$$L_1 = \begin{cases} \frac{0.3TV_g^2}{a\%P_o} & D < 0.5 \\ \frac{0.3DTV_g^2}{(1-D)a\%P_o} & D \geq 0.5. \end{cases} \tag{23}$$

B. Parameter Design of the Capacitor

The capacitors are designed according to the capacitor voltage ripple. The current flow to the C_1 capacitor in the negative mode of the proposed converter, as shown in Fig. 3(g), can be rewritten as

$$C_1 \frac{\Delta V_{C1}}{D_A T} = n\bar{i}_{\rm sc}. \tag{24}$$

If the peak-to-peak capacitor voltage ripple is limited passing through by $b\%$, the capacitance for C_1 in the proposed converter should be

$$C_1 = \frac{0.3(1-D)^2 TP_o}{b\%V_g^2}. \tag{25}$$

Because the slope of di_{DS3}/dt affects the peak-to-peak capacitor voltage ripple, the selection of capacitance C_1 in (25) compensates for the effect of the over-stress on the S_3 switch.

The output capacitors (C_2 and C_3) of the VDR are selected as follows. When the converter is in zero mode, as shown in Fig. 3(d) and (f), the C_2 and C_3 capacitor currents, respectively, are equal to the negative load current. To limit the ripple on the output voltage at $c\%$, the capacitance should be

$$C_2 = C_3 = \frac{0.4(1-D)^2 TP_o}{4c\%n^2 V_g^2}. \tag{26}$$

IV. Simulation and Experimental Results

A. Simulation Results

To verify the operating principle of the proposed converter shown in Fig. 2, PSIM simulation was performed with the following parameters: $L_1 = 1\,\text{mH}, C_1 = 220\,\mu\text{F}, C_2 = C_3 = 150\,\mu\text{F}$, and $R = 600\,\Omega$. The drain-to-source on-resistance of metal-oxide-semiconductor field-effect transistors (MOSFETs) was set to 8 MΩ. The forward voltage of the diodes was set to 0.7 V. The turn ratio of the high-frequency transformer was 2.5. The magnetic inductance measured from the primary side was set to 1.4 mH. The leakage inductance was set to 11 μH. The switching frequency was 10 kHz and the output voltage was 400 V. The deadtime between S_1 and S_2 is 2 μs. Table I shows the simulation parameters for the proposed three-switch isolated boost converter.

Fig. 6 shows the simulation results for the proposed converter when $V_g = 60$ V. The input current is continuous, with a peak-to-peak ripple of 1.71 A. The primary voltage of the transformer has three levels. Fig. 7 shows the simulation results for the proposed converter when $V_g = 40$ V. The input current is continuous, with a peak-to-peak ripple of 1.31 A. The primary and secondary voltage waveforms of the transformer shown in Fig. 7(a) are the same as those shown in Fig. 6(a). As shown in Fig. 7, an extra mode is applied to the zero state to boost the voltage when a minimum input voltage is used. Therefore, the primary and secondary voltage waveforms of the transformer are unchanged, even though the input voltage changes from maximum to minimum. These simulation results are in agreement with the theoretical analysis.

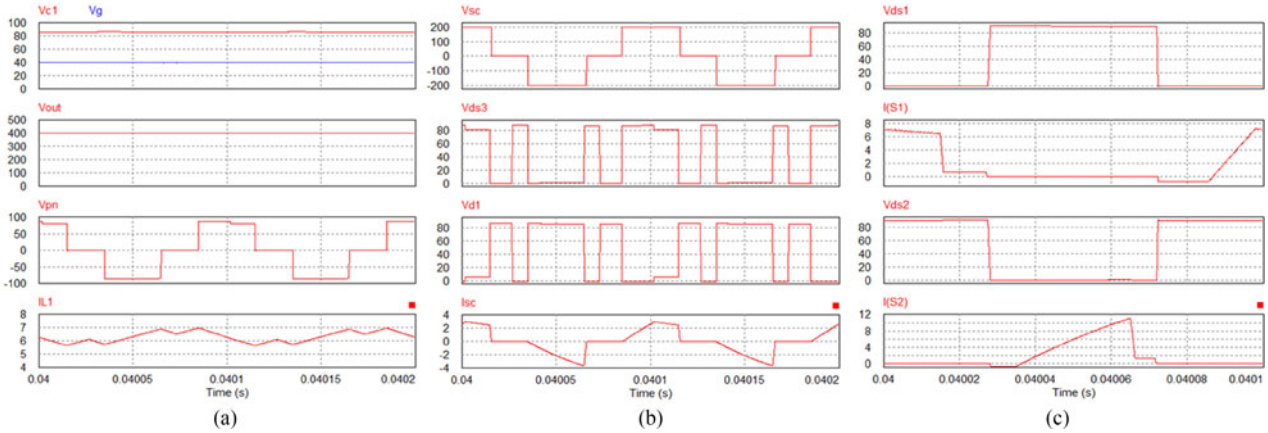

Fig. 7. Simulation results when $V_g = 40$ V. From top to bottom: (a) capacitor and input voltages, output voltage, primary voltage of the transformer, and input current; (b) secondary voltage of the transformer, drain–source voltage of S_3, diode D_1 voltage, and secondary current of the transformer; and (c) drain–source voltage of S_1, drain–source current of S_1, drain–source voltage of S_2, drain–source current of S_2.

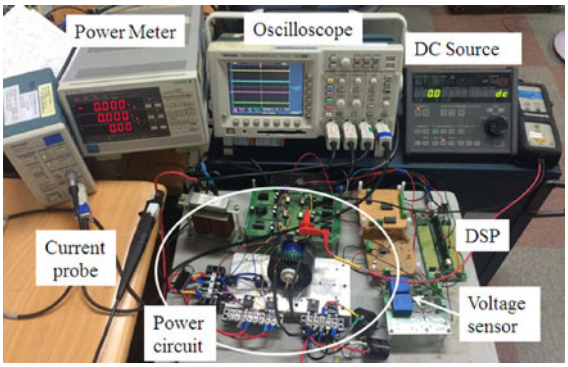

Fig. 8. Photograph of the experimental setup.

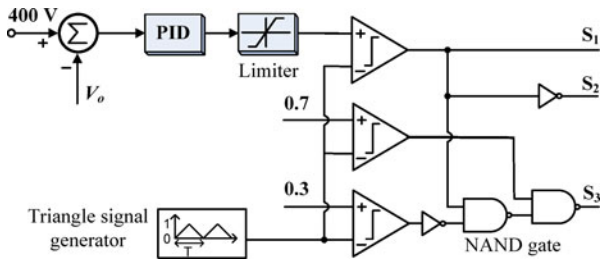

Fig. 9. Output voltage control algorithm for the proposed converter.

B. Experimental Results

A 400 W laboratory prototype based on a TMS320F28335 DSP was built to verify the properties of the proposed three-switch isolated boost dc–dc converter. Fig. 8 shows the experimental setup in the laboratory. The same parameters as those in the simulation were used. The C_1 capacitor is 220 μF/450 V. Two 150 μF/450 V capacitors were used for C_2 and C_3. The L_1 inductor was 1 mH/ 20 A (Changsung Corporation). The transformer utilized a B65686 N27 core (EPCOS). The primary windings had 38 turns, while the secondary windings hadxbrk 95 turns. The magnetic inductance measured from the primary side was 1.4 mH. The leakage inductance measured at the primary winding by shorting the second winding was 11 μH. Three IRFP4668PbF MOSFETs and one STPS60SM200C Schottky diode were used on the primary side, while two DSEP30-12A diodes were used on the secondary side. The deadtime between S_1 and S_2 is 2 μs.

To maintain the output voltage at 400 V, a proportional–integral–derivative (PID) voltage controller is used as shown in Fig. 9. The error signal between the output voltage sensor and the reference value of 400 V is passed over the PID controller. The PID control output is limited to the range of [0.3, 0.7]. This control value is used to generate the control signals of S_1 and S_2. To generate the control signal of S_3, reference voltages of 0.3 and 0.7 V are compared to the high-frequency triangle waveform. Two NAND logic gates are used to insert the zero state into S_3.

Fig. 10 shows the experimental results for the proposed converter when the maximum input voltage of 60 V was used at the output power of 266 W. An extra mode, in which both S_1 and S_3 are turned "ON," was not applied to the switching state, and $D = 0.3$. The calculated capacitor C_1 voltage from (10) was approximately 86 V when $V_g = 60$ V and $D = 0.3$. The measured value of the capacitor C_1 voltage was 85 V.

Fig. 11 shows the experimental results for the proposed converter when the minimum input voltage of 40 V is used at the output power of 266 W. An extra mode was inserted into the zero state of the converter. The duty cycle of S_3 in this case was 0.55. The measured value of the capacitor C_1 voltage was 87 V, while the calculated value from (10) was approximately 89 V. The capacitor C_1 voltage in the simulation and experiment was always lower than the calculated value due to the parasitic effect of the components.

In Figs. 10(a) and 11(a), the waveforms from top to bottom are the capacitor C_1 voltage, input voltage, primary voltage, and primary current. In Figs. 10(b) and 11(b), the waveforms from top to bottom are the secondary voltage, input current, secondary current, and output current. In Figs. 10(c) and 11(c), the waveforms from top to bottom are the gate–source voltage, the drain–source voltage of S_1, the drain–source current of S_1,

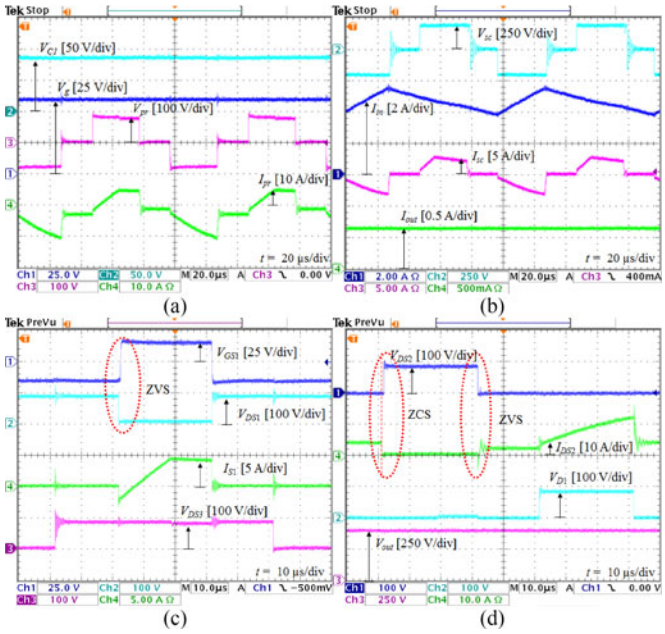

Fig. 10. Experimental voltage waveforms of the proposed converter when $V_g = 60$ V at the output power of 266 W.

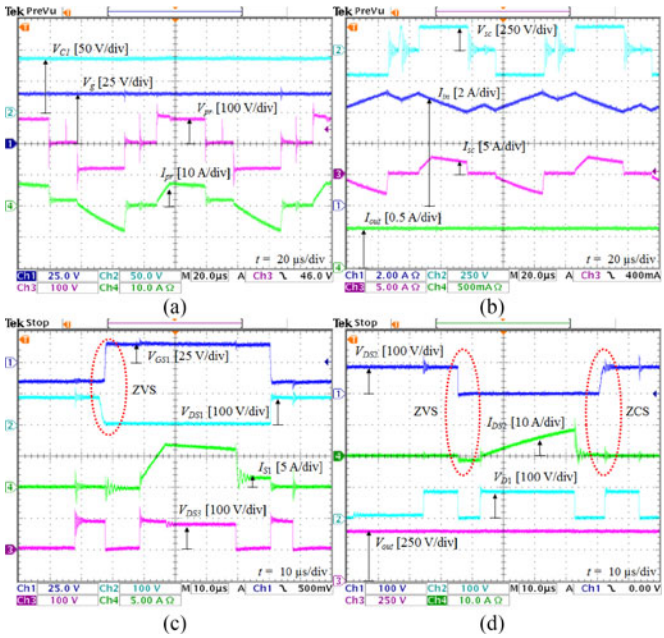

Fig. 11. Experimental voltage waveforms of the proposed converter when $V_g = 40$ V at the output power of 266 W.

and the drain–source voltages of S_3. In Figs. 10(d) and 11(d), the waveforms from top to bottom are the drain–source voltage of S_2, the current of S_2, the diode D_1 voltage, and the output voltage. As shown in Figs. 10 and 11, the S_1 and S_2 switches are turned ON with ZVS, and the S_2 switch is turned OFF with ZCS.

Table II compares the peak-to-peak inductor L_1 current in the simulation and experiment to that in the theory in (16). The experimental results differ only slightly from the theoretical and simulation results.

TABLE II
PEAK-TO-PEAK INDUCTOR L_1 CURRENT RIPPLE

	Calculation	Simulation	Experiment
$V_g = 40$ V	1.47 A	1.31	1.43 A
$V_g = 60$ V	1.8 A	1.71A	1.71 A

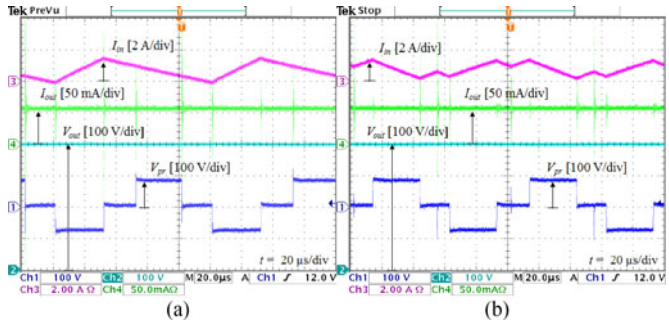

Fig. 12. Experimental results with light load (5.8% of full load) (a) $V_g = 60$ V and (b) $V_g = 40$ V.

Fig. 12 shows the experimental result of the proposed converter with light load (5.8% of full load). As shown in Fig. 12, the input current is continuous when a very light load is used. Fig. 13 shows the dynamic response of the proposed converter under a PID controller. In Fig. 13(a), the input voltage is changed from 40 to 60 V while the resistive load is kept at 800 Ω. In Fig. 13(b), the input voltage is changed from 60 to 40 V, while the resistive load is kept at 800 Ω. In Fig. 13(c), the input voltage is kept constant at 60 V while the load is changed from 50% load (800 Ω) to full load (400 Ω). In Fig. 13(d), the input voltage is kept constant at 60 V, while the load is changed from full load to 50% load. In Fig. 13(e) and (f), the input voltage is kept constant at 60 V while the load is changed from full load (400 Ω) to light load (5.8% of full load). In Fig. 13(a)–(e), the waveforms from top to bottom are the input voltage, the output voltage, and the output current. The transient stress on the components when the load is changed from full load to light load is shown in Fig. 13(f). In Fig. 13(f), the waveforms from top to bottom are the drain–source voltage stress of the S_2 switch, the diode D_1 voltage stress, the drain–source current stress of the S_2 switch, and the output current. In Fig. 13, the output voltage is kept at 400 V, despite the change in the input voltage or load.

Fig. 14 shows the measured efficiency of the proposed converter under different operating conditions. The proposed converter reaches a maximum efficiency of 95.7% when the maximum input voltage is used. The efficiency is reduced when the input voltage is decreased to 40 V. This is due to the increased switching loss of S_3 and high conduction loss in the devices when a higher boost voltage is required. The measured efficiency of the proposed converter at the very light load is 88.9% when the input voltage is 40 and 60 V. Compared to the conventional converters, the efficiency of the proposed converter is not high. This is because both the S_1 and S_3 switches of the proposed converter are switched OFF with hard-switching. Moreover, the test conditions are not the optimal operation conditions, where

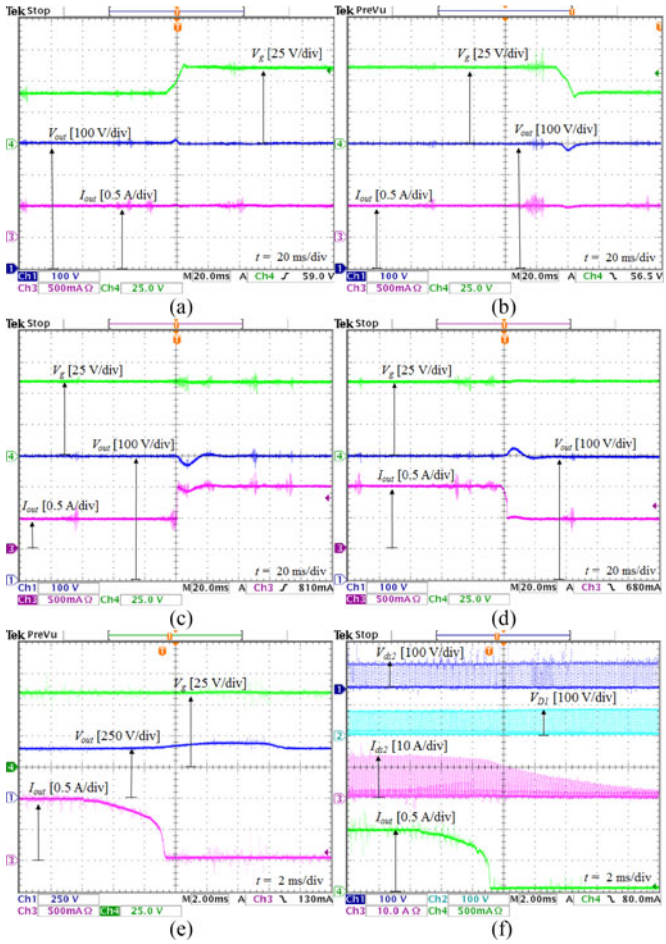

Fig. 13. Experimental results with (a) input voltage change from 40 to 60 V, (b) input voltage change from 60 to 40 V, (c) load change from half load to full load, (d) load change from full load to half load, and (e) and (f) load change from full load to light load (5.8% full load).

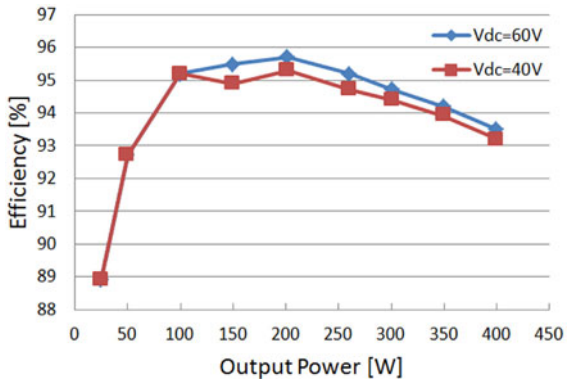

Fig. 14. Measured efficiency versus output power of the proposed converter.

the inductor, capacitors, and high-frequency transformer are not well designed.

V. Conclusion

A new three-switch isolated boost dc–dc converter was proposed in this paper. The proposed converter has the following characteristics: continuous input current, reduced one active switch, unchanged primary and secondary voltage waveforms of the transformer, and no snubber circuit. The limitations of the proposed converter compared to the conventional CFFB converter are as follows: one extra diode and one extra capacitor are used, a higher input current ripple is needed, and it is operated in hard-switching. The operating principles, analysis, parameter design guidelines, and simulation results are presented. A laboratory prototype with a PID controller was constructed to verify the operating theory of the proposed converter. The proposed converter is applicable for fuel-cell applications in which a varying low-dc input voltage is boosted to a high fixed dc output voltage with a continuous input current and galvanic isolation.

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Minh-Khai Nguyen (S'09–M'12) received the B.S. degree in electrical engineering from the Ho Chi Minh City University of Technology, Ho Chi Minh, Vietnam, in 2005, and the M.S. and Ph.D. degrees in electrical engineering from Chonnam National University, Gwangju, South Korea, in 2007 and 2010, respectively.

From 2010 to 2013, he was a Lecturer at Nguyen Tat Thanh University, Ho Chi Minh, Vietnam. Since 2013, he has been a Lecturer with the Ho Chi Minh City University of Technology and Education, Ho Chi Minh, Vietnam. Since 2016, he has been an Assistant Professor with Chosun University, Gwangju, South Korea. His current research interests include renewable energy systems, power quality, and power converters.

Truong-Duy Duong received the B.S. degree in electronic telecommunication engineering from the Ho Chi Minh City University of Technology and Education, Ho Chi Minh, Vietnam, in 2015. He is currently working toward the M.S. degree in the Department of Electrical Engineering, Chonnam National University, Gwangju, South Korea.

His research interests include topology and control of soft-switching dc–dc converter.

Young-Cheol Lim (M'85) was born in Chonnam, South Korea, in 1953. He received the B.S. degree in electrical engineering from Chonnam National University, Gwangju, South Korea, in 1975, and the M.S. and Ph.D. degrees from Korea University, Seoul, South Korea, in 1977 and 1990, respectively.

In 1981, he became a Professor at Chonnam National University, where he was the Director of the Research Center for High-Quality Electric Components and Systems from 1998 to 2007. He is the coauthor of three books. He has authored or coauthored more than 200 published technical papers. His current research interests include power electronics, control instruments, and neurofuzzy control.

Dr. Lim was the President of the Korea Institute of Power Electronics (KIPE) in 2009. He has been involved in various academic societies, such as the KIPE, the Korean Institute of Electrical Engineers, and the Institute of Control, Automation, and Systems Engineers, South Korea. He has received a number of awards, including the 2000 KIPE Best Paper Award and the 2001 KIPE Academic Award.

Yong-Jae Kim (S'04–M'07) was born in Gwnagju, South Korea, in 1973. He received the B.Eng. degree in electrical engineering from Chosun University, Gwangju, South Korea, in 1996, and the M.Eng. and Dr.Eng. degrees in electrical and electronic engineering from Musashi Institute of Technology, Tokyo, Japan, in 2003 and 2006, respectively.

He was a Researcher of electrical and electronic engineering at Musashi Institute of Technology from 2006 to 2007. He is currently an Associate Professor in the Department of Electrical Engineering, Chosun University. His current research interests include the design and the numerical analysis of electric machines and ac servo drive systems.