Investigation and Implementation of a Starting and Voltage Spike Suppression Scheme for Three-Phase Isolated Full-Bridge Boost PFC Converter

Tao Meng, *Member, IEEE*, Hongqi Ben, and Yilin Song

***Abstract*—A starting and voltage spike suppression scheme is proposed and investigated in a three-phase isolated full-bridge boost power factor correction (PFC) converter with the passive flyback auxiliary circuit. In steady state, the auxiliary circuit in the PFC converter is operating as a passive clamp circuit, by which the voltage spike across primary side of the power transformer is suppressed, and the absorbed energy can be transferred to the load during one charging period by the resonance of the inductors and capacitors in the auxiliary circuit. In starting state, the output filter capacitor is charged by the flyback inductor in the auxiliary circuit, and the PFC converter can achieve normal starting-up. The operational processes of the PFC converter are analyzed in both steady and starting states. Furthermore, the design considerations of the key parameters are discussed. Finally, experimental study has been done on a laboratory-made three-phase PFC prototype, and the feasibility of the proposed scheme and the validity of the theoretical analysis are verified by the experimental results.**

***Index Terms*—Boost, starting, three-phase power factor correction (PFC), voltage spike suppression.**

I. Introduction

POWER factor correction (PFC) is one of the most effective methods to reduce harmonics current and increase PF [1]–[4]. Compared to the two-stage PFC, single-stage PFC integrates the function of PFC and isolated dc/dc conversion into a single power converter, and it has the advantages such as simplicity and low cost. Single-stage PFC is an important developing orientation in PFC technique. Presently, many low power single-stage PFC converters have been investigated, however, fewer medium and high-power schemes, but very few the three-phase schemes [4]–[8].

The isolated full-bridge boost topology has the advantages including electrical isolation, soft switching, and inherent short-current protection, and it is suitable for the isolated dc/dc converter and single-stage PFC converter in medium or high power applications. However, the reasons why it has not been widely used can be mainly attributed to the following two problems: 1) it cannot achieve starting-up normally, so an additional starting-up circuit is required to establish an initial output voltage, and 2) due to the existence of the transformer leakage inductance, there is a large voltage spike across the bridge leg [9]–[11]. To resolve these two problems, many effective methods have been proposed and investigated.

For the starting problem, the typical solutions are as follows. A direct starting scheme is presented in [12], which can only be used when the converter is starting with no load. A lossy starting circuit made up of resistor, capacitor, and diode (RCD) is connected in parallel with the bridge leg of the dc/dc converter in [13], and a lossy starting method which connects a resistor in series with the output filter capacitor is used in the three-phase single-stage PFC converter in [14]. In [15], a buck starting scheme is investigated in the single-phase single-stage PFC converter. In [10], [14], and [16], the flyback windings are coupled with the boost inductors of the dc/dc converter or three-phase single-stage PFC converter, and the flyback starting schemes are proposed.

For the voltage spike problem, the solutions can be divided into two categories: the active and the passive approaches. The typical active solutions are as follows. A method based on the basic active clamping technique is presented in [17]–[19], and it has been the most widely investigated. Two new active clamping techniques are proposed in [20] and [21]. A two-switch clamping circuit is presented in [22]. Some active auxiliary circuits with a single-switch are adopted in [18], [23], and [24]. In addition, many passive solutions have also been proposed. For example, the *LC* resonance schemes are studied in [25]–[27], which can also achieve soft switching of the switches. A RCD snubber is used in [28], and a passive clamping technique is proposed in [29]. Some passive snubbers are proposed and investigated in [9], [30], and [31]. In [32] and [33], a family of multilevel passive clamp circuits and a passive flyback auxiliary circuit are

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T. Meng and Y. Song are with the School of Mechanical and Electrical Engineering, Heilongjiang University, Harbin 150080, China (e-mail: mengtao@hit.edu.cn; syl@hlju.edu.cn).

H. Ben is with the School of Electrical Engineering and Automation, Harbin Institute of Technology, Harbin 150001, China (e-mail: benhq@hit.edu.cn).

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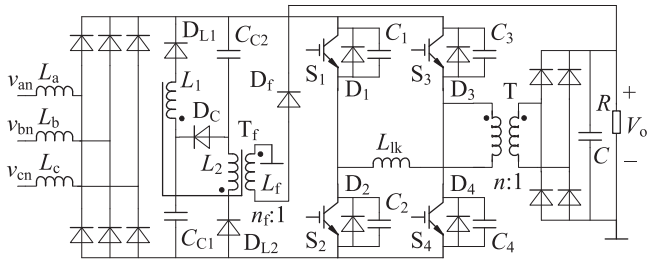

Fig. 1. Three-phase isolated full-bridge boost PFC converter with the passive flyback auxiliary circuit.

used in single-phase and three-phase single-stage PFC converter, respectively.

It can be seen that the above two problems of the isolated full-bridge boost topology have been resolved basically. However, after adoption of each of the existing solutions, some additional devices or control circuits will be introduced. Generally, each of the existing solutions can resolve only one of the above two problems, as a result, if both of the above two problems are resolved efficiently, the complexity of the whole PFC system will increase largely, and the advantages of single-stage PFC will be lost.

In this paper, to resolve the above two problems more efficiently, a starting and voltage spike suppression scheme based on a common passive circuit is proposed and investigated in the three-phase isolated full-bridge boost PFC converter. The proposed scheme in this paper is based on the passive flyback auxiliary circuit in [33], however, the purposes of the same auxiliary circuit are different. In [33], the auxiliary circuit is only used to suppress the voltage spike of the three-phase isolated full-bridge boost PFC converter, which is only aiming at steady state of the PFC converter. While, in this paper, the auxiliary circuit is used to resolve both starting and voltage spike problems of the three-phase isolated full-bridge boost PFC converter, which is aiming at both starting and steady states of the PFC converter. Therefore, the operational principle and design method of the auxiliary circuit in this paper are also different from that in [33]. In this paper, the flyback inductor in the auxiliary circuit is only used in starting state, by which the output filter capacitor can be charged, and the PFC converter can achieve normal starting-up, and in steady state, the auxiliary circuit is operating as a passive clamp circuit, by which the voltage spike of the PFC converter can be suppressed efficiently. The rest of this paper is organized as follows. In Section II, the operational principles of the PFC converter in both steady and starting states are presented. In Section III, the conversion power of the PFC converter is analyzed for the design considerations of the proposed scheme in Section IV. The proposed method and theoretical analysis are verified by the experimental results in Section V. Finally, conclusions are given in Section VI.

II. PFC Converter and its Operational Principles

Fig. 1 shows the three-phase isolated full-bridge boost PFC converter with the passive flyback auxiliary circuit proposed in [33]. $L_{\rm a}$, $L_{\rm b}$, $L_{\rm c}$ ($L_{\rm a} = L_{\rm b} = L_{\rm c} = L$) are the boost inductors, $\rm D_1 \sim D_4$ and $C_1 \sim C_4$ ($C_1 = C_2 = C_3 = C_4$) are the parasitic components of switches $\rm S_1 \sim S_4$, and $L_{\rm lk}$ and n are the equivalent leakage inductance and turns ratio of the transformer T, respectively. The auxiliary circuit is composed of C_{C1}, C_{C2} ($C_{C1} = C_{C2}$), $\rm D_{L1}$, $\rm D_{L2}$, $\rm D_C$, $\rm D_f$, and the flyback integrated transformer $\rm T_f$, where L_1, L_2 ($L_1 = L_2$) are the equivalent inductance in primary side, $L_{\rm f}$ is the inductance in secondary side, and $n_{\rm f}$ is the turns ratio.

To achieve normal starting-up and voltage spike suppression for the three-phase isolated full-bridge boost PFC converter, the auxiliary circuit is operating as a passive clamp circuit in steady state, and the flyback inductor $L_{\rm f}$ and diode $\rm D_f$ are only used in starting state, from which the input energy of the PFC converter can be transferred to the load in starting state. Because $L_{\rm f}$ and $\rm D_f$ are only used in starting state (transient state), the current density in the winding of $L_{\rm f}$ can be much higher than that of L_1 and L_2 (that is to say, the volume and weight of winding for $L_{\rm f}$ will be much lower than that for L_1 and L_2), and the heat dissipation problem of $\rm D_f$ is not considered here. Therefore, compared to the configuration in [33], the volume and cost of $L_{\rm f}$ and $\rm D_f$ will be much lower.

The following is operational process of the PFC converter during one charging period in steady and starting states, respectively, and the analysis is during the time phase of $0 \le \omega t \le \pi/6$, in which the relation of three-phase voltage is $v_{\rm bn} \le 0 \le v_{\rm an} \le v_{\rm cn}$, where $v_{\rm an} = V\sin\omega t$, $v_{\rm bn} = V\sin(\omega t - 2\pi/3)$, and $v_{\rm cn} = V\sin(\omega t + 2\pi/3)$. To simplify the analysis, the following assumption are made:

1) all devices are ideal;
2) during one charging period of the boost inductors (T), the change of $v_{\rm an}$, $v_{\rm bn}$, $v_{\rm cn}$ are negligible because T is much shorter than the line period;
3) the capacitors C_{C1}, C_{C2}, and C are large enough, so their voltages can be considered as constant values during each charging period.

A. Operational Process in Steady State

In steady state, the PFC converter operates in discontinuous current mode (DCM). The auxiliary circuit is operating as a passive clamp circuit, $L_{\rm f}$ and $\rm D_f$ are not used, and $\rm T_f$ is equal to a coupled-inductor (L_1, L_2). During one charging period, there are six basic stages in steady state, and the theoretical waveforms and the equivalent circuit of each stage are shown in Figs. 2 and 3, respectively.

Stage 1 (before t_0): $\rm S_2$, $\rm S_3$ are turning ON, and $\rm S_1$, $\rm S_4$ are turning OFF. Before t_0, the current in both primary and secondary sides of T is zero, and the voltage across primary side of $\rm T: V_{C1} = V_{C4} = nV_o$, $V_{C2} = V_{C3} = 0$, $V_{\rm Cc1} = V_{\rm Cc2} = nV_o/2$. In this stage, the output current is only provided by capacitor C.

Stage 2 ($t_0 \sim t_1$): At t_0, $\rm S_1$ turns ON, and $\rm S_3$ turns OFF with zero voltage and zero current. The current of $L_{\rm a}$, $L_{\rm b}$, $L_{\rm c}$ increases from zero with the charging of $v_{\rm an}$, $v_{\rm bn}$, $v_{\rm cn}$, and the current of L_1, L_2 increases from zero with the charging of C_{C1}, C_{C2}. The capacitors C_{C1} and C_{C2} are large enough, so the decreasing of their voltages can be ignored in this stage. At

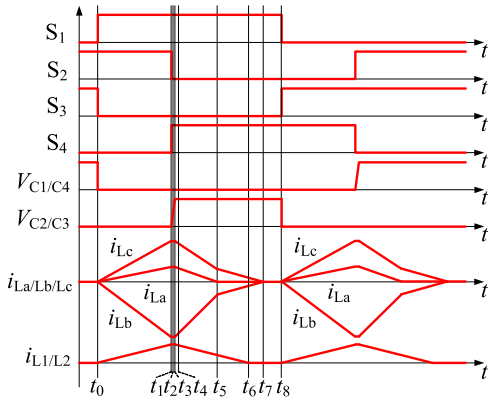

Fig. 2. Theoretical waveforms in steady state.

t_1, the current of each inductor reaches the maximum value of the whole charging period

$$i_{\mathrm{La/Lb/Lc}}(t_1) = \frac{v_{\mathrm{an/bn/cn}}}{L} DT \tag{1}$$

$$i_{\mathrm{L1/L2}}(t_1) = \frac{V_{\mathrm{Cc}}}{L_1} DT = \frac{nV_o}{2L_1} DT. \tag{2}$$

where $D = (t_1 - t_0)/T$ is the duty cycle of the PFC converter in steady state, V_{Cc} is the voltage of C_{C1}, C_{C2} in steady state, and V_{o} is the output voltage in steady state.

In this stage, $V_{C1} = V_{C2} = V_{C3} = V_{C4} = 0$, $V_{\mathrm{Cc1}} = V_{\mathrm{Cc2}} = nV_{\mathrm{o}}/2$, and the output current is only provided by capacitor C.

Stage 3 ($t_1 \sim t_2$): At t_1, $\mathrm{S_2}$ turns OFF, and $\mathrm{S_4}$ turns ON with zero voltage. C_2, C_3 are charged by L_{a}, L_{b}, L_{c}, and their voltages increase from zero immediately. At t_2, $V_{C2} = V_{C3} = V_{\mathrm{Cc1}} = V_{\mathrm{Cc2}} = nV_{\mathrm{o}}/2$, and the charging of L_1, L_2 is over. In this stage, the output current is only provided by capacitor C.

Stage 4 ($t_2 \sim t_3$): At t_2, $\mathrm{D_C}$ is turned ON, L_1 is connected in series with L_2, and C_2, C_3 are charged by L_{a}, L_{b}, L_{c} and L_1, L_2. At t_3, $V_{C1} = V_{C4} = 0$, and $V_{C2} = V_{C3} = nV_{\mathrm{o}}$. In this stage, the output current is only provided by capacitor C.

The values of C_2, C_3 are very small, so the duration of stages 3 and 4 are very small, and the current changing in each inductor can be ignored during these two stages.

Stage 5 ($t_3 \sim t_4$): After t_3, C_{C1}, C_{C2} and C_2, C_3 are charged by L_{a}, L_{b}, L_{c} and L_1, L_2. The current of L_{lk} increases from zero, and the input energy is transferred to the load through T. In this stage, the following relationships can be obtained:

$$\begin{cases} (2C_2 + C_{C1}/2)\frac{\mathrm{d}\Delta V_{\mathrm{C2/C3}}(t)}{\mathrm{d}t} = 2i_{\mathrm{C2/C3}}(t) + i_{\mathrm{Cc}}(t) \\ i_{\mathrm{Llk}}(t) + 2i_{\mathrm{C2/C3}}(t) + i_{\mathrm{Cc}}(t) = 2i_{\mathrm{L1/L2}} - i_{\mathrm{Lb}} \\ L_{\mathrm{lk}}\frac{\mathrm{d}i_{\mathrm{Llk}}(t)}{\mathrm{d}t} = \Delta V_{\mathrm{C2/C3}}(t) \end{cases} \tag{3}$$

where $i_{\mathrm{C2/C3}}$ and i_{Cc} are the charging current of C_2, C_3 and C_{C1}, C_{C2}, and $\Delta V_{\mathrm{C2/C3}}$ is the voltage increasing of C_2, C_3 after t_3.

The values of C_2, C_3 are much smaller than that of C_{C1}, C_{C2}, so they can be ignored when compared to C_{C1}, C_{C2}. During a short time after t_3, $i_{\mathrm{L1/L2}}$ and i_{Lb} can be considered as a constant value, so the following equation can be obtained

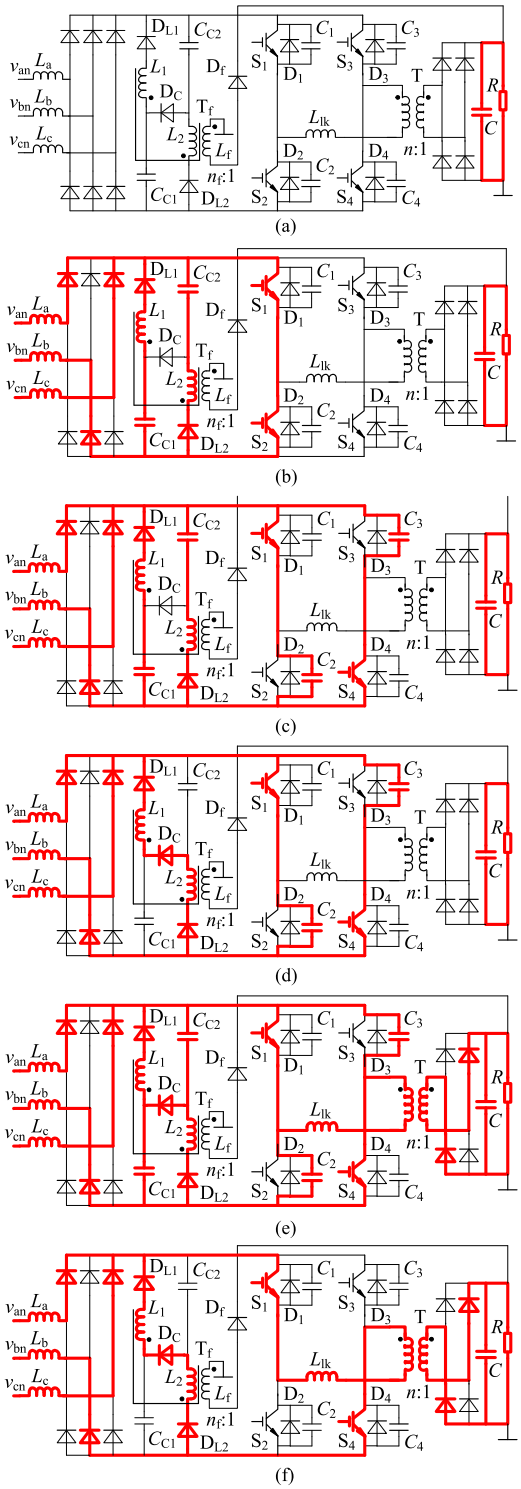

Fig. 3. Equivalent circuit of each stage in steady state. (a) Stage 1. (b) Stage 2. (c) Stage 3. (d) Stage 4. (e) Stage 5. (f) Stage 6.

from (3):

$$\Delta V_{\mathrm{C2/C3}}(t) + \frac{L_{\mathrm{lk}}C_{C1}}{2}\frac{\mathrm{d}\Delta V_{\mathrm{C2/C3}}(t)}{\mathrm{d}t} = 0. \tag{4}$$

Equation (4) has the initial data: $\Delta V_{\mathrm{C2/C3}}(t_3) = 0$, $i_{\mathrm{Llk}}(t_3) = 0$, and $i_{\mathrm{C2/C3}}(t_3) + i_{\mathrm{Cc}}(t_3) = 2i_{\mathrm{L1/L2}} - i_{\mathrm{Lb}}$. So

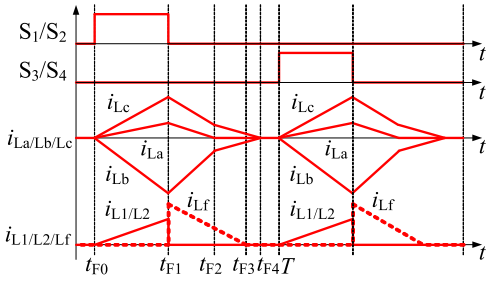

Fig. 4. Theoretical waveforms in starting state.

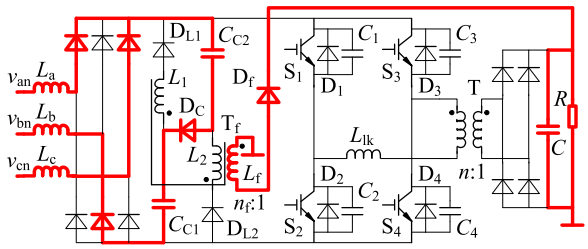

Fig. 5. Equivalent circuit of stage 2 in starting state.

it can be obtained that

$$\Delta V_{\mathrm{C2/C3}}(t) = (2i_{\mathrm{L1/L2}} - i_{\mathrm{Lb}})\sqrt{\frac{2L_{\mathrm{lk}}}{C_{C1}}}\sin\sqrt{\frac{2}{L_{\mathrm{lk}}C_{C1}}}(t-t_3) \tag{5}$$

$$i_{\mathrm{Llk}}(t) = (2i_{\mathrm{L1/L2}} - i_{\mathrm{Lb}})[1-\cos\sqrt{\frac{2}{L_{\mathrm{lk}}C_{C1}}}(t-t_3)]. \tag{6}$$

At t_4, $i_{\mathrm{Llk}}(t_4) = 2i_{\mathrm{L1/L2}} - i_{\mathrm{Lb}}$. From (5), it can be seen that if the values of C_{C1}, C_{C2} are large enough, the voltage increasing of C_2, C_3 can be ignored in this stage.

Stage 6 ($t_4 \sim t_8$): In this stage, the current of L_{a}, L_{b}, L_{c} and L_1, L_2 flows through S_1, S_4 and T to the load, and it can be calculated that

$$i_{\mathrm{L1/L2}}(t) = \frac{nV_o}{2L_1}DT - \frac{nV_o}{2L_1}(t-t_3). \tag{7}$$

At t_5, i_{La} reduces to zero, and $i_{\mathrm{L1/L2}}$, i_{Lb} (or i_{Lc}) reduce to zero at t_6, t_7, respectively. During the time t_7 to t_8, the current in both primary and secondary sides of T is zero.

After t_8, the PFC converter operates in another charging period, and the switching state between S_1 and S_3, and S_2 and S_4 are exchanged.

B. Operational Process in Starting State

In starting state, the PFC converter and the auxiliary circuit operate in DCM, the input energy is transferred to the load through L_{f} and D_{f}, and the switching frequency of each switch is the same as that in steady state. During one charging period, there are two basic stages in starting state, and the theoretical waveforms of each stage are shown in Fig. 4.

Stage 1 ($t_{F0} \sim t_{F1}$): The equivalent circuit of this stage is the same as that in Fig. 3(b). In this stage, the bridge leg switches are shorted (it is assumed that S_1, S_2 are turning ON), the current of L_{a}, L_{b}, L_{c} and L_1, L_2 increases from zero with the charging of v_{an}, v_{bn}, v_{cn} and C_{C1}, C_{C2}, respectively, and the output current is only provided by capacitor C. At t_{F1}, the current of each inductor reaches the maximum value of the whole charging period

$$i_{\mathrm{La/Lb/Lc}}(t_{F1}) = \frac{v_{\mathrm{an/bn/cn}}}{L}D_FT \tag{8}$$

$$i_{\mathrm{L1/L2}}(t_{F1}) = \frac{V_{\mathrm{CcF}}}{L_1}D_FT = \frac{\alpha nV_o}{2L_1}D_FT \tag{9}$$

where $D_{\mathrm{F}} = (t_{F1} - t_{F0})/T$ is the duty cycle of the PFC converter in starting state, and V_{CcF} ($2V_{\mathrm{CcF}} = \alpha nV_{\mathrm{o}}$) is the voltage of C_{C1}, C_{C2} in starting state.

Stage 2 ($t_{F1} \sim T$): The equivalent circuit of this stage is shown in Fig. 5. At t_{F1}, S_1, S_2 are turned OFF. In this stage, C_{C1}, C_{C2} is charged by L_{a}, L_{b}, L_{c}, and the increasing energy of C_{C1}, C_{C2} is equal to the decreasing energy of C_{C1}, C_{C2} in stage 1. In the auxiliary circuit, the energy of L_1, L_2 is transferred to the load through L_{f}. The current expression of L_{f} in this stage is

$$i_{\mathrm{Lf}}(t) = \frac{\alpha nV_oD_FTn_f}{L_1} - \frac{V_{\mathrm{oF}}}{L_f}(t-t_{F1}) \tag{10}$$

where V_{oF} ($V_{\mathrm{oF}} \le V_{\mathrm{o}}$) is the output voltage in starting state.

At t_{F2}, i_{La} reduces to zero, and i_{Lf}, i_{Lb} (or i_{Lc}) reduce to zero at t_{F3}, t_{F4}, respectively. After t_{F4}, the current in both primary and secondary sides of T is zero.

III. Analysis of the Conversion Power

A. Power Requirement in Starting State

From the analysis in Section II, it can be seen that input energy of the PFC converter is transferred to the load through the auxiliary circuit entirely in starting state. Therefore, as to design of the proposed scheme, the output power of the PFC converter in starting state should be analyzed according to that in steady state.

In steady and starting states, the output power of the PFC converter can be expressed, respectively

$$P_o = \frac{V_o^2}{R} \quad P_{\mathrm{oF}} = \frac{V_{\mathrm{oF}}^2}{R_F} \tag{11}$$

where R, R_{F} ($R_{\mathrm{F}} = \lambda R$, $\lambda \ge 1$) are the load of the PFC converter in steady and starting states, respectively.

It can be seen that $\lambda = \infty$ means that the PFC converter achieves starting-up with no load, and $\lambda = 1$ means that the PFC converter achieves starting-up with the same load as that in steady state.

The PFC converter operates in boost mode in steady state, so it must be achieved that

$$M = \frac{nV_o}{\sqrt{3}V} \ge 1 \tag{12}$$

where M is the voltage ratio of the PFC converter in steady state.

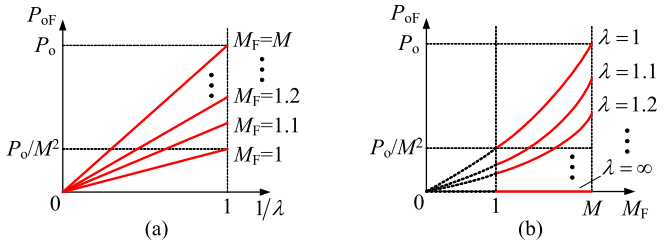

Fig. 6. Relationships between P_{oF}, M_F, and λ. (a) Relationship between P_{oF} and λ. (b) Relationships between P_{oF} and M_F.

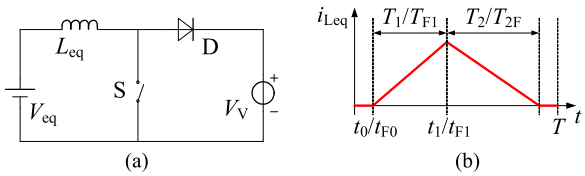

Fig. 7. Equivalent model of the PFC converter. (a) The equivalent circuit. (b) Current of L_{eq} during one charging period.

Similarly, the PFC converter can realize normal starting-up only if the following relationship is achieved:

$$M_F = \frac{nV_{oF}}{\sqrt{3}V} \geq 1 \tag{13}$$

where $1 \leq M_F \leq M$.

From (11)–(13), it can be obtained that

$$P_{oF} = \left(\frac{M_F}{M}\right)^2 \frac{1}{\lambda} P_o. \tag{14}$$

From (14), the relationships between P_{oF}, M_F and λ can be obtained as shown in Fig. 6. It can be seen that:

1) P_{oF} will increase as λ decreases or M_F increases;
2) when $M_F = 1$, the minimum value of P_{oF} is $P_o/\lambda M^2$;
3) if $\lambda = \infty$, and then $P_{oF} = 0$ (the charging energy of C is not considered here).

B. Input Power Estimation in Steady and Starting State

To simplify the calculation, the equivalent circuit in Fig. 7(a) is adopted to estimate the input power of the PFC converter approximately. Where V_{eq} is the equivalent dc input voltage, L_{eq} is the equivalent boost inductor, and the current of L_{eq} during one charging period is shown in Fig. 7(b).When the switch S is turning ON, it is equal to the bridge leg switches are shorted (S_1, S_2 or S_3, S_4 are turning ON), and when S is turning OFF, it is equal to the bridge diagonal-leg switches are turning ON (S_1, S_4 or S_2, S_3 are turning ON). V_V is the equivalent bridge leg voltage (in steady state, $V_V = nV_o$, and in starting state, $V_V = \alpha n V_o$).

In steady state, during the time phase of $0 \leq \omega t \leq \pi/6$, output current of the input rectifier in Fig. 1 is equal to $-i_{Lb}$, therefore it should be achieved at t_1

$$i_{Leq}(t_1) = \frac{V_{eq}}{L_{eq}} DT = \frac{6}{\pi} \int_0^{\frac{\pi}{6}} [-i_{Lb}(t_1)] \mathrm{d}\omega t. \tag{15}$$

At t_1, the sum energy of L_a, L_b, L_c in Fig. 1 can be calculated

$$W_L = \frac{1}{2} L[i_{La}^2(t_1) + i_{Lb}^2(t_1) + i_{Lc}^2(t_1)] = \frac{3V^2D^2T^2}{4L}. \tag{16}$$

Therefore, it should be achieved at t_1

$$W_L = W_{Leq} = \frac{1}{2} L_{eq} i_{Leq}^2(t_1). \tag{17}$$

From (15) to (17), it can be obtained that

$$V_{eq} = \frac{\pi}{2} V \quad L_{eq} = \frac{\pi^2}{6} L. \tag{18}$$

In starting state, the same expressions of V_{eq} and L_{eq} can also be obtained through the similar calculated process, so it is not presented again.

From Fig. 7, the following relationships can be obtained:

$$\begin{cases} i_{Leq}(t_1) = \frac{V_V - V_{eq}}{L_{eq}} T_2 = \frac{nV_o - V_{eq}}{L_{eq}} T_2 \\ i_{Leq}(t_{F1}) = \frac{V_V - V_{eq}}{L_{eq}} T_{2F} = \frac{\alpha n V_o - V_{eq}}{L_{eq}} T_{2F} \end{cases}. \tag{19}$$

It can be calculated from (15), (18), and (19) that

$$T_2 = \frac{\pi DT}{2\sqrt{3}M - \pi} \quad T_{2F} = \frac{\pi D_F T}{2\sqrt{3}\alpha M - \pi}. \tag{20}$$

Therefore, the average input power of the PFC converter can be calculated in steady and starting states

$$\begin{cases} P_i = nV_o \frac{i_{Leq}(t_1)}{2} \frac{T_2}{T} = \frac{3\sqrt{3}MV^2D^2T}{2L(2\sqrt{3}M - \pi)} \\ P_{iF} = \alpha n V_o \frac{i_{Leq}(t_{F1})}{2} \frac{T_{2F}}{T} = \frac{3\sqrt{3}MV^2D_F^2T}{2L(2\sqrt{3}M - \pi/\alpha)} \end{cases}. \tag{21}$$

IV. Design Considerations

In steady state, T_f is equal to a coupled-inductor (L_1, L_2), and in starting state, T_f is operating as a flyback integrated-transformer. With the help of T_f, the voltage and current in the auxiliary circuit will be balance in both steady and starting states, that is to say, it will be achieved that $V_{Cc1} = V_{Cc2}$ and $i_{L1} = i_{L2}$. These mechanisms have been analyzed in details in [32] and [33], so they are not discussed here again.

To realize the proposed scheme, the key parameters such as the equivalent inductance L_1, the turn ratio n_f, and the maximum duty cycle D_{max} and D_{Fmax} are important. So design considerations of these key parameters are discussed as follows (L, M, and n are the parameters of the PFC converter itself, which are not determined by the auxiliary circuit, so they are not discussed here).

A. Equivalent Inductance L_1 and Capacitance C_{C1}

In starting state, the input energy is transferred to the load from the auxiliary circuit entirely, so the output power of the PFC converter in starting state is equal to the average discharging power of C_{C1} and C_{C2}. It can be calculated from (9) and (12) that

$$P_{oF} = \frac{1}{2} L_1 [i_{L1/L2}(t_{F1})]^2 \frac{2}{T} = \frac{3\alpha^2 M^2 V^2 D_F^2 T}{4L_1}. \tag{22}$$

If the power losses are ignored in the PFC converter, it can be obtained that $P_{\mathrm{iF}} = P_{\mathrm{oF}}$. Therefore, the equivalent inductance L_1 can be calculated from (21) and (22):

$$L_1 = M\alpha\left(M\alpha - \frac{\pi}{2\sqrt{3}}\right)L. \tag{23}$$

From the analysis in Section II, the voltage of C_{C1} (or C_{C2}) in steady and starting state are $nV_{\mathrm{o}}/2$ and $\alpha nV_{\mathrm{o}}/2$, respectively, their discharging current in steady and starting state is i_{L1} (or i_{L2}), and their charging current in steady and starting state are $i_{L1} - i_{\mathrm{Lb}}$ and $-i_{\mathrm{Lb}}$, respectively.

In this auxiliary circuit, the voltage of C_{C1} (or C_{C2}) is considered as a constant value during the charging and discharging process. As a result, there must be a minimum value for C_{C1} (or C_{C2}) to limit the voltage ripple itself. The design of C_{C1} (or C_{C2}) is equivalent to that of the other conventional capacitor in the power converter such as the output filter capacitor C in this PFC converter, therefore, the conventional design principle is not discussed here.

B. Turn Ratio of the Flyback Transformer n_{f}

In steady state, the flyback inductor L_{f} is not used, so it must be achieved that

$$V_{\mathrm{Cc}} = \frac{nV_o}{2} \le n_f V_o \Rightarrow \frac{2n_f}{n} \ge 1. \tag{24}$$

In starting state, the energy of L_1 and L_2 is transferred to L_{f} entirely, so it must be achieved that

$$V_{\mathrm{CcF}} = \frac{\alpha nV_o}{2} \ge n_f V_{\mathrm{oF}}. \tag{25}$$

From (12), (13), (24), and (25), the limitation of n_{f} can be obtained

$$1 \le \frac{2n_f}{n} \le \frac{\alpha M}{M_F}. \tag{26}$$

C. Maximum Duty Cycle in Steady and Starting States

In steady state, $\mathrm{T_f}$ is operating as a coupled-inductor. In order to avoid the magnetic saturation, the current of L_1, L_2 must reduce to zero during each charging period. Therefore, the limitation of $D_{\max}$ can be obtained from (7):

$$\frac{nV_o}{2L_1}DT \le \frac{nV_o}{2L_1}(1-D)T \Rightarrow D_{\max} \le 0.5. \tag{27}$$

It is considered that to make sure the PFC converter operates in DCM, the maximum duty cycle must be lower than some a certain limitation D_{D} (the value D_{D} is not determined by the auxiliary circuit, so its calculation process is not discussed here). Therefore, both $D_{\max} \le 0.5$ and $D_{\max} \le D_{\mathrm{D}}$ must be achieved.

From (14) and (21), the relationship between D_{Fmax}, M_{F}, λ and $D_{\max}$ can be obtained (the power losses are ignored in the PFC converter, so it is considered that $P_{\mathrm{i}} = P_{\mathrm{o}}$ and $P_{\mathrm{iF}} = P_{\mathrm{oF}}$)

$$D_{\mathrm{Fmax}}{}^2 = \frac{M_F{}^2}{\lambda M^2}\frac{2\sqrt{3}M - \pi/\alpha}{2\sqrt{3}M - \pi}D_{\max}{}^2. \tag{28}$$

From (14) and (28), it can be seen that the relationships between D^2_{Fmax}, M_{F}, λ and $D^2_{\max}$ are similar to the relationships between P_{oF}, M_{F}, λ and P_{o} as shown in Fig. 6, so the related curves are not given here again. It can be seen that D_{Fmax} will increase as M_{F}, α or $D_{\max}$ increase and D_{Fmax} will decrease as λ increases.

From (13) and (28), the first limitation of D_{Fmax} can be obtained

$$D_{\mathrm{Fmax}} \ge \frac{1}{M\sqrt{\lambda}}\sqrt{\frac{2\sqrt{3}M - \pi/\alpha}{2\sqrt{3}M - \pi}}D_{\max}. \tag{29}$$

In starting state, it can be obtained that $P_{\mathrm{iF}} = P_{\mathrm{oF}} = V^2_{\mathrm{oF}}/\lambda R$. And then it can be calculated from (21) that

$$V_{\mathrm{oF}} = \sqrt{\frac{3\sqrt{3}M\alpha\lambda RT}{(4\sqrt{3}M\alpha - 2\pi)L}}VD_F. \tag{30}$$

From (13) and (30), the second limitation of D_{Fmax} can be obtained

$$D_{\mathrm{Fmax}} \ge \frac{1}{n}\sqrt{\frac{(4\sqrt{3}M\alpha - 2\pi)L}{3M\alpha\lambda RT}}. \tag{31}$$

In starting state, the auxiliary circuit operates in DCM, therefore, it must be achieved from (10) that

$$\frac{\alpha nV_oD_FTn_f}{L_1} \le \frac{V_{\mathrm{oF}}}{L_f}(1-D_F)T. \tag{32}$$

Therefore, from (12), (13), and (32), the third limitation of D_{Fmax} can be obtained

$$D_{\mathrm{Fmax}} \le \frac{2n_fM_F}{\alpha nM + 2n_fM_F}. \tag{33}$$

From the analysis in Section II, it can be seen that the charging processes of L_{a}, L_{b}, L_{c} and L_1, L_2 in starting state are the same as that in steady state, so to avoid overcurrent of L_{a}, L_{b}, L_{c} and L_1, L_2 in starting state, it must be achieved from (1), (2), (8), and (9) that

$$\begin{cases} \frac{v_{\mathrm{an/bn/cn}}}{L}D_{\mathrm{Fmax}}T \le \frac{v_{\mathrm{an/bn/cn}}}{L}D_{\max}T \\ \frac{\alpha nV_o}{2L_1}D_FT \le \frac{nV_o}{2L_1}DT \end{cases}. \tag{34}$$

From (34), the fourth limitations of D_{Fmax} are obtained

$$D_{\mathrm{Fmax}} \le D_{\max} \quad D_{\mathrm{Fmax}} \le D_{\max}/\alpha. \tag{35}$$

D. Design Summary

From (23), (26), (29), (31), (33), and (35), it can be seen that the key parameters of the auxiliary circuit including the equivalent inductance L_1, turn ratio of the flyback transformer n_{f} and the maximum duty cycle in starting state D_{Fmax} are mainly determined by the value α. Therefore, α is an important value for design of the auxiliary circuit.

The PFC converter operates in DCM during both steady and starting states. Therefore, it can be obtained from Fig. 7(b) that

$$T_2 \le (1-D)T \quad T_{2\mathrm{F}} \le (1-D_F)T. \tag{36}$$

From (20) and (36), the DCM limitations of the PFC converter in steady and starting states can be calculated

$$D_{\max} \le 1 - \frac{\pi}{2\sqrt{3}M} \quad D_{\mathrm{F}\max} \le 1 - \frac{\pi}{2\sqrt{3}\alpha M}. \tag{37}$$

The DCM condition of the PFC converter in steady state is not considered here. If the PFC converter operates in DCM in steady state, the sufficient condition to make sure that the PFC converter operates in DCM in starting state can be obtained from (35) and (37) that

$$\alpha \ge 1. \tag{38}$$

From (22) and (23), it can be obtained that

$$P_{\mathrm{oF}} = \frac{3V^2 D_F^2 T}{4L}\left(1 + \frac{\pi}{2\sqrt{3}M\alpha - \pi}\right). \tag{39}$$

From the analysis in Section II, the voltage stress of $\mathrm{S}_1 \sim \mathrm{S}_4$ in steady and starting states, and the current stress of $\mathrm{S}_1 \sim \mathrm{S}_4$ in steady state can be obtained as follows:

$$V_S = 2V_{\mathrm{Cc}} = nV_o \quad V_{\mathrm{SF}} = 2V_{\mathrm{CcF}} = \alpha n V_o \tag{40}$$

$$I_S = -I_{\mathrm{Lbmax}} + 2i_{\mathrm{L1/L2}}(t_1) = \frac{VDT}{L} + \frac{6VDT}{\alpha(2\sqrt{3}M\alpha - \pi)L}. \tag{41}$$

From [33], it can be seen that $n_{\mathrm{f}}^2 = L_{11}/L_{\mathrm{f}}$, where $L_{11} = L_1/2$ is the self-inductance in primary side of $\mathrm{T_f}$. Therefore, the *AP* value of $\mathrm{T_f}$ can be calculated

$$AP_{\mathrm{Tf}} = \frac{L_{11}[2i_{\mathrm{L1/L2}}(t_1)]^2}{BJK} = \frac{3\sqrt{3}MV^2D^2T^2}{BJK\alpha(2\sqrt{3}M\alpha - \pi)L}. \tag{42}$$

where *B* is the maximum magnetic induction intensity, *J* is the current density, and *K* is the utilization of the window area.

From (39) to (42), it can be seen that the values P_{oF}, V_{SF}, I_{S} and AP_{Tf} are also determined by the value α, when α increases, P_{oF}, I_{S}, AP_{Tf} will decrease, but V_{SF} will increase. Therefore, in the practical case, the value α should be determined according to the requirements or limitations of the values P_{oF}, V_{SF}, I_{S} and AP_{Tf}.

V. Experimental Verifications

To verify the proposed method and theoretical analysis, the experimental study has been done on a laboratory-made prototype of the three-phase isolated full-bridge boost PFC converter. The main utilized components and the key parameters of the PFC prototype are $v_{\mathrm{an/bn/cn}} = 110\ \mathrm{Vrms} \pm 10\%$, $V_{\mathrm{o}} = 200\ \mathrm{Vdc}$, $L_{\mathrm{a}} = L_{\mathrm{b}} = L_{\mathrm{c}} = 76\ \mu\mathrm{H}$, S_1–S_4: BSM75GB120DN2 (the switching frequency is 20 kHz), $n = 2$, $L_{\mathrm{lk}} = 6\ \mu\mathrm{H}$, $C = 1000\ \mu\mathrm{F}$.

From (38) and (40), it can be seen that the voltage stress of $\mathrm{S}_1 \sim \mathrm{S}_4$ in starting state may be higher than that in steady state. If the overvoltage in starting state is limited within 20%, and then the design limitation of the value α is determined here: $1 \le \alpha \le 1.2$. Accordingly, the key parameters of the auxiliary circuit are determined as follows, where $\lambda = 1$ and $M_{\mathrm{F}} \approx 1$ (or M_{F} is only a litter larger than 1) are selected here: $C_{C1} = C_{C2} = 5.4\ \mu\mathrm{F}$, $L_1 = L_2 = 720\ \mu\mathrm{H}$, $n_{\mathrm{f}} = 1.25$ and $D_{\mathrm{F}\max} = 28\%$ ($D_{\max} = 40\%$).

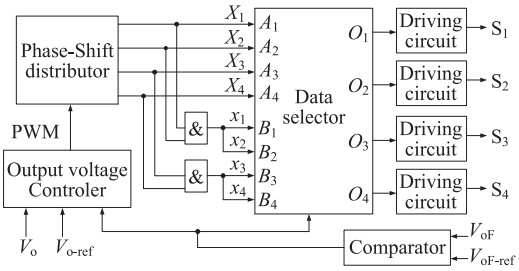

Fig. 8. Basic control principle of the PFC converter.

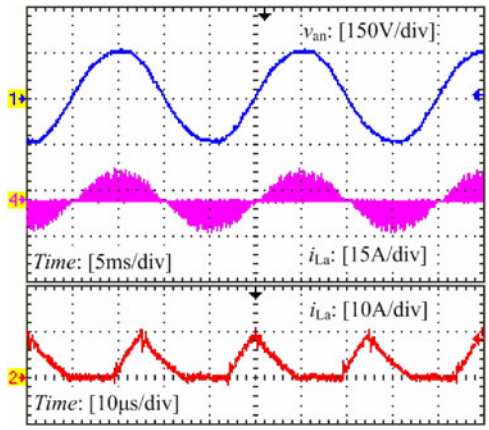

Fig. 9. Input waveforms of phase A in starting state.

The basic control principle of this PFC prototype is shown in Fig. 8. A traditional output voltage controller is adopted, from which a PWM signal is generated. $X_1 \sim X_4$ and $x_1 \sim x_4$ ($x_1 = x_2 = X_1 \cdot X_2$, $x_3 = x_4 = X_3 \cdot X_4$) are the switching signals of $\mathrm{S}_1 \sim \mathrm{S}_4$ when the PFC converter operating in steady and starting states respectively, which are generated from the phase-shift distributor with the PWM signal input. The logic waveforms of $X_1 \sim X_4$ and $x_1 \sim x_4$ are the same as that of $\mathrm{S}_1 \sim \mathrm{S}_4$ in steady and starting states as shown in Figs. 2 and 4, respectively, so they are not given here again. In starting state, the output voltage V_{oF} is increasing from zero, and $x_1 \sim x_4$ are selected by the data selector for the driving circuits of $\mathrm{S}_1 \sim \mathrm{S}_4$. When the output voltage is increased to a suitable value ($V_{\mathrm{oF}} = V_{\mathrm{oF-ref}}$), $X_1 \sim X_4$ are selected by the data selector for the driving circuits of $\mathrm{S}_1 \sim \mathrm{S}_4$, and the PFC converter is transferred to steady state.

A. Experimental Results in Starting State

Fig. 9 shows the input waveforms of phase A in starting state when the flyback inductor L_{f} in the auxiliary circuit is used. It can be seen that the PFC converter operates in DCM and the PFC function can also be realized in starting state. During this transient state, the PF value is not important to the PFC converter, which is not given here.

Fig. 10 shows the voltage and current waveforms of the auxiliary circuit in starting state. From Fig. 10(a), it can be seen

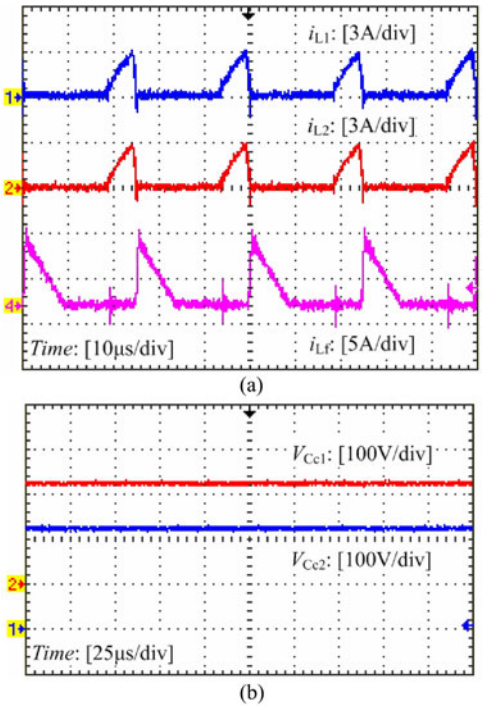

Fig. 10. Voltage and current waveforms of the auxiliary circuit in starting state. (a) Current in primary and secondary sides of T_f. (b) Voltage of C_{C1} and C_{C2}.

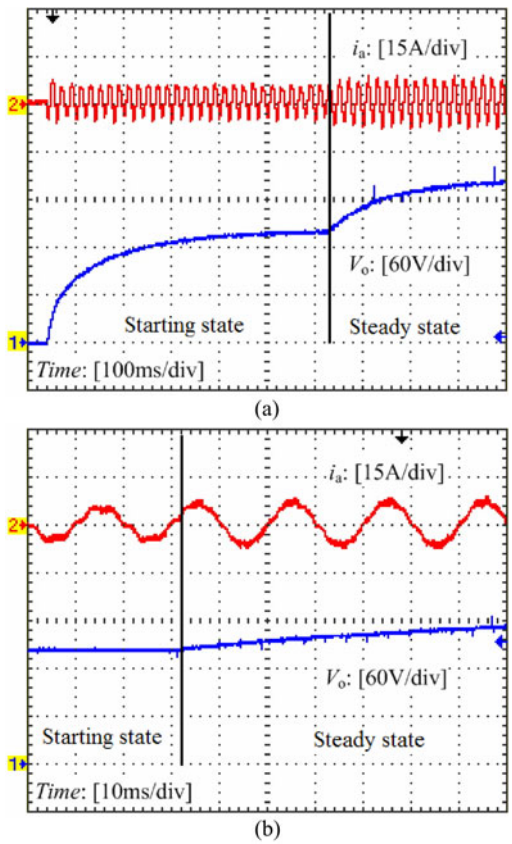

Fig. 11. Input current of phase A and output voltage waveforms during the starting process. (a) Waveforms during the whole starting process. (b) The transitional waveforms between starting and steady state.

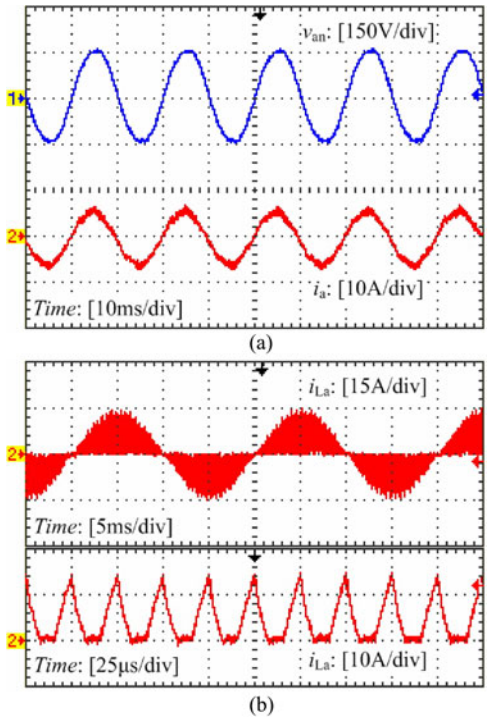

Fig. 12. Input waveforms of phase A in steady state. (a) Input voltage and current. (b) Discontinuous current.

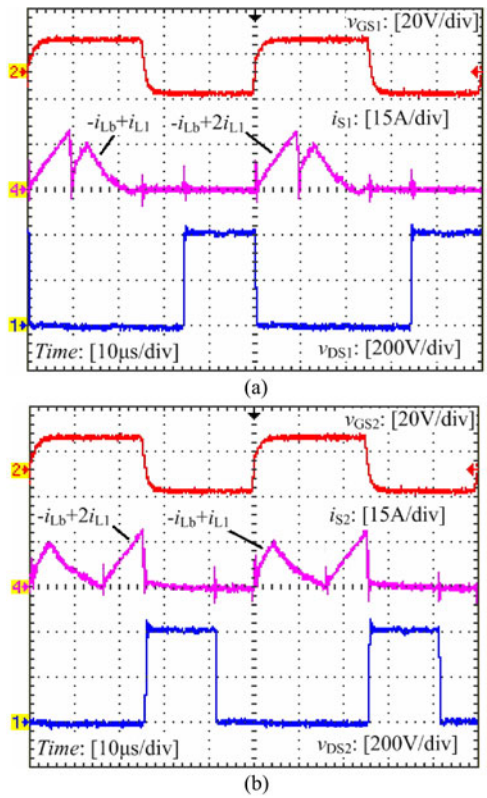

Fig. 13. Voltage and current waveforms of S_1 and S_2 in steady state. (a) Driving, current, and voltage of S_1. (b) Driving, current, and voltage of S_2.

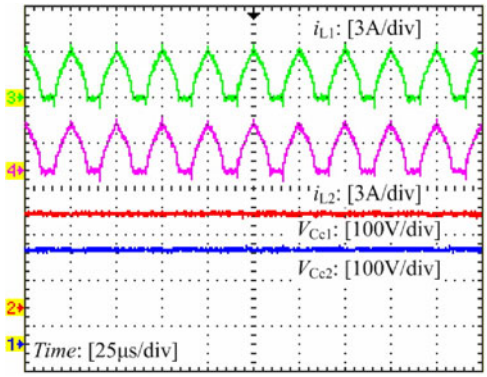

Fig. 14. Voltage and current waveforms of the auxiliary circuit in steady state.

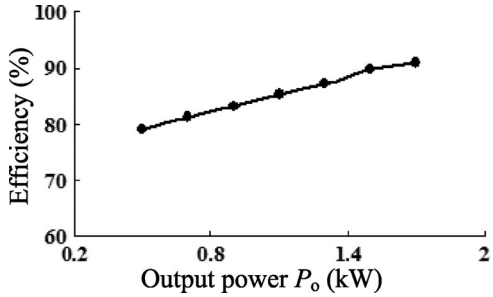

Fig. 15. Efficiency curve of the PFC prototype in steady state.

that the flyback integrated transformer T_f operates in DCM and the energy is transferred through the auxiliary circuit in starting state. Compare the voltage waveforms of C_{C1} and C_{C2} in Fig. 10(b) to those in Fig. 14, it can be seen that the over-voltage of C_{C1} and C_{C2} in starting state is within 20%, which is satisfy with the design requirement of the value α.

Fig. 11 shows the input current of phase A and the output voltage of the PFC converter during its starting process, where i_a is the input current of phase A when a simple *LC* low-pass filter is introduced. It can be seen that there are no over-current appearing in the whole starting process, and the PFC converter has achieved starting-up normally.

B. Experimental Results in Steady State

Fig. 12 shows the input waveforms of phase A when the PFC converter operating in steady state, and the testing PF value is about 0.99. Compared to the experimental results in Fig. 7 of [33], it can be seen that after implementation of the proposed scheme, the PFC converter also operates in DCM, and the PFC function are almost the same.

Fig. 13 shows the driving, current, and voltage waveforms of S_1 and S_2 in steady state. It can be seen that S_1 turns OFF with zero voltage and zero current, S_2 turns ON with zero voltage, and the voltage spike of the PFC converter has been suppressed effectively. Compared to the experimental results in Fig. 9 of [33], it can be seen that after implementation of the proposed scheme, the related features of the PFC converter such as soft-switching and voltage spike suppression are almost the same.

Fig. 14 shows the voltage and current waveforms of the auxiliary circuit in steady state. It can be seen that the flyback integrated-transformer T_f is operating as a coupled-inductor (L_1, L_2) in steady state, and the current of two equivalent inductors has reduced to zero in each charging period. From Figs. 10 and 14, it can also been seen that the voltage between C_{C1} and C_{C2} and the current between L_1 and L_2 are balance in both starting and steady states.

Fig. 15 shows the efficiency curve according to output power of the PFC prototype. It can be seen from the operational analysis that the energy of the auxiliary circuit is not determined by the current $(-i_{Lb})$ of the PFC converter but the voltage (nV_o) of the PFC converter, so if the converter was used in much larger application, its efficiency will be improved furthermore. Compared to the experimental result in Fig. 12 of [33], it can be seen that after implementation of the proposed scheme, the conversion efficiency of the PFC converter is almost the same.

VI. Conclusion

In this paper, aiming at the three-phase isolated full-bridge boost PFC converter, a starting and voltage spike suppression scheme based on a common passive circuit is proposed and investigated. The investigation is based on a three-phase isolated full-bridge boost PFC converter with the passive flyback auxiliary circuit. The auxiliary circuit is operating as a passive clamp circuit in steady state, and the voltage spike in the PFC converter can be suppressed. In starting state, the flyback inductor in the auxiliary circuit is used, by which the output filter capacitor is charged, and the output voltage of the PFC converter can be established. The operational processes of the PFC converter are analyzed in both steady and starting states as well as its conversion power based on which the design considerations of the key parameters are discussed, and the proposed scheme is implemented in a laboratory-made three-phase PFC prototype. The theoretical analysis and experimental results show that after implementation of the proposed scheme, the voltage spike in the PFC converter is suppressed efficiently, and the PFC converter can achieve normal starting-up.

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Tao Meng (M'15) was born in Liaoning Province, China, in 1980. He received the B.S., M.S., and Ph.D. degrees in electrical engineering from Harbin Institute of Technology, Harbin, China, in 2003, 2005, and 2010, respectively.

He is currently an Associate Professor in the School of Mechanical and Electrical Engineering, Heilongjiang University, Harbin, China. His research interests include power factor correction technique, high frequency ac/dc and dc/dc conversion technique, magnetic integration technique, and its applications.

Hongqi Ben was born in Heilongjiang Province, China, in 1965. He received the B.S. degree in electrical engineering from Shenyang University of Technology, Shenyang, China, in 1988, the M.S. degree in electrical engineering and the Ph.D degree in mechanical engineering both from Harbin Institute of Technology, Harbin, China, in 1991 and 1999, respectively.

He is currently a Professor in the School of Electrical Engineering and Automation, Harbin Institute of Technology. His research interests include high frequency power conversion technique and power factor correction technique.

Yilin Song was born in Shandong Province, China, in 1960. He received the B.S. degree in mechanical engineering from Tongji University, Shanghai, China, in 1982, the M.S. degree in mining machinery from the University of Science and Technology Beijing, Beijing, China, in 1987, and the Ph.D degree in division of innovative technology and science from Kanazawa University, Jinze, Japan, in 2002.

He is currently a Professor in the School of Mechanical and Electrical Engineering, Heilongjiang University, Harbin, China. His research interests include theory and application of Mechatronics.