Letters

High-Efficiency Self-Driven Circuit With Parallel Branch For High Frequency Converters

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***Abstract*—With the development of high frequency converters, driving circuits have gained more and more attention. Self-driven methods can effectively simplify system design and reduce components' number. A basic self-driven circuit can be achieved by adding a series resonant inductor at the switch gate; however the losses of driving circuit are high. To reduce the corresponding losses, a high efficiency self-driven network with an additional parallel branch is proposed, which can significantly improve the system efficiency. A 13 MHz prototype is built to verify the feasibility of the proposed self-driven circuit. The system efficiency can be improved from 80% to 83.9%.**

***Index Terms*—High efficiency, high frequency, self-driven.**

I. Introduction

OVER the past several years, with the rapid development of electronic power conversion technology, system operating frequencies continue to increase [1]–[16]. In [11]–[16], the operating frequencies have risen to around tens of megahertz, which can greatly reduce the system volume and improve power density. However, despite the merits of high frequency converters operating at tens of megahertz, driving circuit losses restrict the improvement of system efficiency. To solve this problem, resonant driving circuits have been gradually proposed. For most resonant driving circuits, the driving signal is generated by an oscillator. Furthermore, several parallel inverters are adopted to enhance the driving ability. These chips increase the number of components. More important, their power consumption also increases the driving circuit losses and reduces system efficiency. To simplify the driving circuit in high frequency conditions, the concept of the self-driven circuit for high frequency converters is proposed in [12], and is built by adding only a bias voltage and an inductor at the switch gate. Thus, the aforementioned losses can be avoided. However, the losses of the basic self-driven circuit are still quite high, especially the great losses of the bias voltage source. Thus, it is necessary to analyze the characteristics of the self-driven circuit and propose other self-driven topologies to improve driving circuit efficiency.

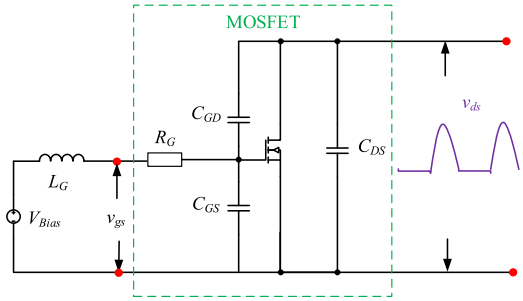

Fig. 1. Diagram of the basic self-driven circuit.

This paper proposes a high efficiency self-driven circuit with a parallel branch. Section II derives the voltage transfer function of switch drain–source voltage and gate voltage. To improve the self-driven circuit efficiency, a high efficiency self-driven network with an additional parallel branch is proposed in Section III. In Section IV, a 13 MHz prototype with the proposed self-driven circuit is designed and built to verify the feasibility of the circuit. The conclusion is provided in Section V.

II. Analysis of the Basic Self-Driven Circuit

In high frequency converters, the inverter stage with a single switch structure is usually adopted because of the simplicity of ground-reference driving circuits. The drain–source voltage of the switch is in a half-sinusoid form. Thus, self-driven characteristics may be realized by feeding back the drain–source voltage to the switch gate. Fig. 1 shows the basic self-driven circuit. It can be seen that a series resonant inductor and a dc bias voltage source are added to the driving circuit.

To realize self-driven ability, the relationship between the switch gate voltage v_{gs} and switch drain–source voltage $v_{\rm ds}$ should satisfy the following the rules:

1) there should be an almost 180° phase difference between the gate voltage v_{gs} and drain–source voltage $v_{\rm ds}$;
2) the amplitude of v_{gs} should be within the proper driving voltage range of the selected switch.

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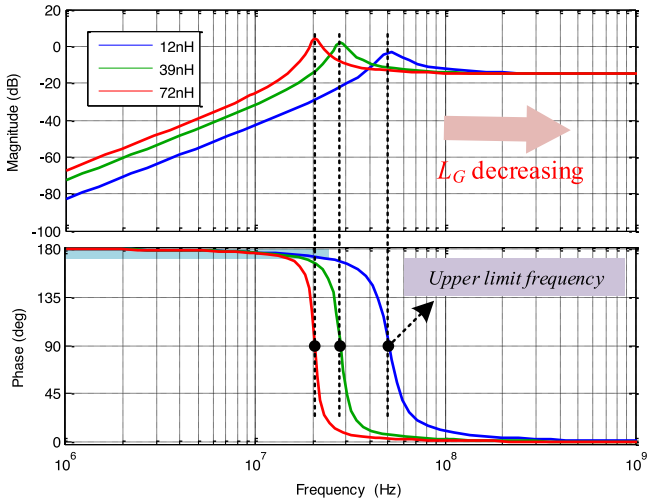

Fig. 2. Bode plots of the voltage transfer function V_{gs}/V_{ds} in basic self-driven circuit.

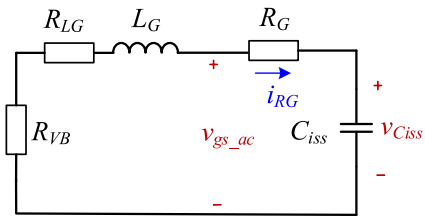

Fig. 3. Equivalent circuit of the basic self-driven network.

The switch gate voltage can be obtained by the sum of dc component v_{gs_dc} and ac component v_{gs_ac}, which is represented by

$$v_{gs}(t) = v_{gs\_\mathrm{dc}} + v_{gs\_\mathrm{ac}}(t) = V_{\mathrm{Bias}} + V_{gs}\sin(2\pi ft) \quad (1)$$

where V_{gs} is the amplitude of the ac component and f is the operating frequency. With voltage V_{Bias} at zero, the relationship between gate voltage and drain–source voltage can be represented as (2). Because of the high quality factor, the parasitic resistances of the inductor and capacitor are neglected

$$\frac{V_{gs}}{V_{ds}} = \frac{s^2 L_G C_{GD}}{s^2 L_G (C_{GS}+C_{GD}) + sR_G(C_{GS}+C_{GD})+1}. \quad (2)$$

Based on (2), Fig. 2 shows the Bode plot of the voltage transfer function V_{gs}/V_{ds} in basic self-driven circuit. It can be seen that when the frequency is lower than the upper limit frequency, the phase of the transfer function is almost 180°. Meanwhile, the gain of the transfer function can be adjusted by changing the value of the series inductor L_G to meet the requirement of selected switch. Thus, the network can satisfy the requirements of a self-driven circuit.

Based on above analysis, the losses of the basic self-driven circuit can be analyzed as follows. Fig. 3 shows the equivalent circuit of the basic self-driven circuit, where R_{LG} is the equivalent series resistor (ESR) of inductor L_G, and C_{iss} represents the input capacitance of the switch, which approximately equal to C_{GS}.

Meanwhile, R_{VB} is the equivalent resistance of the bias voltage source, where an adjustable voltage regulator chip is usually adopted. Thus, R_{VB} can be approximately calculated by the relationship between chip power dissipation P_{VB} and output current amplitude I_{VB}

$$R_{VB} = \frac{P_{VB}}{I_{VB}^2} = \frac{T_J - T_A}{I_{VB}^2 R_{\theta JA}} \quad (3)$$

where T_J is the chip junction temperature, T_A is the ambient temperature, and $R_{\theta JA}$ is the junction-to-ambient thermal resistance. These parameters can be obtained from experimental results and datasheets.

Because the impedance of R_G is quite small compared to that of C_{iss}, the difference between gate voltage and the voltage across the input capacitance v_{Ciss} is ignored. Thus, the voltage of C_{iss} is

$$v_{Ciss}(t) = v_{gs\_ac}(t) = V_{gs}\sin(2\pi ft). \quad (4)$$

The current through R_G is

$$\begin{aligned} i_{RG}(t) &= i_{Ciss}(t) = C_{iss}\frac{dv_{Ciss}(t)}{dt} \\ &= 2\pi f V_{gs} C_{iss}\cos(2\pi ft). \end{aligned} \quad (5)$$

As shown in Fig. 3, the losses of basic self-driven circuit can be divided into three parts, which are represented as P_{RG}, P_{LG}, and P_{VB}, respectively. The losses P_{RG} are caused by the switch gate resistance R_G, which can be calculated as

$$P_{RG} = I_{RG}^2 R_G = 2\pi^2 f^2 V_{gs}^2 C_{iss}^2 R_G. \quad (6)$$

The losses P_{LG} are caused by the inductor equivalent series resistance R_{LG}, which can be calculated as

$$P_{LG} = I_{RG}^2 R_{LG} = 2\pi^2 f^2 V_{gs}^2 C_{iss}^2 R_{LG}. \quad (7)$$

The losses P_{VB} are caused by the equivalent resistance R_{VB}, which can be calculated as

$$P_{VB} = I_{RG}^2 R_{VB} = 2\pi^2 f^2 V_{gs}^2 C_{iss}^2 R_{VB}. \quad (8)$$

The total losses P_{Basic} of basic self-driven circuit can be calculated by the sum of P_{RG}, P_{LG} and P_{VB}

$$\begin{aligned} P_{\mathrm{Basic}} &= P_{RG} + P_{LG} + P_{VB} \\ &= 2\pi^2 f^2 V_{gs}^2 C_{iss}^2 (R_G + R_{LG} + R_{VB}). \end{aligned} \quad (9)$$

Usually, the gate resistance R_G is several ohms, and the equivalent resistance R_{VB} is around tens of ohms. For resonant inductors with high quality factor, the ESR is quite small. Fig. 4 shows the curves of losses P_{RG}, P_{LG}, and P_{VB}, respectively. From the figure, it can be seen that the losses of equivalent resistance R_{VB} occupy most of the driving circuit losses. Thus, it is necessary to reduce the losses of R_{VB} in order to improve the efficiency of driving circuit.

III. Self-Driven Circuit With Parallel Branch

To solve the aforementioned problem, this latter proposes a self-driven circuit with an additional parallel branch to reduce the current flowing through R_{VB}. Fig. 5 shows the self-driven circuit with a parallel branch between the switch gate and source. At the beginning, the magnitude and phase characteristics of

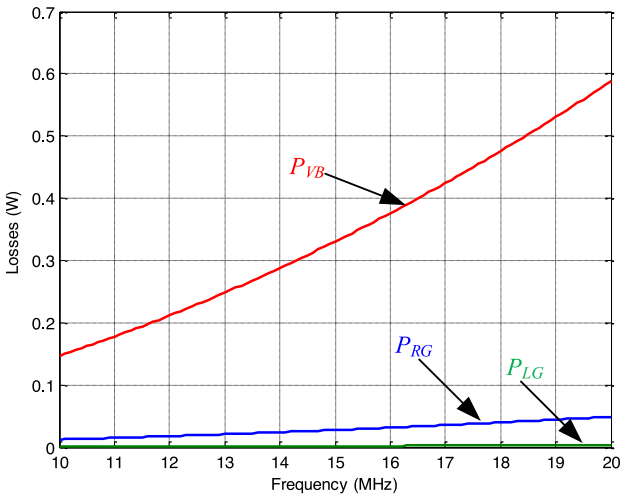

Fig. 4. Curves of losses P_{RG}, P_{LG}, and P_{VB} in basic self-driven circuit.

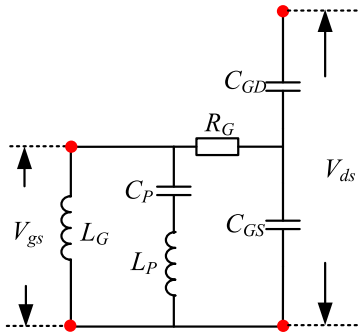

Fig. 5. Proposed circuit with an additional *LC* branch.

the feedback network should be analyzed in order to meet the requirements of a self-driven circuit.

The transfer function of the proposed circuit is shown in (10), and Fig. 6(a) and (b) shows the Bode plots of the voltage transfer function V_{gs}/V_{ds} in proposed self-driven circuit, (10) as shown at the bottom of this page.

FromFig. 6, it can be seen that the bode plot of the voltage transfer function V_{gs}/V_{ds} in proposed self-driven circuit is similar to that of the basic self-driven circuit within a certain range. In the shadow region, the phase of the proposed feedback network is almost 180°, which meets the requirements of a self-driven circuit. Meanwhile, the gain of the transfer function is similar as that of the basic self-driven circuit.

Fig. 7 shows the equivalent circuit of the proposed self-driven network. With a similar method, the losses of R_G can be calculated by (6). The voltage across C_P equal to V_{bias}. Because of the small impedance R_{LP}, the difference between the ac component of the gate voltage and the voltage across the inductor L_P is ignored. Thus, v_{Lp} can be represented as

$$v_{Lp}(t) = v_{gs\_ac}(t) = V_{gs}\sin(2\pi f t). \tag{11}$$

Then, the current flowing through inductor L_P is

$$i_{Lp}(t) = \frac{1}{L_P}\int v_{Lp}(t)\,dt = -\frac{V_{gs}}{2\pi f L_P}\cos(2\pi f t). \tag{12}$$

Thus, the losses in the ESR of L_P can be calculated as

$$P_{R_{LP}} = I_{LP}^2 R_{LP} = \frac{V_{gs}^2}{8\pi^2 f^2 C_{iss}^2} R_{LP}. \tag{13}$$

The current flowing through the inductor L_G and bias voltage source can be obtained as

$$\begin{aligned} i_{LG}(t) &= i_{RG}(t) + i_{LP}(t) \\ &= 2\pi f V_{gs} C_{iss}\cos(2\pi f t) - \frac{V_{gs}}{2\pi f L_P}\cos(2\pi f t). \end{aligned} \tag{14}$$

Thus, the losses in R_{LG} and R_{VB} can be calculated as

$$\begin{aligned} P_{R_{LG}} + P_{R_{VB}} &= I_{LG}^2 (R_{LG}+R_{VB}) \\ &= \left(\sqrt{2}\pi f V_{gs} C_{iss} - \frac{V_{gs}}{2\sqrt{2\pi f L_P}}\right)^2 (R_{LG}+R_{VB}). \end{aligned} \tag{15}$$

Therefore, the total losses P_P of the proposed self-driven circuit can be calculated by the sum of above losses as follows:

$$P_P = P_{RG} + P_{R_{LP}} + P_{R_{LG}} + P_{R_{VB}}. \tag{16}$$

According to aforementioned analysis, the equivalent resistance R_{VB} is quite large compared with other system resistances, such as R_G, R_{LG}, and R_{LP}. Thus, to reduce the total losses P_P, the most effective method is to reduce the current i_{LG}. Fig. 8 shows the losses curves of the basic self-driven circuit and proposed self-driven circuit in different L_P conditions. It can be seen that the value of L_P should not be too small. When L_P is smaller than the critical value, the losses will be higher than that of the basic self-driven circuit. There is an optimal value of L_P that can help to achieve minimum losses. At the optimal point, the losses can be decreased by 94% compared with that of the basic self-driven circuit. The optimal value is usually near the resonant inductor value, which is determined by the operating frequency f and switch input capacitance C_{iss}. In this condition, the current through R_{VB} is quite small. Thus, the losses can be greatly reduced. On the basis of a similar idea, an *LC* branch can also be added between the drain and gate; this is not analyzed in detail here.

$$\frac{V_{gs}}{V_{ds}} = \frac{s^4 L_G C_{GD} L_P C_P + s^2 L_G C_{GD}}{s^4 L_G L_P C_P (C_{GS}+C_{GD}) + s^3 R_G C_P (C_{GS}+C_{GD})(L_G+L_P) + s^2\left[L_G(C_{GS}+C_{GD}) + C_P(L_G+L_P)\right] + sR_G(C_{GS}+C_{GD}) + 1} \tag{10}$$

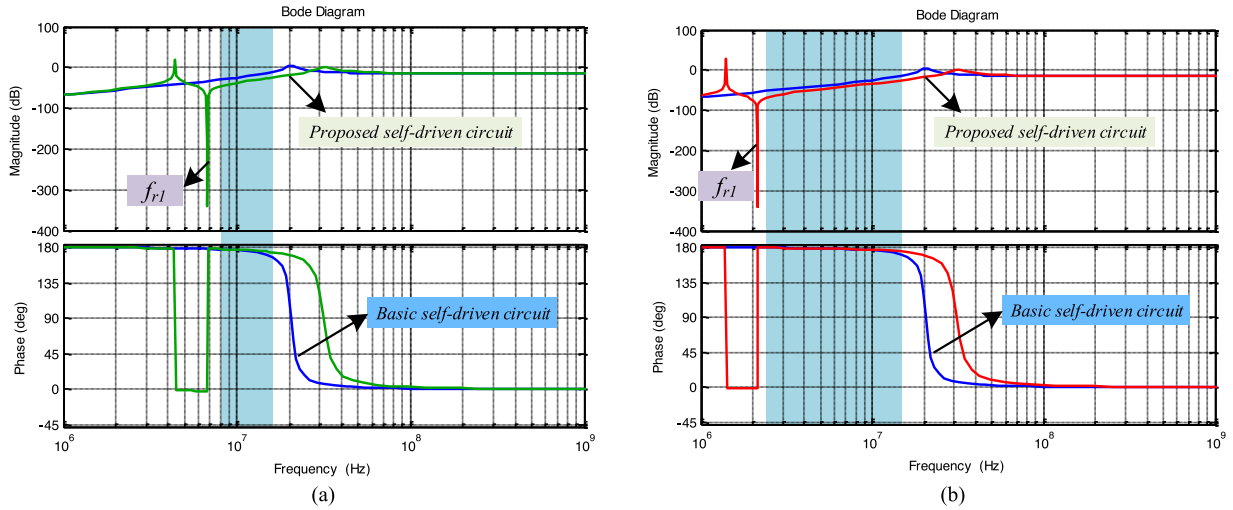

Fig. 6. Bode plot of the voltage transfer function V_{gs}/V_{ds} in proposed self-driven circuit. (a) $L_P = 56$ nH, $C_P = 10$ nF. (b) $L_P = 56$ nH, $C_P = 100$ nF.

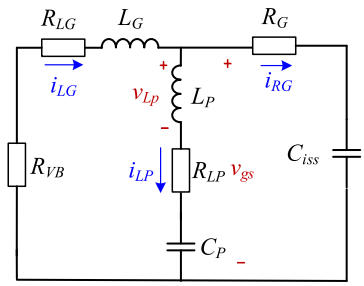

Fig. 7. Equivalent circuit of proposed self-driven network.

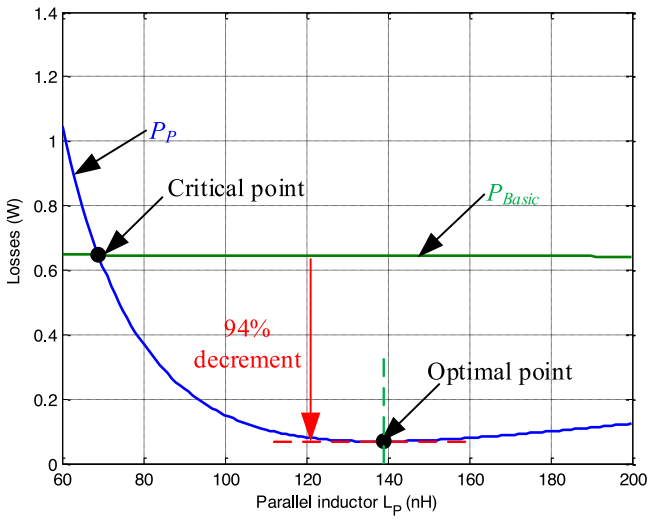

Fig. 8. Comparison between basic self-driven circuit losses and proposed self-driven circuit losses.

IV. System Design and Experimental Results

From the preceding analysis, a 13 MHz high-frequency resonant converter with the proposed self-driven circuit is designed and built in the laboratory. The circuit is shown in Fig. 9. The input voltage is 8 V, the output voltage is 5 V and the output power is 10 W.

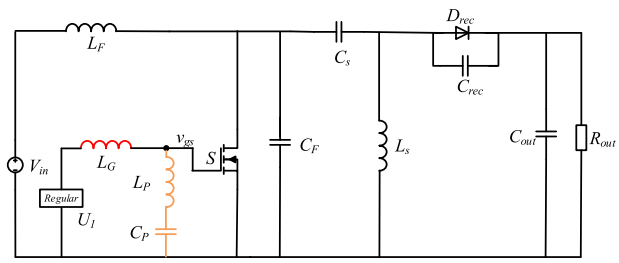

Fig. 9. High frequency converter with proposed self-driven circuit.

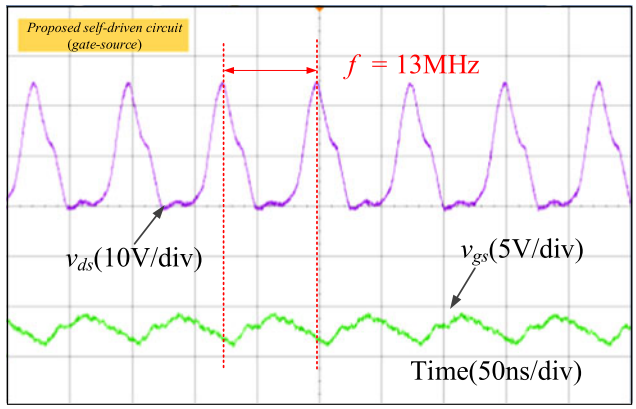

Fig. 10. Switch gate and drain–source voltages of proposed circuit.

Fig. 10 shows the switch gate and drain–source voltage of the proposed self-driven circuit with a branch between the drain and gate. It can be seen that the switch turns on in zero voltage switching (ZVS) condition, which can reduce the switching losses in high frequency conditions. The operating frequency is almost 13 MHz. Here C_P is designed to be 100 nF, and L_P is designed to be 250 nH. It can be seen the waveform of v_{GS} is in approximate sinusoidal form, where the high order harmonics also affect the shape of the driving signal. By resonating between the inductor and the switch input capacitance, the energy stored in the switch capacitance

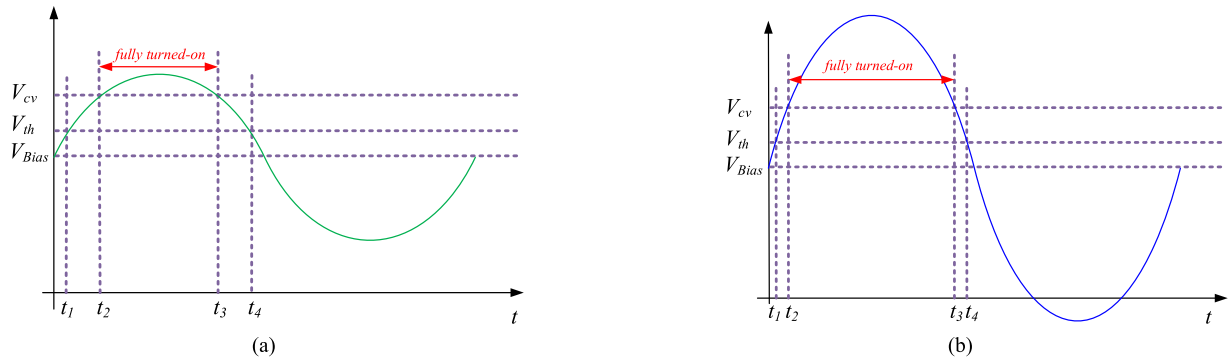

Fig. 11. Diagram of sinusoidal driving voltage waveform in different amplitude conditions. (a) Small amplitude. (b) Large amplitude

can be saved during each switching period. Thus, the driving circuit losses in high frequency conditions can be reduced with the sinusoidal driving signal. However, in this condition, the switch fully turned-ON time is shortened as Fig. 10 shown. Fig. 11(a) and (b) shows the diagram of sinusoidal driving voltage waveform, where $V_{\rm Bias}$ represents the bias voltage, $V_{\rm th}$ represents the switch threshold voltage, and V_{cv} represents the switch critical voltage. The switch can be considered as fully turned-ON when the driving voltage is higher than V_{cv}. From the figure, it can be seen that the fully turned-ON time is short when the driving signal amplitude is small. With the increment of driving signal amplitude, the switch fully turned-ON time is effectively extended.

In the current prototype, the main purpose is to test the feasibility of the proposed self-driven circuit. The input voltage and switch drain–source voltage are not designed to be high, which can guarantee the system currents and voltages within the rated value of switch and diode. Thus, in the prototype, the driving voltage amplitude of the proposed self-driven circuit is not high, which leads to a short fully turned-ON time. In the future work, the system input voltage and driving voltage will be further increased to extend the switch fully turned-ON time.

Besides these self-driven methods, in high frequency conditions, the square-wave driving method and the resonant (sine-wave) driving method based on oscillator, driving chip and parallel inverters are also two typical methods. Fig. 12 shows the efficiency curves of the proposed self-driven circuit, basic self-driven circuit, resonant driving circuit, and square-wave driving circuit. It can be seen that the efficiencies of the basic self-driven circuit and square-wave driving circuit are not very high. The resonant driving circuit can reduce the losses of input capacitance, thus, the system efficiency is improved. However, the oscillator, inverters, and power chip also cause additional losses and increase the system cost and volume. It can be seen that the proposed self-driven circuit owns a higher efficiency than the other driving methods. Meanwhile, the number of corresponding chips can be greatly reduced.

Fig. 13 shows the losses comparison between the square-wave driving circuit and proposed self-driven circuit. It can be seen that the square-wave driving method owns smaller switch losses because of the long fully turned-ON time and small on-resistance. However, the driving circuit losses are quite larger than those of the proposed self-driven circuit. Also, it can be seen that, in high

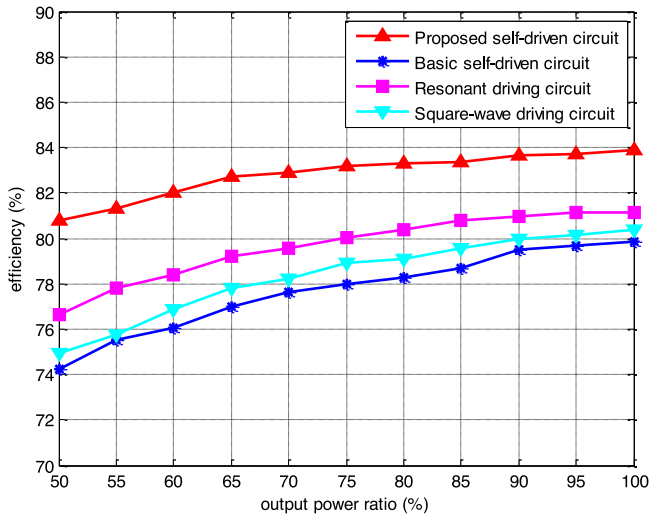

Fig. 12. Converter efficiency curves with different driving methods.

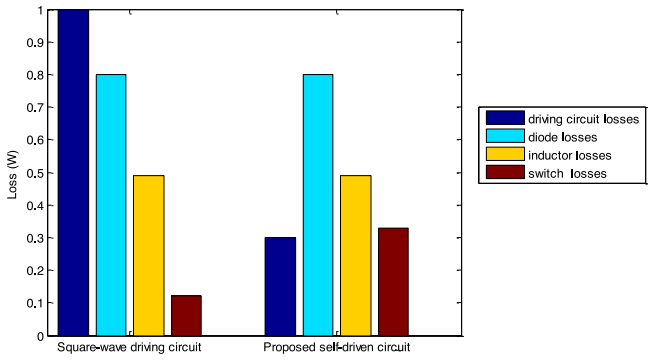

Fig. 13. Losses of high frequency converter with different driving methods.

frequency conditions, the switch conduction losses only take a small part of the total losses. Thus, the proposed self-driven network still can effectively improve the system efficiency.

Also, it can be seen that the diode losses and the inductor losses occupy more than half of the system total losses. Thus, the efficiency improvement is greatly limited. To reduce the inductor losses, inductors with high quality factor need to be adopted. In the prototype, the solenoid air core inductors manufactured by Coilcraft are used. In the future work, the

planar spiral inductors can be adopted, which own higher quality factor and smaller ac resistance in high frequency conditions. Meanwhile, the forward voltage drop of the diode is high, which causes large conduction losses. The synchronous rectification technology may be adopted to reduce the losses of diode in rectifier stage. With the adoption of synchronous rectification, the conduction losses can be reduced. However, it will cause extra driving losses. Thus, deep analysis needs to be conducted to achieve the optimal system efficiency.

V. Conclusion

This letter proposes and investigates a high efficiency self-driven circuit for high frequency converters. The voltage transfer function characteristics of the basic self-driven circuit and proposed self-driven circuits with a parallel branch are described in detail. The losses of the driving circuit are analyzed. To reduce the corresponding losses, a high efficiency self-driven network with an additional parallel branch between the gate and source is proposed. A 13 MHz prototype is built and validates the feasibility of the proposed self-driven method. The system efficiency can be improved from 80% to 83.9% in the rated 10W output power condition.

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