High-Efficiency Current-Fed Dual Active Bridge DC–DC Converter With ZVS Achievement Throughout Full Range of Load Using Optimized Switching Patterns

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***Abstract*—For current-fed dual active bridge bidirectional dc–dc converters, all the possible switching patterns are summarized in view of the combinations of both side pulse-width modulation duty cycles and phase-shift angle. A control strategy is proposed for the current-fed dual active bridge converter to operate with the optimized patterns. The equivalent duty cycle of the secondary side is smaller than that of the primary side by a fixed value, which is optimized based on the soft-switching achievement and the circulating current minimization. The closed-loop control is easy to be implemented since there are only two independent variables, one-side duty cycle and the phase-shift angle. With the proposed control, zero-voltage switching can be achieved for all power switches throughout full range of load even at no-load condition. The typical working modes with the proposed control are given. The optimal design of the system parameters including the fixed time delta and dead time is illustrated. The converter has a very good performance, not only under steady states but also in transients. The conversion efficiency is high. The effectiveness of the proposed control is verified by the experimental results of a 1-kW laboratory prototype.**

***Index Terms*—Battery charging/discharging, bidirectional dc–dc converter, dual active bridge, pulse-width modulation (PWM) control, ZVS.**

I. Introduction

BATTERY charging/discharging is widely used in energy storage systems, electrical vehicles, and microgrids [1]–[3]. The voltage ratings for each battery cell in the energy storage device are very low. Series connection of battery packs reduces reliability [4]. Bidirectional dc–dc converters work as the interface between the battery and the high voltage bus. Although the nonisolated buck/boost converter is simple, its voltage conversion gain is limited, which makes it unsuitable to be used in high voltage conversion gain situations [5]. High-frequency isolated bidirectional dc–dc converters are widely used, since the voltage conversion can be adjusted flexibly by changing the transformer turns ratio.

Dual active bridge (DAB) dc–dc converter is widely used for bidirectional power flow situations. For voltage-fed DAB, many control strategies have been proposed. Single phase shift (SPS) control is very simple [6]–[8], but the circulation loss is comparatively large. To minimize the circulation duration length and loss at heavy load, an adaptive inductor was proposed [9]. To extend the zero-voltage switching (ZVS) range and minimize losses, single H-bridge (HB) pulse-width modulation (PWM) plus phase-shift control is useful [10]–[14]. To improve the conversion efficiency at light-load conditions, Burst mode can be implemented by varying the switching frequency; therefore, losses are minimized in all the elements of the converter to mitigate the conduction, switching, and magnetic power dissipation [14]. The circulation loss can be reduced further by active methods. Both the two-side HBs can be modulated with the same duty ratio, while the power is regulated by the phase shift between them [15]. A current-stress-optimized switching strategy can reduce the current stress [16].

A dual PWM control strategy with independent duty ratios for each HB was presented [17], thus the current stress can be optimized further. All the possible combinations of the two duty cycles and phase-shift angles have been studied extensively [18], [19]. Among all the combinations, an optimal control strategy to obtain the minimum inductor root-mean-square (RMS) current was introduced, where independent duty cycles and phase shift between the two HBs can be calculated in the most optimized way.

Although ZVS can be achieved in a wide load range by employing a hybrid control [20], it is very difficult for the voltage-fed DAB to achieve ZVS at no-load condition. To improve the conversion efficiency especially at light load, varying switching frequency control is used according to different power levels [21]. To widen the conversion ratio range, a center-tapped transformer was used on one side [22]. Current stress optimized

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scheme using unified triple phase shift is useful to reduce the circulation loss and achieve instantaneous closed-loop control [23], [24]. Actually, the optimal duty-cycle expressions are more complicated, and a very fast speed controller is needed to handle the real-time computation. To simplify the controller, the two-side duty cycles can be determined by the phase-shift angle and the two-side dc voltages. A unified boundary trapezoidal control utilizing the fixed duty-cycle compensation is proposed [25], the duty-cycle compensation is fixed despite the load. However, the bias current induced by the fixed compensation is helpful for some switches to achieve ZVS, but for other switches, ZVS is more difficult to achieve. Thus, magnetizing current is used in order to counteract the bias current resulting from the duty-cycle compensation. This brings more nonactive current and reduction of the conversion efficiency.

However, there are three independent variables, including the two duty cycles and one phase-shift angle. A linear interpolation can be used to determine the selection of the three variables based on data stored in the digital signal processor (DSP) memory to achieve the closed-loop control, so the system dynamic response is poor. Besides, if the transformer two-side voltages are not matched well, the current stress during the power transfer stage is high. This is a disadvantage of the voltage-fed DAB. Actually, during the charging or discharging process, the voltage range of the battery is very wide. Besides, the current ripple of the voltage-fed DAB port is comparatively higher and the battery lifetime may be affected [26]. The aforementioned attributes of the voltage-fed DAB make it unsuitable to be used in charging/discharging a battery whose voltage variation range is wide. Besides, the high current ripple makes the voltage-fed DAB to not be used directly for battery interface. Therefore, an inductor can be used between the battery and voltage-fed DAB to reduce the battery charging/discharging current ripple [27].

In contrast, current-fed DAB is a good option for battery charging/discharging situations. A novel current-fed DAB, characterized by reducing one-side current ripple dramatically, was introduced for battery application in [28]. The current ripple reduction makes it very attractive for battery charging/discharging. When the conversion ratio varies, the conduction loss during the power transfer stage is not minimized. To adapt to the wide voltage conversion ratio situations, a PWM plus phase-shift control was proposed, in which the battery side is PWM modulated, while duty cycles for the high-voltage side (HVS) switches are fixed at 50%. Since the active clamp voltage can be regulated based on the HVS voltage value and the turns ratio, the current stress during the power transfer stage can be suppressed, as the voltage conversion ratio varies widely by employing the PWM control [29]–[32]. Although minimum conduction loss during the power transfer stage can be obtained, for the nonpower transfer stage, especially when the battery voltage is rather low, the current spike and circulation loss may be high, causing conversion efficiency reduction and reliability issues. Of course, the current stress can be suppressed by adding an additional inductor in series, connected with the transformer to increase the equivalent leakage inductance value, but the maximum transferred power capability is limited due to the large inductance value.

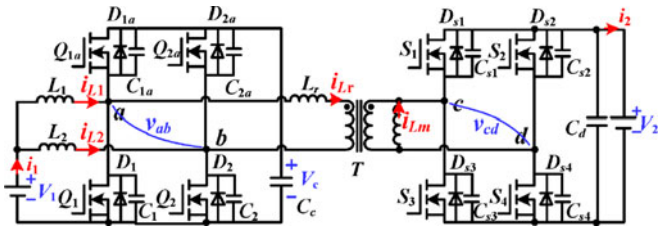

Fig. 1. Circuit of the current-fed bidirectional dc–dc converter.

Besides, the circulation stage length increases and results in low conversion efficiency. PWM control can be also employed for HVS switches to reduce the circulation loss [33]–[36]. To ensure the ZVS for HVS switches, unequal duty cycles for both side switches is a very good option with unmatched voltage control [33]. But the current stress is relatively high due to the unmatched voltage control. For voltage-matched control, although identical duty-cycle control can achieve ZVS for all the power switches in current-fed semi-DAB converter employing diodes [34], ZVS cannot be ensured for all the switches in current-fed DAB [35]. The duty-cycle relationship for both sides has to vary according to the specific working conditions. This complicates the control system design [36].

In this paper, for current-fed DAB, all the possible switching patterns have been illustrated and analyzed with voltage-matching control. Based on the analysis, optimized switching patterns are proposed. In which, the difference between the two-side duty cycles is fixed in spite of working conditions. Thus, the closed-loop control is very simple and can be implemented easily. Besides, ZVS can be achieved for all power switches even at no-load condition with reduced circulating current. This paper is organized as follows. Operation principle and working modes of the proposed control strategy is given in Section II. Section III illustrates the soft-switching condition and the parameter design criterion. In Section IV, experiments are made to verify the effectiveness of the proposed control. Section V gives the conclusion.

II. Operation Principle of the Proposed Control

A. Topology of the Current-Fed DAB and the Operating Modes With Voltage-Matching Control

Fig. 1 illustrates the power circuit of the current-fed DAB. In the low-voltage side (LVS), there are two interleaved buck/boost circuits in parallel connection. L_1 and L_2 are dc inductors with the same inductance, and C_c is the clamp capacitor. The duty cycle D_p of the bottom switches makes the clamp voltage V_c to be matched with the secondary-side voltage V_2, which means the slew rate of the leakage inductance current during the main power transfer stage maintains zero in spite of the V_1 variation. The primary-side voltage of the transformer is a three-level waveform, employing the PWM control. The ac inductor L_r represents the sum of the external inductance and the high-frequency transformer leakage inductance. In the HVS, L_m is the secondary-side magnetizing inductance. An inner phase shift

is employed in the full bridge, and the secondary-side voltage of the transformer also becomes a three-level waveform. So an equivalent duty cycle D_s can be defined similarly as the primary duty cycle D_p. The output power P varies as the phase-shift angle φ_E between the primary side and secondary side varies. The power flow is bidirectional. The boost mode is defined as the power flowing from LVS to HVS, while the reversed power flow is referred to as the buck mode.

For the current-fed DAB, there are totally 12 patterns when the primary- and secondary-side voltage waveforms are both three-level waveforms with voltage-matching control. However, not all of them are practical operation modes. The six practical patterns shown in Fig. 2 are divided into two groups according to the relationship between two-side duty cycles. Modes IA–VIA are the switching patterns when $D_p > D_s$, while Modes IB–VIB occur when $D_p < D_s$. In Fig. 2, v_{ab} is the voltage of the primary side, v_{cd} is the voltage of the secondary side, and i_{Lr} is the leakage inductance current. Modes I–III occur in the boost mode at light load, medium load, and heavy load, respectively, while Modes IV–VI occur in the buck mode at the aforementioned three kinds of loads, respectively.

However, ZVS for secondary-side switches cannot be achieved in half of the above modes. To achieve ZVS, there should be a reversed current to discharge the parasitic junction capacitor before the switch turns ON. The ZVS condition is described as $i_{Lr}(\theta_a) > 0$ and $i_{Lr}(\theta_b) > 0$, when the magnetizing current and parasitic junction output capacitance are neglected. As seen in Fig. 2, the conditions of $i_{Lr}(\theta_a) > 0$ and $i_{Lr}(\theta_b) > 0$ can be ensured for all the A modes. That means for $D_p > D_s$, ZVS can be achieved even at light load theoretically. However, when $D_p < D_s$, ZVS cannot be achieved at light load or medium load, because the value of I_b is negative. Even at heavy load, ZVS cannot be ensured, since I_y might be negative in some cases. As a result, it is better to let $D_p > D_s$ for the ZVS achievement.

The six unpractical patterns Modes VII–XII are listed in Fig. 3, and the leakage inductance current i_{Lr} during circulation stages is shown in shadow. As can be seen, the circulating current is high in these modes but the transferred power is limited. In addition, for most of the DAB converters, the range of φ_E is limited within $[-\pi/2, \pi/2]$ to ensure that the output power P increases as φ_E is increased. However, the output power P is constant in Modes VII and VIII regardless of the phase-shift angle variation, and thus the power is out of control. In Modes IX–XII, the output power P decreases as φ_E is increased, making the transferred power curve nonmonotonic. Hence, these patterns should be avoided in practice. Normally, φ_E is selected within the range of $[-\pi/2, \pi/2]$ so that power is a monotonously increasing function of the phase-shift angle.

To sum up, for Modes VII–XII, the transferred power does not increases as φ_E is increased, and the circulating current is high. For Modes IB–VIB, the ZVS is lost for HVS switches. Modes IA–VIA are the optimized patterns in which ZVS can be achieved for all switches with low circulation loss. In this paper, a novel control strategy is proposed to make the converter work in these optimized patterns.

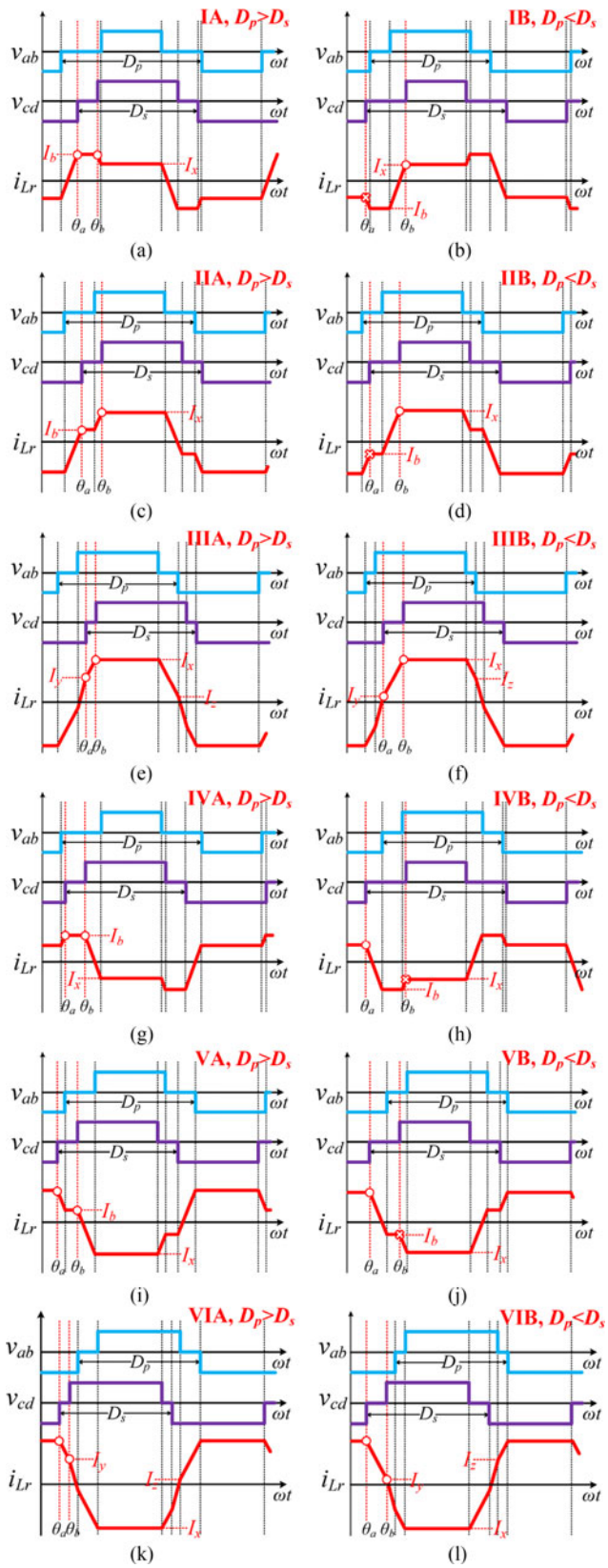

Fig. 2. Six practical patterns for the current-fed DAB with voltage-matching control: (a) Mode IA, (b) Mode IB, (c) Mode IIA, (d) Mode IIB, (e) Mode IIIA, (f) Mode IIIB, (g) Mode IVA, (h) Mode IVB, (i) Mode VA, (j) Mode VB, (k) Mode VIA, (l) Mode VIB.

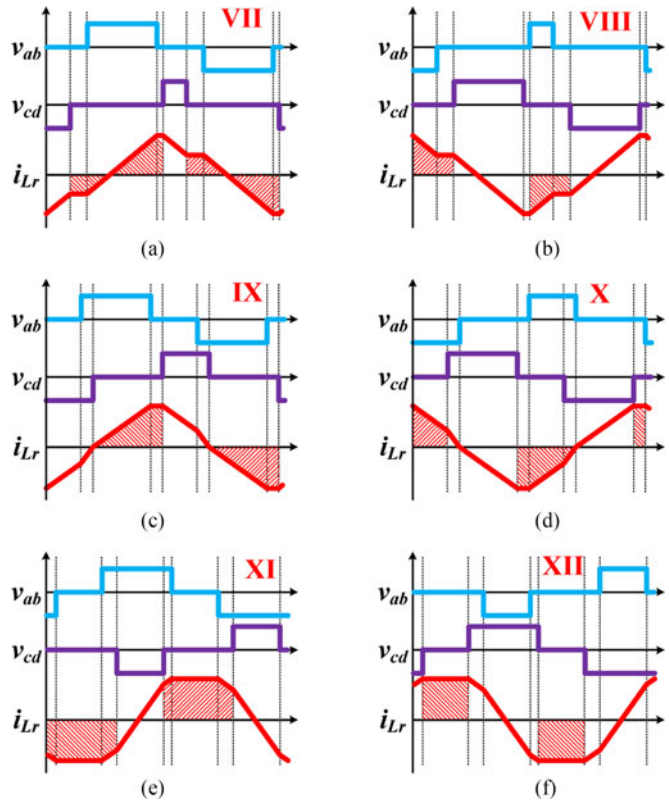

Fig. 3. Six unpractical patterns for the current-fed DAB with voltage-matching control: (a) Mode VII, (b) Mode VIII, (c) Mode IX, (d) Mode X, (e) Mode XI, (f) Mode XII.

TABLE I
SWITCHING CURRENTS IN EACH MODE

$I_b = \frac{V_c T \Delta\varphi}{4\pi L_r}$	$I_x = \frac{V_c T \varphi_E}{2\pi L_r}$
$I_y = \frac{V_c T}{2\pi L_r}(\lvert\varphi_E\rvert - \xi_s)$	$I_z = \frac{V_c T}{2\pi L_r}(\lvert\varphi_E\rvert - \xi_p)$

B. Power Expressions of the Proposed Control

In this paper, a PWM plus dual phase shift with fixed duty-cycle delta control is developed to make the converter operating in optimized patterns. The difference between duty cycles of the two ports are fixed at any conditions, which is defined as the fixed delta in this paper. The closed-loop design is simple to be implemented because the HVS equivalent duty cycle is determined by that of the LVS. The fixed delta $\Delta D = D_p - D_s$ is chosen to be a positive constant, so that ZVS of all the switches in the HVS can be obtained in a wide load range. With the proposed control, the converter works in Modes IA–VIA; the modes in which ZVS is lost and some unpractical ones are avoided.

The expressions of the switching currents marked in Fig. 2 are listed in Table I. Applying these switching currents, the power expression of each mode can be obtained as shown in Table II, where φ_E is the phase-shift angle, $\Delta\varphi = 2\pi\Delta D$ is the fixed delta, and ξ_p and ξ_s are the freewheeling intervals of v_{ab} and v_{cd}, respectively, which are denoted in Fig. 5. The three-

TABLE II
POWER EXPRESSIONS IN EACH MODE

Description	Power expression
Mode VIA Buck Heavy load	$\frac{V_c{}^2 T}{4\pi^2 L_r}[2\pi\varphi_E + 2\varphi_E{}^2 + 2\pi^2(D_p{}^2 + D_s{}^2 - D_p - D_s) + \pi^2]$
Mode VA Buck Medium load	$\frac{V_c{}^2 T}{4\pi^2 L_r}[\varphi_E{}^2 + 2\pi(2 - D_p - D_s)\varphi_E + \pi^2(D_p - D_s)^2]$
Mode IA, IVA Buck/Boost Light load	$\frac{V_c{}^2 T}{4\pi^2 L_r}[4\pi\varphi_E(1 - D_p)]$
Mode IIA Boost Medium load	$\frac{V_c{}^2 T}{4\pi^2 L_r}[-\varphi_E{}^2 + 2\pi(2 - D_p - D_s)\varphi_E - \pi^2(D_p - D_s)^2]$
Mode IIIA Boost Heavy load	$\frac{V_c{}^2 T}{4\pi^2 L_r}[2\pi\varphi_E - 2\varphi_E{}^2 - 2\pi^2(D_p{}^2 + D_s{}^2 - D_p - D_s) - \pi^2]$

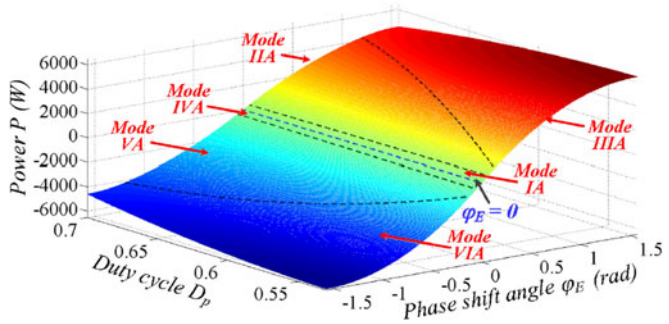

Fig. 4. P curve versus D_p and φ_E, when $\Delta\varphi = 0.1256$.

dimensional (3-D) power curve has been plotted according to the power expressions in Table II. Fig. 4 illustrates output power curve versus primary-side duty cycle D_p and phase-shift angle φ_E with the proposed control.

As seen, the converter with the proposed control can work in the expected Modes IA–VIA in a wide battery voltage range (18–28V, corresponding duty-cycle range is 0.7–0.53). The output power increases monotonously as the phase-shift angle increases in the range of $-\pi/2 - \pi/2$. As shown in Fig. 4, Mode IIIA may happen more often at lighter load conditions at higher battery voltage than lower ones. Besides, the maximum output power is higher as well, because of shorter freewheeling intervals.

C. Working Principle of the Proposed Switching Pattern

The proposed control shows better performance especially at light-load and medium-load conditions. Mode IIA can be chosen as an example to illustrate the working principle of the converter with the proposed control at medium load in the boost mode. Detailed waveforms and mode analysis of Mode IIA are given to show the operation principle. Fig. 5 gives detailed steady-state

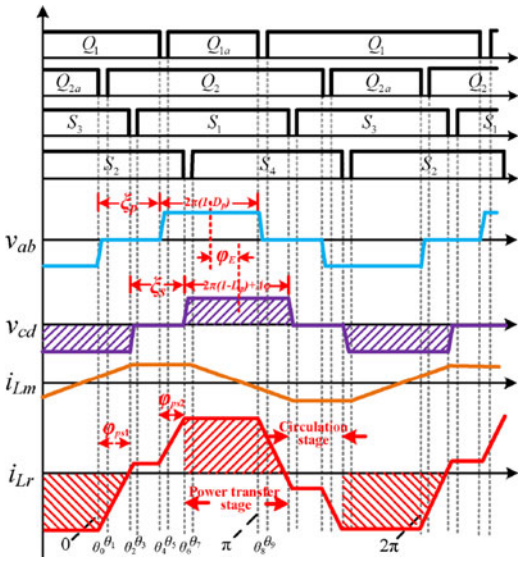

Fig. 5. Steady-state waveforms of the proposed control in Mode IIA.

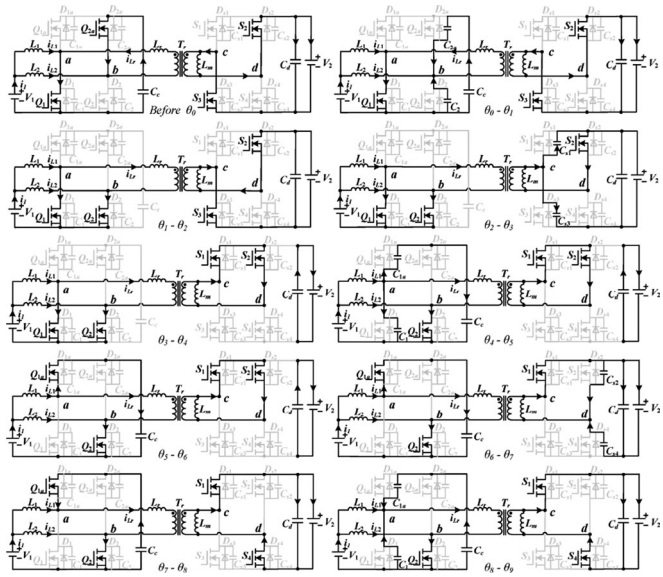

Fig. 6. Working modes for half period in Mode IIA.

waveforms of the proposed control working at Mode IIA. There are nine working stages in a half switching period according to the state of switches. In addition to the waveforms of v_{ab}, v_{cd}, and i_{Lr}, the waveform of magnetizing current i_{Lm} is also shown. Besides, φ_E is the phase-shift angle, ξ_p and ξ_s are the freewheeling intervals, φ_{ps1} and φ_{ps2} are the phase shift between $\theta_0 - \theta_2$ and $\theta_4 - \theta_6$, respectively. The fixed delta $\Delta\varphi$ is the difference between φ_{ps1} and φ_{ps2}.

Among all the working stages, the stages that power is transferred to the high-voltage dc bus are defined as power transfer stages. They have been shown in shadow in Fig. 5. Other stages can be referred to as circulation stages.

The detailed mode analysis is described as follows:

Stage 1 (Before θ_0): Q_1, Q_{2a}, S_2, and S_3 conduct. During this stage, the power flows from LVS to HVS.

Stage 2 ($\theta_0 - \theta_1$): At θ_0, Q_{2a} turns OFF. The sum of i_{L2} and i_{Lr} charges C_{2a} and discharges C_2 until the body diode of Q_2 begins to conduct. Then Q_2 turns ON under ZVS.

Stage 3 ($\theta_1 - \theta_2$): At θ_1, Q_2 turns ON under ZVS.

Stage 4 ($\theta_2 - \theta_3$): At θ_2, S_3 turns OFF after the current i_{Lr} flows in the opposite direction. C_{s3} is charged and C_{s1} is discharged until the body diode of S_1 begins to conduct.

Stage 5 ($\theta_3 - \theta_4$): At θ_3, S_1 turns ON under ZVS.

Stage 6 ($\theta_4 - \theta_5$): At θ_4, Q_1 turns OFF. The difference of i_{L1} and i_{Lr} charges C_{1a} and discharges C_1 until the body diode of Q_{1a} begins to conduct.

Stage 7 ($\theta_5 - \theta_6$): At θ_5, Q_{1a} turns ON under ZVS.

Stage 8 ($\theta_6 - \theta_7$): At θ_6, S_2 turns OFF. Then, the current i_s charges C_{s2} and discharges C_{s4}, causing the body diode of S_4 conduct finally.

Stage 9 ($\theta_7 - \theta_8$): At θ_7, S_4 turns ON under ZVS. The current i_{Q1a} flows from source to drain at first, but flows from drain to source after $i_{L1} = i_{Lr}$. During this stage, the power flows from LVS to HVS.

Stage 10 ($\theta_8 - \theta_9$): At t_8, Q_{1a} turns OFF. The second half cycle similar to the first half cycle. The difference between the current i_{Lr} and i_{L1} charges and discharges junction capacitors of Q_{1a} and Q_1 until the body diode of Q_1 begins to conduct.

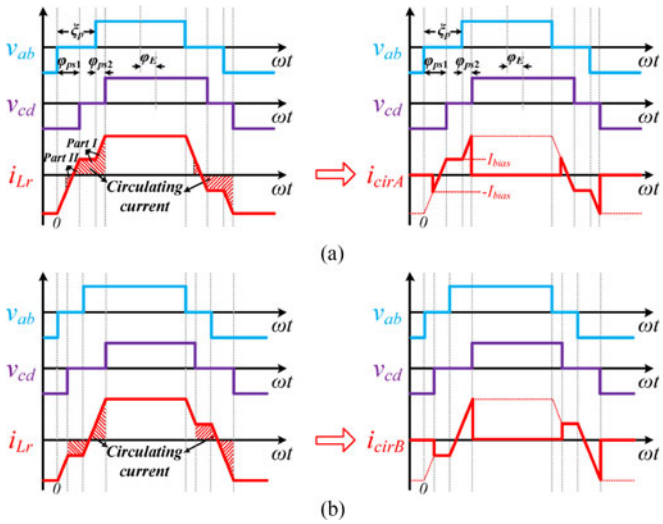

Fig. 7. Discussion of the circulating current: (a) Nonpower transfer stages and circulating current in Mode IIA, (b) nonpower transfer stages and circulating current in Mode IIB.

D. Discussion of the Circulating Current

The fixed delta value needs to be designed with a trade-off in view of the ZVS achievement and circulation loss reduction. On one hand, the fixed delta should be designed with a large value to discharge the output capacitor of the MOSFETs in the HVS. On the other hand, the large fixed delta causes higher circulation loss. The circulating current is defined as the i_{Lr} in the nonpower transfer stages, as shown in Fig. 7. The circulating current includes two parts in Mode IIA. One is the leakage inductance current during the freewheeling intervals; another is the nonactive power stage when power transfers. There is no active power transfer in both these two stages.

The resonant process during the dead time interval is neglected to simplify the analysis. According to the definition, the circulating current in Mode IIA can be described as

$$i_{\mathrm{cir}A} = \begin{cases} i_{Lr}, & \varphi_E - \dfrac{1}{2}\Delta\varphi + k\pi < \theta < \varphi_E - \dfrac{1}{2}\Delta\varphi + \xi_p + k\pi \\ 0, & \text{others} \end{cases} \tag{1}$$

where k can be any arbitrary .The circulating current $i_{\mathrm{cir}A}$ in a half switching cycle can be expressed as follows:

$$i_{cirA}(\theta) = \begin{cases} 0, & 0 < \theta < \varphi_E - \dfrac{1}{2}\Delta\varphi \\ \dfrac{V_c T}{2\pi L_r}(\theta - \varphi_E), & \varphi_E - \dfrac{1}{2}\Delta\varphi < \theta < \varphi_E + \dfrac{1}{2}\Delta\varphi \\ \dfrac{V_c T}{2\pi L_r}\dfrac{1}{2}\Delta\varphi, & \varphi_E + \dfrac{1}{2}\Delta\varphi < \theta < \xi_p \\ \dfrac{V_c T}{2\pi L_r}\left(\dfrac{1}{2}\Delta\varphi + \theta - \xi_p\right), & \xi_p < \theta < \varphi_E - \dfrac{1}{2}\Delta\varphi + \xi_p \\ 0, & \varphi_E - \dfrac{1}{2}\Delta\varphi + \xi_p < \theta < \pi \end{cases} \tag{2}$$

Then its RMS value is written by

$$I_{cirA\_\mathrm{RMS}} = \sqrt{\frac{1}{2\pi}\int_0^{2\pi} {i_{cirA}}^2 d\theta} = \frac{V_c T}{4\pi L_r}\sqrt{\frac{-3\varphi_E\Delta\varphi^2 - \Delta\varphi^3 + 4{\varphi_E}^3 + 3\Delta\varphi^2\xi_p}{3\pi}} \tag{3}$$

Likewise, the circulating current and RMS value in Mode IIB can be written by, respectively

$$i_{\mathrm{cir}B} = \begin{cases} i_{Lr}, \varphi_E + \dfrac{1}{2}\Delta\varphi + k\pi < \theta < \varphi_E - \dfrac{1}{2}\Delta\varphi + \xi_p + k\pi \\ 0, \quad \text{others} \end{cases} \tag{4}$$

$$I_{\mathrm{cir}B\_\mathrm{RMS}} = \sqrt{\frac{1}{2\pi}\int_0^{2\pi} {i_{\mathrm{cir}B}}^2 d\theta} = \frac{V_c T}{4\pi L_r}\sqrt{\frac{-3\varphi_E\Delta\varphi^2 - 2\Delta\varphi^3 + 4{\varphi_E}^3 + 3\Delta\varphi^2\xi_p}{3\pi}}. \tag{5}$$

Fig. 8 plots the RMS value of circulating current curve versus the LVS voltage V_1 and delta $\Delta\varphi$. The circulation loss is high at low LVS voltage because of the large freewheeling intervals. As seen, when $\Delta\varphi$ is too large or too small, the circulating current is high. The circulation loss becomes minimum when $\Delta\varphi = 0$, in spite of the LVS voltage. However, there should be a positive $\Delta\varphi$ to ensure ZVS for HVS switches. Therefore, the fixed delta should be designed as small as possible, as long as ZVS can be obtained. Besides, a large fixed delta results in a large difference

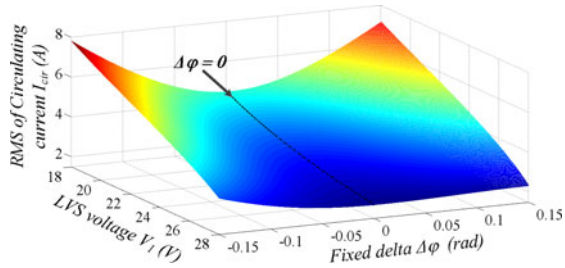

Fig. 8. Circulating current with respect to V_1 and $\Delta\varphi$.

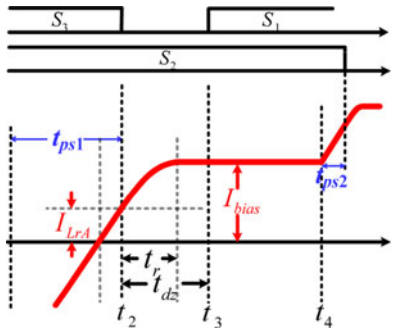

Fig. 9. Expanded waveforms of the resonant process in the boost mode.

between the primary-side duty cycle D_p and the secondary-side equivalent duty cycle D_s. Since D_s must be larger than 50%, the range of the LVS voltage will be limited. A small fixed delta also lead to a wide voltage range for the converter.

III. Soft-Switching Condition

ZVS can be achieved for all switches within whole load range with the proposed control. For the battery side, the output capacitances of the switches are charged/discharged by the difference between the dc inductance current i_L and the leakage inductance current i_{Lr}. ZVS can be achieved easily as long as the dc inductance value is selected properly [34].

The key is to achieve ZVS for HVS switches. Just like most of the DAB converters, soft-switching can be achieved easily at heavy load, but it is difficult to ensure ZVS at light load. With the proposed control, a bias current generated by the given fixed delta ΔT helps to charge/discharge the junction capacitors of HVS switches, and ZVS can be obtained even at no load. The resonant process and how to design the fixed delta to ensure ZVS are discussed in detail in this section.

A. Resonant Process Analysis

At medium-load or light-load conditions, the bias current helps to charge/discharge the output capacitances of the HVS switches. This resonant process is analyzed in detail.

Take the boost mode operation at medium load as an example, the resonant process curve is zoomed-in and plotted in Fig. 9. The working modes have already been shown in $\theta_1 - \theta_3$ in Fig. 6. It is assumed that the leading leg switch S_3 turns OFF at t_2, when the leakage inductance current $i_{Lr} = I_{LrA}$. The resonance begins at t_2, the magnetizing current i_{Lm} and

i_{Lr} are reflected to HVS charges C_{s3} and discharges C_{s1} until the leakage inductance current slew rate decays to zero. If the dead time is chosen large enough, S_1 turns ON under ZVS. In fact, i_{Lr} itself can be designed large enough to discharge the parasitic output capacitance, and the magnetizing current i_{Lm} is not necessary for the ZVS implementation. Therefore, the magnetizing inductance can be designed freely to derive an optimal transformer design with the lowest total losses, making the transformer design easier.

This resonant process can be described by differential equations. The moment when S_3 turns OFF can be defined as $t = 0$. The magnetizing current i_{Lm} can be viewed constant and equal to the maximum value $i_{Lm\max}$ in this resonant process. The value of leakage inductance current when the resonant process is completed is denoted as the bias current $I_{\rm bias}$, and the resonance ends at time t_r. The relationship between i_{Lr} and the drain-to-source voltage v_{ds1} of the switch S_1 can be written by

$$i_{Lm\,\max} + \frac{N_1}{N_2} i_{Lr} = -2C_{\rm oss.eff}\frac{dv_{ds1}}{dt} \tag{6}$$

$$\frac{N_1 v_{ds1}}{N_2} = L_r \frac{di_{Lr}}{dt} \tag{7}$$

where $C_{\rm oss.eff}$ is the charge-equivalent parasitic output capacitance of the MOSFETs under the condition that $v_{\rm ds}$ = 0–300 V. $i_{Lm\max}$ is the peak value of the magnetizing current which can be written by $i_{Lm\max} = V_2(1-D_p)T/2L_m$. The initial conditions for the differential equations are $v_{ds1}(0) = V_2$ and $i_{Lr}(0) = I_{LrA}$.

The angle frequency of the resonant process can be expressed by

$$\omega_1 = \frac{N_1}{N_2}\sqrt{\frac{1}{2C_{\rm oss.eff}L_r}}. \tag{8}$$

Then, expressions of the resonant current and voltage can be written by, respectively

$$\begin{cases} i_{Lr}(t) = \sqrt{\left(\dfrac{N_2}{N_1} i_{Lm\,\max} + i_{LrA}\right)^2 + \dfrac{2C_{\rm oss.eff}{V_2}^2}{L_r}} \\ \qquad \times \sin\left(\omega_1 t + \arctan\left(\left(\dfrac{N_2}{N_1} i_{Lm\,\max} + i_{LrA}\right)\right.\right. \\ \qquad \left.\left. \times \sqrt{\dfrac{L_r}{2C_{\rm oss.eff}{V_2}^2}}\right)\right) - \dfrac{N_2}{N_1} i_{Lm\,\max} \\ v_{ds1}(t) = \sqrt{{V_2}^2 + \left(\dfrac{N_2}{N_1} i_{Lm\,\max} + i_{LrA}\right)^2 \dfrac{L_r}{2C_{\rm oss.eff}}} \\ \qquad \times \sin\left(\omega_1 t - \arctan\left(\dfrac{N_1 V_2}{N_2 i_{Lm\,\max} + N_1 i_{LrA}}\right.\right. \\ \qquad \left.\left. \times \sqrt{\dfrac{2C_{\rm oss.eff}}{L_r}}\right)\right). \end{cases} \tag{9}$$

When $v_{\rm ds1}(t) = 0$, the resonant process is completed. The resonant time-duration length t_r and the bias current $I_{\rm bias}$ can be obtained from (9), and they are expressed as, respectively

$$\begin{cases} t_r = \dfrac{\arctan\left(\frac{N_1 V_2}{N_2 i_{Lm\,\max} + N_1 I_{LrA}}\sqrt{\frac{2C_{\rm oss.eff}}{L_r}}\right)}{\omega_1} \\ I_{\rm bias} = \sqrt{\left(\frac{N_2}{N_1} i_{Lm\,\max} + I_{LrA}\right)^2 + \frac{2C_{\rm oss.eff}{V_2}^2}{L_r}} - \frac{N_2}{N_1} i_{Lm\,\max}. \end{cases} \tag{10}$$

As seen, both t_r and the $I_{\rm bias}$ are affected with the initial current I_{LrA}, which is determined by the fixed delta and operation mode. The bias current $I_{\rm bias}$ increases as I_{LrA} is increased, while t_r decreases with the increase in I_{LrA}.

The resonant processes in other cases are similar to this, since the equivalent resonant circuits are identical. In the buck mode, the resonant process begins at $i_{Lr} = I_{\rm bias}$ and ends at $i_{Lr} = I_{LrA}$, thus the results shown in (10) are also suitable for the buck mode.

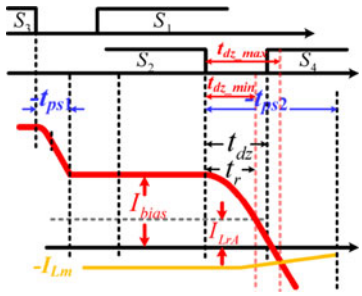

Fig. 10. Expanded waveform of the resonant process in the buck mode.

B. Soft Switching Condition

To achieve soft switching, the given fixed delta ΔT should be large enough to ensure $I_{LrA} \geq 0$. Then, if the dead time is selected properly, the HVS switches can be turned ON with ZVS. However, the relationships between ΔT and I_{LrA} are not same in different operation modes. In this section, the resonant processes of the primary side are neglected because of the low drain-to-source voltages and the large switching currents.

As aforementioned, the fixed delta ΔT is the difference between t_{ps1} and t_{ps2}. According to Fig. 9, if the resonance in t_{ps1} is neglected, the fixed time delta ΔT in the boost mode can be expressed as

$$\Delta T = t_{ps1} - t_{ps2} = L_r \frac{I_{\rm bias} + I_{LrA}}{V_c}. \tag{11}$$

The detailed resonant procedure in the buck mode is illustrated in Fig. 10. It is worth noting that, t_{ps1} and t_{ps2} are negative here. As can be seen, both t_{ps1} and t_{ps2} include resonant process, which are different from those of the boost mode. When the resonance in t_{ps1} is neglected, the fixed time delta ΔT can be written by

$$\Delta T = t_{ps1} - t_{ps2} = L_r \frac{I_{\rm bias} + I_{LrA}}{V_c} + t_r. \tag{12}$$

As seen in (11) and (12), when the fixed time delta ΔT is identical, the bias current in the buck mode is less than that

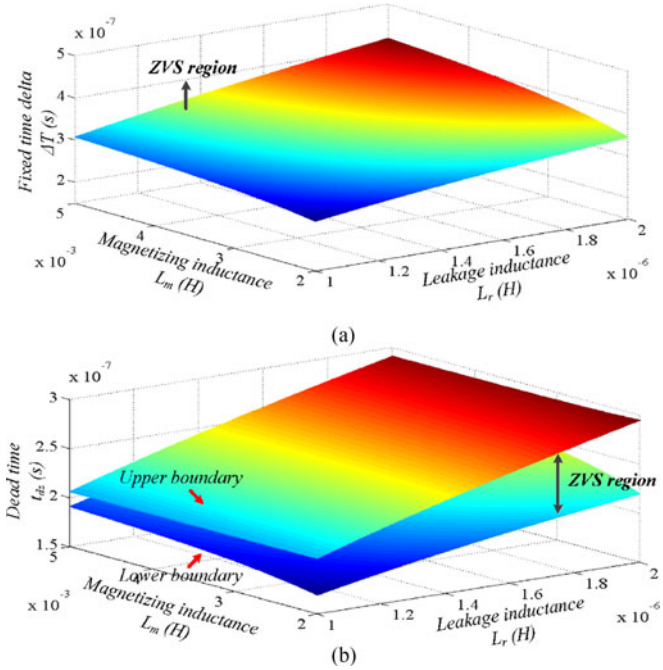

Fig. 11. ZVS condition for HVS. (a) Fixed time delta ΔT, (b) dead time t_{dz}.

in the boost mode. In other words, once the ZVS condition is ensured for the buck mode, the ZVS condition for the boost mode can be achieved absolutely. So the fixed delta ΔT should be designed large enough to ensure $I_{LrA} \geq 0$ in (12).

The dead time also should be selected properly to ensure ZVS. As shown in Fig. 10, the dead time t_{dz} should be large enough to make the switch turn-on after the resonant process is completed. On the other hand, t_{dz} should be less than a value to avoid the charging of HVS switch junction capacitors in the reverse direction. In summary, to achieve ZVS in spite of the working modes, the fixed time delta ΔT and the dead time t_{dz} for HVS can be designed as follows:

$$\begin{cases} \Delta T \geq L_r \dfrac{I_{\text{bias}}}{V_c} + t_r \\ t_r \leq t_{dz} \leq t_r + \dfrac{N_2 L_r i_{Lm\max}}{N_1 V_c} \end{cases} \tag{13}$$

where I_{bias} and t_r are the bias current and the resonant time duration length, respectively, when $I_{LrA} = 0$, as given in (10). The relationship among the boundary of ΔT and t_{dz}, the magnetizing inductance L_m and the leakage inductance L_r is plotted in Fig. 11 in 3-D form, when $I_{LrA} = 0$ and $C_{\text{oss.eff}} = 342$ pF. Fig. 11(a) indicates that ZVS can be achieved as the fixed time delta is larger than the boundary value. Fig. 11(b) shows that the dead time of the HVS switches must be selected between the two boundaries in order to achieve ZVS.

If ΔT is large enough, the ZVS of the HVS MOSFETs can be obtained. However, as ΔT increases, I_{bias} increases and the conduction loss increases as well. Therefore, the fixed delta should be designed as small as possible as long as ZVS can be achieved.

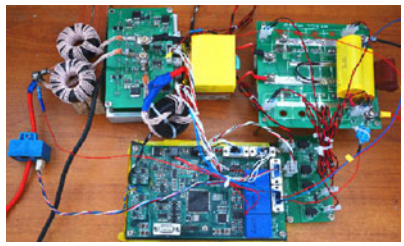

Fig. 12. Experimental prototype.

TABLE III
SYSTEM SPECIFICATIONS

V_1	18–28 V	V_2	300 V
P	1-kW	f	50 kHz
L_1, L_2	11-μH	C_c	30 μF
L_r	1.5 μH	L_m	1 mH
N_1:N_2	2:10	$C_{oss.eff}$	342 pF
ΔT	400 ns	t_{dz}	250 ns

IV. EXPERIMENTAL RESULTS

A. Prototype and Specifications

A 1-kW experimental prototype has been built in order to verify the effectiveness of the current-fed bidirectional dc–dc converter with the proposed control. Fig. 12 gives the lab prototype picture.

The parameter specifications are illustrated in Table III. It must be pointed out that the dc bus is 300 V to supply the voltage for aviation static inverter, which is used to achieve integrated starter and generator function [36]. Besides, battery side switches: IPT015N10N5; HVS switches: FDA50N50, whose charge-equivalent output capacitance $C_{\text{oss.eff}}$ is about 342 pF, according to the datasheet. The secondary-side magnetizing inductance $L_m = 5$ mH, then the minimum $i_{Lm\max}$ can be calculated to be 0.18 A. According to Fig. 11, the fixed time delta should be selected as $\Delta T \geq 368$ ns, and the dead time t_{dz} should be selected around 250 ns. For LVS, two parallel MOSFETs are used as a bottom switch, so the conduction loss can be reduced. Besides, a planar transformer is used and the conversion efficiency can be improved further. The entire control of the system is implemented with a Texas Instruments TM320F28335 DSP.

B. Steady-State Operation

Fig. 13 gives the steady-state waveforms with the proposed control under different battery voltages and different loads. The waveforms at no load are shown in Fig. 13(a) and (b). As seen, although the leakage inductance current in the power transfer stage is zero, there is a bias current to help achieve ZVS for HVS switches. The duty cycles are different with different battery voltages, but the deltas between primary- and secondary-side duty cycles are identical. This causes almost identical bias currents. Fig. 13(c)–(f) shows the waveforms at rated power 1-kW in the boost and buck modes, respectively. The primary-side bias current is about 7 A under any conditions. The ZVS can be achieved and the circulation loss is low. Thus, the proposed con-

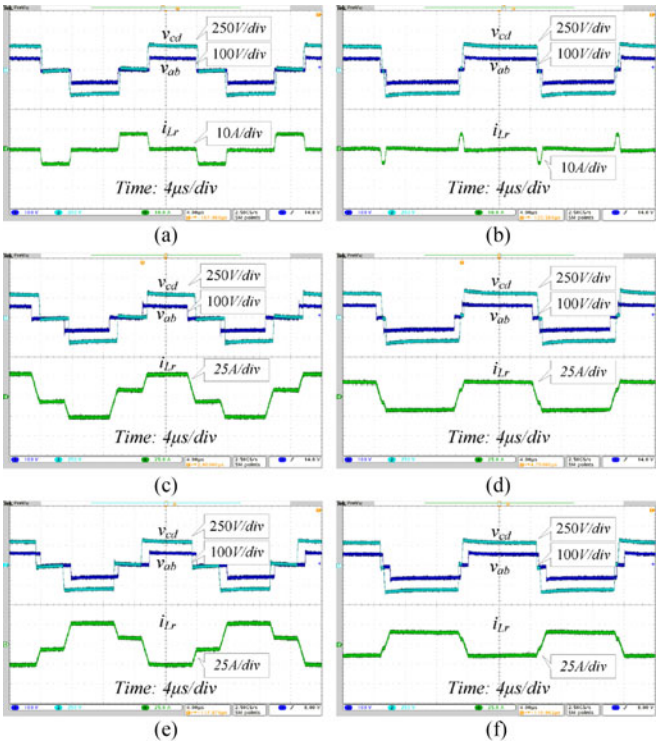

Fig. 13. Steady-state operating waveforms with the proposed control: (a) at no load with $V_1 = 18$ V, (b) at no load with $V_1 = 28$ V, (c) at 1-kW output with $V_1 = 18$ V in the boost mode, (d) at 1-kW output with $V_1 = 28$ V in the boost mode, (e) at 1-kW output with $V_1 = 18$ V in the buck mode, and (f) at 1-kW output with $V_1 = 28$ V in the buck mode.

trol strategy can adapt to the power flow direction and battery voltage variation automatically.

C. Soft Switching Waveforms

All the switches can achieve ZVS in full load range employing the proposed control. Because the magnetizing current is minimum with the minimum LVS voltage (18V), ZVS can be ensured in the full load range once ZVS can be obtained with minimum LVS voltage. ZVS achievement for the HVS switches with $V_1 = 18$ V at no load is illustrated in Fig. 14. For all the power switches, under no-load condition, they can achieve ZVS turn-on.

Fig. 15 shows the ZVS achievement with the proposed control at 1-kW output. Only the waveforms of upper switches are illustrated in Fig. 15, since the upper and lower switches in each switching leg operate symmetrically. As shown, ZVS can be achieved in both boost and buck modes at 1-kW output.

According to the aforementioned analysis, the fixed delta ΔT should be large enough to ensure ZVS of HVS switches, and ΔT is selected to be 400 ns in the experiment. Fig. 16(a) illustrates the switching waveforms of secondary-side switch S_4 when $\Delta T = 300$ ns. As shown, the bias current is about 4 A in this case, and the leakage inductance current reflected to the secondary side is not large enough to discharge the junction capacitor completely within the dead time, and the MOSFETs turn ON with hard switching. In contrast, ZVS can be obtained

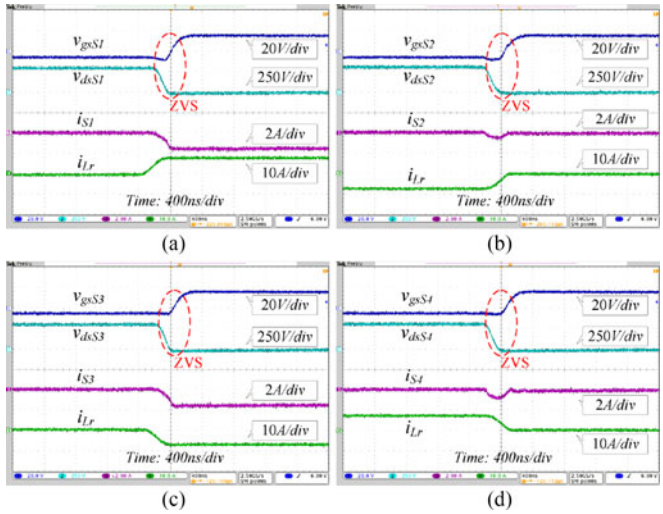

Fig. 14. Experimental results of soft-switching waveforms with the proposed control at no load with $V_1 = 18$ V: (a) ZVS of S_1, (b) ZVS of S_2, (c) ZVS of S_3, and (d) ZVS of S_4.

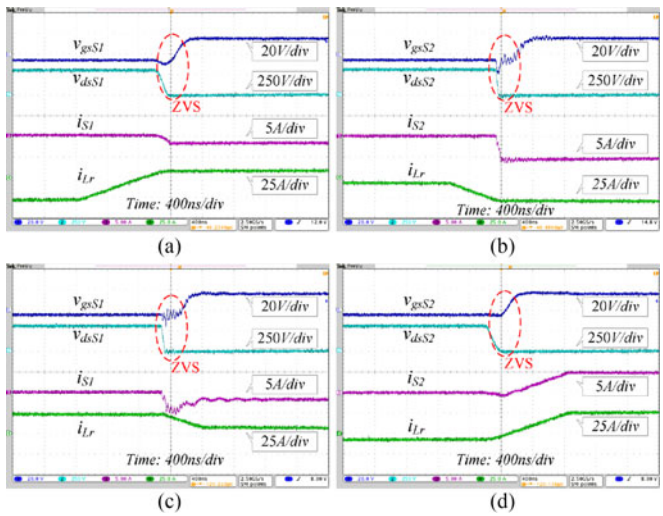

Fig. 15. Soft-switching waveforms with the proposed control at 1-kW output with $V_1 = 18$ V: (a) ZVS of S_1 in the boost mode, (b) ZVS of S_2 in the boost mode, (c) ZVS of S_1 in the buck mode, and (d) ZVS of S_2 in the buck mode.

when $\Delta T = 400$ ns, as shown in Fig. 16(b). The experimental results agree well with the theoretical analysis.

D. Dynamical operation

Fig. 17 illustrates the load-step experimental result from 250 W to 750 W with $V_1 = 23$ V in the boost mode and the zoomed waveforms are shown on the right side. In Fig. 17, V_2 and i_2 are the voltage and current of HVS, respectively. The working mode switches from Mode IA to Mode IIA as the out power increases, indicating that the working mode can be switched between different switching patterns automatically. The output current i_2 is increased from 0.83 A to 2.5 A for the load step change. V_2 drops a little bit and returns to the steady state value within 20ms, meaning that the system has better dynamic performance employing the proposed control.

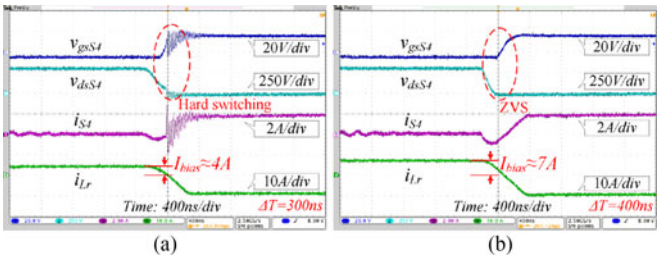

Fig. 16. Switching waveforms with different ΔT at 400-W output with $V_1 = 23$ V in the buck mode: (a) $\Delta T = 300$ ns, (b) $\Delta T = 400$ ns.

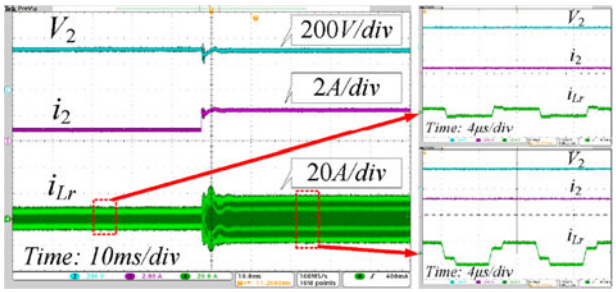

Fig. 17. Load-step experimental result from 250 to 750 W with $V_1 = 23$ V in the boost mode.

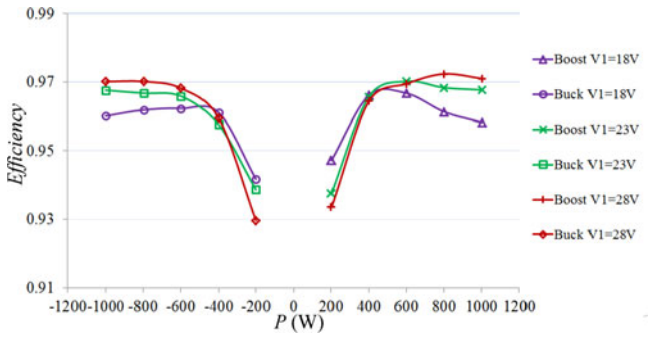

Fig. 18. Power-stage conversion efficiency.

E. Conversion Efficiency and Loss Breakdown Analysis

Fig. 18 shows the power-stage conversion efficiency at different loads and different battery voltages using the proposed optimized control. The overall conversion efficiency is high. At heavy loads, the conduction loss makes up the majority of the total loss, so the efficiency at 28-V battery voltage is higher than that at 18-V battery voltage. However, core losses of the dc inductors and the transformer dominate at light loads, so the efficiency at 28-V battery voltage is higher than that at 18-V battery voltage. Fig. 19 illustrates the loss breakdown analysis with different LVS voltages at 1-kW load. It is worth noting that the control circuit and driving loss are not included. The predicted loss is a little bit lower than measured loss, because of the stray loss in the circuit, such as resistance of PCB layout lines and connectors, ESR of capacitors, etc. As seen, the switching loss is low due to ZVS achievement, and the conduction loss is also reduced significantly with the proposed control. Copper losses are higher at low LVS voltage, while the core losses are higher at a high LVS voltage.

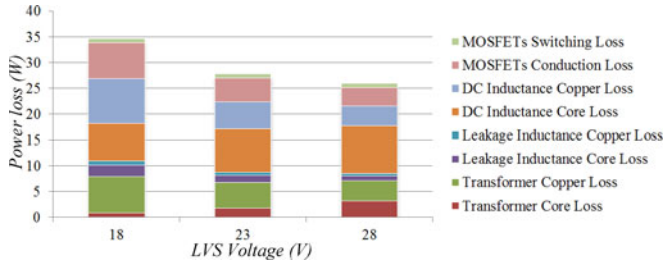

Fig. 19. Loss breakdown with different LVS voltages at 1-kW rated power.

V. Conclusion

All possible combinations of the switching patterns employing the voltage-matching control, including the practical and unpractical ones for current-fed DAB have been studied extensively in this paper. Among all the possibilities, optimized switching patterns are proposed. With which, the equivalent duty cycle for the HVS bridge is smaller than that of the battery-side bridge with a constant delta regardless of the power flow direction, load, and battery voltage variations. Thus, the closed-loop control is simplified and very easy to be implemented on line. The duty-cycle delta is optimized to obtain the minimum circulating current under conditions where ZVS can be achieved for all the switches. The key parameter design to achieve ZVS was addressed in detail in this paper. With the proposed modulation, ZVS can be achieved for all switches throughout the full range of load, in spite of the variation of the operation mode and the battery voltage with reduced circulating current. Thus, the overall conversion efficiency is high. Besides, the converter has a very good dynamic performance employing the proposed control. Experimental results from a 1-kW prototype have verified the theoretical analysis and the effectiveness of the proposed switching pattern.

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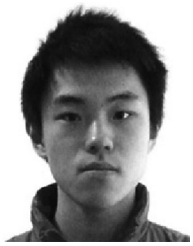

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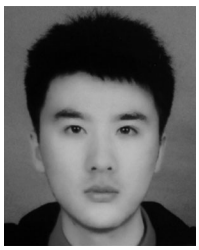

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