Ground Leakage Current Analysis and Suppression in a 60-kW 5-Level T-Type Transformerless SiC PV Inverter

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***Abstract*—In this paper, ground leakage current suppression in a 60-kW 5-level T-type ($5LT^2$) transformerless SiC photovoltaic (PV) inverter has been presented. The common mode (CM) equivalent circuit is analyzed based on a high frequency (HF) CM loop and a low frequency (LF) CM loop, respectively. In the $5LT^2$ inverter, the derived HF CM voltage (CMV) is found to have 86% reduction compared to that of a 3-level T-type ($3LT^2$) inverter. The simulation and experiment results are provided to demonstrate the advantages of $5LT^2$ inverter on HF leakage current suppression. In addition, LF CMV caused by neutral point (NP) voltage oscillation has been analyzed in this paper. It is shown that the LF CMV is nearly proportional to the NP voltage oscillation. Furthermore, an LF CMV compensation method is proposed to suppress the LF CMV by 64%, which is verified by simulation and experiment results. Finally, the leakage current shows 79% reduction in the $5LT^2$ inverter compared to the conventional $3LT^2$ inverter in the experiment. A further 52% leakage current reduction is achieved by the LF CMV compensation in the $5LT^2$ inverter.**

***Index Terms*—5-level, leakage current, photovoltaic (PV), T-type inverter.**

NOMENCLATURE

3L	3-level.
$3LT^2$	3-level T-type.
5L	5-level.
$5LT^2$	5-level T-type.
CM	Common mode.
CMV	CM voltage.
HF	High frequency.
ICT	Intercell transformer.
LF	Low frequency.
NP	Neutral point.
PD	Phase disposition.
PF	Power factor.
POD	Phase opposition disposition.
PS	Phase shift.
PWM	Pulse width modulation.
RMS	Root mean square.
SVM	Space vector modulation.
THD	Total harmonic distortion.
$L_{\rm CM}$	CM inductance.
L_f	Leakage inductance of ICT.
L_g	Sum of line inductance and 480-V transformer leakage inductance.
M	Modulation index.
s	Device switching function.
v_{0N}	Voltage between the NP and the negative line.
$V_{\rm bus}$	DC bus voltage.
$v_{\rm CM}$	CM voltage.
$v_{\rm CM1}$	DC side CM voltage.
$v_{\rm CM2}$	AC side CM voltage.
$v_{\rm CM2\_LF}$	AC side LF CM voltage.
$v_{\rm CM\_COMP}$	LF compensated CM voltage.
$v_{\rm CM\_HF}$	HF CM voltage.
$v_{\rm CM\_HF\_5L}$	HF CM voltage with 5L modulation.
$v_{\rm CM\_HF\_PD}$	HF CM voltage with PD modulation.
$v_{\rm CM\_HF\_POD}$	HF CM voltage with POD modulation.
$V_{\rm CM\_HF}{}_{\omega_c}$	Weighted voltage RMS over switching frequency.
$v_{\rm CM\_LF}$	LF CM voltage.
v_{P0}	Voltage between positive line and the NP.
$v_{\rm NP}$	Voltage difference between v_{P0} and $v_{\rm NP}$.
v_{x0}	Three-phase voltage between output and the NP $(x \in \{A, B, C\})$.
θ	PF angle.
ω_0	Fundamental angular frequency.
ω_c	Carrier angular frequency.

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I. INTRODUCTION

THE three-phase T-type inverter is a well-accepted topology for transformerless photovoltaic (PV) inverter application in tens of kW range and above [1]–[4]. The T-type inverter combines the advantages of 2-level inverters and 3-level inverters, such as low conduction losses, low switching losses, and superior output voltage quality [1]–[5]. SiC device shows

improvement of efficiency and power density in T-type PV inverters [3], [4], [6]. A CM leakage current flows through the parasitic capacitor between the PV array and the ground, once a variable CMV is generated in transformerless grid-connected inverters [7]. This ground leakage current will lead to safety issues, cause potential induced degradation to solar panels, increase the system loss, and reduce the output current quality [7]–[10].

In the three-phase T-type inverters, one conventional method of leakage current suppression is to connect the NP of the ac side capacitors to the NP of the dc bus split capacitors [11]–[13]. The main idea is to provide a low impedance bypass path for the CM current, so that less CM current will pass through the panel leakage capacitance [11]. This method is easy to implement but only applicable to inverters with shunt capacitors in the output, such as an *LCL* filter-based inverter. With the bypass path, the voltage drop on the ac filter changes from half of the line voltage to the phase voltage. There will be additional current ripple and loss in the ac filter's inductor, especially when the switching frequency is high. Therefore, the design tradeoff is between the capability of bypass leakage current and the additional loss in the ac filter.

Another approach to suppress the leakage current is to reduce the CMV by modulation [14]–[17]. In [14]–[16], modulation strategies are proposed to reduce the variation of CMV by selecting voltage vector combinations, while equivalent switching frequency or output THD are increased. A modulation method applying 120° PS between three-phase carriers is proposed in [17]. This method is able to reduce the CMV by 50% compared to the conventional PD PWM, but the THD of output line-to-line voltage will be increased since the harmonic peak at the switching frequency cannot be canceled like the conventional PD PWM. Also this carrier PS method is not applicable to the POD modulation. A dual-bridge inverter approach is presented in [18] to eliminate the common-mode voltage and resulting bearing and leakage currents for induction motor drive. However, if this approach is applied in grid-connected application, an extra HF circulating current occurs between inverter modules, which will cause extra power loss and possible stability issues [19]. The interleaved inverter with coupled inductors or ICT on the other hand has the advantages to suppress the HF circulating current without increasing the size of magnetic components [20]–[22].

A recently emerged issue is that the LF ground leakage current cannot be ignored when the power rating of transformerless PV systems keep on increasing. In the U.S. 50–250-kW commercial scale PV system, there is a trend to eliminate the isolation transformers to further increase the efficiency and reduce the size and weight [11]. As the parasitic capacitance of PV panel is proportional to the power rating, these newly developed higher power commercial PV systems have much smaller LF grounding impedance. Therefore, the LF ground leakage current issue becomes more severe than that in conventional ones. For example, in the 60-kW PV application, the LF leakage current generated is 20% of the 300-mA RMS limitation from the standard [23]. HF ground leakage current does not change with the power rating, so the LF ground leakage current becomes a critical issue

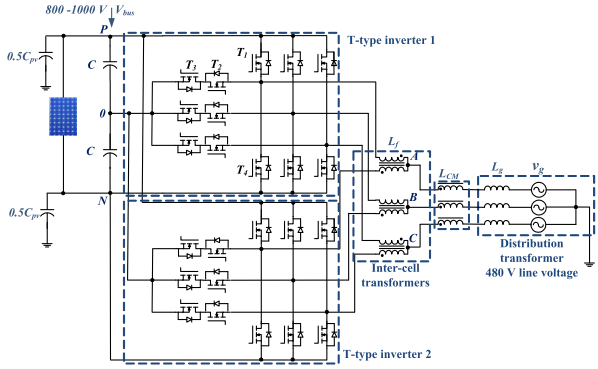

Fig. 1. 5-level T-type transformerless PV inverter.

when the transformerless PV system power rating increases. In this paper, the relationship between LF ground leakage current and NP voltage oscillation has been analyzed and quantified for three-phase T-type inverters. Two mechanisms to generate the LF ground leakage current are identified. The first mechanism is that the NP voltage oscillation will directly generate odd triple harmonic CMV, which is referred as dc side LF CMV in this paper. The second mechanism is that NP voltage oscillation will be modulated by switching functions and will propagate to the ac side with odd triple harmonic CMV, which is referred as ac side LF CMV in this paper. As the LF ground leakage current of T-type inverters is generated by these two mechanisms, the previous approaches presented in the literature to suppress NP oscillation [24]–[30] or reduce CMV [14]–[17] cannot be directly used for LF ground leakage current suppression since the former methods will increase ac side LF CMV and the latter ones assume there is no NP oscillations.

In this paper, the ground leakage current suppression of a 60-kW transformerless SiC PV inverter based on a 5-level T-type inverter, which consists of two $3LT^2$ inverters interleaved with ICT, namely $5LT^2$ topology, has been presented. The advantages of $5LT^2$ topology with ICT in terms of HF ground leakage current suppression is quantified in a 60-kW PV application with mathematical analysis and experiment demonstration. 86% reduction of HF CMV is achieved in the $5LT^2$ inverter compared to the $3LT^2$ inverter, which is a popular topology in commercial transformerless PV string inverters. In addition, this paper has provided a solution for the LF ground leakage suppression based on the analysis of LF CMV generated by those two mechanisms. The proposed technology has been verified in a 60-kW SiC based $5LT^2$ PV inverter prototype.

II. $5LT^2$ Inverter and CM Voltage Analysis

A. System Description

The $5LT^2$ topology is shown in Fig. 1: T-type inverter 1 and T-type inverter 2 are paralleled through ICT and then connected to the 480 V three-phase three-line grid without any extra filters. There are six SiC T-type modules operating at 50 kHz switching frequency. ICT is able to reduce the current ripple in each commutation cell of a parallel converter [21]. Compared to a 3-level *LCL* transformerless PV inverter, $5LT^2$ topology has smaller

TABLE I
SYSTEM PARAMETERS

Items	Value	Items	Value
DC bus voltage $V_{\rm bus}$	800–1000 V	Leakage inductance of ICT L_f	11 μH
Output power P_o	60 kW	Line inductance + leakage inductance of the distributed transformer L_g	~100 μH
Carrier frequency f_c	50 kHz	PV parasitic capacitance $C_{\rm pv}$	10 μF
Distribution transformer	480 V *l-l*, 60 Hz	Half dc bus capacitance C	1.2 mF

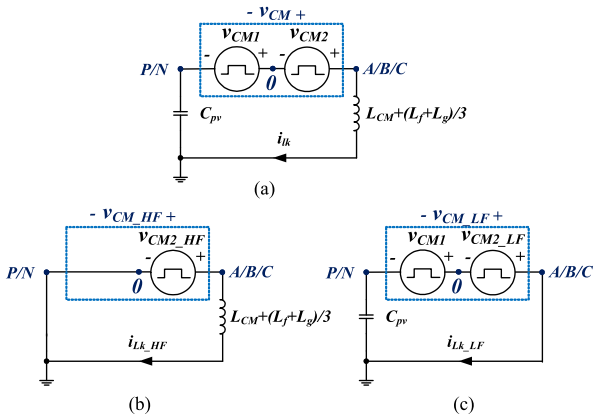

Fig. 2. CM equivalent circuit of 5LT^2 inverter: (a) Overall CM equivalent circuit; (b) HF CM equivalent circuit; and (c) LF CM equivalent circuit.

magnetic size, core loss, and CMV. Also there is no stability issue brought by the *LCL* filter, so this topology is more suitable for weak grid and multiconverter operation. The advantages and the design application of this topology in SiC PV inverters have been presented in [22]. This paper is focused on the ground leakage current suppression analysis and solution.

System parameters of the 60-kW PV inverter in this paper are listed in Table I. $C_{\rm pv}$ is the parasitic capacitance between the PV array and the ground, which varies with the panel frame structure and the weather condition. The capacitance is 60–110 nF/kW in the standard PV modules and 100–160 nF/kW in the thin-film PV modules [33]. The capacitance value $C_{\rm pv}$ used in this paper is 10 μF for 60-kW power. L_f is the leakage inductance of the ICT, L_g is the line inductance plus the leakage inductance of the distributed transformer, both of them act as the ac filter. $L_{\rm CM}$ is the CM choke used to suppress the switching frequency ground leakage current.

B. CM Equivalent Circuit

The overall leakage current loop of the 5LT^2 topology is shown in Fig. 2(a). The CMV consists of $v_{\rm CM1}$ and $v_{\rm CM2}$, which is denoted in (1). $v_{\rm CM1}$ is the CMV between the PV panel and the dc bus NP, which is defined in (2). $v_{\rm CM2}$, denoted in (3), is the CMV between the dc bus NP and the grid connection point. CMV can be analyzed in HF range and LF range, respectively, since the HF CMV is related to the switching frequency modulation method and the LF CMV is related to the fundamental frequency power. Fig. 2(b) and (c) shows the HF and LF equivalent circuit respectively. $v_{\rm CM1}$ only includes LF oscillation because the HF oscillation in the NP is filtered by the dc bus HF capacitors. In Fig. 2(b), the capacitor is considered as short-circuit in the HF range. Also in Fig. 2(c), the inductor is considered short-circuit in the LF range

$$v_{\rm CM} = v_{\rm CM1} + v_{\rm CM2} \tag{1}$$

$$v_{\rm CM1}(t) = \frac{v_{0P}(t) + v_{0N}(t)}{2} = \frac{v_{0N}(t) - v_{P0}(t)}{2} \tag{2}$$

$$v_{\rm CM2}(t) = \frac{v_{A0}(t) + v_{B0}(t) + v_{C0}(t)}{3} \tag{3}$$

where $v_{x0}(x \in \{A, B, C\})$ is the output phase voltage. The phase voltage can be calculated by the PWM gain multiplying the switching function [34], as shown in (4)

$$v_{x0}(t) = K_{{\rm PWM}\_x}(t) \times S_x(t),\ x \in \{A, B, C\} \tag{4}$$

$$K_{{\rm PWM}\_x}(t) = \frac{1}{2}V_{\rm bus} + K_{{\rm PWM\_LF}\_x}(t) \tag{5}$$

$$S_x(t) = S_{x\_{\rm LF}}(t) + S_{x\_{\rm HF}}(t) \tag{6}$$

where $K_{\rm PWM}(t)$ is the magnitude gain of the inverter. With the NP voltage oscillation, there is a LF PWM gain $K_{\rm PWM\_LF}(t)$ existing besides the constant half dc bus voltage, as shown in (5). $S_x(t)$ in (6) is the phase voltage's switching function including the fundamental sinusoidal part $S_{x\_{\rm LF}}(t)$ and the switching harmonics part $S_{x\_{\rm HF}}(t)$.

Based on (4)–(6), the $v_{\rm CM2}(t)$ can be derived in (7), which consists of four parts: The first one is zero when the three-phase current is symmetrically controlled without zero-sequence component; the second one is the LF component; the third one is the HF component; and the last one can be neglected in the HF range because the LF PWM gain magnitude is much smaller than the dc PWM gain

$$v_{CM2}(t) = \underbrace{\frac{1}{2}V_{bus} \times \frac{1}{3}\sum S_{x\_LF}(t)}_{\text{Equals to 0}} + \underbrace{\frac{1}{3}\sum K_{PWM\_LF\_x}(t) \times S_{x\_LF}(t)}_{\text{LF component}} + \underbrace{\frac{1}{2}V_{bus} \times \frac{1}{3}\sum S_{x\_HF}(t)}_{\text{HF component}} + \underbrace{\frac{1}{3}\sum K_{PWM\_LF\_x}(t) \times S_{x\_HF}(t)}_{\text{HF component, small, neglected}} \tag{7}$$

Combing (2) and (7), the HF CMV $v_{\rm CM\_HF}(t)$ and LF CMV $v_{\rm CM\_LF}$ can be derived in (8) and (9), respectively

$$v_{\rm CM\_HF}(t) = \frac{1}{2}V_{\rm bus} \times \frac{1}{3}\sum {\rm S}_{x\_{\rm HF}}(t) \tag{8}$$

$$v_{\rm CM\_LF} = \frac{v_{0N}(t) - v_{P0}(t)}{2} + \frac{1}{3}\sum {\rm K}_{{\rm PWM\_LF}\_x}(t) \times {\rm S}_{x\_{\rm LF}}(t). \tag{9}$$

From (8) and (9), it can be noticed that HF CMV is related to the modulation method and LF CMV is related to the NP voltage oscillation. In order to suppress the leakage current, both the HF and LF CMV need to be investigated and suppressed. Sections III and IV will analyze the HF CMV and LF CMV, respectively.

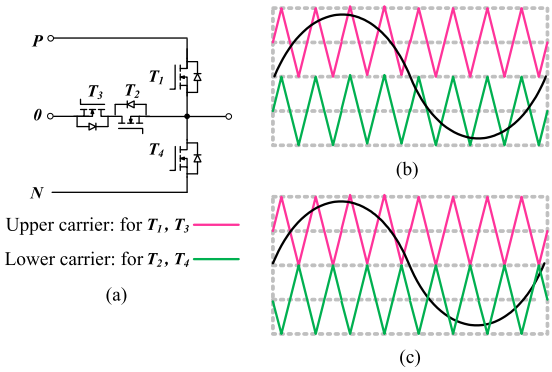

Fig. 3. Modulation methods for 3LT^2 inverters: (a) One T-type phase leg; (b) PD modulation; and (c) POD modulation.

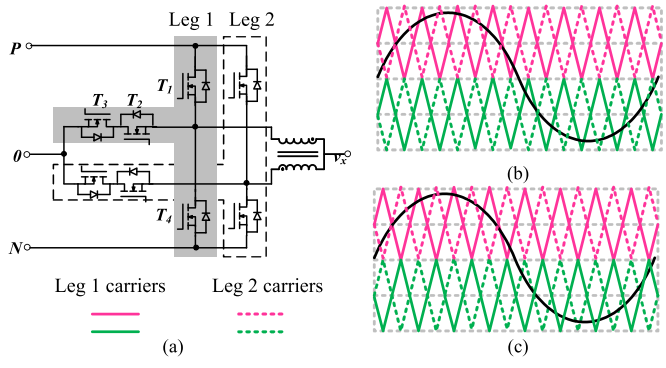

Fig. 4. Modulation methods for the 5LT^2 inverter: (a) Two T-type phase legs; (b) interleaved modulation based on PD; and (c) interleaved modulation based on POD.

III. HF CMV Suppression in the 5LT^2 Inverter

A. PS Modulation Method for the 5LT^2 Inverter

There are two conventional CB PWM methods for 3LT^2 inverters: PD and POD. Fig. 3(b) shows the basic principle of the PD PWM scheme using double triangle carrier signals. The upper carrier signal is used to generate the gate signals for the switch T_1, T_3. The lower carrier signal is used to generate the gate signals for the switch T_2, T_4. For POD schemes in Fig. 3(c), the upper carrier signal and the lower carrier signal are in the opposite phase.

Fourier series of the 3-level output phase voltage was derived in [34] and the phase A's switching function is listed here in (10) and (11). In PD modulation (10), there are odd central harmonics, odd sidebands around the even carrier multiples, and even sidebands around the odd carrier multiples. In POD modulation (11), there are only sidebands without central harmonics. POD has lower output phase voltage THD, and PD has lower output line-to-line voltage THD

$$S_{A\_PD}(t) = M\sin(\omega_0 t) + \frac{8}{\pi^2}\sum_{m=1}^{\infty}\frac{1}{2m-1} \times \sum_{k=1}^{\infty}\frac{J_{2k-1}[(2m-1)\pi M]}{2k-1} \cdot \sin[(2m-1)\omega_c t] + \frac{2}{\pi}\sum_{m=1}^{\infty}\frac{1}{2m}\sum_{n=-\infty}^{\infty}J_{2n+1}(2m\pi M) \cdot \cos n\pi \cdot \sin[2m\omega_c t + (2n+1)\omega_0 t] + \frac{8}{\pi^2}\sum_{m=1}^{\infty}\frac{1}{2m-1}\sum_{\substack{n=-\infty \\ n\neq 0}}^{\infty}\sum_{k=1}^{\infty} \times \frac{J_{2k-1}[(2m-1)\pi M](2k-1)\cos n\pi}{(2k-1+2n)\cdot(2k-1-2n)} \cdot \sin[(2m-1)\omega_c t + 2n\omega_0 t] \quad (10)$$

$$S_{A\_POD}(t) = M\sin(\omega_0 t) + \frac{2}{\pi}\sum_{m=1}^{\infty}\frac{1}{m}\sum_{n=-\infty}^{\infty}J_{2n+1}(m\pi M) \cdot \cos n\pi \cdot \sin[m\omega_c t + (2n+1)\omega_0 t] \quad (11)$$

where M is the modulation index, ω_0 is the fundamental angular frequency, and ω_c is the carrier angular frequency. $J_{2n+1}(m\pi M)$ is the Bessel function, which is used to represent the coefficient after double Fourier integral analysis of the PWM waveform, as shown in [34].

In the 5LT^2 inverter, carriers can be interleaved between two inverters in both PD and POD, as shown in Fig. 4. The Fourier series of the interleaved phase voltage's switching function is derived in (12). Interleaved PD and interleaved POD are found to have the same phase voltage spectrum, and the voltage spectrum is the same as 5L APOD modulation's [34]. After interleaved modulation, the 5LT^2 inverter achieves 5-level output phase voltage. The output voltage harmonics begin at the twice of switching frequency, which makes filterless possible in this grid-tie PV inverter

$$S_{A\_5L}(t) = M\sin(\omega_0 t) + \frac{2}{\pi}\sum_{m=1}^{\infty}\frac{1}{2m}\sum_{n=-\infty}^{\infty}J_{2n+1}(2m\pi M) \cdot \cos(n\pi)\cdot\sin[2m\omega_c t + (2n+1)\omega_0 t] \quad (12)$$

B. HF CMV Spectrum Analysis for the 5LT^2 Inverter

In a symmetrical three-phase system, generalized Fourier series of HF CMV is derived in (13) based on (8). There are only carrier harmonics and its triple-fundamental sideband in the CMV spectrum. C_{mn} is the magnitude at the *n*th fundamental sideband around the *m*th carrier frequency in the switching function's spectrum

$$v_{\mathrm{CM\_HF}}(t) = \frac{1}{3}\left(v_{A0}(t) + v_{B0}(t) + v_{C0}(t)\right) = \frac{V_{\mathrm{bus}}}{2}\sum_{m=1}^{\infty}\sum_{n=-\infty}^{\infty}C_{mn}\cdot\cos[m\omega_c t + 3n\omega_0 t]. \quad (13)$$

In the conventional 3LT^2 PV inverters, the Fourier series of HF CMV based on PD and POD can be derived from (10), (11), and (8). HF CMV harmonics in PD (14) is concentrated at carrier frequency with large magnitude. HF CMV harmonics in POD (15) is distributed at the triple sideband of the carrier

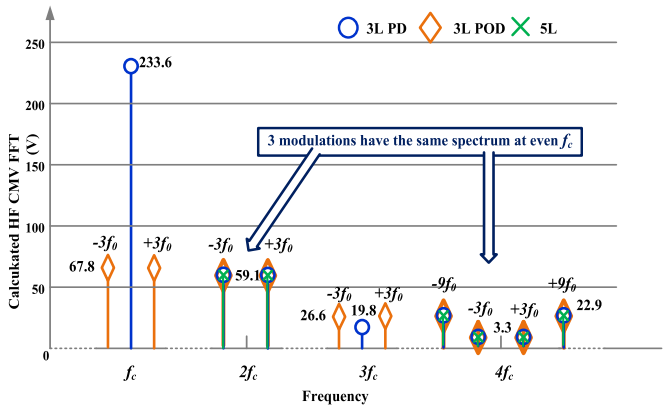

Fig. 5. Calculated HF CMV harmonics distribution with three modulation methods at $V_{\rm bus}$= 1000 V.

frequency, and the magnitude peak is less than half of PD's

$$v_{\rm CM\_HF\_PD}(t) = \frac{4V_{\rm bus}}{\pi^2}\sum_{m=1}^{\infty}\frac{1}{2m-1}\sum_{k=1}^{\infty} \times \frac{J_{2k-1}\left[(2m-1)\pi M\right]}{(2k-1)} \cdot \sin\left[(2m-1)\omega_c t\right] + \frac{V_{\rm bus}}{\pi}\sum_{m=1}^{\infty}\frac{1}{2m}\sum_{n=-\infty}^{\infty} J_{3\cdot(2n+1)}(2m\pi M) \cdot \cos(3n+1)\pi \cdot \sin\left[2m\omega_c t + 3\cdot(2n+1)\omega_0 t\right] \quad (14)$$

$$v_{\rm CM\_HF\_POD}(t) = \frac{V_{\rm bus}}{\pi}\sum_{m=1}^{\infty}\frac{1}{m}\sum_{n=-\infty}^{\infty} J_{3\cdot(2n+1)}(m\pi M) \cdot \cos(3n+1)\pi \cdot \sin\left[m\omega_c t + 3\cdot(2n+1)\omega_0 t\right]. \quad (15)$$

Combining (8) and (12), the HF CMV in a 5LT^2 inverter is derived in (16), harmonics are distributed at the triple sideband of even carrier harmonics that follows the general HF CMV spectrum in (13)

$$v_{\rm CM\_HF\_5L}(t) = \frac{V_{\rm bus}}{\pi}\sum_{m=1}^{\infty}\frac{1}{2m}\sum_{n=-\infty}^{\infty} J_{3\cdot(2n+1)}(2m\pi M) \cdot \cos(3n+1)\pi \cdot \sin\left[2m\omega_c t + 3\cdot(2n+1)\omega_0 t\right]. \quad (16)$$

With derived HF CMV in three modulation methods (14)–(16), the FFT results of HF CMV ($V_{\rm bus}$= 1000 V) is calculated and shown in Fig. 5. Among them 3-level PD modulation generates the maximum HF CMV. Three modulation methods generate the same HF CMV at even carrier frequency, which is the only spectrum existed in 5-level modulation.

In the simulation, three modulation methods are applied in the 5LT^2 inverter. The $v_{\rm CM\_HF}$ waveforms and FFT results are shown in Fig. 6 and they are consistent with the calculation in Fig. 5. 5-level modulation has reduced the HF CMV and pushed it to higher frequency domain, which brings the advantage for HF leakage current suppression.

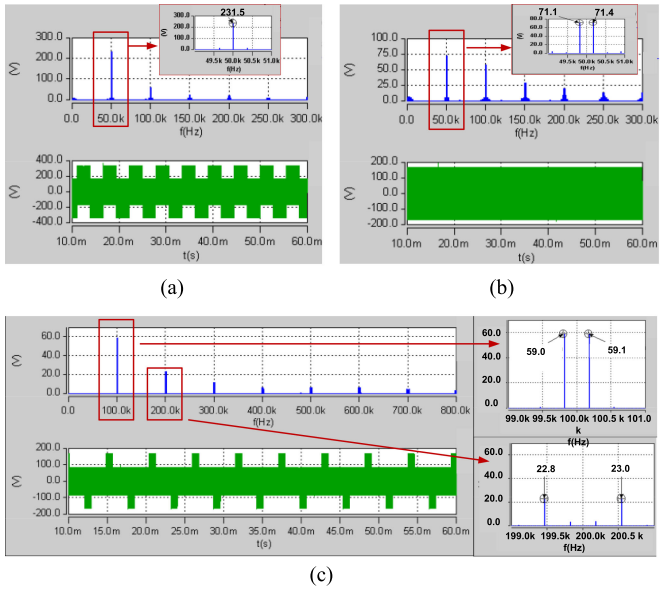

Fig. 6. Simulation of HF CMV waveforms and harmonics distribution at $V_{\rm bus}$= 1000 V in the T-type inverter: (a) 3-level PD modulation; (b) 3-level POD modulation; and (c) 5-level modulation.

C. CM Choke Inductance Comparison Between Different Modulations

The HF leakage current is related to the CMV spectrum voltage at all the switching frequency harmonics. In order to quantify the required CM choke inductance, the HF CMV from (13) is weighted over the switching frequency, as shown in (17). With fixed switching frequency, the HF leakage current RMS value is decided by the weighted HF CMV RMS value and the inductance in the CM loop, as shown in (18). So the required CM choke inductance $L_{\rm CM}$ is decided by the harmonics' magnitude and the corresponding frequency in CMV. The weighted HF CMV RMS value (17) is used in this paper to compare the CM choke value between three different modulations

$$V_{\rm CM\_HF\_\omega_c} = \frac{1}{\sqrt{2}}\cdot\sqrt{\sum_{m=1}^{\infty}\left(\frac{\max_{n\in(-\infty,\infty)} C_{mn}}{m}\right)^2} \quad (17)$$

$$I_{\rm lk\_HF\_RMS} = \frac{V_{\rm CM\_HF\_\omega_c}}{\omega_c\cdot\left(L_{\rm CM}+\frac{L_f+L_g}{3}\right)}. \quad (18)$$

In the HF CMV spectrums, the voltage magnitude decreases rapidly with the frequency. So only $f_c \sim 6f_c$ voltage spectrum is considered in the weighted HF CMV calculation, the higher frequency component is neglected. Based on (14)–(17), the weighted HF CMV in different modulations is calculated and compared in Fig. 7. 5-level modulation has much lower weighted HF CMV than the conventional 3-level modulations. HF CMV magnitude increases obviously when the dc bus voltage increases in both 3-level PD and 5-level modulation. In 3-level POD, the weighted HF CMV RMS value is nearly constant with the bus voltage varying.

For the 60-kW PV inverter presented in this paper, the nominal dc bus voltage is selected as 825 V. At 825 V, the weighted

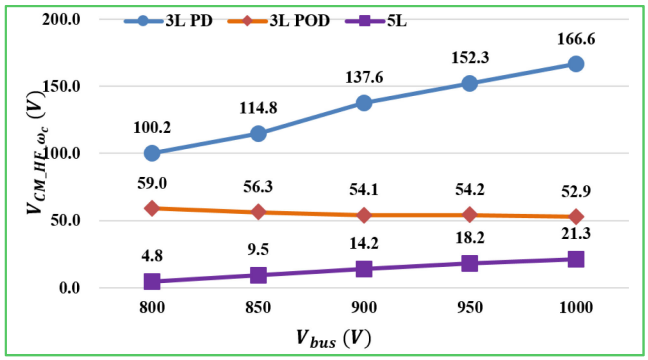

Fig. 7. Calculated 50 kHz weighted HF CMV RMS value under different dc bus voltages.

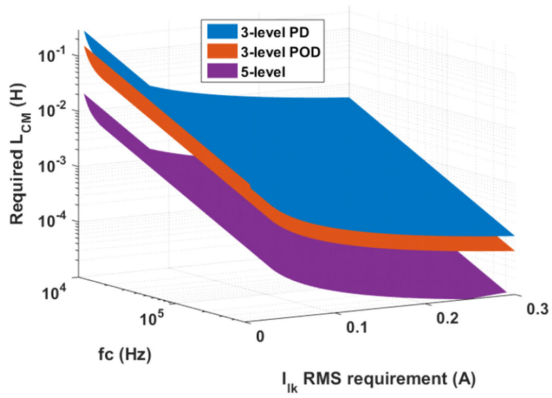

Fig. 8. Required CM choke value in different modulation methods with different leakage current requirements at $V_{\rm bus}$ = 825 V.

HF CMV RMS at switching frequency is 107.5, 57.6, and 8.0 V with 3-level PD, 3-level POD, and 5-Level modulation, respectively. Therefore, with the same leakage current requirement, the required CM choke inductance in the 5LT^2 inverter can be reduced by 86% compared with the conventional 3LT^2 inverters. With different leakage current requirements, the required CM choke inductance in different modulation methods is drawn in Fig. 8. Higher switching frequency and larger CM choke helps suppressing the leakage current. The German national standard DINV V DEV 0126-1-1 [23] limits the leakage current below 300-mA RMS. For the 300 mA requirement, the CM choke required for 3-level PD, 3-level POD, 5-level modulation is 1.1 mH, 611.1 μH, and 84.9 μH, respectively.

IV. LF CMV Analysis and Compensation in the 5LT^2 Inverter

As shown in Fig. 9, three phases are absorbing and injecting energy to the NP simultaneously in the 5LT^2 inverter. The NP voltage oscillation is caused by the NP current (i_0) variation. Generally, the NP voltage oscillation only includes LF part and the switching frequency part is filtered by the HF dc bus capacitors. As shown in Fig. 9, the dc side LF CMV $v_{\rm CM1}(t)$ is directly generated by the NP voltage oscillation. The ac side LF CMV $v_{\rm CM2\_LF}(t)$ is caused by LF PWM gain which is also related to the NP voltage oscillation. In order to find out the equation for the LF CMV, NP voltage oscillation needs to be analyzed first.

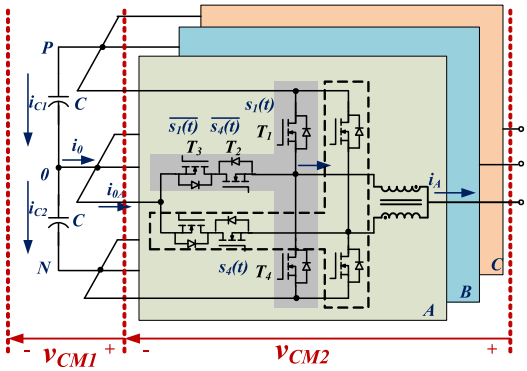

Fig. 9. Three-phase 5LT^2 inverter circuit diagram.

A. DC Side LF CMV Analysis in the 5LT^2 Inverter

The NP voltage $v_{\rm NP}$ is defined in (19) as the difference between two half voltages in the dc bus

$$v_{\rm NP} = v_{P0} - v_{0N} = \frac{1}{C}\int_0^t (i_{C1} - i_{C2})\,dt = \frac{1}{C}\int_0^t i_0\,dt. \tag{19}$$

When the dc bus is balanced and the three-phase current is symmetrical without zero sequence component, the three-phase current is shown in (20) and LF phase voltage switching function from (6) is listed in (21)

$$\begin{cases} i_A = I_g \cdot \sin(\omega_0 t + \theta) \\ i_B = I_g \cdot \sin\left(\omega_0 t - \dfrac{2}{3}\pi + \theta\right) \\ i_C = I_g \cdot \sin\left(\omega_0 t + \dfrac{2}{3}\pi + \theta\right) \end{cases} \tag{20}$$

$$\begin{cases} S_{\rm A\_LF}(t) = M \cdot \sin(\omega_0 t) \\ S_{\rm B\_LF}(t) = M \cdot \sin\left(\omega_0 t - \dfrac{2}{3}\pi\right) \\ S_{\rm C\_LF}(t) = M \cdot \sin\left(\omega_0 t + \dfrac{2}{3}\pi\right) \end{cases} \tag{21}$$

where I_g is the magnitude of the grid-tie inverter's output current, $\cos\theta$ is the PF of the inverter. Because there is no external filter in this PV system, fundamental voltage switching function $S_{x\_\rm LF}(t)$ is in the same phase as the grid voltage.

The device switching function $s(t) = \{1, 0\}$ is defined in [35] to calculate the NP current. Equation (22) shows that the phase voltage switching function $S_x(t)$ is the difference of T_1 and T_4's device switching function, where $s_{x1}(t)$ generates the positive half-period voltage and $s_{x4}(t)$ generates the negative half period voltage. The NP phase current $i_{0x}(t)$ can also be calculated by devices' switching function, as shown in (23), where $i_x(t)$ is the phase current defined in (20), $x \in \{A, B, C\}$

$$S_x(t) = s_{x1}(t) - s_{x4}(t) \tag{22}$$

$$i_{0x}(t) = i_x(t) - i_x(t) \times [s_{x1}(t) + s_{x4}(t)]. \tag{23}$$

Only LF component is considered in the NP current, so $S_x(t)$ is represented by $S_{x\_\rm LF}(t)$ for NP current calculation. The NP phase current can be derived from (22) and (23), as shown in

(24). Whereby, the sign function of three-phase LF phase voltage switching function is listed in (25)

$$i_{0x}(t) = i_x(t) - i_x(t) \times S_{x\_\mathrm{LF}}(t) \times sgn\left(S_{x\_\mathrm{LF}}(t)\right) \quad (24)$$

$$\begin{cases} sgn\left(S_{A\_\mathrm{LF}}(t)\right) = \frac{4}{\pi}\sum_{k=1}^{\infty}\dfrac{\sin\left[(2k-1)\cdot\omega_0 t\right]}{2k-1} \\ sgn\left(S_{B\_\mathrm{LF}}(t)\right) = \dfrac{4}{\pi}\sum_{k=1}^{\infty}\dfrac{\sin\left[(2k-1)\cdot\omega_0 t - \frac{2}{3}\pi\right]}{2k-1} \\ sgn\left(S_{C\_\mathrm{LF}}(t)\right) = \dfrac{4}{\pi}\sum_{k=1}^{\infty}\dfrac{\sin\left[(2k-1)\cdot\omega_0 t + \frac{2}{3}\pi\right]}{2k-1} \end{cases} . \quad (25)$$

Therefore, NP current is derived in (26). It is shown that NP current is composed by odd triple harmonics

$$\begin{aligned} i_0(t) &= i_{0A}(t) + i_{0B}(t) + i_{0C}(t) \\ &= \frac{3I_g \cdot M}{\pi} \sum_{\substack{k=1 \\ k \text{ is odd}}}^{\infty} \left[\left(\frac{1}{3k-2} - \frac{1}{3k} \right) \cdot \sin(3k\omega_0 t + \theta) \right. \\ &\quad \left. + \left(\frac{1}{3k+2} - \frac{1}{3k} \right) \cdot \sin(3k\omega_0 t - \theta) \right] \end{aligned} \quad (26)$$

Substitute (26) into (19), NP voltage can be derived in

$$\begin{aligned} v_{\mathrm{NP}} &= \frac{3I_g \cdot M}{\pi \cdot C} \sum_{\substack{k=1 \\ k \text{ is odd}}}^{\infty} \left[\frac{2}{9k^2 \cdot (3k+2)} \cdot \cos(3k\omega_0 t - \theta) \right. \\ &\quad \left. - \frac{2}{9k^2 \cdot (3k-2)} \cdot \cos(3k\omega_0 t + \theta) \right] \\ &\approx \frac{2I_g \cdot M}{15\pi \cdot C \cdot \omega_0} \left[\cos(3\omega_0 t - \theta) - 5\cos(3\omega_0 t + \theta) \right]. \end{aligned} \quad (27)$$

Only third harmonics is considered in the NP voltage since the higher harmonics' magnitude is small enough to be neglected. In the 5LT^2 inverter's design, NP voltage oscillation is limited by the device's voltage rating and decided by the dc capacitance, grid current, modulation index, and PF. In this paper, dc capacitance C is selected as 1.2 mF for the 1200-V voltage rating devices.

Based on (2), (19), and (27) the dc side LF CMV is proportional to the NP voltage and shown in

$$\begin{aligned} v_{\mathrm{CM1}} &= -\frac{1}{2} v_{\mathrm{NP}} = \frac{I_g \cdot M}{15\pi \cdot C \cdot \omega_0} \left[5\cos(3\omega_0 t + \theta) \right. \\ &\quad \left. - \cos(3\omega_0 t - \theta) \right]. \end{aligned} \quad (28)$$

B. AC Side LF CMV Analysis in the 5LT^2 Inverter

NP voltage oscillation is propagated to the ac side through the oscillation in the PWM gain. Fig. 10(a) shows the NP voltage third oscillation pattern when PF = 1. Accordingly, the PWM gain for three-phase is shown in Fig. 10(b)–(d). The PWM gains are in the same pattern and have $2\pi/3$ phase difference within three-phase, which is the same as their phase voltage.

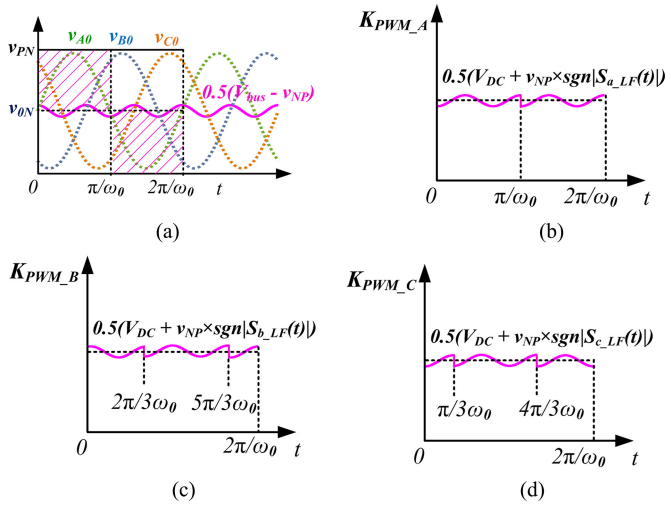

Fig. 10. Oscillation pattern when PF = 1: (a) NP voltage oscillation; (b) PWM gain variation in phase A; (c) PWM gain variation in phase B; and (d) PWM gain variation in phase C.

The LF PWM gain of phase A is derived in (29) based on (27) and (25), and there are only even harmonics observed in the PWM gain

$$\begin{aligned} K_{\mathrm{PWM\_LF\_}A}(t) &= \frac{2I_g \cdot M}{15\pi^2 \cdot C \cdot \omega_0} \sum_{k=1}^{\infty} \left[\left(\frac{1}{2k+3} - \frac{5}{2k-3} \right) \right. \\ &\quad \cdot \sin(2k\omega_0 t + \theta) + \left(\frac{1}{2k-3} - \frac{5}{2k+3} \right) \\ &\quad \left. \cdot \sin(2k\omega_0 t - \theta) \right]. \end{aligned} \quad (29)$$

With LF PWM gains and phase voltage switching functions, the ac side LF CMV can be derived from (9), (21), and (29). Similar to the dc side LF CMV, the ac side LF CMV includes only odd triple harmonics and the harmonics above third is small enough to be neglected, as shown in

$$\begin{aligned} v_{\mathrm{CM2\_LF}} &= \frac{I_g \cdot M^2}{15\pi^2 \cdot C \cdot \omega_0} \sum_{\substack{k=1 \\ k \text{ is odd}}}^{\infty} \left[\frac{8(3k+1)(3k+8)}{(9k^2-16)(9k^2-4)} \right. \\ &\quad \cdot \cos(3k\omega_0 t + \theta) + \frac{8(3k-1)(3k-8)}{(9k^2-16)(9k^2-4)} \\ &\quad \left. \cdot \cos(3k\omega_0 t - \theta) \right] \approx \frac{I_g \cdot M^2}{15\pi^2 \cdot C \cdot \omega_0} \cdot \frac{16}{7} \\ &\quad \cdot \left[\cos(3\omega_0 t - \theta) - \frac{22}{5} \cdot \cos(3\omega_0 t + \theta) \right]. \end{aligned} \quad (30)$$

C. LF CMV Analysis and Simulation

In order to combine the dc side LF CMV and the ac side CMV, phase angles α_1 and α_2 are defined as the leading angle of the dc side LF CMV and the ac side LF CMV from the phase A voltage. Based on (28) and (30), the relationship between α_1,

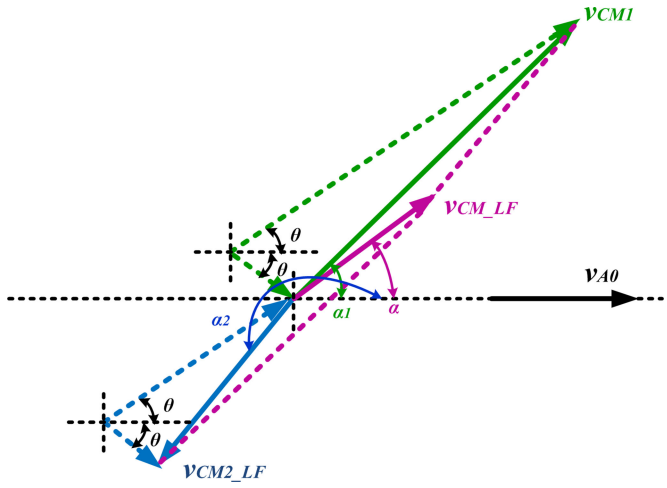

Fig. 11. Voltage vectors of LF CMVs.

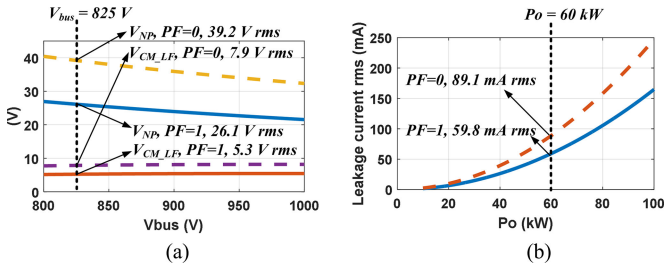

Fig. 12. Calculated LF CMV RMS and LF leakage current RMS: (a) P_o = 60 kW, LF CMV RMS value with different bus voltage; and (b) $V_{\rm bus}$ = 825 V, LF leakage current RMS with different P_o.

α_2 and the PF angle θ can be derived in

$$\tan\alpha_1 = \frac{3}{2}\cdot\tan\theta, \quad \tan\alpha_2 = -\frac{27}{17}\cdot\tan\theta. \tag{31}$$

The LF CMV vectors are drawn in Fig. 11, where phase angle α is the total LF CMV's leading angle from the phase A voltage. Both $v_{\rm CM1}$ and $v_{\rm CM2\_LF}$ are composed of two vectors, each of them are in the opposite direction between these two LF CMVs. The magnitude of $v_{\rm CM1}$ is larger than $v_{\rm CM2}$. The absolute value of $\tan\alpha_2$ is larger than $\tan\alpha_1$, so α is smaller than α_1. The total LF CMV is derived in (32) with only third harmonics

$$v_{\rm CM_{LF}} = \frac{I_g\cdot M}{15\pi\cdot C\cdot\omega_0}\sqrt{(A-B)^2+4AB\cdot(\sin 2\theta)^2}\cdot\cos(3\omega_0 t+\alpha) \tag{32}$$

where $A = 5-\frac{16\cdot 22M}{35\pi}$, $B = 1-\frac{16M}{7\pi}$, $\tan\alpha = \frac{A+B}{A-B}\cdot\tan\theta$.

Based on LF CM equivalent circuit in Fig. 2(c), the LF leakage current is shown in

$$i_{\rm lk\_LF} = 3\omega_0\cdot C_{\rm pv}\cdot v_{\rm CM\_LF}. \tag{33}$$

Fig. 12 shows the calculated RMS value of the LF CMV and the LF leakage current at $V_{\rm bus}$ = 825 V. In Fig. 12(a), although the NP voltage oscillation decreases with the increased dc bus voltage at 60 kW, the LF CMV value does not change much. In Fig. 12(b), the LF CMV and the LF leakage current increases

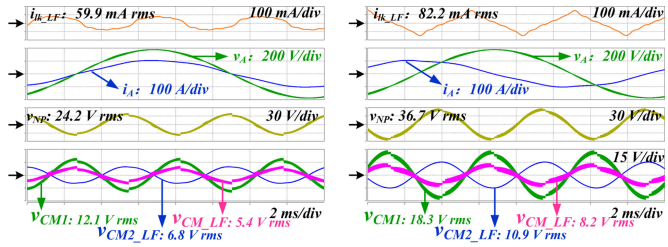

Fig. 13. Circuit simulation LF CMV and leakage current at $V_{\rm bus}$ = 825 V, C = 1.2 mH, P_o = 60 kW: (a) PF = 1; and (b) PF = 0.

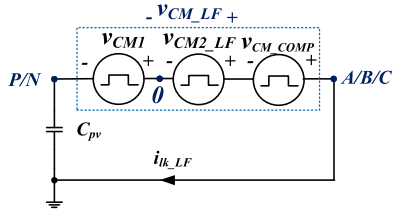

Fig. 14. LF CM equivalent circuit with CMV compensation.

with the quadratic dependence of power rating since the PV capacitance is also proportional to the power. When PF = 1, the NP oscillation causes 5.3-V RMS LF CMV and 59.8-mA leakage current. When PF = 0, the NP oscillation causes 7.9-V RMS LF CMV and 89.1-mA leakage current. The LF CMV magnitude increases with the PF decreasing. When PF is 0, $v_{\rm CM\_LF}$ and $i_{\rm lk\_LF}$ is 1.5 times of the value in unit PF.

In order to verify the calculation, Fig. 13 shows the simulation LF CMV and LF leakage current results of the 60-kW 5LT^2 PV inverter. The RMS value of the NP oscillation, LF CMV, LF leakage current, and the PF impact are all consistent with the calculation in Fig. 12.

D. LF CMV Compensation

When the dc bus capacitance reduces or the inverter's power rating increases, LF leakage current will increase with the LF CMV. Also, suppressing the LF leakage current is able to reduce the CM choke size for the HF leakage current suppression. However, it is hard to increase the LF impedance in the CM loop through passive components. CM choke has little effect on the LF impedance and reducing the PV capacitance $C_{\rm pv}$ is not practical. An LF CMV compensation method is proposed in this paper, as shown in Fig. 14. With the compensated LF CMV ($v_{\rm CM\_COMP}$) added to the three-phase modulation voltage, the total LF CMV is able to be suppressed so as the LF leakage current.

One way to generate $v_{\rm CM\_COMP}$ is to add an LF leakage current control loop. Theoretically this method is able to control the LF leakage current to zero. But it needs extra grounding leakage current sensor and digital PR controller, which requires more hardware components and brings more computation burden to the intensive interruption time in the DSP.

Observed from the LF CMV in (32), the coefficient (A + B)/(A – B) between $\tan\alpha$ and $\tan\theta$ is between 1.36 and 1.42 when the modulation index varies with 800–1000 Vdc. Since

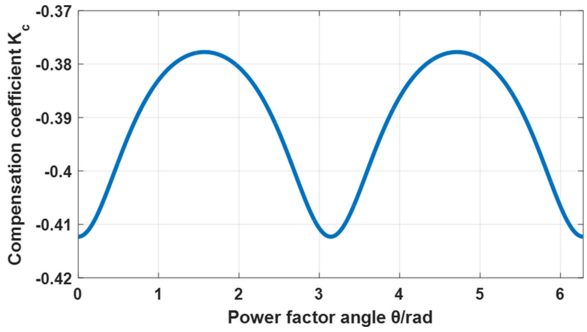

Fig. 15. LF CMV compensation coefficient K_c with different PF angles.

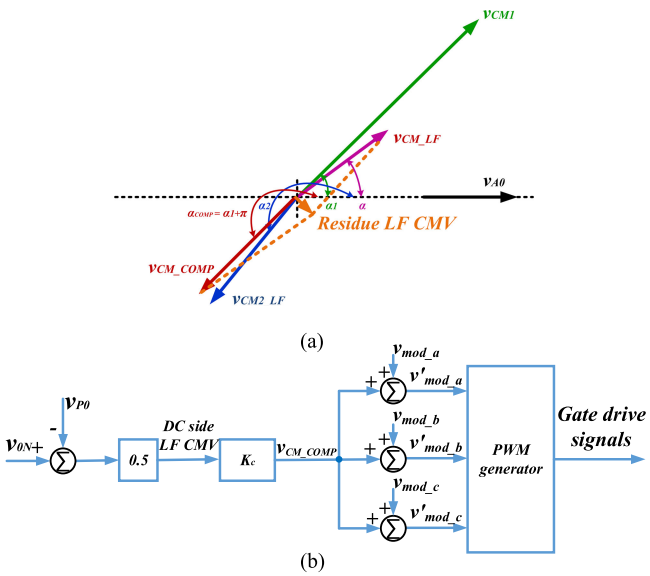

Fig. 16. LF CMV with compensation: (a) Voltage vectors; and (b) control diagram.

the coefficient is close to 1.5 ($\tan\alpha_1/\tan\theta$), the total CMV can be estimated to be in the same direction as the dc side LF CMV. Therefore, dc side and ac side LF CMV can be considered in the opposite direction. Therefore, another approach for the LF CMV compensation is the dc side CMV feedforward control. The compensation voltage $v_{\mathrm{CM\_COMP}}$ is proportional to v_{CM1}, as shown in

$$v_{\mathrm{CM\_COMP}} = K_c \cdot v_{\mathrm{CM1}} \tag{34}$$

where the compensation coefficient $K_c = \frac{|v_{\mathrm{CM2\_LF}}|}{|v_{\mathrm{CM1}}|} - 1 = \frac{16M}{35\pi} \cdot \sqrt{22 - \frac{63}{16+20\sin\theta^2}} - 1$, derived from (28) and (30). Fig. 15 presents variations of K_c with PF angle θ. It can be observed that K_c is not sensitive to θ. Therefore, a constant K_c of –0.41 is used for compensation in this paper.

Fig. 16 shows the compensation voltage vector and the control diagram for LF CMV compensation. After compensation, there will be a small amount of residual LF CMV, which is shown in (35) and Fig. 16(a). After compensation, the residual LF CMV's

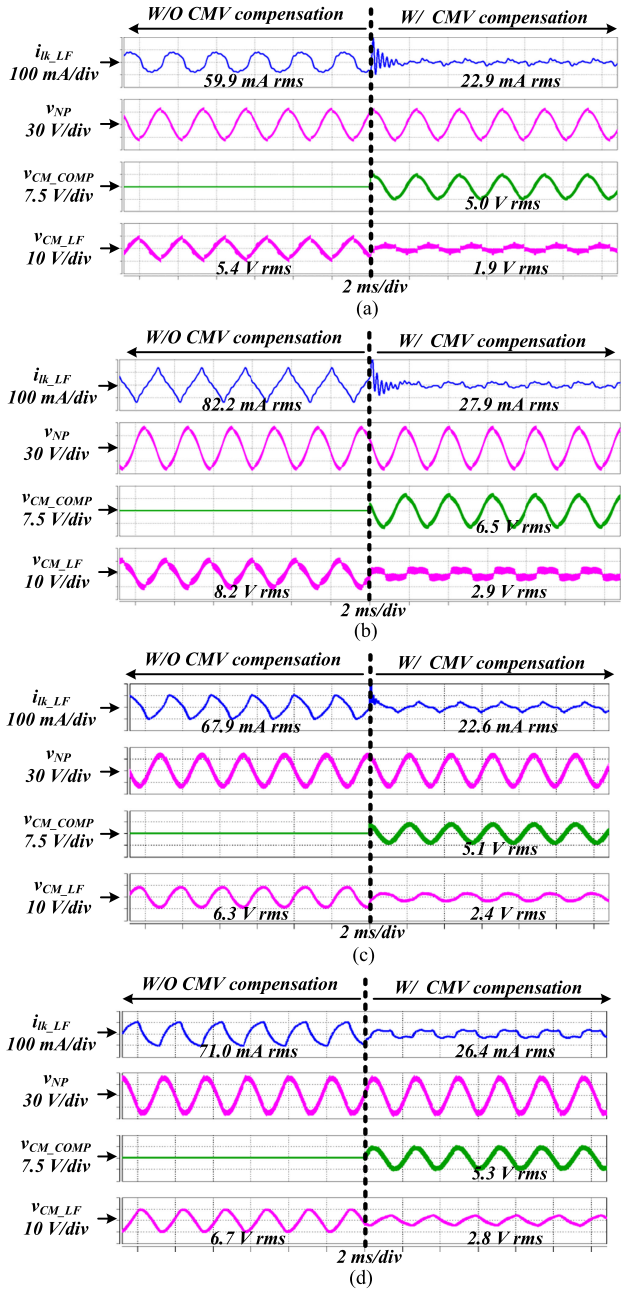

Fig. 17. Simulation of LF leakage current suppression at V_{bus}= 825 V, P_o = 60 kW: (a) PF = 1; and (b) PF = 0. (c) PF = –0.8; and (d) PF = 0.8.

magnitude is small

$$v_{\mathrm{CM\_LF\_Residue}} = \frac{I_g \cdot M}{15\pi \cdot C \cdot \omega_0}\left[0.09 \cdot \cos\left(3\omega_0 t - \theta\right) - 0.10 \cdot \cos\left(3\omega_0 t + \theta\right)\right]. \tag{35}$$

As shown in the simulation results of Fig. 17, LF leakage current $i_{\mathrm{lk\_LF}}$ is able to be suppressed by 62% with the LF CMV compensation. Since a constant coefficient K_c is used for LF CMV compensation, there exists a small residual LF CMV after compensation. The PF = 0 case in Fig. 17(b) is selected as

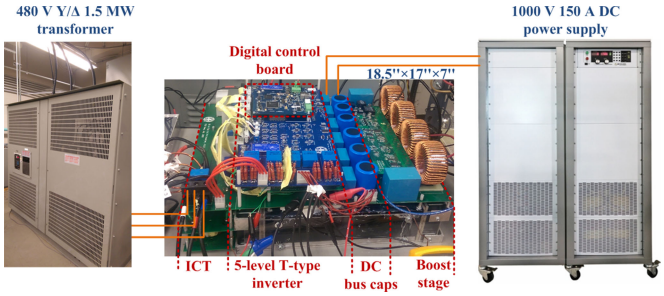

Fig. 18. 60 kW 5LT^2 transformerless SiC PV inverter prototype.

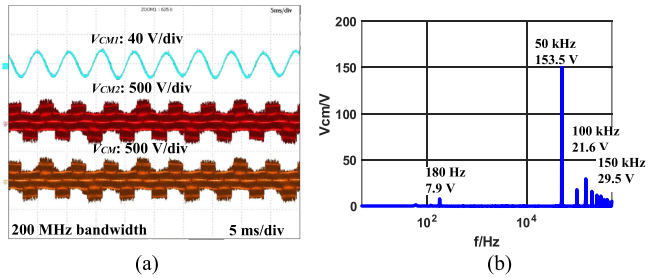

Fig. 19. Experimental CMV waveforms with 3-level PD modulation at $V_{\rm bus}=$ 825 V: (a) CMV waveforms; and (b) CMV FFT results.

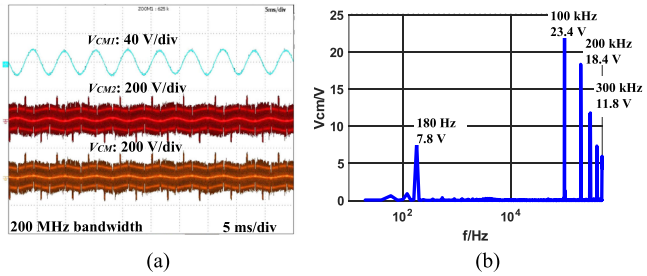

Fig. 20. Experimental CMV waveforms with 5-level modulation at $V_{\rm bus}=$ 825 V, P_o = 60 kW: (a) CMV waveforms; and (b) CMV FFT results.

an extreme case to demonstrate that the LF CMV compensation is not sensitive to PF. In field application, a commercial scale PV inverter is working between +/–0.8 PF [36]. Between +/–0.8, the influence of PF on LF CMV is small, as shown in Fig. 17(c) and (d).

V. Experimental Results

A 60-kW 5LT^2 transformerless SiC PV inverter prototype has been built in the lab, as shown in Fig. 18. There are two stages in this PV inverter. The first stage is a four-channel interleaved boost converter using two SiC boost modules. The second is the inverter stage using six SiC T-type modules, two of each are parallel coupled through an ICT. The boost stage is controlled by analog circuit. The inverter stage is controlled by DSP and FPGA, where DSP is the main controller and the FPGA is used to generate 12 channels' gate drive signals. If the traditional 3-level PD and POD modulation method are implemented, the output phase-to-neutral output voltage will be 3-level. When the PS modulation method is implemented, the output phase-to-neutral output voltage will be 5-level. In the test, a 1000-V 150-A dc power supply is used to emulate the PV panels input. The three-phase output is connected to the grid through a 480-V three-phase 1.5-MW transformer.

A. CMV Comparison Between 3L PD and 5L Modulation

As mentioned in Section III, PD modulation has lower output line-to-line voltage THD compared to POD modulation in 3LT^2 inverters. Since the 60-kW inverter prototype is connected to a three-phase three-wire grid, 3-level PD modulation is implemented in the experiment for comparison. The Yokogawa oscilloscope DL9710L 5GS/s 1GHz is used to measure the waveforms and the voltage probe is PBDH0150 1400-V peak 150-MHz bandwidth. $v_{\rm CM1}$ is measured by $v_{0N}-0.5v_{\rm dc}$, and $v_{\rm CM2}$ is measured by $(v_{A0}+v_{B0}+v_{C0})/3$. The CMV comparison between 3-level PD and 5-level modulation is shown in Figs. 19 and 20, where the switching frequencies are both 50 kHz.

In the HF range, the CMV experiment waveform with PD modulation in Fig. 19 is consistent with the simulation results in Fig. 6(a). The CMV peak is happened at 50 kHz. The HF weighted CMV magnitude is 109.1 V, which is consistent with the calculated value in Fig. 7. In Fig. 20, the 5-level CMV waveform is consistent with the simulation results in Fig. 6(c), and the harmonics start at twice the switching frequency due to the interleaved carries. The HF weighted CMV magnitude is 9.0 V, which is also consistent with the calculated result in Fig. 7. In 3-level PD, the weighted CMV RMS is more than ten times of the 5-level's. The experiment demonstrates that the HF CMV is greatly reduced in the 5-level modulation so the ground leakage current can be suppressed from the source.

In the LF range, 3-level PD and 5-level modulation generate a similar third harmonic magnitude in the CMV FFT, as shown in Figs. 19(b) and 20(b). In order to clearly show the third harmonics in the CMV, the voltage probes are set as 8-kHz bandwidth to remove the HF impact. As shown in Fig. 21, 3-level PD and 5-level modulation have the same LF CMVs, which demonstrate that the LF CMV is not related to the switching frequency modulation. The dc side and ac side LF CMV are in the opposite direction. All the RMS values are consistent with the calculation in Fig. 12 and the simulation in Fig. 13.

B. Leakage Current Comparison Between 3L PD and 5L Modulation

A commercial CM choke is used to suppress the HF leakage current, which is TPC-222U-B65A with nanocrystalline core, shown in Fig. 22(a). The measured CM choke's inductance is 832 μH at 100 kHz. Three-phase current is measured by 150-A 10-MHz Yokogawa current probe. The ground leakage current is measured by current sense transformer (CT) CT07-1000 with 0.1% 1-kΩ output resistor, as shown in Fig. 22(b). The current transformer shows up to 300-kHz bandwidth (–3dB) capability, which covers all the main harmonics in the ground leakage current in this prototype.

Both 3-level PD and 5-level modulation are implemented in the 60-kW grid-tie experiment, and the test result is shown

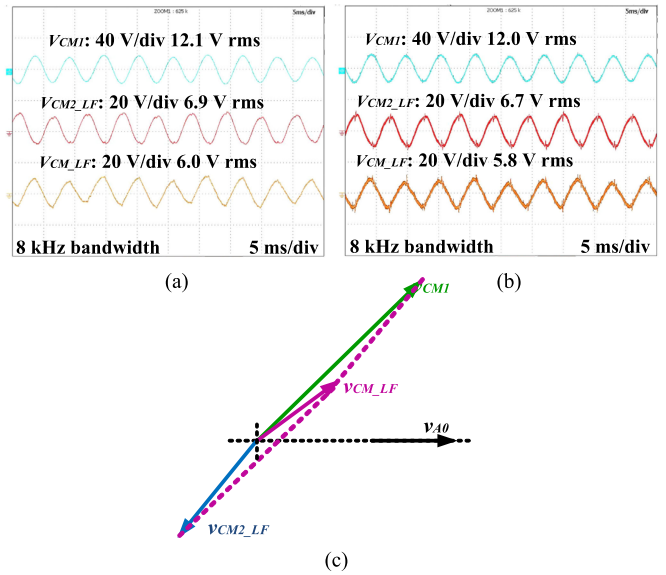

Fig. 21. Experimental waveforms of LF CMV at $V_{\rm bus}$= 825 V, P_o = 60 kW, PF = 1: (a) 3-level PD modulation; (b) 5-level modulation; and (c) phasor diagram.

Fig. 22. Photo of CM chock and CT: (a) CM choke; and (b) CT for leakage current measurement.

in Fig. 23. 3-level modulation shows more HF harmonics than 5-level modulation in the phase current, which is consistent with theoretical analysis. The measured leakage current is 826-mA RMS in 3-level PD modulation and 172-mA RMS in the 5-level modulation. With the same CM choke and hardware configuration, 5-level modulation reduces the leakage current by 79%. The reduction percentage is less than the HF CMV's because of two reasons: The CM choke inductance decreases with the increased frequency, and the total leakage current also includes the LF component, which is the same in different modulations.

C. LF Leakage Current Suppression in the 5LT^2 Inverter

The LF CMV compensation method presented in Fig. 16 is implemented in the 60-kW test. As shown in Fig. 24, this method can reduce the LF CMV by 64% and further reduce the total leakage current by 52%. The injected third CMV is 3.7 V, which only reduces the modulation index by 1%. This LF CMV compensation method only requires several sum operators in the software without any extra hardware. Although this method cannot fully remove the LF CMV, the total leakage current has obvious improvement with little cost.

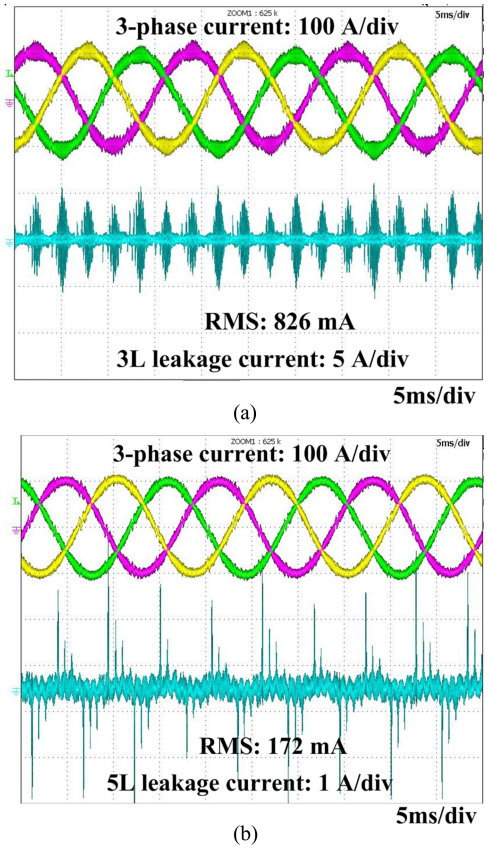

Fig. 23. Experimental waveforms of ground leakage current at $V_{\rm bus}$= 825 V, P_o = 60 kW: (a) 3-level PD modulation; and (b) 5-level modulation.

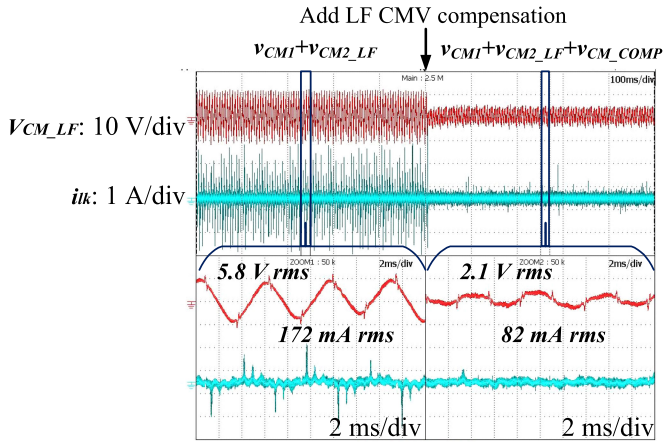

Fig. 24. Leakage current reduction with LF CMV compensation at $V_{\rm bus}$= 825 V, P_o = 60 kW.

VI. Conclusion

This paper has demonstrated that 5LT^2 topology has the advantages to suppress the ground leakage current for PV inverter applications. HF CMV spectrum of this topology is derived and compared with that of traditional commercial 3LT^2 PV inverters. The CM choke inductance comparison based on weighted HF CMV is presented. The leakage current is reduced by 79% of the value in conventional 3-level T-type PV inverters using

PD modulation. LF CMV caused by NP voltage oscillation has been analyzed and found to be independent from the modulation methods. LF CMV compensation method based on NP voltage is proposed and shows 52% further reduction in the leakage current. This LF CMV compensation method can be used for all neutral-point-clamped topologies for the leakage current suppression. The experimental results of a 60-kW prototype show that the CMV consistent with the analysis and simulation results, and ground leakage current is well suppressed with 5-level modulation and LF CMV compensation method.

DISCLAIMER

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REFERENCES

[1] K. Fujii, "1-MW advanced T-type NPC converters for solar power generation system," in *Proc. IEEE Power Electron. Appl. Conf.*, Sep. 2013, pp. 1–10

[2] "PV grid-connected inverters 2015 $\sim$ 2016," Sungrow Corp., Product Report, Mar. 2015. [Online]. Available: http://www.sungrowpower.com

[3] J. Mooken, B. Agrawal, and J. Liu, "Efficient and compact 50kW Gen2 SiC device based PV string inverter," in *Proc. IEEE Int. Exhib. Conf. Power Electron., Intell. Motion, Renewable Energy Energy Manag. PCIM Eur.*, May 2014, pp. 1–7.

[4] G. Deboy, R. Rupp, R. Mallwitz, and H. Ludwig, "New SiC JFET boost performance of solar inverters," *Power Electron. Eur.*, vol. 4, 2011, pp. 29–33.

[5] M. Schweizer and J. W. Kolar, "Design and implementation of a highly efficient three-level T-type converter for low-voltage applications," *IEEE Trans. Power Electron.*, vol. 28, no. 2, pp. 899–907, Feb. 2013.

[6] R. M. Burkart and J. W. Kolar, "Comparative evaluation of SiC and Si PV inverter systems based on power density and efficiency as indicators of initial cost and operating revenue," in *Proc. IEEE Workshop Control Model. Power Electron.*, Jun. 2013.

[7] B. Yang, W. Li, Y. Gu, W. Cui, and X. He, "Improved transformerless inverter with common-mode leakage current elimination for a photovoltaic grid-connected power system," *IEEE Trans. Power Electron.*, vol. 27, no. 2, pp. 752–762, Feb. 2012.

[8] S. Pingel *et al.*, "Potential induced degradation of solar cells and panels," in *Proc. 35th IEEE Photovolt. Spec. Conf.*, Jun. 2010, pp. 002817–002822.

[9] H. Xiao and S. Xie, "Transformerless split-inductor neutral point clamped three-level PV grid-connected inverter," *IEEE Trans. Power Electron.*, vol. 27, no. 4, pp. 1799–1808, Apr. 2012.

[10] Y. Zhou and H. Li, "Analysis and suppression of leakage current in cascaded-multilevel-inverter-based PV systems," *IEEE Trans. Power Electron.*, vol. 29, no. 10, pp. 5265–5277, Oct. 2014.

[11] T. Zhao, V. Bhavaraju, P. Nirantare, and J. Xu, "Evaluation of commercial scale transformerless solar inverter technology," in *Proc. IEEE Energy Convers. Congr. Expo.*, Sep. 2015, pp. 5342–5348.

[12] D. Dong, F. Luo, D. Boroyevich, and P. Mattavelli, "Leakage current reduction in a single-phase bidirectional ac–dc full-bridge inverter," *IEEE Trans. Power Electron.*, vol. 27, no. 10, pp. 4281–4291, Oct. 2012.

[13] Y. Koyama, J. Tsuda, and H. Mochikawa, "Grid-tie inverter," *U.S. Patent 2012/0275201 A1*, Jul. 12, 2012.

[14] M. C. Cavalcanti, A. M. Farias, K. C. de Oliveira, F. A. S. Neves, and J. L. Afonso, "Eliminating leakage currents in neutral point clamped inverters for photovoltaic systems," *IEEE Trans. Ind. Electron.*, vol. 59, no. 1, pp. 435–443, Jan. 2012.

[15] J.-S. Lee and K.-B. Lee, "New modulation techniques for a leakage current reduction and a neutral-point voltage balance in transformerless photovoltaic systems using a three-level inverter," *IEEE Trans. Power Electron.*, vol. 29, no. 4, pp. 1720–1732, Apr. 2014.

[16] X. Guo, M. C. Cavalcanti, A. M. Farias, and J. M. Guerrero, "Single carrier modulation for neutral point-clamped inverters in three-phase transformerless photovoltaic systems," *IEEE Trans. Power Electron.*, vol. 28, no. 6, pp. 2635–2637, Jun. 2013.

[17] T. D. Nguyen, D. Q. Phan, D. N. Dao, and H. Lee, "Carrier phase-shift PWM to reduce common-mode voltage for three-level T-type NPC inverters," *J. Power Electron.*, vol. 14, no. 6, pp. 1197–1207, Nov. 2014.

[18] A. V. Jouanne and H. Zhang, "A dual-bridge inverter approach to eliminating common-mode voltages and bearing and leakage currents," *IEEE Trans. Power Electron.*, vol. 14, no. 1, pp. 43–48, Jan. 1999.

[19] D. Shin, J. Lee, D. Yoo, and H. Kim, "Stability improvement of interleaved voltage source inverters employing coupled inductors for grid-connected applications," *IEEE Trans. Ind. Electron.*, vol. 62, no. 10, pp. 6014–6023, Oct. 2015.

[20] D. Zhang, F. Wang, R. Burgos, R. Lai, and D. Boroyevich, "Impact of interleaving on AC passive components of paralleled three-phase voltage-source converters," *IEEE Trans. Ind. Appl.*, vol. 43, no. 3, pp. 1042–1054, Mar. 2010.

[21] B. Cougo, T. Meynard, and G. Gateau, "Parallel three-phase inverters: Optimal PWM method for flux reduction in intercell transformers," *IEEE Trans. Power Electron.*, vol. 26, no. 8, pp. 2184–2191, Aug. 2011.

[22] Y. J. Shi, Y. X. Shi, R. Xie, L. Wang, and H. Li, "A 50 kW high power density paralleled-five-level PV converter based on SiC T-type MOSFET modules," in *Proc. IEEE Energy Convers. Congr. Expo.*, Sep. 2016, pp. 1–8.

[23] *Automatic Disconnection Device Between a Generator and the Public Low-Voltage Grid*, German National Standard DIN VDE V 0126-1-1, Aug. 2013.

[24] U. Choi, F. Blaabjerg, and K. Lee, "Method to minimize the low-frequency neutral-point voltage oscillations with time-offset injection for neutral-point-clamped inverters," *IEEE Tran. Ind. Appl.*, vol. 51, no. 2, pp. 1678–1691, Mar. 2015.

[25] J. Pou *et al.*, "Fast-processing modulation strategy for the neutral-point clamped converter with total elimination of low-frequency voltage oscillations in the neutral point," *IEEE Trans. Ind. Electron.*, vol. 54, no. 4, pp. 2288–2294, Aug. 2007.

[26] A. Pevere and R. Petrella, "Discontinuous hybrid modulation technique for three-phase three-level neutral point clamped inverters," in *Proc. IEEE Energy Convers. Congr. Expo.*, Sep. 2013, pp. 3992–3999.

[27] J. Zaragoza, J. Pou, S. Ceballos, E. Robles, P. Ibanez, and J. Villate, "A comprehensive study of a hybrid modulation technique for the neutral-point-clamped converter," *IEEE Trans. Ind. Electron.*, vol. 56, no. 2, pp. 294–304, Feb. 2009.

[28] Y. Jiao, F. C. Lee, and S. Lu, "Space vector modulation for three-level NPC converter with neutral point voltage balance and switching loss reduction," *IEEE Trans. Power Electron.*, vol. 29, no. 10, pp. 5579–5591, Oct. 2014.

[29] J. Pou, J. Zaragoza, S. Ceballos, M. Saeedifard, and D. Boroyevich, "A carrier-based PWM strategy with zero-sequence voltage injection for a three-level neutral-point-clamped converter," *IEEE Trans. Power Electron.*, vol. 27, no. 2, pp. 642–651, Feb. 2012.

[30] J. Shen, S. Schroder, B. Duro, and R. Ronesner, "A neutral-point balancing controller for a three-level inverter with full power-factor range and low distortion," *IEEE Trans. Ind. App.*, vol. 49, no. 1, pp. 138–148, Jan./Feb. 2013.

[31] R. G. A. Cacau, R. P. T. Bascopé, J. A. F. Neto, and G.V.T. Bascopé, "Five-level T-type inverter based on multistate switching cell," *IEEE Trans. Ind. Appl.*, vol. 50, no. 6, pp. 3857–3866, Nov./Dec. 2014.

[32] L. Wang, Y. J. Shi, Y. X. Shi, R. Xie, and H. Li, "Ground leakage current suppression in a 50 kW 5-level T-type transformerless PV inverter," in *Proc. IEEE Energy Convers. Congr. Expo.*, Sep. 2016, pp. 1–6.

[33] "Capacitive leakage currents," SMA Technical Information, Ableitstrom-TI-en-25, version 2.5.
[34] D. G. Holmes and T. A. Lipo, *Pulse Width Modulation for Power Converters: Principles and Practice*, Piscataway, NJ, USA: Wiley, 2003, ch. 11.
[35] B. P. McGrath and D. G. Holmes, "A general analytical method for calculating inverter DC-link current harmonics," *IEEE Trans. Ind. Appl.*, vol. 45, no. 5, pp. 1851–1859, Sep./Oct. 2009.
[36] "SMA Sunny tripower 60-US datasheet," [Online]. Available: http://www.sma-america.com/products/solarinverters/sunny-tripower-60-us.html

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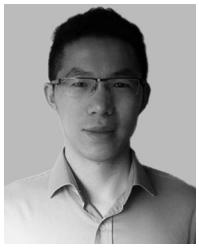

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