Design of a High Efficiency DC–DC Buck Converter With Two-Step Digital PWM and Low Power Self-Tracking Zero Current Detector for IoT Applications

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***Abstract*—In this paper, a high efficiency dc–dc buck converter with two-step digital pulse width modulation (DPWM) and low power self-tracking zero current detector (ST-ZCD) is proposed for Internet of Things (IoT) and ultralow power applications. The hybrid DPWM core with high linearity and low power consumption is proposed to implement the high efficiency DPWM dc–dc converter. It is composed of a two-step delay control using the counter and delay line. An adaptive window analog to digital converter is proposed to reduce the output voltage ripple within 20 mV. A dead time generator is implemented with the proposed ST-ZCD to minimize the reverse current. The ST-ZCD can improve efficiency by reducing the control loss that accounts for a large proportion of the dc–dc converter. Also, all digital type-III compensator is implemented for the low power and small die area. This chip is fabricated with a 55 nm CMOS process, which uses the standard supply voltage of 1.5–3 V to generate the output voltage of 1.2 V. The total active area is 500 μm $\times$ 300 μm. The measured peak efficiency of the DPWM dc–dc buck converter is 91.5% with a quiescent current consuming only 130 μA.**

***Index Terms*—Adaptive window analog to digital converter (ADC), dc–dc buck converter, digital compensator, digital pulse width modulation (DPWM), hybrid digital pulse width modulation core, self-tracking zero current detector (ST-ZCD).**

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I. Introduction

RECENTLY, an Internet of Things (IoT) has been developed with a reduced size to enhance flexibility in response to customers' needs. The IoT applications are developed to operate for years without replacing the battery. However, the lifetime and charging technology of the battery have not kept up with the demand of IoT. Therefore, the attention paid to developing power management techniques is gradually increasing in response to the need to solve low power requirements [1].

Digital controllers could be a very attractive solution in low-to-medium power dc–dc buck converters because of their inherently lower sensitivity to process variation and programmability, as well as their reduction or elimination of passive components for tuning without compromising dynamic performance, simplicity, or cost [2]–[5]. Furthermore, it is relatively easier to design an advanced control algorithm using a digital approach to achieve optimal transient performance.

On the other hand, despite these advantages, the output voltage ripple of conventional digital pulse width modulation (DPWM) based dc–dc buck converter is proportional to the resolution of DPWM. To improve the ripple characteristics of output voltage, the resolution of the analog to digital converter (ADC) must be increased. Therefore, as the DPWM has a higher resolution for lower output voltage ripple characteristics, the current consumption and area of the DPWM are increased. It makes some of DPWM's advantages disappear [5], [6]. In order to design a digital dc–dc converter with the low power, the resolution needs to be lowered requiring the circuit compensation. In addition, when the dc–dc buck converter is operated in the discontinuous conduction mode (DCM) region, it needs functions to prevent the reverse current. The conventional dc–dc buck converter prevents the reverse current with the zero current detection (ZCD) [7]. The conventional ZCD structure senses the zero current through the internal switching (V_X) node; it has a voltage drop caused by the resistance component of the power metal-oxide-semiconductor field-effect transistor (MOSFET). Also, the power consumption required by the conventional

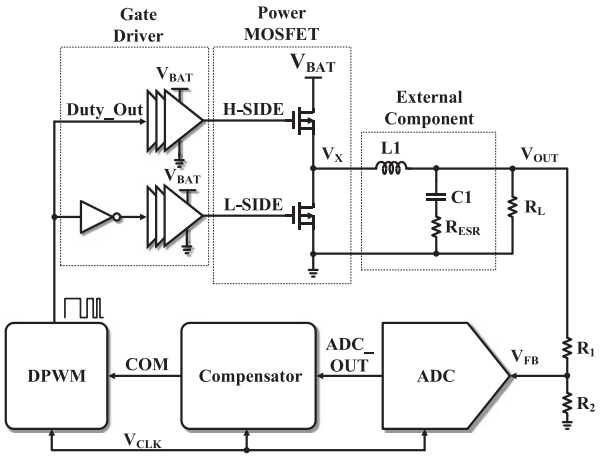


Fig. 1. Conventional DPWM dc–dc buck converter.

ZCD to sense the point of the zero inductor current using the high performance comparator is considerable [8].

In this paper, a high efficiency dc–dc buck converter with two-step DPWM and low power self-tracking zero current detector (ST-ZCD) is proposed. The hybrid DPWM core with high linearity and low power consumption is proposed to implement the high efficiency DPWM dc–dc converter. It is composed of a two-step delay control using the counter and delay line, where the most significant bit (MSB) of the DPWM duty value is determined by the counter based method which has high linearity and he least significant bit (LSB) of the DPWM duty value is determined by the delay line method which has low power consumption. An adaptive window ADC is proposed to reduce the output voltage ripple within 20 mV. A dead time generator is implemented with the proposed ST-ZCD to minimize the reverse current. The ST-ZCD can improve efficiency by reducing the control loss that accounts for a large proportion of the dc–dc converter under the light load current conditions. As a result, process, voltage, and temperature (PVT) characteristic and current consumption of dc–dc converter are enhanced with ST-ZCD optimized for DPWM in DCM. Also, all digital type-III compensator is implemented for the low power and small die area.

The remainder of this paper is structured as follows: Section II presents the architecture of the DPWM dc–dc buck converter. Section III explains the building blocks. In Section IV, the experimental results are discussed. Section V presents the conclusion.

II. Architecture of DPWM DC–DC Buck Converter

The conventional structure of the DPWM dc–dc buck converter is composed of a power MOSFET, external components, a gate driver, and a digital controller as shown in Fig. 1. The rectangular wave signal is generated by the DPWM to control the ON-time and OFF-time of power MOSFET switches in each switching period. The output voltage (V_{OUT}) is adjusted to the desired value. In order to obtain good performances, the three functional blocks (DPWM, compensator, and ADC) should be well-designed [9].

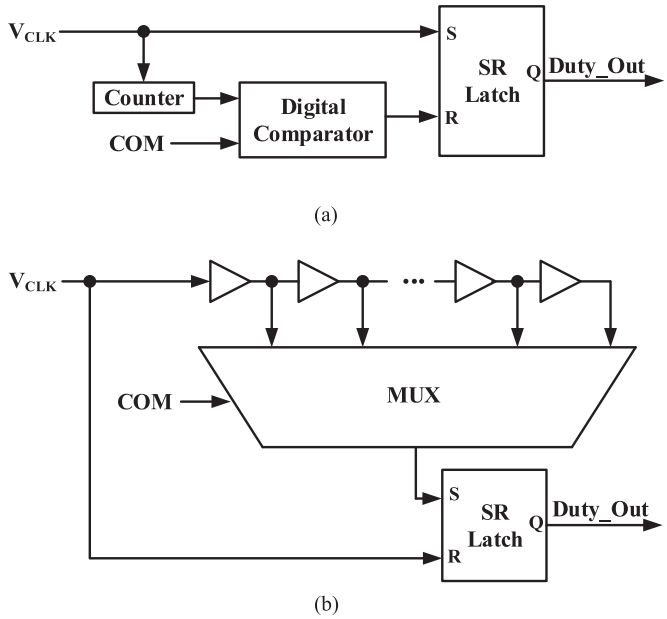


Fig. 2. Block diagram of the conventional DPWM with counter (a) and delay line based (b) method.

Fig. 2(a) and (b) shows the conventional DPWM which is composed of counter or delay line based method for controlling the duty of power MOSFET gate signals. The counter based method has good linearity and high resolution. On the other hand, frequency of clock is increased depending on number of bit. Therefore, it causes the current consumption to be increased [9]. If the delay line based method is used, there is a problem with the linearity according to PVT. In addition, if the delay line based DPWM needs to increase delay, area is increased proportionally [10].

Generally, the counter-based method requires high frequency as it demands high linearity. Therefore, it consumes a large amount of current. The counter-based method is directly dependent on the number of counter bits (n) of the counter and the switching frequency (f_{SW}) as

$$f_{\mathrm{CLK}} = 2^n \times f_{\mathrm{SW}}. \tag{1}$$

For example, if a 10-bit counter is used and f_{SW} is 2 MHz, the frequency of the oscillator (f_{CLK}) should be at least 2 GHz, which requires enormous power dissipation for the hybrid DPWM core.

In contrast, the delay line with the digital delay-locked loop (DLL) occupies a very large area as the number of bits is increased [3]. In the case of using only delay line with digital DLL, the required number ($\mathrm{DLL}_{\mathrm{NUMBER}}$) of delay lines in the DLL is related to the number of counter bits (n), as

$$\mathrm{DLL}_{\mathrm{NUMBER}} = 2^n. \tag{2}$$

Generally, the compensator in DPWM dc–dc converters is implemented by external microcontrollers, field programmable gate arrays, and compact reconfigurable input output modules [11]–[13]. Therefore, the compensator in conventional architecture has large current consumption and area.

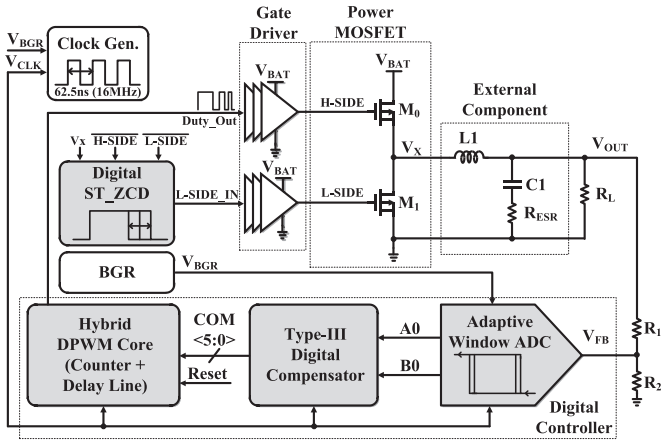


Fig. 3. Top block diagram of the DPWM dc–dc buck converter.

The resolution of ADC is related to the ripple of V_{OUT}, and higher resolution of ADC makes enhanced regulation characteristic of V_{OUT}. Ideally, the resolution of DPWM should be greater than or equal to compensator, which can be greater than or equal to ADC to avoid limit cycling. It is depicted mathematically by

$$R_{\mathrm{DPWM}} \geq R_{\mathrm{COMP}} \geq R_{\mathrm{ADC}}. \tag{3}$$

As the resolution of the ADC is increased for enhancing characteristic of V_{OUT}, current consumption and area of the ADC are increased. There is a problem that total area and complexity of DPWM are also increased for improving resolution of the compensator and DPWM with the ADC high resolution as shown in (3).

Thus, the conventional DPWM dc–dc buck converter is not suitable for light load applications due to the higher power dissipation and large area in each block and lower switching frequency that result in poor efficiency.

Fig. 3 shows the overall architecture of the proposed DPWM dc–dc buck converter. It is composed of a hybrid DPWM core, adaptive window ADC, digital ST-ZCD, type-iii digital compensator, power stage, and gate driver. The adaptive window ADC takes the feedback voltage (V_{FB}) from the output (V_{OUT}). The output of the adaptive window ADC is applied to the digital compensator, which generates the A0, B0 signals for the duty information. The type-iii digital compensator determines the delay control information (COM<5:0>) of the DPWM.

Proposed hybrid DPWM core, by mixing the counter-based method and delay line method, is designed to implement the high linearity and low power consumption. The MSB of the DPWM duty value is determined by the counter-based method which has high linearity. The LSB of the DPWM duty value is determined by the delay line method which has low power consumption. The hybrid DPWM core is proposed to implement the wide delay control range with the fine resolution. It is composed of a two-step delay control using the counter and delay line. The coarse and fine delays are implemented with the digital counter and delay line, respectively.

The resolution of the proposed DPWM dc–dc buck converter is 6-bit considering the power dissipation and area. By reducing the resolution of the hybrid DPWM core with a digital compensator and adapting a low current consumption circuit, this dc–dc converter only consumes a current of up to 130 μA. However, a high output voltage ripple can occur due to the low resolution of 6-bit [14]. To reduce the high output voltage ripple, the adaptive window ADC is proposed. A trade-off is needed between the regulation speed and the accuracy of the window ADC. Therefore, the input range of the adaptive window ADC is adaptively selected by the feedback voltage (V_{FB}) to reduce the output voltage ripple to within 20 mV. Also, the adaptive window ADC is proposed for enhancing characteristic of V_{OUT} with smaller current consumption and area by controlling reference voltage of the ADC adaptively instead of higher resolution.

The proposed compensator is implemented with the type-III digital compensator considering the phase margin and crossover frequency in the digital domain by the Tustin's method, so its current consumption and area are minimized.

The proposed DPWM dc–dc buck converter does not need the dead-time generator to prevent the leakage current when the p-channel MOSFET (PMOS) and n-channel MOSFET (NMOS) are turned ON at the same time. The ST-ZCD is proposed to replace the conventional dead-time generator.

The conventional ZCD has a large power consumption to sense the zero inductor current point using the high performance comparator. In addition, the comparator in the conventional ZCD has the voltage offset and is sensitive to the PVT variations [8]. The ST-ZCD senses the pulse of the high side duty, low side duty, and V_X node without using comparators to reduce the current consumption. The ST-ZCD controls the NMOS duty so that it follows the fine duty. The ST-ZCD prevents the reverse current and minimizes the operating current.

The low power consumption DPWM dc–dc buck converter is proposed which is composed of a hybrid DPWM core, adaptive window ADC, digital ST-ZCD, type-III digital compensator, power stage, and gate driver. This proposed scheme can reduce the output voltage ripple and the power dissipation increasing the power conversion efficiency.

III. Building Blocks

A. Hybrid DPWM Core

Fig. 4 shows the hybrid DPWM core circuit. The hybrid DPWM core generates the duty of the DPWM dc–dc buck converter following the resolution of DPWM. This block ultimately determines the resolution of the DPWM dc–dc buck converter. The resolution of an analog dc–dc buck converter is very fine, whereas that of the digital dc–dc converter is limited. Therefore, the accurate duty is one of the most important characteristics in the digital dc–dc converter. The proposed hybrid DPWM core is composed of a counter and a delay line using a digital DLL-based method.

The overall structure is similar to that in [14], but the delay cells have an adjustable delay as shown in Fig. 4. The counter-based method can achieve high accuracy based on linearity, but the operating frequency is dominated by the number of counter bits. It increases the current dissipation. The delay line with digital DLL methods consumes less current than the counter-

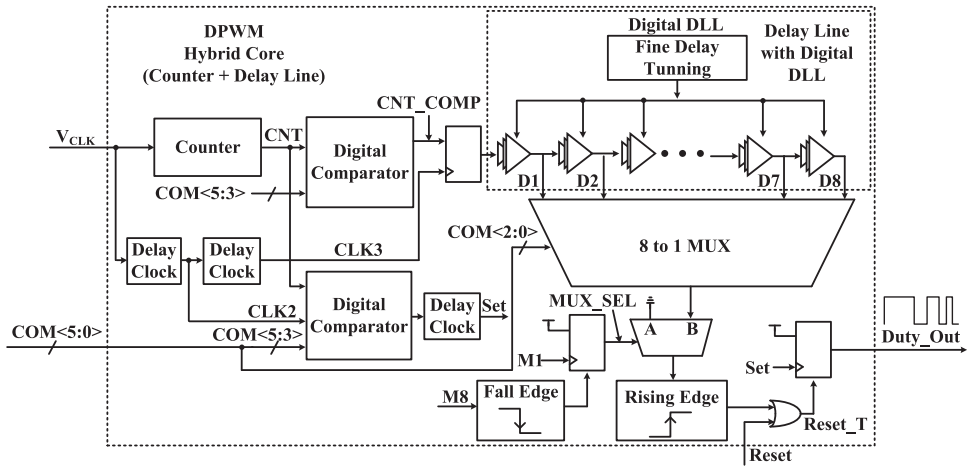


Fig. 4. Block diagram of the hybrid DPWM core.

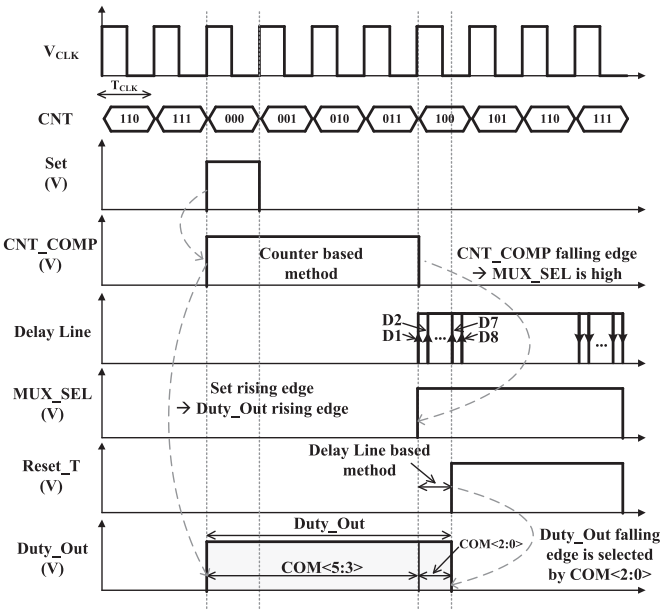


Fig. 5. Timing diagram of the hybrid DPWM core.

based method, but this method also has a disadvantage. With the counter-based method, when the number of bits is increased by one bit, the active area is doubled. Therefore, the hybrid DPWM core can overcome this disadvantage by combining the counter-based method with the delay line method. The resolution of the proposed DPWM dc–dc buck converter is 6-bit considering the power dissipation and area.

Fig. 5 shows a timing diagram of the hybrid DPWM core. Duty_Out is the time interval between the rising edges of Set and Reset_T signals and it is controlled by the counter based on the MSB 3-bit (COM<5:3>) and LSB 3-bit (COM<2:0>) from the delay line with the digital DLL. The counter measures the cycles of the 16 MHz clock from 0 to 7. This counter value generates the total duty signal compared with the MSB 3-bit (COM<5:3>) in the digital comparator. The resolution of the delay line with digital DLL is decided by LSB 3-bit (COM<2:0>) for selecting the number of unit delays to generate the fine duty, Duty_Out. The delay control block is fed back to match the period of the delay cell. The delay signal (M1–M7) is compared with the output signals of the delay cells to match the fine duty. The output signals are continually changed to reduce any error duty.

B. Adaptive Window ADC

Fig. 6 shows the circuit of the adaptive window ADC. To implement a fast operation with low power dissipation, a flash ADC type is used with two high speed comparators which minimize the effect of the offset and noise. The adaptive window ADC compares the band gap reference (V_{BGR}) designed according to the concept in [15] with 460 mV, with the output sensed by the feedback voltage signal (V_{FB}) to separate the error code. The size of the window is a dominant factor for the regulation speed and accuracy.

If a small window size is selected, the accuracy of the output voltage is improved, although the regulation speed becomes slow and operates abnormally. Therefore, the adaptive window ADC is used to optimize the window size following the output signal.

For the first time, the V_{FB} input signal is compared with $V_{\mathrm{REF\_H1}}$ and $V_{\mathrm{REF\_L2}}$ and it generates 2-bit error signals with values of 00, 01, and 11 which are stored in the shift register. The shift register is synchronized with the reference clock signal V_{CLK}.

Fig. 7 shows the timing diagram of the adaptive window ADC. If the AD signal is turned OFF, $V_{\mathrm{REF\_H1}}$ and $V_{\mathrm{REF\_L1}}$ are selected and a high output voltage ripple of up to 50 mV is obtained. On the other hand, if the AD signal is turned ON, the compared voltages $V_{\mathrm{REF\_H2}}$ and $V_{\mathrm{REF\_L2}}$ are selected to reduce the window size and limit the output voltage ripple by up to 20 mV after two clocks. The AD signal controls the 2x1 MUX to select the window size. The 6-bit output of adaptive window ADC is the input of the digital compensator for matching.

C. Digital Self-Tracking Zero Current Detector (ST-ZCD)

The conventional ZCD structure senses the zero current through the internal switching (V_X) node; it has a voltage drop

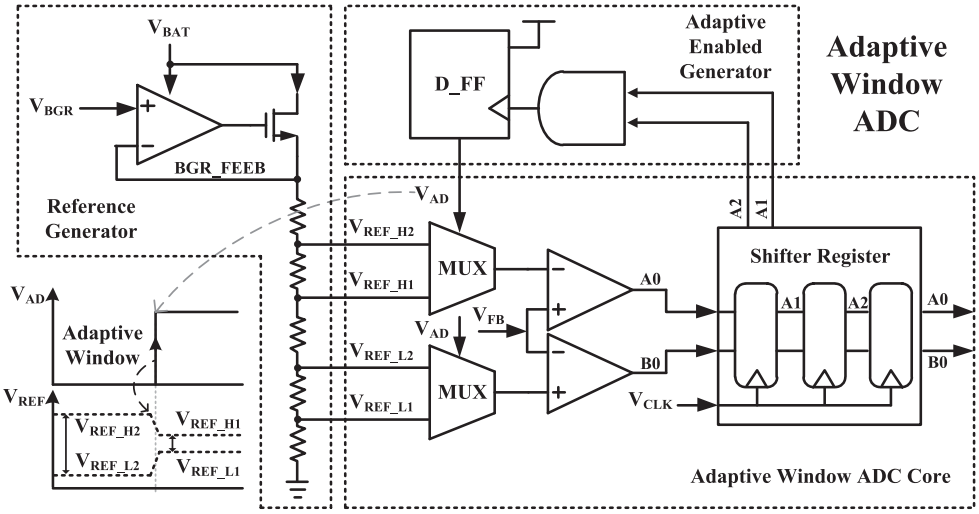


Fig. 6. Block diagram of adaptive window ADC.

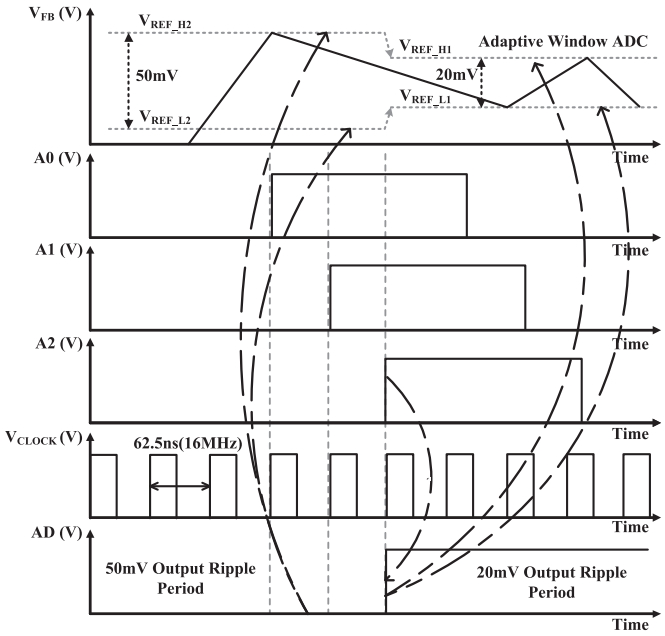


Fig. 7. Timing diagram of adaptive window ADC.

caused by the resistance component of the power MOSFET. Also, the power consumption required by the conventional ZCD to sense the point of the zero inductor current using the high performance comparator is considerable [8].

Fig. 8 shows a block diagram of the proposed digital ST-ZCD. The current consumption of the digital ST-ZCD is 10 μA, which is smaller than that of the conventional ZCD. Therefore, the digital ST-ZCD can improve efficiency by reducing the control loss that accounts for a large proportion of the DCM dc–dc converter under light load current conditions. It is also possible to prevent the efficiency reduction due to ZCD timing errors caused by the comparator offset. Also, the detection timing error of the digital ST-ZCD does not cause instability or malfunction under the PVT variations, even though it is larger than the resolution of the digitally controllable pulse generator.

In the proposed digital ST-ZCD, the comparator is not used when it detects the point at which the inductor current is 0 A. On the other hand, the digital ST-ZCD detects the inductor current indirectly at the time of the switch OFF in the previous period while monitoring the V_X node voltage for the NMOS switching at every cycle. If an NMOS switch is quickly turned OFF, the energizing current in the inductor must de-energize through the NMOS diode conduction. In this case, the value (S1, S2) which is made from a flip-flop with V_X and DELAY_1 or DELAY_2 is (0, 0). If (S1, S2) is (0, 0), the input of the UP/DOWN counter of the digital ST-ZCD circuit is the UP signal. The pulse width of the L-SIDE_IN signal is increased as the output signal of the UP/DOWN counter, DUTY_CONT<7:0>, is increased.

In contrast, if the NMOS switch is turned OFF late, (S1, S2) is (1, 1). In this case, the inductor energizing current must be de-energized through the PMOS diode conduction when NMOS is turned OFF, and the DN signal is made for the input of the UP/DOWN counter. The pulse width of the L-SIDE_IN signal is decreased as the output signal of the UP/DOWN counter, DUTY_CONT<7:0>, is decreased. Through the operation of the digital ST-ZCD, when the digitally controllable pulse generator is thereby generating a suitable pulse width values, the signals (S1, S2) are (0,1) by a flip-flop. In this case, since the STAY signal is made for the input of the UP/DOWN counter, the pulse width of the L-SIDE_IN is fixed by the DUTY_CONT<7:0> signals.

The ST-ZCD senses V_X node continuously with DELAY_1 and DELAY_2 signals also after lock state. So, if (S1, S2) value is changed by the load condition or PVT variations, the ST-ZCD detects when inductor current is 0 A with duty control of L-SIDE and UP/DOWN counter similar to the way mentioned before. As a result, the ST-ZCD keeps STAY state independent of environmental changes with the zero current sensing through continuous sensing (S1, S2) signals.

Fig. 9 shows the state diagram of the digital ST-ZCD. When the digital ST-ZCD starts to operate, the pulse width of the NMOS switch gate control signal is controlled by the UP/DN/STAY signals.

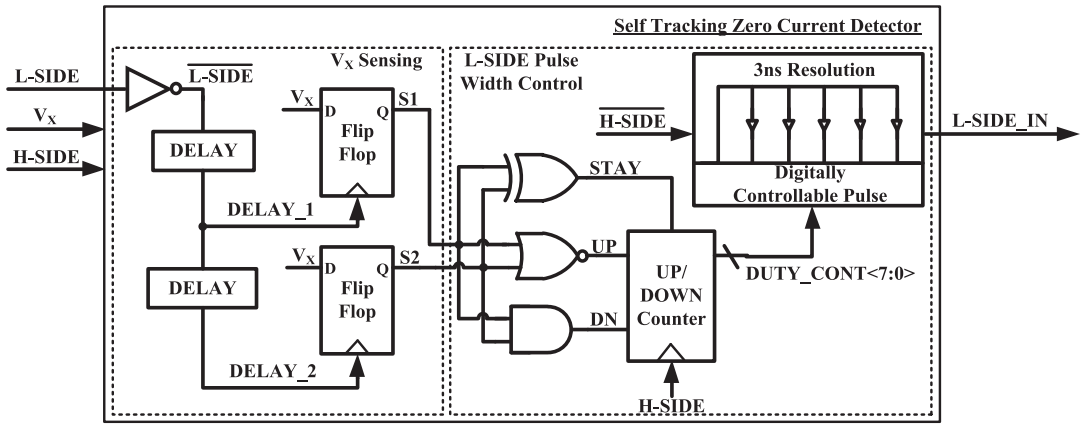


Fig. 8. Block diagram of the digital ST-ZCD.

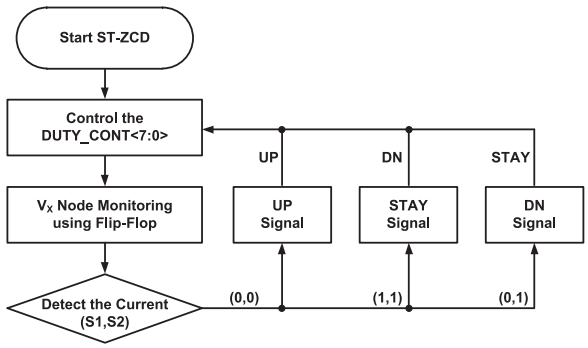


Fig. 9. State diagram of digital ST-ZCD.

The NMOS switch turns OFF and after a certain amount of delay, the inductor current is detected by monitoring the V_X using flip-flop. The digital ST-ZCD determines whether to increase or decrease the pulse width of the NMOS switch gate control signal through the detecting inductor current. When the detected inductor current is 0 A, the NMOS switch does not have diode conduction. Therefore, the digital ST-ZCD generates the STAY signal, and the digital ST-ZCD then operates in the locked state.

Fig. 10 shows the timing diagram of the digital ST-ZCD according to the state. In the case shown in Fig. 10(a) and (b), due to the diode conduction, the efficiency of the dc–dc converter is reduced. In particular, in Fig. 10(b), the reverse current decreases the output ripple characteristics as well as the efficiency. As seen in Fig. 10(a) and (b), the direction of the inductor current is in accordance with the direction of the energizing current. Consequently, the diode conduction is positive (+) if it is through NMOS and negative (–) if it is through PMOS. The V_X voltage immediately drops to less than 0 V if the NMOS switch is turned OFF when the NMOS diode conduction occurs. Alternatively, when the PMOS diode conduction occurs, V_X voltage increases to a voltage higher than the input voltage V_{IN}.

When the digitally controllable pulse generator is thereby generating a suitable pulse width values in Fig. 10(c) waveform, the signals (S1, S2) are (0,1) by a flip-flop. If the value of (S1, S2) is (0, 1), the signal is sent to the UP/DOWN counter and the pulse width of the NMOS is fixed. When the switch pulse width of the dc–dc buck converter reaches the steady state, the digital ST-ZCD exports the NMOS switch pulse with the "ON" time pulse width at which the inductor current is constant at 0 A. The DCM operation of the dc–dc buck converter can obtain maximum efficiency when the NMOS switch is "OFF" at the time at which the inductor current is 0 A as shown in Fig. 10(c).

D. Type-III Digital Compensator

In this paper, the type-III digital compensator is proposed to reduce the current consumption and area. By designing type-III compensator as all digital, low power and low area can be realized. Type-III compensation is used to improve the transient response, and to boost the crossover frequency, and phase margin. It guarantees the targeted bandwidth and phase margin, as well as an unconditionally stable control loop [15].

The digital compensator improves the accuracy of the output voltage through increase in the dc gain of the dc–dc converter close-loop transfer function, and it ensures the stability by compensating the pole location of the dc–dc converter. It also compensates the pole/zero location by the output filter of the dc–dc converter.

In this paper, the digital compensator has the 2-bit input from the adaptive window ADC, and the 6-bit output to the hybrid DPWM core. As described in Section II, the characteristic of the output voltage ripple is improved as the resolution of the compensator increases. On the other hand, the area and current of the dc–dc converter are increased since the resolution of the DPWM and ADC increases. The type-III digital compensator is implemented using the 6-bit resolution to realize the small area and low current consumption in this paper, and the DPWM dc–dc converter with an enhanced characteristic of the output voltage and high stability is designed using the adaptive window ADC.

In the proposed type-III digital compensator approach, the analog compensator is designed with the required phase margin and crossover frequency in the s-domain. Once the design is verified, it is ready for its conversion to the digital domain (z-domain) for which Tustin's method is used. The type-III analog compensator s-domain transfer function for a gain of 13 dB and

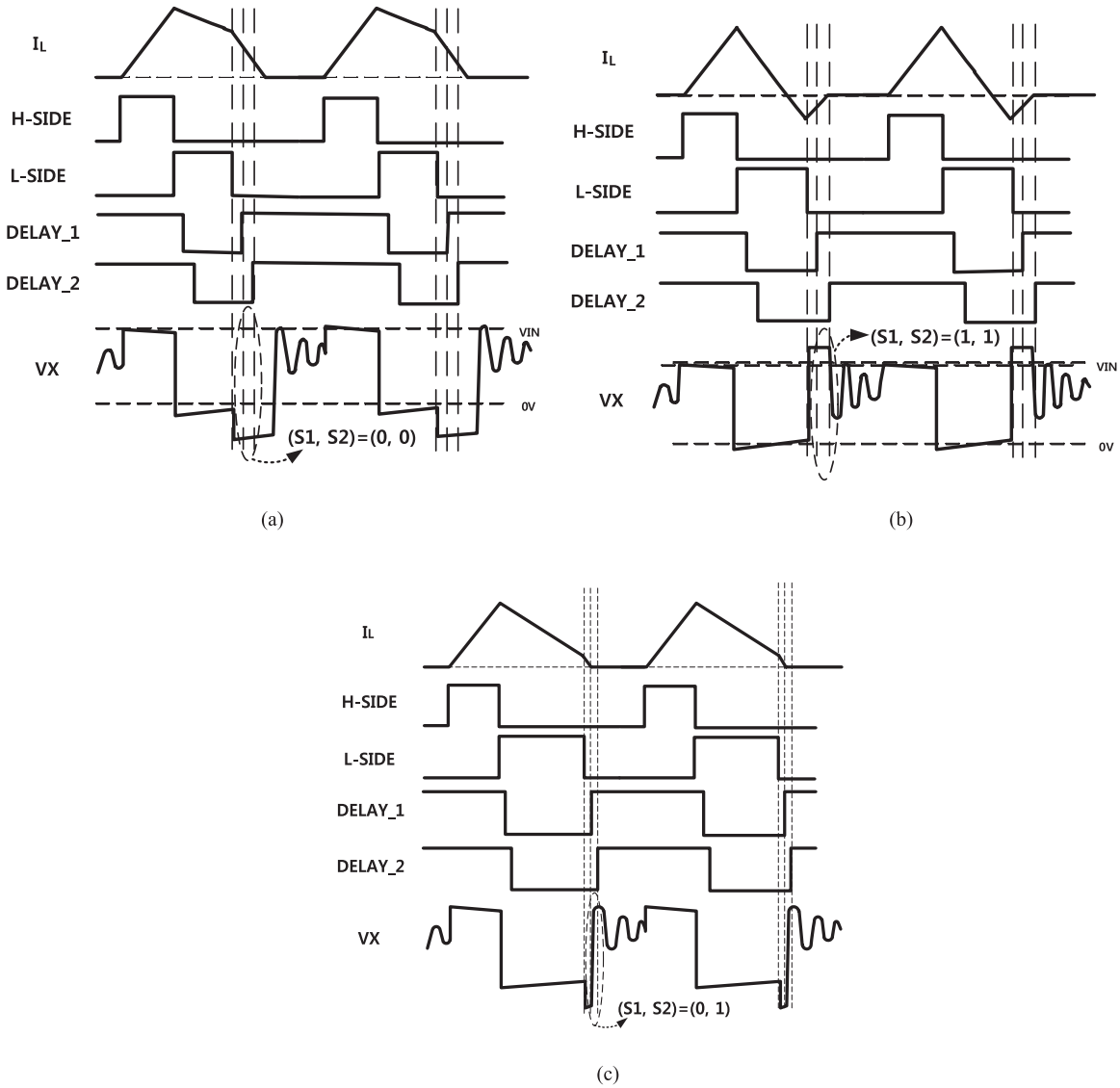


Fig. 10. Timing diagram of the digital ST-ZCD at (a) UP state, (b) DN state, and (c) STAY.

a phase margin of 55° is given as

$$H(s) = \frac{6.30707\mathrm{e}^{-10}s^2 + 5.02277\mathrm{e}^{-5}s + 1}{3.51537\mathrm{e}^{-16}s^3 + 5.0498\mathrm{e}^{-11}s^2 + 1.8135\mathrm{e}^{-6}s}. \quad (4)$$

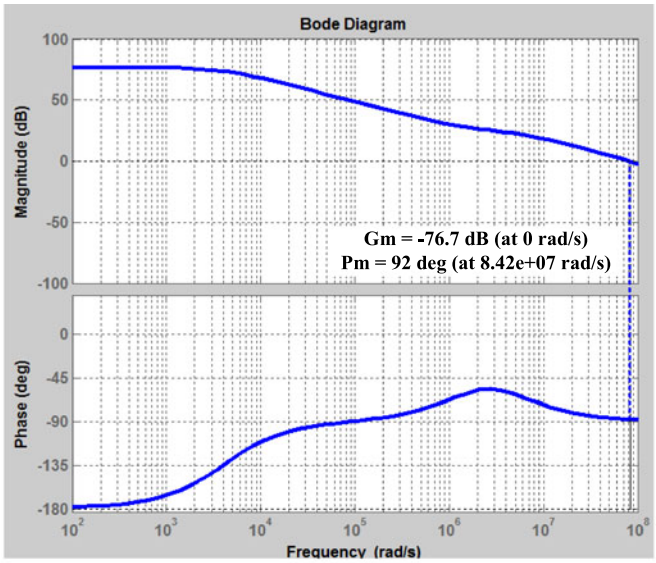
The generalized form of the digital compensator z-transfer function is given as

$$H(z) = \frac{b_0 z^N + b_1 z^{N-1} + Lb_N}{a_0 z^N + a_1 z^{N-1} + La_N} \quad (5)$$

where *N* is the order of the system, $b_0 \ldots b_N$ is the coefficients of the numerator, and $a_0 \ldots a_N$ is the coefficients of the denominator. The obtained third-order discrete-transfer function is given as

$$H(z) = \frac{0.441z^{-3} - 0.441z^{-2} - 0.424z^{-1} + 0.441}{-0.930z^{-3} - 2.860z^{-2} - 2.929z^{-1} + 1}. \quad (6)$$

Bilinear transformation [16], [17] and Tustin's method [18] are used to convert the transfer function from the s domain to the z domain. Tustin's method and the pole-zero match are very useful methods. The controller is initially designed in the s-domain and fulfills the criteria for stability, i.e., all of the poles are on the left half of the s-plan. The poles on the z-plan are inside the unit circle to ensure stability, as shown in Fig. 11(a) and (b). The location of the three poles P1, P2, and P3 is as follows: P1 [1 + 0i], [0.9647 + 0.0011i], and [0.9647 – 0.0011i]. The phase margin in the z-domain is 92°. The magnitude and phase are shown in Fig. 11(a), and the pole-zero location is shown in Fig. 11(b). Since the type-III digital compensator is designed considering the inductor of 3 μH, capacitor of 3 μF used as the output filter under the input voltage range of 1.5–3 V, and load current conditions of 1–10 mA, it can be confirmed that the loop phase margin of the DPWM dc–dc converter is 92° and sufficient stability is ensured as shown in Fig. 11(b). In



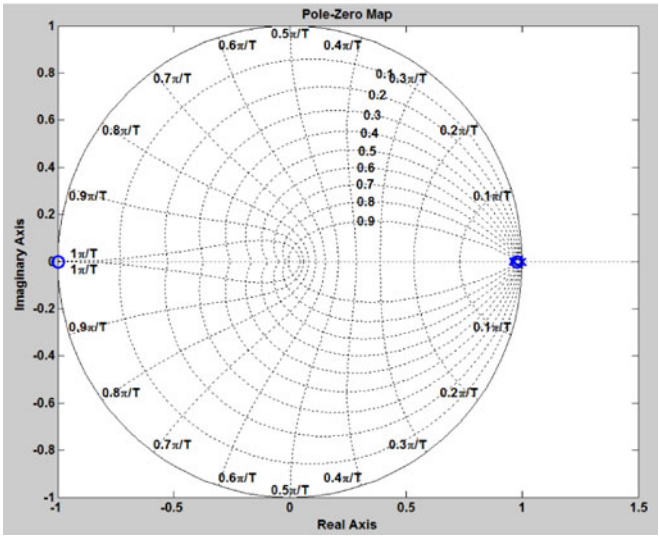


Fig. 11. (a) Magnitude and phase of the digital controller, and (b) pole-zero locations on z-plan ($1 + 0i$, $0.9647 + 0.0011i$, $0.9647 - 0.0011$i).

addition, the pole/zero locations of the z-domain which must be considered in the digital compensator are all within the stability as shown in Fig. 11(b).

IV. Experimental Results

Fig. 12 shows the chip microphotograph. The chip is fabricated using a 55 nm CMOS process with a single poly layer, four layers of metal, metal–insulator–metal capacitors, and high sheet resistance poly resistors. The die area of the DPWM dc–dc buck converter is 500 μm $\times$ 300 μm.

Fig. 13 shows the simulation results of the DPWM dc–dc buck converter. In the start-up sequence with open-loop, the initial voltage is generated. The DPWM dc–dc buck converter is then switched to close-loop, and is operated in the DPWM mode. The output voltage (V_{OUT}) of the DPWM dc–dc buck converter

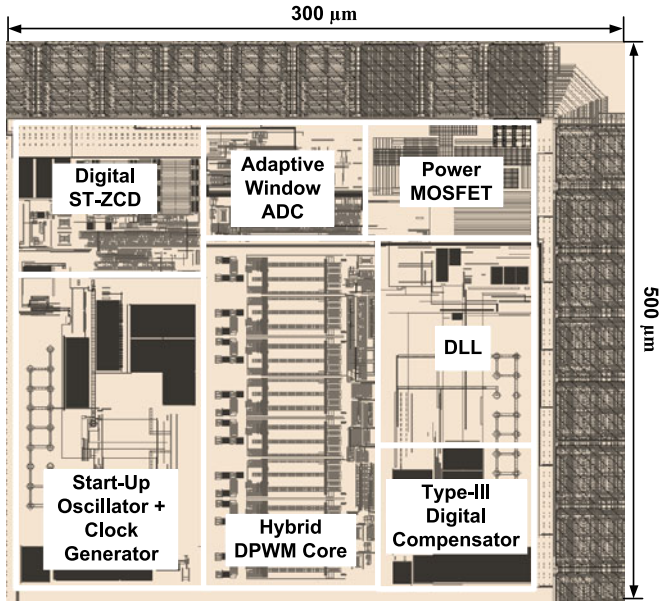


Fig. 12. Chip microphotograph of the DPWM dc–dc buck converter.

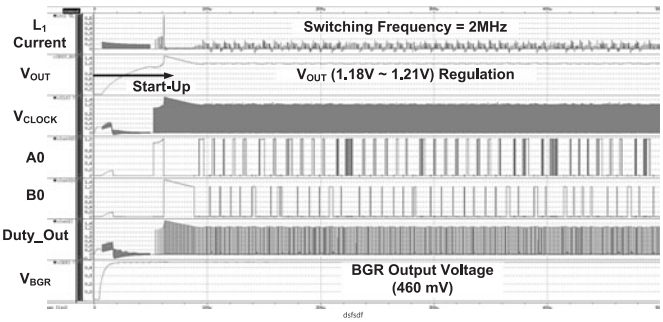


Fig. 13. Top simulation results of the dc–dc buck converter.

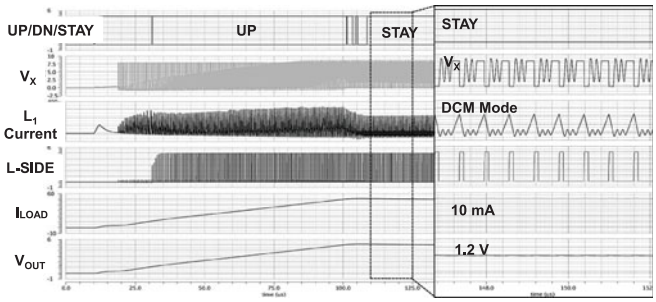


Fig. 14. Digital ST-ZCD simulation results of the dc–dc buck converter.

operation is in accordance with that of regulation output voltage of 1.2 V. The output ripple voltage is approximately 20 mV. The load current condition is 10 mA. The switching frequency of the DPWM dc–dc buck converter is 2 MHz.

Fig. 14 shows the simulation results in the DCM region when the load current is 10 mA. The UP, DN, and STAY signals are generated repeatedly by sensing the instant when V_X is zero by digital ST-ZCD.

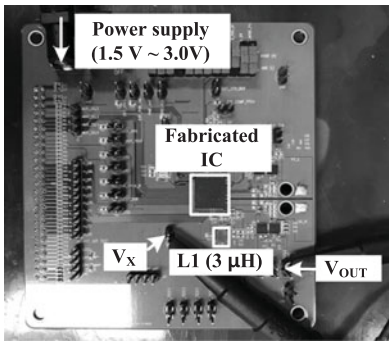


Fig. 15. Measurement environment of the DPWM dc–dc buck converter.

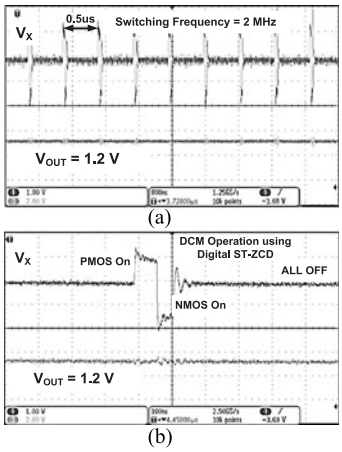


Fig. 16. Measured waveform of the DPWM dc–dc buck converter at (a) DPWM operation using digital ST-ZCD and (b) zoom measurement result.

The information reflects the output of the low side driver, the L-SIDE signal, which is one of the critical signals for the DCM region. As digital ST-ZCD converges to the steady state, the STAY signal continues to minimize the high side and low side conduction losses due to the voltage at V_X node. The output voltage of the DPWM dc–dc buck converter, V_{OUT}, settles to 1.2 V.

The measurement environment of the DPWM dc–dc buck converter is illustrated in Fig. 15. The test board is composed of a test port for the IC measurement. In the test board, the DPWM operation and regulation characteristics are measured through the output voltage of the DPWM dc–dc buck converter and the inductor V_X voltage by applying an external power supply of 1.5–3 V.

Fig. 16(a) shows the measured waveform of the DPWM dc–dc buck converter, illustrating the internal V_X node and output voltage (V_{OUT}) at the switching frequency of 2 MHz. Fig. 16(b) shows the magnified waveform, illustrating the operation of digital ST-ZCD in more detail. It shows the digital ST-ZCD in the normal DPWM, which detects the point at which the inductor current is zero and turns OFF the NMOS. Therefore, it can prevent the reverse current and the NMOS is turned OFF without the diode conduction of NMOS and PMOS as shown in Fig. 16(b).

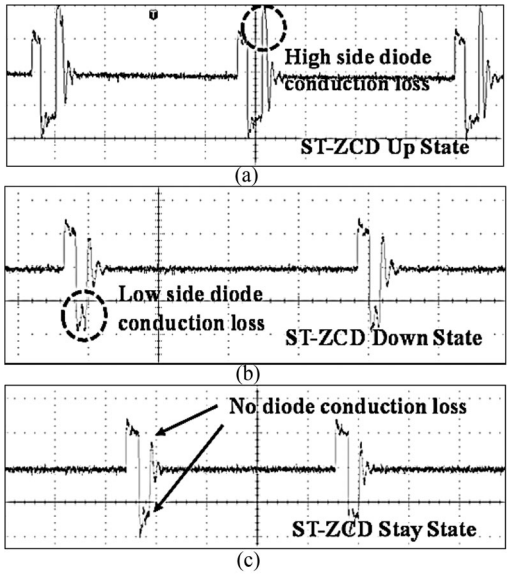


Fig. 17. Measured waveform of ST_ZCD (a) UP state, (b) DOWN state, and (c) STAY state.

TABLE I
ANALYSIS OF THE POWER LOSSES OF THE DPWM DC–DC BUCK CONVERTER

	Power losses (%)			
Supply Power	1.5 V	2.0 V	2.5 V	3.0 V
Hybrid DPWM Core	0.17	0.22	0.27	0.31
Type-III Digital Compensator	0.11	0.14	0.18	0.21
Adaptive Window ADC	0.17	0.22	0.27	0.31
Digital ST_ZCD	0.11	0.14	0.18	0.21
Clock Generator	0.57	0.73	0.90	1.05
Gate Driver	0.34	0.44	0.54	0.63
Total circuit consumption	1.47	1.89	2.34	2.72
Measured Conduction losses	4.38	7.03	8.06	9.38
Measured Switching losses	2.65	2.78	3.00	3.40
Measured Efficiency (%)	91.5	88.3	86.6	84.5

Fig. 17(a)–(c) shows the operation of digital ST-ZCD. In Fig. 17(a) and (b), high side diode conduction loss and low side diode conduction loss occur since the digital ST-ZCD is turned OFF earlier and later than the optimum timing, respectively. Fig. 17(c) shows the normal operation of digital ST-ZCD, where no high side and low side diode conduction losses occur at the STAY state after repeating the UP and DOWN states.

Table I presents the analysis of the power losses of the DPWM dc–dc buck converter. Load current is 10 mA and supply voltage is 1.5–3.0 V for simulation and measurement conditions. Hybrid DPWM core, type-III digital compensator, adaptive window ADC, digital ST-ZCD, clock generator, and gate driver blocks are checked with simulation results. The total current consumption is 130 μA in simulation and measurement. The power loss in circuits with respect to the supply voltage is 1.47–2.72%.

Fig. 18(a) shows the measured efficiency of the proposed DPWM dc–dc buck converter with respect to load current when the input voltage of the DPWM dc–dc buck converter is 3 V. The peak efficiency is 84.5% when the load current is 10 mA. Fig. 18(b) shows the measured efficiency of the pro-

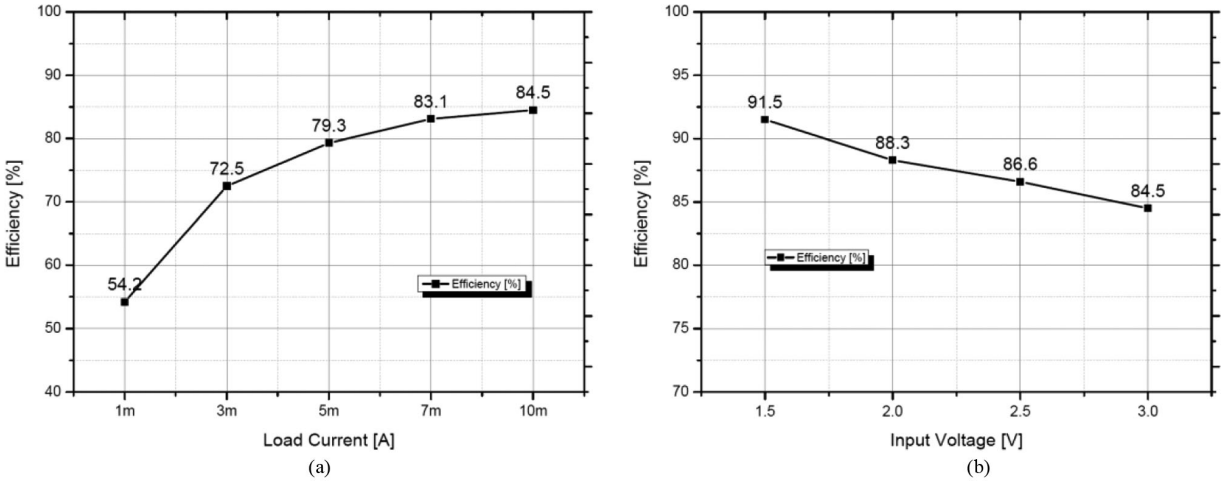


Fig. 18. Measured efficiency of dc–dc buck converter with respect to (a) load current and (b) input voltage.

TABLE II
PERFORMANCE COMPARISON OF THE DPWM DC–DC BUCK CONVERTER WITH PRIOR WORKS

Reference	[5] ISSCC 07	[21] JSSC 11	[22] ISSCC 10	[23] JSSC 11	This Work
Technology	0.18 μm CMOS	45 nm CMOS	40 nm CMOS	0.13 μm CMOS	55 nm CMOS
Operating Mode	DPWM	PWM	DPWM	PWM	DPWM
Peak Efficiency (%)	93.2	87.4	90	90	91.5
Operation Frequency	5 MHz	2 MHz	3.125 MHz	7 kHz to 5 MHz	2 MHz
Input Voltage Range (V)	2.9–3.3	2.8–4.2	0–3.3	1.8	1.5–3
Load Current (A)	10–450 m	20 μ to 100 m	–	700 n to 107 μ	1–10 m
Output Voltage (V)	1.0–1.7	0.4–1.2	0.1–3.3	0.575–1	1.2
Die Area (mm^2)	0.6	2.25	0.7	–	0.15
Inductor / Capacitor	1 μH/10 μF	10 μH/2 μF	2.2 μH/10 μF	–	3 μH/3μF

posed DPWM dc–dc buck converter with respect to the input voltage when the load current is 10 mA. The peak efficiency is 91.5% when the input voltage is 1.5 V.

Table II shows the performance comparison of the DPWM dc–dc buck converter with prior works. The proposed dc–dc buck converter has the best overall efficiency under 10 mA load current condition. Also, the capacitor value and die area are smaller than those of [5], [21], [22], and [23].

V. CONCLUSION

A high efficiency DPWM dc–dc buck converter and low power digital ST-ZCD are proposed for IoT and ultralow power applications. The hybrid DPWM core with high linearity and low power consumption is proposed to implement the high efficiency DPWM dc–dc converter. It is composed of a two-step delay control using the counter and delay line, where the MSB of the DPWM duty value is determined by the counter-based method which has high linearity and the LSB of the DPWM duty value is determined by the delay line method which has low power consumption. An adaptive window ADC is proposed to reduce the output voltage ripple within 20 mV. A dead time generator is implemented with the proposed ST-ZCD to minimize the reverse current. The ST-ZCD can improve efficiency by reducing the control loss that accounts for a large proportion of the dc–dc converter under the light load current conditions. Also, all digital type-III compensator is implemented for the low power and small die area.

This chip is fabricated with a 55 nm CMOS process, which uses the standard supply voltage of 1.5–3 V to generate the output voltage of 1.2 V. The total active area is 500 μm $\times$ 300 μm. The measured peak efficiency of the DPWM dc–dc buck converter is 91.5% with a quiescent current consuming only 130 μA.

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