Design, Control, and Analysis of a Fault-Tolerant Soft-Switching DC–DC Converter for High-Power High-Voltage Applications

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***Abstract*—A modular isolated soft-switching dc–dc converter that can offer two levels of fault tolerance is proposed. A typical application is the wind energy conversion system used in offshore series-dc wind farm concept. The converter consists of input-parallel-output-series (IPOS) connected modules. Each module is a full-bridge dc–dc converter with an active rectifier, which can achieve zero voltage switching for all primary side switches and zero current switching for all secondary side switches and diodes. Under normal operation, the converter is operated with secondary phase-shifted modulation. When tolerable fault occurs in certain module, reconfiguration method ensures uninterrupted operation for the system. Additionally, modular structure provides another level of fault tolerance. More benefits of IPOS structure include reduced input current and output voltage of each module, module shedding capability, reduced ripple content due to interleaving, intrinsic balancing, and scalable control method. Both normal and faulty operations are simulated and also verified by scaled-down prototype experiment.**

***Index Terms*—DC–DC power converters, fault tolerance, interleaving, zero current switching (ZCS), zero voltage switching (ZVS).**

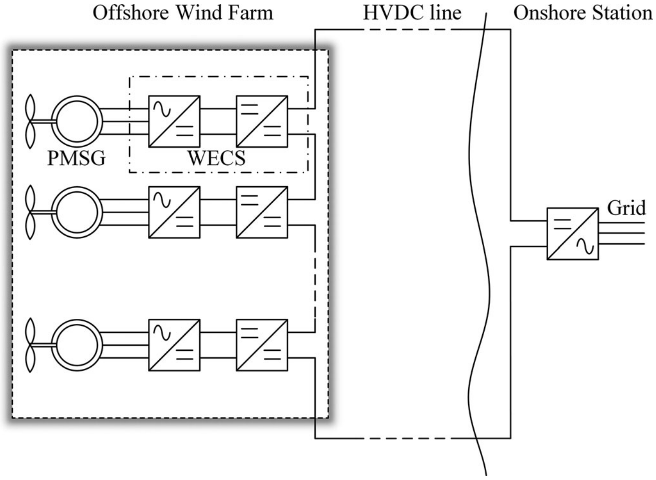

Fig. 1. Series-dc wind farm.

I. INTRODUCTION

RENEWABLE energy research has received a lot of attention with the growing concern for challenges such as global warming and fossil fuel depletion. Wind energy is one of the most mature forms of renewable energy. Global cumulative installed wind capacity passed 369 GW at the end of 2014, and is projected to reach 666 GW by 2019 [1]. Offshore wind farms generally enjoy stronger and more consistent wind velocity, arouse less acoustic pollution concern, and are adjacent to major demand centers. Though operational offshore wind generation is only about 12 GW, a total capacity of nearly 250 GW is announced globally [1], [2]. With the increasing distance from wind farm to shore, traditional HVac transmission system will suffer from substantial loss in cables. Comparatively, HVdc transmission system would only have 50%–70% of cable loss [3]. Therefore, HVdc solution may have lower overall loss for remote wind farms. The overall economical break point is around 100 km. A major part of cost goes to the offshore platforms, which are usually much costlier for HVdc than for HVac systems [4]. One solution is the series-dc based wind farm shown in Fig. 1 [5]–[13]. The output of permanent magnet synchronous generator (PMSG) is converted by the wind energy conversion system (WECS). Then, the dc outputs of WECS are series connected to reach HVdc voltage level. Each WECS can be installed locally at the wind turbine, thus eliminating the need for substation platform.

DC–DC converter is the key component in WECS as it needs to ensure continuous current flow in the HVdc line. Moreover, fault tolerance is highly desired for dc–dc converter, especially for high-power high-voltage applications such as offshore wind farm. One major reason for converter failure is semiconductor device malfunction, i.e., short-circuit fault (SCF) and open-circuit fault (OCF) [14], [15]. SCF is usually caused by wrong gate voltage or intrinsic failure. SCF can lead to shoot-through fault and consequently damage other parts of the system. Therefore, in many commercially available drivers, the detection and protection of SCF is a standard built-in feature [16]. An OCF may happen due to lifting of bonding wires, driver fault or

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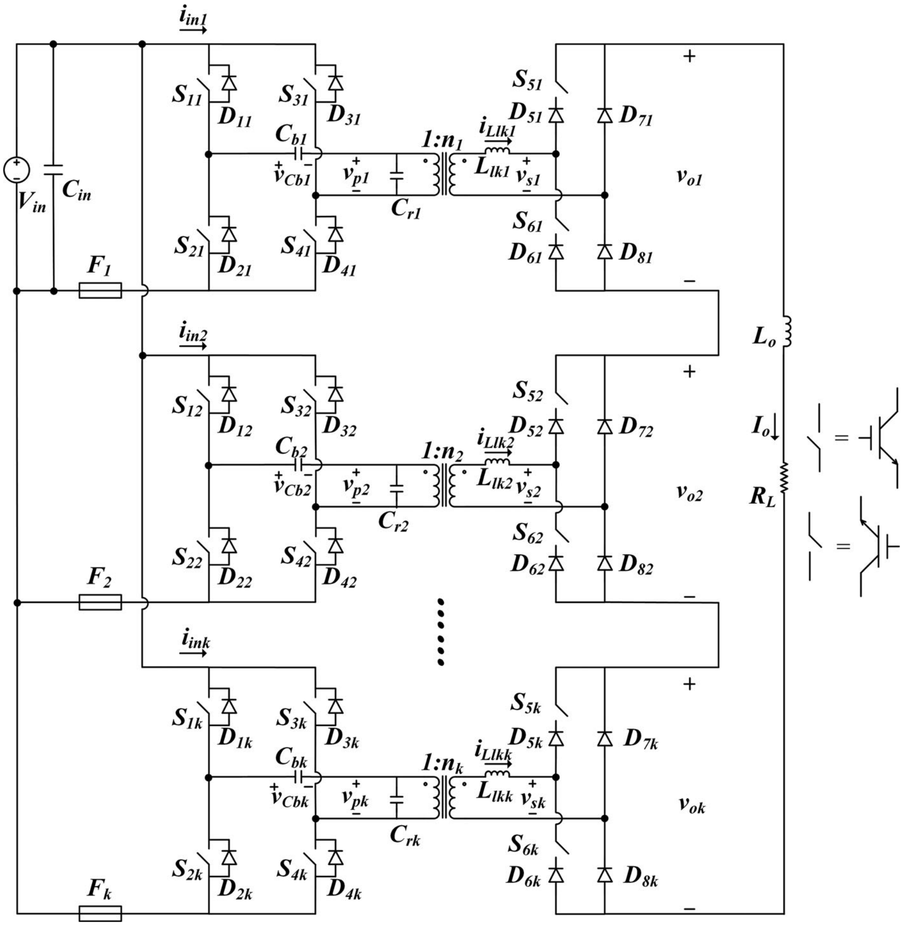

Fig. 2. Proposed IPOS SPS-FB converter.

SCF-induced insulated-gate bipolar transistor (IGBT) rupture. Unlike SCF, OCF typically will not cause abrupt system failure. Nevertheless, OCF will cause dc voltage offset, which leads to reduced performance, transformer saturation, and higher voltage stress on healthy switches.

Fault-tolerant control strategy usually includes three subtasks: fault detection, fault identification/location, and reconfiguration action [14]. In [15], fault diagnosis and protection methods are reviewed for SCF and gate driver induced OCF of IGBTs in inverters. More recently, Zhang *et al.* [17] categorized converter fault-tolerant techniques into switch-level, leg-level, module-level, and system-level. However, the surveys are focused on fault-tolerant techniques developed for inverters. Many methods are not applicable to dc–dc converters as information from Park's transformation or space vectors are utilized. A nonisolated multilevel modular capacitor-clamped dc–dc converter and corresponding fault-tolerant method is proposed in [18]. Redundant modules in offline mode are required by the proposed method. Both SCF and OCF tolerance for an H-bridge with auxiliary leg and selector cells converter are achieved at the cost of many voltage/current sensors as well as one auxiliary leg [19]. Jamshidpour *et al.* [20] proposed a fault-tolerant strategy based on monitoring inductor current slope that can detect both SCF and OCF in less than one switching cycle for simple boost converter. However, aforementioned converters are not suitable for high-power application such as series-dc wind farm. Fault detection method based on monitoring flying capacitor voltage of three-level parallel resonant converter is presented in [21]. Nevertheless, neither fault identification nor reconfiguration action is discussed. A general fault detection and identification method for both SCF and OCF in most pulse width modulation converters is proposed in [14]. This method compares the measured magnetic component voltage with the theoretical voltage calculated based on gate signals. However, as instantaneous values are used, switch turn-on delay and inevitable measurement delays may cause false alarm. The pulse shapes of dc-link current are used to detect both SCF and OCF for a full-bridge zero voltage switching (ZVS) converter in [22]. The method does not require high-resolution A/D converter, but cannot provide fault identification and reconfiguration.

Phase-shift full-bridge (PSFB) converter featuring inductive output filtering is found in many literature works targeting series-dc wind farm application [7], [9]. Pei *et al.* proposed an OCF-tolerant strategy for the PSFB converter [16]. The averaged voltage across transformer primary winding is used as fault indicator. After the fault is detected, phase shift is set at 0.5 in order to obtain more information from transformer voltage level and pinpoint the OCF switch.

Comparatively, the dc–dc converter studied in this paper is based on IPOS connected secondary phase-shifted full-bridge

(SPS-FB) converter. ZVS is achieved for all primary switches and zero current switching (ZCS) is achieved for all secondary switches and diodes. Compared to PSFB converter, the SPS-FB converter has larger soft-switching range, less circulating current and diode reverse recovery current [23]–[25]. The main focus is to develop corresponding fault-tolerant strategy using voltages across dc blocking capacitor and lower switches. The converter can provide both switch-level and module-level fault tolerance. Switch-level fault tolerance can deal with an OCF of any switch and SCF at secondary switches, allowing the faulty module to operate at reduced performance. When other faults occur, module-level tolerance can isolate the faulty module without disrupting the operation of healthy modules. Soft-switching can be retained in post-fault operation. The fault induced output voltage/current dip can be compensated by healthy modules without additional boosting stage.

The paper is organized as follows. Section II presents the topology of the proposed converter and its healthy operation. The advantages of IPOS structure are also explained. Section III analyzes different fault scenarios and develops the fault detection, identification, and reconfiguration methods. Simulation and experimental setup, results, and discussion are presented in Section IV. Finally, Section V concludes this paper.

II. Converter Topology

The schematic drawing of proposed converter is shown in Fig. 2. Each building block is an SPS-FB converter that achieves ZVS for primary switches and ZCS for secondary switches and diodes. The converter is suitable for series-dc wind farm application. The converter takes a voltage input, which can be easily obtained from three-phase voltage source converter or diode rectifier bridge. The output is designed to be a current source and interface with current source converters. Thus, there is no output capacitor which is prone to fault. Compared to voltage output configuration, the proposed scheme has advantages such as simple structure and reliable short-circuit protection [7]. Fuse should be included at the input side of each module, which is denoted as F_i in Fig. 2.

A. Operation Principle of a Single Module

Only brief description of operation principle and modeling will be provided, since comprehensive analysis for a single module has been covered in [24]. In steady state, the converter has 12 half-cycle symmetric operation modes. On primary side, diagonal switches are operated in pairs, and complementary (with proper deadtime t_d) to the other pair. Secondary switches have a duty ratio of 0.5 and are phase shifted by ϕ compared to corresponding primary switch pairs. The key waveforms during normal operation are shown in Fig. 3. If small soft transition modes during $[t_1, t_4]$, $[t_5, t_6]$, $[t_7, t_{10}]$ and $[t_{11}, t_0 + T_s]$ are ignored, where T_s is the switching cycle length, the module works as a full-bridge isolated buck converter. By selecting appropriately sized filters, input voltage V_{in} and output current I_o can be considered constant over a switching cycle. Soft switching is achieved via clamped resonance between transformer leakage inductance L_{lk} and resonant capacitor C_r. All secondary switches can be zero current switched for entire load range. In contrast, the following inequality should be valid to ensure ZVS for primary switches:

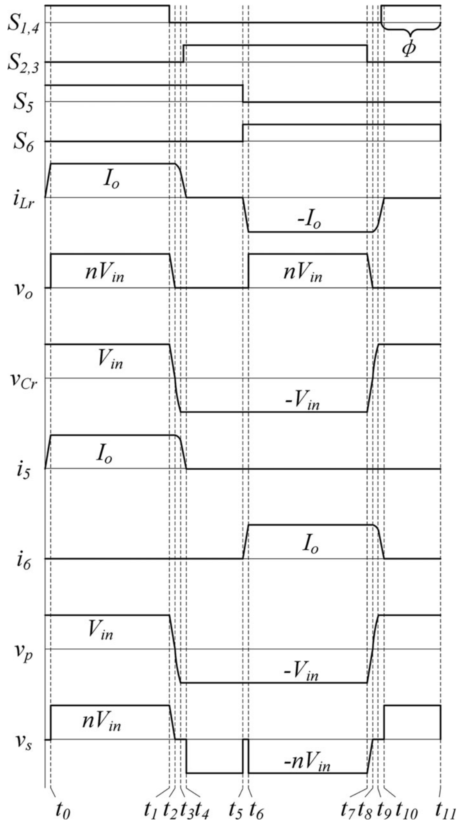

Fig. 3. Normal operation waveforms of one module.

$$\frac{L_{\text{lk}}}{C_r} > \left(\frac{V_{\text{in}}}{I_o}\right)^2. \tag{1}$$

Thus, the size of C_r is inversely proportional to ZVS range. DC capacitors can be used if resonant capacitors are placed across primary switches instead of across transformer primary winding. Value of each dc capacitor should be $C_r/2$. Comparatively, C_b is the dc blocking capacitor that protects transformer from saturation incurred by asymmetric gate signals, etc. Therefore, C_b should be large enough that it would not influence normal operation.

Let us define duty ratio *D* as the overlap between primary and secondary switch gating signals, i.e.,

$$D = \frac{t_7 - t_5}{T_s}. \tag{2}$$

D is the ideal duty ratio when all resonant modes are ignored and the converter is treated as a full-bridge isolated buck converter. The effective duty ratio D_{eff} is defined as follows:

$$D_{\text{eff}} = \frac{M}{2n} = \frac{\overline{V_o}}{2nV_{\text{in}}} = \frac{\overline{I_{\text{in}}}}{2nI_o} \tag{3}$$

where *M* is the normalized voltage transfer ratio, and a bar dictates the average value over a switching cycle. From input/output

TABLE I
DESIGN PARAMETERS

	Full-scale design	Prototype design
Power P	1.25 MW	3 kW
Input voltage V_{in}	1 kV	150 V
Output current I_o	208 A	10 A
Leakage inductance $L_{\rm lk}$	30 μH	9 μH
Resonant capacitance C_r	100 nF	20 nF
Switching frequency f_s	2 kHz	20 kHz
Transformer turns ratio $n = N_s/N_p$	2.5	1
DC blocking capacitance C_b	1 mF	10 μF
Output filtering inductance L_o	50 mH	0.6 mH
Magnetizing inductance L_m	40 mH	1.2 mH
Rated phase shift ϕ_0	0.09	0.12
Number of modules k	3	3

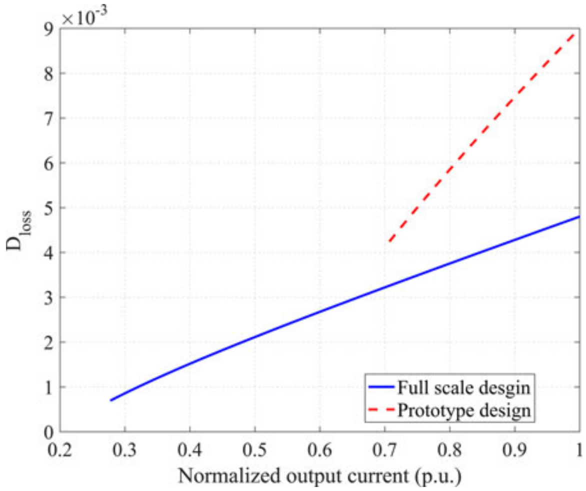

Fig. 4. Duty ratio loss versus output current.

energy balance, we have

$$T_s \bar{I}_{\rm in} = nI_o \left[2\left(DT_s - \frac{L_{\rm lk} I_o}{nV_{\rm in}} \right) + \frac{C_r V_{\rm in}}{nI_o} \right]. \tag{4}$$

Therefore, duty ratio loss can be calculated as

$$D_{\rm loss} = \frac{\frac{2L_{\rm lk} I_o}{V_{\rm in}} - \frac{C_r V_{\rm in}}{I_o}}{2nT_s} \tag{5}$$

and effective duty ratio is

$$D_{\rm eff} = D - D_{\rm loss} < D. \tag{6}$$

The inequality is found based on (1). As expected, $D_{\rm eff}$ is smaller than D, indicating a slightly reduced output voltage compared to hard switching case. For the parameters in (5), $V_{\rm in}$, $L_{\rm lk}$ and C_r are considered constant for a given design, while I_o may vary with the load level. Therefore, $D_{\rm loss}$ increases with output current, and maximum duty ratio loss $D_{\rm loss,max}$ can be obtained at rated output current. To facilitate the following discussion, two sets of design parameters are listed in Table I. Using the values from Table I, $D_{\rm loss,max}$ is 0.0048 for full-scale design and 0.009 for prototype design. The relationship of $D_{\rm loss}$ versus normalized output current is plotted in Fig. 4. The lines are limited to the range that output current would satisfy the soft-switching constraint in (1). Full-scale design can retain ZVS until around 0.279 per unit (p.u.) output current, corresponding to around 7.78% of rated power. Prototype design can retain ZVS until around 0.708 p.u. output current, corresponding to around 50% rated power. The ZVS range is decided by the selected prototype parameters in Table I, which are limited by available lab equipment.

B. *IPOS Benefit*

Let subscript "*mod*" stand for the corresponding quantity for single module. When k modules are connected in IPOS manner, the following benefits are introduced:

1) Higher Output Voltage: Module output voltages are stacked to a higher value

$$V_o = k\overline{V_{o,\rm mod}} \tag{7}$$

$$\overline{V_{o,\rm mod}} = 2nD_{\rm eff} V_{\rm in}. \tag{8}$$

2) Lower Input Current: Input current is split between all modules, allowing lower current capability switches such as high-voltage high-power MOSFETs to be used

$$\overline{I_{\rm in,mod}} = \overline{I_{\rm in}} / k. \tag{9}$$

3) Module Shedding to Improve Efficiency: During light load condition, the converter can deliver power using only a fraction of all modules. Therefore, each deployed module is operating closer to rated value, yielding a higher overall efficiency.

4) Reduced Ripples: By properly interleaving the gate signals for each module, input current and output voltage ripples can be greatly reduced. As a result, the required passive filters $C_{\rm in}$ and L_o sizes are also decreased. For this converter, a phase shift of $1/2k$ should be inserted between adjacent modules to achieve symmetrical interleaving.

5) Intrinsic Balancing: Unlike input series output series (ISOS) or input parallel output parallel (IPOP) converters, IPOS converter has intrinsic balancing if common duty cycle is applied to all modules.

Input voltage, effective duty ratio and transformer turns ratio are the three elements that affect module output voltage. Mismatches in parameters will not unbalance the system. First, all the converter modules have the same effective input voltage ($V_{\rm in} - 2V_{\rm CE(SAT)}$), where $V_{\rm CE(SAT)}$ is collector-emitter saturation voltage of switch. All primary bridges are parallel connected and $V_{\rm in}$ is the same. Due to the positive thermal coefficient of IGBTs, the difference in $V_{\rm CE(SAT)}$ will be minimized when a temperature imbalance occurs due to the heating of the IGBT with the lower saturation voltage. Second, differences in resonant parameters C_r and $L_{\rm lk}$ will create mismatch in $D_{\rm eff}$ though all modules have the same output current I_o and phase shift ϕ. Module with smaller C_r or larger $L_{\rm lk}$ has lower $D_{\rm eff}$, and therefore lower average output voltage and power. However, from Fig. 4 it is clear that $D_{\rm loss}$ is a very small quantity, and the mismatch of $D_{\rm loss}$ would be even smaller. Therefore, the most significant cause of output voltage mismatch is difference in turns ratio, which is also negligible with modern manufacturing technology [26].

If there is no delay in switching, average output voltage from each module can be found by (8). Mismatches in switch turn-on/off delays do not introduce unbalance either. If all switches within certain module are delayed for the same amount of time, the only consequence would be a less effective output interleaving: This is equivalent to changing the phase shift between modules. If switches within certain module are delayed differently, then small dc component could be generated in high-frequency link, which should be blocked by C_b.

6) Scalable Control Method: The control of the IPOS converter is similar to the control of a single module, regardless of k. Stability is guaranteed as I_o and V_{in} are the same for all modules.

C. Controller Design

Output current rather than voltage is the control target in this converter. It is convenient to connect the outputs of several converters sharing the same output current command in series to further increase the power rating. Transition modes should be small enough with proper design parameters so that they can be ignored during control design process. For example, with the values in Table I, the transition modes only take up 2.1% and 6.6% of the switching cycle in full-scale and prototype design, respectively.

Given the symmetry of the IPOS structure, the average model of the converter would be the similar to that of a single module. If constant resistive load is considered, following equation holds from volt-second balance of output inductor:

$$L_o \frac{di_o}{dt} + i_o R = \overline{V_o} = 2kD_{\text{eff}} nV_{\text{in}} \approx k(1-2\phi) nV_{\text{in}}. \quad (10)$$

Therefore, the transfer function from the ϕ to i_o can be written as

$$G_{\phi i(s)} = \frac{I_o(s)}{\Phi(s)} = -\frac{2knV_{\text{in}}}{sL_o + R}. \quad (11)$$

Conventional PI controller can be designed to regulate output current according to reference value. Actual phase-shift command sent to modulator would be the difference between rated phase shift ϕ_0 and the output of controller. The modulator then generates the carrier waves accordingly. This simple control method delivers stable operation for both steady state and transient under healthy conditions, which is later verified by simulation and experiment. The converter is immune to instabilities caused by parameter mismatches as discussed previously. Unlike ISOS or IPOP topologies, intermodular balancing control is not necessary.

To further demonstrate the advantages of proposed converter, the control-to-output relationship is plotted in Fig. 5. All data points are obtained via detailed model that considers transition modes. Each line is a linear fit of data points of matching design. Only load range that can achieve ZVS is shown. As can be seen, a linear relationship exists between control parameter ϕ and output I_o, which is valid for the entire soft-switching range. Therefore, output is less sensitive to slight variation of ϕ than dual active bridge derived topologies. Hence, resolution requirement for phase shift timer is reduced [27].

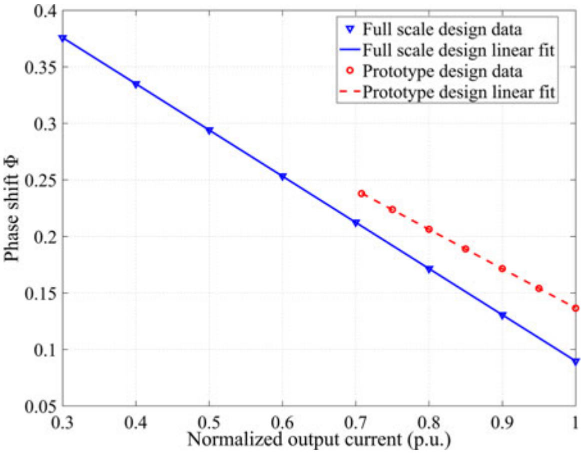

Fig. 5. Linear control-to-output relationship.

III. Fault-Tolerant Control

In this section, the consequences of several fault scenarios are first summarized. Then, the method for detecting fault and its location is introduced. The proposed converter can provide two levels of fault tolerance. Several types of faults can be tolerated intrinsically or via the switch-level tolerance. Other faults, including SCF of any primary switch can be tackled by module-level tolerance. The proposed fault-tolerant strategy requires only *3k* voltage sensors for a converter consisting of *k* modules.

A. Fault Scenarios Analysis

In following discussion, assume the converter is composed of *k* identical modules and the fault occurs at module #*i*.

1) Scenario 1: OCF at Secondary Switch: Leakage inductance current may be disrupted if OCF occurs at one of the secondary switches while it is conducting. Output current can still flow through other paths without interruption. Voltage stress across healthy switches will not be affected. However, average current through leakage inductance will no longer be zero during post-fault transient. Oscillation will occur in transformer voltage, with frequency determined by L_m and C_b. Maximum amplitude of transformer primary voltage will be approximately $4V_{\text{in}}/\pi$. The oscillation will rapidly attenuate and transformer voltage will return to normal levels. Therefore, this scenario does not require additional attention.

For module #*i*, power transfer during the half cycle when the OCF switch should have turned ON is now stopped by the fault. In steady state, this scenario can be regarded as setting $\phi = 0.5$ for half switching cycle. The total power transferred can still be regulated by the phase shift of the other half cycle and other healthy modules. Based on (10)

$$I_o R = \overline{V_o} = \left(k - \frac{1}{2}\right)(1 - 2\phi_1) nV_{\text{in}} \quad (12)$$

where ϕ_1 is post-fault phase shift under OCF at secondary switch. In order to sustain the same output current, the following relationship should be valid

$$\phi_1 = \frac{4k\phi_0 - 1}{4k - 2}. \tag{13}$$

Thus, if the calculated ϕ_1 is still in the allowed range, output current can maintain prefault value [24]. However, maximum power that can be transferred will decrease. Also, primary switches will no longer be zero voltage switched, which calls for provisions in thermal design.

2) Scenario 2: SCF at Secondary Switch: If SCF occurs at one of the secondary switches, the impact on transformer voltage and peak voltage across other switches are negligible. For module #*i*, power transfer during the half cycle when the SCF switch should have turned OFF is now at maximum due to the fault. In steady state, the scenario can be regarded as setting $\phi = 0$ for half cycle. Total power transferred can still be regulated by the phase shift of the other half cycle and other healthy modules. Based on (10)

$$I_o R = \overline{V_o} = [k - (2k - 1)\,\phi_2]\, nV_{\text{in}} \tag{14}$$

where ϕ_2 is post-fault phase shift under SCF at secondary switch. In order to sustain the prefault output current

$$\phi_2 = \frac{2k}{2k - 1}\phi_0. \tag{15}$$

Typically, ϕ_2 is still in the allowed range since the design value for rated phase shift ϕ_0 is normally smaller than 0.25 in order to get a reasonable voltage transfer ratio. The minimum power that can be transferred will increase but the converter can operate safely at full load.

3) Scenario 3: OCF at Primary Switch: Unlike secondary switch faults, voltage applied to primary side will have a dc component when OCF occurs at one of the primary switches. The converter can still function, but dc blocking capacitor C_{bi} will be biased. During steady state, the equivalent input voltage of module #*i* is $V_{\text{in}}/2$

$$I_o R = \overline{V_o} = \left(k - \frac{1}{2}\right)(1 - 2\phi_3)\, nV_{\text{in}} \tag{16}$$

where ϕ_3 is post-fault phase shift under OCF at primary switch. In order to maintain the same output current

$$\phi_3 = \frac{4k\phi_0 - 1}{4k - 2}. \tag{17}$$

As can be seen, ϕ_3 equals ϕ_1, which means the effect of OCF at one primary switch is similar to OCF at one secondary switch. With careful design, ϕ_1 and ϕ_3 can stay within the allowed range. Power transfer capability will decrease, same as scenario 1. A more severe problem is that the other switch on the same leg will have to withstand much higher voltage spikes, if the antiparallel diode of the faulty switch is also open. For example, if OCF occurs at $\mathrm{S}_{4\mathrm{i}}$ and $\mathrm{D}_{4\mathrm{i}}$ is also open, C_{ri} voltage will no longer be clamped by input voltage during $[t_9, t_{10}]$. Peak voltage across $\mathrm{S}_{3\mathrm{i}}$ will increase if the fault is not dealt with.

4) Scenario 4: SCF at Primary Switch: When SCF takes place at any of the primary switches, the converter is prone to a shoot-through fault, which calls for immediate attention. The faulty module has to be isolated from the system to stop damage from spreading.

TABLE II
DETECTABLE FAULTS AND CORRESPONDING v_{Cbi} BEHAVIOR

OCF fault	v_{Cbi}
$\mathrm{S}_{1\mathrm{i}}$ or $\mathrm{S}_{4\mathrm{i}}$	Drop
$\mathrm{S}_{2\mathrm{i}}$ or $\mathrm{S}_{3\mathrm{i}}$	Rise
$\mathrm{S}_{5\mathrm{i}}$	Oscillate starting from negative half cycle
$\mathrm{S}_{6\mathrm{i}}$	Oscillate starting from positive half cycle

B. Fault Detection and Location

Since SCF usually leads to drastic consequence, the detection and protection method must be very fast. Therefore, SCF protection circuit is usually incorporated in gate drivers for industrial applications [16]. The driver will turn OFF the switch once potential SCF happens, resulting in an open circuit. Therefore, only OCF detection, location and reconfiguration method is considered in this paper.

Based on the analysis of scenario 1 and 3, DC component of the voltage across C_b is a good indicator of OCF fault. The detectable faults and resultant v_{Cbi} behaviors are summarized in Table II. During normal operation, only minor DC bias will exist in v_{Cb} due to asymmetrical gate signals, etc. When OCF occurs at module #*i*, v_{Cbi} will deviate from zero. From Table II, it is obvious that monitoring v_{Cbi} alone cannot provide exact fault location. Thus, average voltages across the lower primary switches, i.e., v_{S2i} and v_{S4i} are also sensed to obtain further information about the fault.

If OCF occurs at one of the lower primary switches, then the corresponding sensor output will drop. If OCF occurs at one of the upper primary switches, then the sensor across the lower switch on the same leg will have higher output. Lastly, if OCF occurs at one of the secondary switches, then none of the outputs of switch voltage sensors will be affected. The fault detection and location method is shown in Fig. 6. For example, assume $\mathrm{S}_{4\mathrm{i}}$ suddenly suffers from OCF. Then, v_{Cbi} will drop and average voltage across $\mathrm{S}_{4\mathrm{i}}$ will increase beyond normal. Now, the fault can be identified as $\mathrm{S}_{4\mathrm{i}}$ OCF, but not $\mathrm{S}_{1\mathrm{i}}$ OCF. Once the fault is detected and located, the converter can be reconfigured, as will be described in subsection II-C.

C. Reconfiguration Method

Once OCF at primary switch is located, then the signal for the faulty switch will be set to low. The switch on the same leg, as well as all secondary switches will be turned ON permanently. The gate signals for primary switches on the other leg will remain unchanged. For example, once OCF at $\mathrm{S}_{4\mathrm{i}}$ is identified, gate signal for $\mathrm{S}_{4\mathrm{i}}$ will be set to low, while gate signals for $\mathrm{S}_{3\mathrm{i}}$, $\mathrm{S}_{5\mathrm{i}}$ and $\mathrm{S}_{6\mathrm{i}}$ will be high permanently. Gate signals for $\mathrm{S}_{1\mathrm{i}}$ and $\mathrm{S}_{2\mathrm{i}}$ will remain unchanged. Then, the faulty module will essentially be reconfigured into an asymmetric half-bridge converter operating in open loop, as shown in Fig. 7. The duty ratios of $\mathrm{S}_{1\mathrm{i}}$ and $\mathrm{S}_{2\mathrm{i}}$ remain at around 50% (with appropriate deadtime), transferring as much power as possible [28]. After

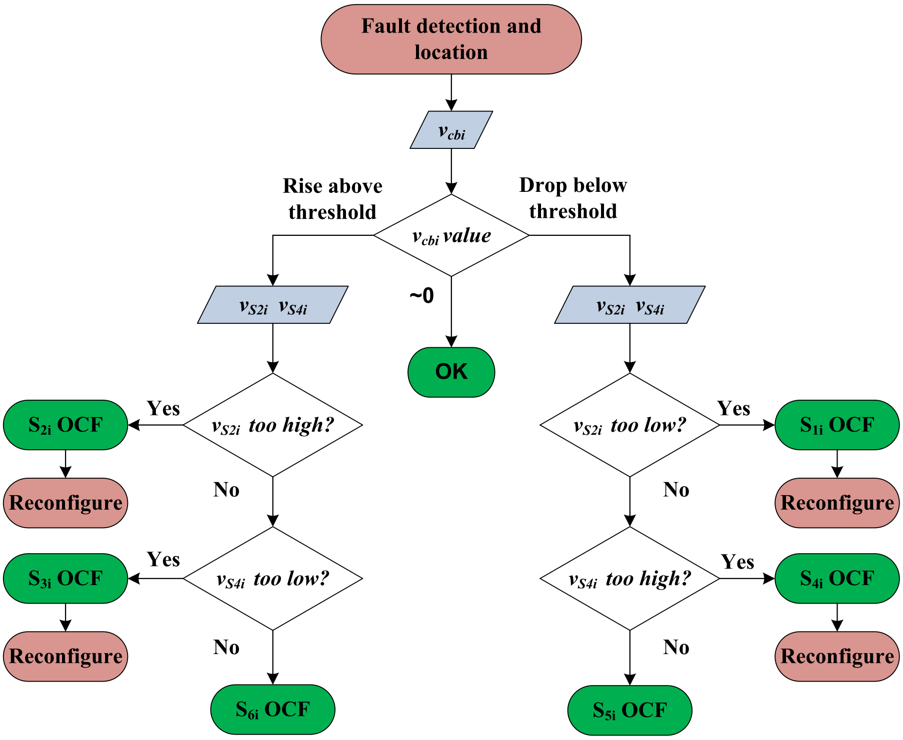

Fig. 6. Flow chart of fault detection and location method.

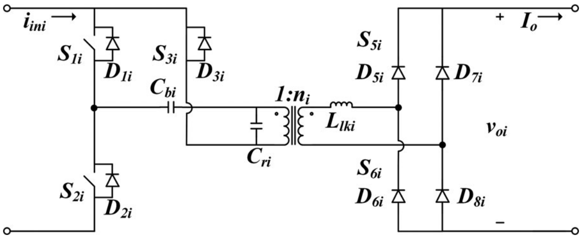

Fig. 7. Equivalent topology after S_{4i} OCF and reconfiguration.

the reconfiguration, the switches on the healthy leg, namely $\mathrm{S_{1i}}$ and $\mathrm{S_{2i}}$ will still remain zero voltage switched. Faults at other primary switches can be detected, located and tolerated in a similar manner. If the fault is located at secondary switches, then according to previous analysis, no actions need to be taken.

If nontolerable faults (SCF at primary switches) happen, the modular structure provides an additional level of fault tolerance. If gate driver has built-in SCF protection, then it will automatically block all gate signals to SCF module. Otherwise, fuse will first disconnect the input side of the faulty module. Then, SCF module will be securely bypassed by blocking all its gate signals when both average voltages across both v_{S2i} and v_{S4i} have dropped below certain threshold. Output current can freewheel through the diode leg formed by $\mathrm{D_{7i}}$ and $\mathrm{D_{8i}}$, assuming module *#i* is bypassed. Phase shift between healthy modules is adjusted to $1/2(k-1)$ to maintain symmetrical interleaving.

IV. SIMULATION AND EXPERIMENT RESULTS

In this section, simulation and experiment results are presented to validate previous analysis. Pure resistive load is used in both simulation and experiment. Therefore, when fault happens and the power transfer capability is severely impaired, to maintain same output current level will not be possible. On the other hand, if output is connected to constant current load, output voltage will vary freely with input power.

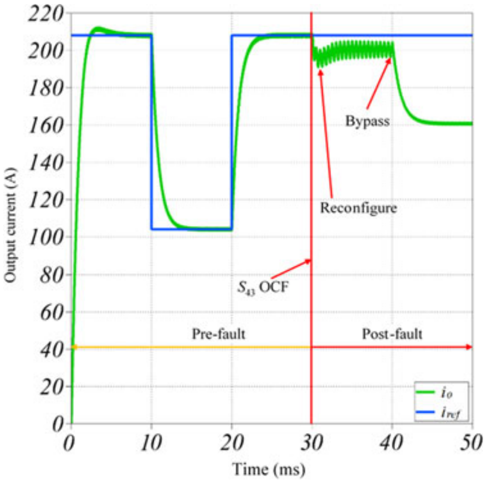

Fig. 8. Output current step response and fault-tolerant control.

A. Simulation Validation

Simulations are carried out in PLECS for both sets of parameters listed in Table I. For simplicity, only results for full-scale design are shown in Fig. 8. The simulation starts with zero initial conditions and current reference $i_{\mathrm{ref}} = 208$ A at $t = 0$. At $t = 10$ ms, i_{ref} steps to 104 A and at $t = 20$ ms it steps back

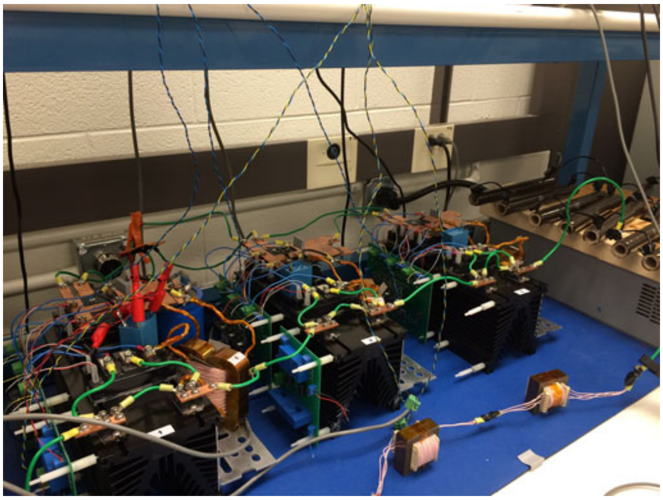

Fig. 9. Prototype converter consisting of three modules.

to 208 A. The output current keeps tracking reference value in approximately 2 ms. At $t = 30$ ms, a timed relay switch is used to imitate S_{43} OCF. The fault is detected and located in approximately 2.1 ms, when reconfiguration method is applied. After the reconfiguration, output current settles at around 200 A despite the reference value. This indicates postfault converter is already operating at maximum capacity as ϕ has reached its lower limit. At $t = 40$ ms, module *#3* is bypassed and I_o gradually drops to around 160 A, approximately 77% of reference value.

B. Experiment Results

A prototype has been constructed with parameters listed in second column of Table I. The design purpose is quick concept validation so the implementation has not been optimized for volume nor efficiency. Hardware-in-the-loop (HIL) fast prototyping method is used in development process. First, control system is set up in LabVIEW and converter circuit model is set up in Multisim. Cosimulation between LabVIEW and Multisim is conducted to evaluate the control performance. The verified control is then implemented in real-time (RT) controller cRIO-9082 using LabVIEW. The cRIO is configured to FPGA interface mode, allowing full access to its embedded FPGA chip. Both levels of fault-tolerant control and user interface are realized in RT operating system, while SPS modulator and ADC are implemented on the FPGA. The power stage of the prototype is shown in Fig. 9. The components used in prototype construction are listed in Table III.

Since IGBT will be the choice of component in full-scale design, it is also used in the prototype. Therefore, 1.2-kV 50-A IGBT modules are used due to their availability. The efficiency measured at different load and input conditions are summarized in Fig. 10. At 150-V input and 10.21-A load, efficiency is 87.9% with three modules operating. It is to be noted that voltage drops across IGBT and diode are relatively high at prototype voltage and current level. Out of the total loss of 432 W, the conduction loss of semiconductors is estimated to be 211 W based on datasheets. The prototype efficiency will be greatly improved using MOSFETs as switches. As for full-scale design, the efficiency is estimated to be around of 97.51% at full load. Moreover, module shedding can improve efficiency at light load condition, as shown in Fig. 10.

TABLE III
PROTOTYPE COMPONENT LIST

Component	Part No./Description
Switches $S_{1i} \sim S_{6i}$	Powerex CM50DU-24F, 1200 V/50 A IGBT
Diode $D_{5i} \sim D_{8i}$	IXYS DSEI2x61-12B, 1200 V/52 A fast recovery
C_{bi}	Vishay MMKP383 double metallized polypropylene film capacitors, 750 V dc
C_{in}	Mallory electrolytic capacitor, 450 V dc
Gate driver	Concept 6SD106EI, 6-pack driver
Voltage sensor	LEM LV-25, Hall effect sensor
Current sensor	LEM LA-55P, Hall effect sensor
Transformer	Core: E-E cores of Metglass AMCC50 Wire: MWS 60/36, 5 branches of 47 turns each
Output inductor	Implemtented by two identical 0.3 mH inductors Cores: E-E cores of Magnetics 00K5528E060 Wire: MWS 125/40, 4 branches of 40 turns each
RT controller	NI cRIO-9082 with 2∗NI 9401, NI 9205, NI 9263

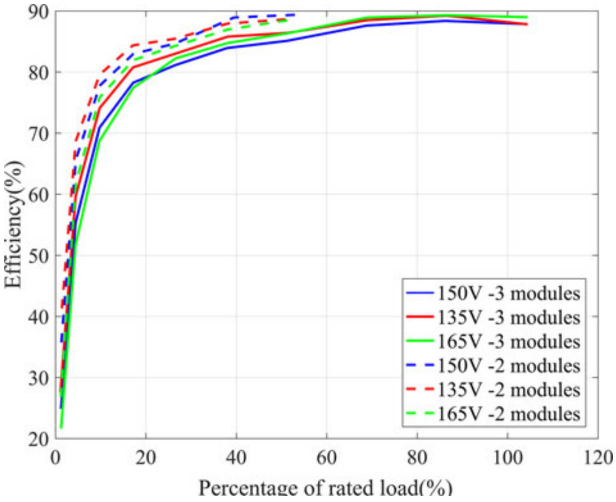

Fig. 10. Efficiency measurement.

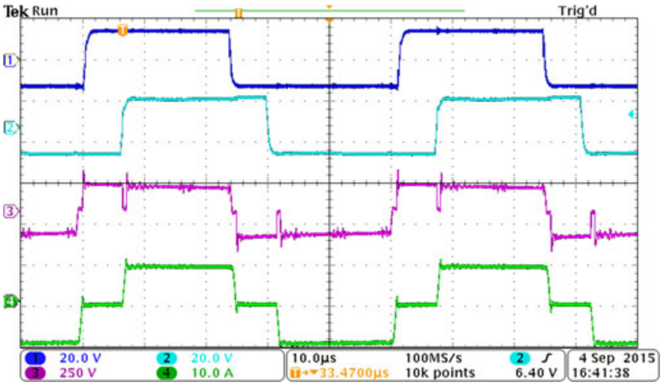

Fig. 11. Steady-state operation (CH1: v_{GE}^{S13}, CH2: v_{GE}^{S53}, CH3:v_{s3}, CH4: i_{Llk3}).

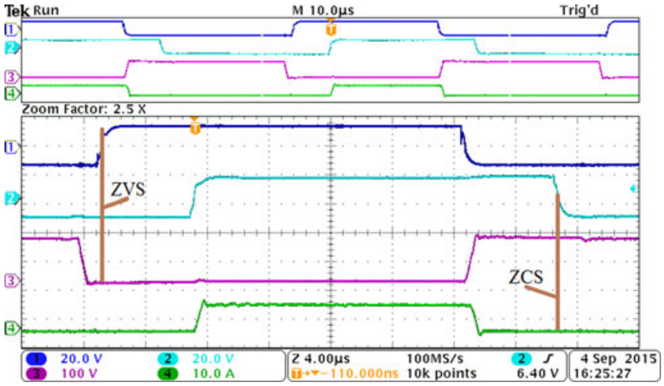

Fig. 12. Soft switching during healthy operation (CH1: v_{GE}^{S13}, CH2: v_{GE}^{S53}, CH3:v_{S13}, CH4: i_{S53}).

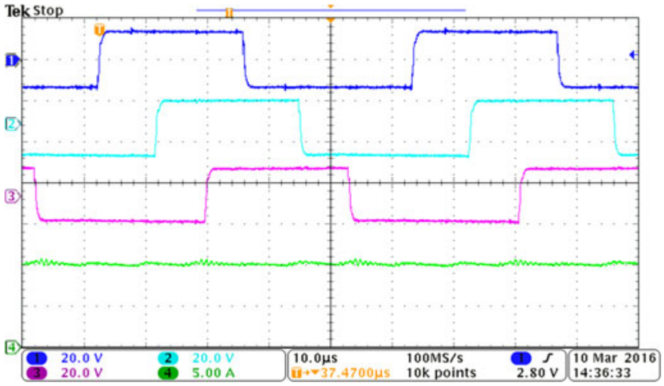

Fig. 13. Interleaving (CH1: v_{GE}^{S41}, CH2: v_{GE}^{S42}, CH3: v_{GE}^{S43}, CH4: i_o).

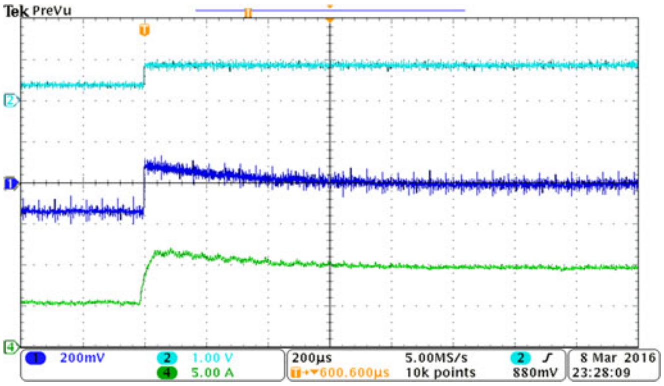

Fig. 14. Closed-loop output current step response (CH1: PI output, CH2:i_{ref}, CH4:i_o).

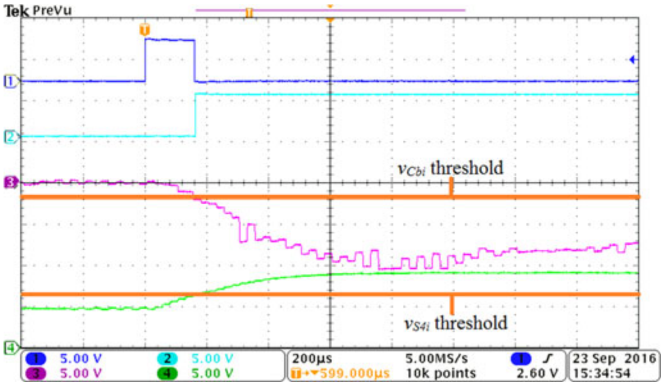

Fig. 15. Primary switch OCF (CH1: Fault triggered/detected; CH2: fault located; CH3: v_{Cb3} processed; CH4: v_{S43} processed).

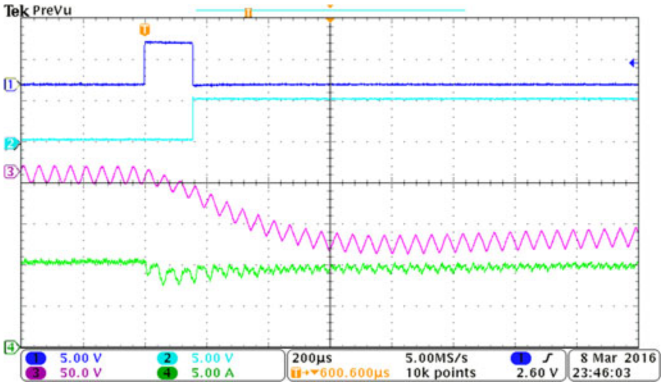

Fig. 16. Primary switch OCF (CH1: Fault triggered/detected; CH2: fault located; CH3: v_{Cb3}; CH4: i_o).

Steady-state operation under healthy condition is verified. Gate driver outputs of S_{13} and S_{53} are shown in channel 1 and 2 of Fig. 11. Transformer secondary voltage v_{s3} and current i_{Llk3} shown in channel 3 and 4 both match the theoretical steady-state waveforms in Fig. 3. ZVS of primary switch and ZCS of secondary switch during healthy operation at rated values are demonstrated in Fig. 12. Since the gate signals of each module is phase shifted by 1/6 switching cycle, output current has very small ripple, as shown in Fig. 13. Then, closed-loop experiment is performed. In the experiment, current reference i_{ref} steps from 5 to 10 A. Current reference command, PI controller output and converter output current are plotted in Fig. 14. Output current tracks reference value in approximately 400 μs. In steady state, PI output is approximately zero, therefore the actual phase shift between $\mathrm{S}_{1\mathrm{i}}$ and $\mathrm{S}_{5\mathrm{i}}$ is just ϕ_0.

Next, switch-level fault-tolerant control is tested and presented in Fig. 15. S_{43} OCF is triggered by blocking its gate signal. Due to limited number of oscilloscope channels, the signals of fault triggering and fault detection based on v_{Cb3} are combined and shown in channel 1. The rising edge stands for the moment of fault triggering, and the falling edge stands for the moment of fault detection. Channel 2 shows the moment that fault is located is indicated. Sensor readings of v_{Cb3}, v_{S43} are filtered and shown in channel 3 and 4 with their corresponding thresholds. After the fault, v_{Cb3} decreases as expected. The fault is detected and located in 160 μs, and the reconfiguration method is activated. In Fig. 16, probe-measured v_{Cb3} and i_o are shown in channel 3 and 4. Output current is supported by healthy modules and the dip is very small. According to measurement, prefault i_o value is 10.35 A, and postfault value is 9.87 A. After the reconfiguration, the switches on healthy leg, i.e., S_{13} and S_{23} are still zero voltage switched, as shown in Fig. 17. In Fig. 18, dc blocking capacitor voltage of healthy module #2 is shown in channel 2. As can be seen, neither fault nor reconfiguration method will disrupt the operation of healthy modules or trigger false positive in other modules. Experiment

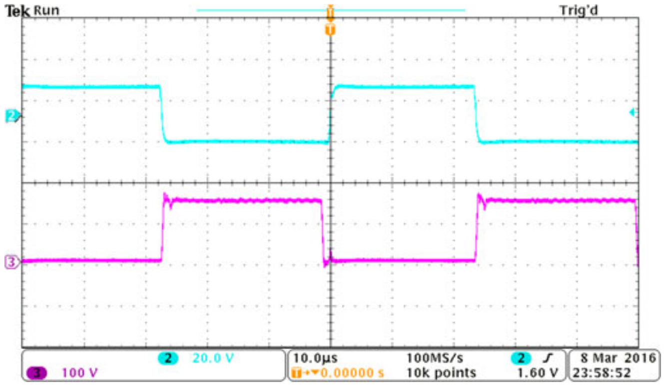

Fig. 17. Postfault ZVS (CH2: v_{GE}^{S13}; CH3: v_{S13}).

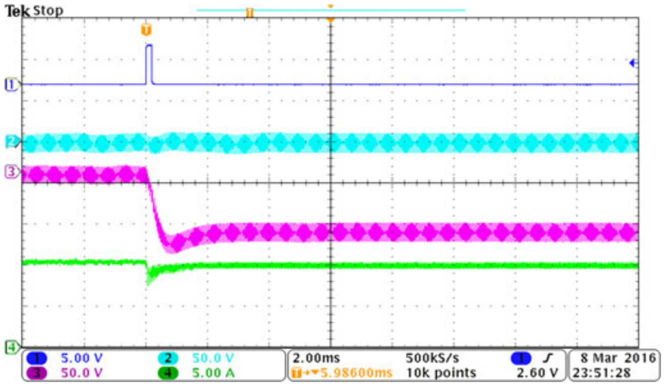

Fig. 18. Fault effect on other modules (CH1: Fault triggered/detected; CH2: v_{Cb2}; CH3: v_{Cb3}; CH4: i_o).

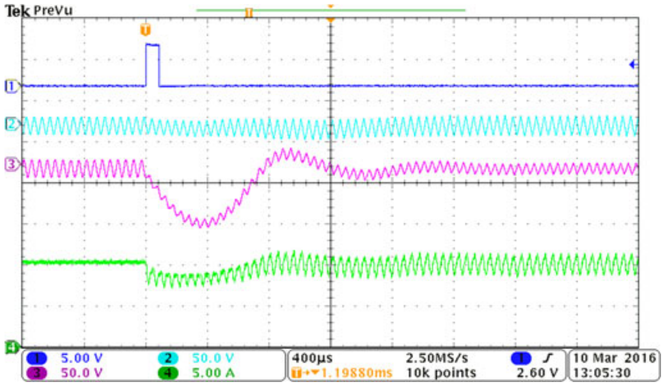

Fig. 19. Secondary switch OCF (CH1: Fault triggered/detected; CH2: v_{Cb2}; CH3: v_{Cb3}; CH4: i_o).

results of secondary switch OCF is shown in Fig. 19. Now, S_{53} OCF is triggered by blocking its gate signal. Fault can be detected by v_{Cb3} as shown in channel 1, but average voltage across S_{23} and S_{43} are not affected. Therefore, the controller decides that it has encountered a secondary OCF and will not deploy any reconfiguration method. As can be seen, dc blocking capacitor voltages of other modules are not affected. The output current is about 9.92 A in post-fault steady state, and ripple is still below 10%. Finally, the response of v_{Cb3} and i_o when module-level tolerant control is applied are shown in Fig. 20. When module *#3* is bypassed, output current is freewheeling through D_{73} and D_{83}. Phase shift of module *#1* and *#2* reaches minimum, and output current drops to 8.91 A.

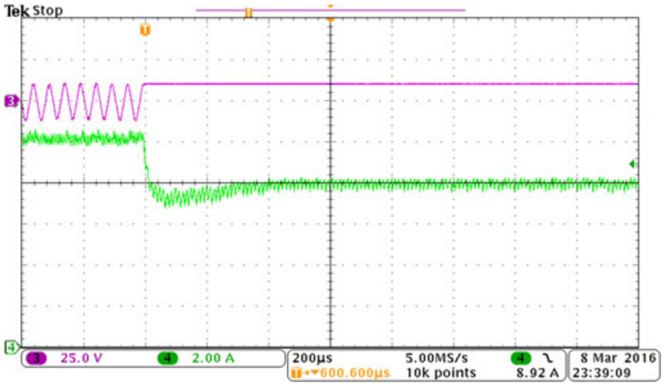

Fig. 20. Module-level tolerance (CH3: v_{Cb3},CH4: i_o).

V. CONCLUSION

In this paper, a novel fault-tolerant isolated dc–dc converter suitable for series-dc offshore wind farm application is proposed. The converter is controlled by secondary phase-shift modulation. ZVS is achieved for all primary switches and ZCS is achieved for all secondary switches and diodes during healthy operation. The converter has relatively large soft-switching range and linear control-to-output relationship.

Fault detection and location method based on monitoring dc blocking capacitor voltage and lower switch voltage is proposed. Switch-level tolerance not only prevents the fault from spreading but also allows full utilization of healthy components. The functioning switches within the faulty module still remain soft switched. Additionally, module-level tolerance can isolate a module with nontolerable fault from the system. Output current can freewheel through the diode leg without any disruption. Simulation and HIL experiment results both verify the proposed converter operation and effectiveness of fault-tolerant control.

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