DTC of Three-Level NPC Inverter Fed Five-Phase Induction Motor Drive With Novel Neutral Point Voltage Balancing Scheme

Saifullah Payami, Ranjan Kumar Behera, *Senior Member, IEEE*, and Atif Iqbal, *Senior Member, IEEE*

***Abstract*—In this paper, direct torque control (DTC) of five-phase induction motor (FPIM) is implemented using three-level neutral point clamped (TL-NPC) inverter. One of the advantages of three-level inverter over two-level one for DTC operation is the low torque ripple. Also TL-NPC inverter through space vector modulation technique gives low dv/dt transition with better voltage waveform. By applying conventional lookup table for DTC, the TL-NPC inverter does not ensures lower dv/dt transition. In this paper, a novel switching scheme for DTC of FPIM using TL-NPC inverter is proposed that ensures the low dv/dt transition and balancing of dc-link capacitor voltages of TL-NPC inverter. To form the lookup table for DTC operation, instead of using voltage vectors directly, virtual vectors (VVs) are utilized. Two switching states are used in one sample time to generate a VV in $\alpha\beta$ plane, which gives zero resultant voltage in xy plane. The switching strategy ensures low number of transitions to reduce the switching losses. The switching state redundancies are used in a novel way to balance the dc-link capacitor voltages without using any additional hardware. The proposed technique to balance the dc-link capacitor voltage gives lower switching frequency. The MATLAB/Simulink environment is used for the simulation and the results are validated through experiments.**

***Index Terms*—Direct torque control (DTC), five-phase induction motor (FPIM), neutral point voltage balancing, neutral point clamped inverter, virtual vector (VV).**

I. Introduction

THE advent of faster power semiconductor switches and digital signal processors has led to the increased research in the area of multiphase (more than three-phase) motor drives. Multiphase motor drive is suitable for various high power and safety critical applications like more-electric aircraft, ship propulsions, locomotives, electric vehicle, *etc.*, because of two main reasons. First, with the increase in the number of phases, the per phase power handling requirement reduces that helps in reducing the series/parallel combination of power semiconductor switches. Second, the increase in number of phases leads to more fault tolerant capability. The m phase machine can run with $(m-1)/2$ number of phase. It has other inherent advantages like lower torque pulsation [1]–[3], higher torque density [4], [5], and lower current ripple [6]. Detailed review regarding the development of multiphase drives is available in [7]–[9].

Three-level neutral point clamped (TL-NPC) inverter is most widely accepted multilevel topology for medium voltage high-power applications because of its inherent advantages like low stress on the power semiconductor switches and low total harmonic distortion [10]–[13] in the current and voltage. Because of these advantages, TL-NPC inverters are also suitable for multiphase motor drives. Various work has been reported in the literature for multilevel multiphase drive. TL-NPC inverter for five-phase induction motor (FPIM) was first reported for ship propulsion in [14]. Later, the space vector modulation scheme for multilevel multiphase inverter is reported in [15]–[20]. The model predictive control for five-phase TL-NPC inverter is reported in [21] and [22].

For high-performance applications, flux and torque of induction motor (IM) are controlled independently. For this vector control and direct torque control (DTC) schemes where developed for three-phase IM [23]–[25]. Various aspects of it is dealt in [26] and [27]. To improve the performance of DTC operation of three-phase IM (low torque pulsation), TL-NPC topology is used in [28]–[30]. In [30], concept of virtual vector (VV) is utilized for DTC operation of three-phase IM using TL-NPC inverter. The VVs are synthesized such that there is smooth transition of voltage from low to higher level. Drive control schemes of three-phase IM is also applicable for multiphase IM. DTC schemes for FPIM is dealt in [31]–[35]. In these papers two-level inverter topology has been used for DTC operation of FPIM. One of the requirement for DTC operation of FPIM with distributed winding is that the voltage in xy plane should be zero. If not so, it will produce large amount of third harmonic component in the stator current [36]. To eliminate voltage in xy plane, the concept of VV has been used in [34] and [35] for DTC operation of FPIM.

Because of the suitability of TL-NPC inverter for medium voltage high-power applications, DTC technique using this topology for FPIM is needed to be developed. In [30], the DTC operation of three-phase IM using TL-NPC inverter is

Manuscript received October 9, 2016; revised January 10, 2017; accepted February 14, 2017. Date of publication March 1, 2017; date of current version November 2, 2017. Recommended for publication by Associate Editor B. Wang.

S. Payami is with the Rolls Royce@ NTU Corporate Lab, Nanyang Technological University Singapore, 639798 (e-mail: saif.payami@gmail.com).

R. K. Behera is with the Department of Electrical Engineering, Indian Institute of Technology Patna, Patna, 801103 India (e-mail: rkb@iitp.ac.in).

A. Iqbal is with the Department of Electrical Engineering, Qatar University, Doha 2713, Qatar (e-mail: atif.iqbal@qu.edu.qa).

Color versions of one or more of the figures in this paper are available online at http://ieeexplore.ieee.org.

Digital Object Identifier 10.1109/TPEL.2017.2675621

reported. The authors have advocated that look-up table based DTC technique developed for two-level inverter cannot be directly extended to TL-NPC inverter fed three-phase IM. This is because the operation of TL-NPC inverter requires two issues to be taken care of. First, the switching should be done in such a way that the dv/dt change is minimum. Second, the dc-link capacitor voltages are balanced. Recently, DTC of FPIM using TL-NPC inverter is reported in [37]. But the authors have not considered the above two issues for the operation of TL-NPC inverter. Thus, there is a requirement to develop a DTC technique for FPIM using TL-NPC inverter. So the main contribution of this paper is the development of a DTC technique for FPIM using TL-NPC inverter considering the following points:

1) the resultant voltage in xy plane should be zero;
2) the switching should be done in such a way that there is smooth transition of voltage level, *i.e.,* low dv/dt;
3) the dc-link capacitor voltage should be balanced.

In this paper, the DTC operation of a FPIM using TL-NPC inverter is presented. The concept of VV is utilized and they are synthesized in such a way that the transitions in the voltage level are smooth, *i.e.,* dv/dt transition is checked and there are least number of switching transitions possible and simultaneously the resultant voltage in xy plane is zero. In the proposed technique, the switching states redundancies are utilized in a novel way to maintain the dc-link capacitor voltage at lower switching frequency as compared with the techniques available in the literature. To show the superiority of the proposed DTC scheme, simulation of DTC technique given by *Tatte and Aware* in [37] for the DTC operation of FPIM using TL-NPC inverter is carried out, and the shortcomings of that scheme is highlighted. These analysis are carried out through simulations in MATLAB/Simulink environment and the results are validated through experiments.

The paper is organized as follows. The five-phase TL-NPC topology and its switching state and the concept of VV is dealt in the Section II. The Section III deals with the neutral point voltage balancing scheme. Section IV deals with DTC scheme for FPIM using TL-NPC inverter. Simulation and experimental results are given in the Section V and finally the paper is concluded in the Section VI.

II. Five-Phase TL-NPC Inverter

TL-NPC inverter is widely accepted in the industries for high-power applications because of better voltage waveform and ease of control as compared with other three-level topologies. This topology is also suitable for FPIM for high-power applications.

A. Circuit Topology and Space Vector of Five-Phase TL-NPC Inverter

Five-phase TL-NPC inverter topology is shown in Fig. 1. Each leg has four switches and two clamping diodes. Each leg has three switching states; $S_i = 1, 0$, and -1 where, subscript $i = a, b, c, d$, and e corresponds to phase A, B, C, D, and E, respectively. $S_i = 1$ means S_{i1} and S_{i2} are ON. $S_i = 0$ means S_{i2} and S_{i3} are ON. And $S_i = -1$ means S_{i3} and S_{i4} are ON. In five-phase TL-NPC inverter there are $3^5 = 243$ switching

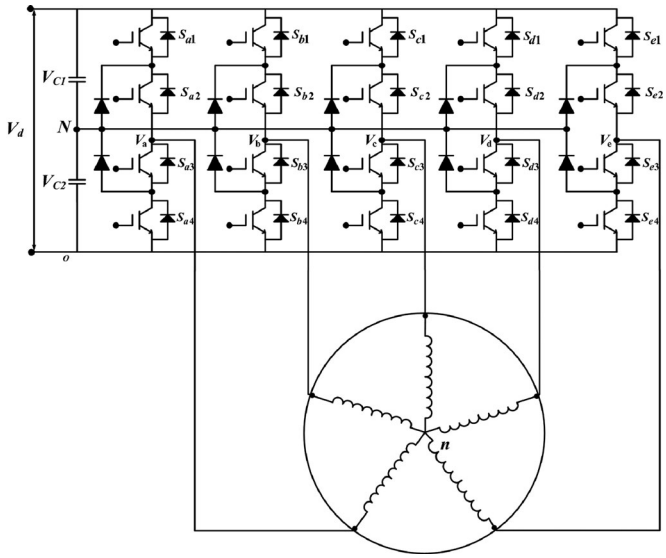


Fig. 1. Circuit topology for five-phase TL-NPC inverter.

states. Corresponding to each states the phase voltage across the stator winding is given by

$$\begin{bmatrix} V_{an} \\ V_{bn} \\ V_{cn} \\ V_{dn} \\ V_{en} \end{bmatrix} = \frac{1}{5}\frac{V_d}{2} \begin{bmatrix} 4 & -1 & -1 & -1 & -1 \\ -1 & 4 & -1 & -1 & -1 \\ -1 & -1 & 4 & -1 & -1 \\ -1 & -1 & -1 & 4 & -1 \\ -1 & -1 & -1 & -1 & 4 \end{bmatrix} \begin{bmatrix} S_a \\ S_b \\ S_c \\ S_d \\ S_e \end{bmatrix} \quad (1)$$

where V_{an}, V_{bn}, V_{cn}, V_{dn}, and V_{en} are phase voltages and V_d is the dc-link voltage of the inverter. The phase voltages of the inverter can be transformed into space vectors in $\alpha\beta$ and xy planes by

$$V_{\alpha\beta} = \frac{2}{5}\left(V_{an} + aV_{bn} + a^2V_{cn} + a^3V_{dn} + a^4V_{en}\right) \quad (2)$$

$$V_{xy} = \frac{2}{5}\left(V_{an} + a^3V_{bn} + aV_{cn} + a^4V_{dn} + a^2V_{en}\right) \quad (3)$$

where $a = e^{j\frac{2\pi}{5}}$. Detailed space vector diagram of $\alpha\beta$ and xy plane is given in [15] and [17]. For simplicity they have not been shown here. The magnitude of vertex and nonvertex vectors in $\alpha\beta$ and xy spaces are given in Table I.

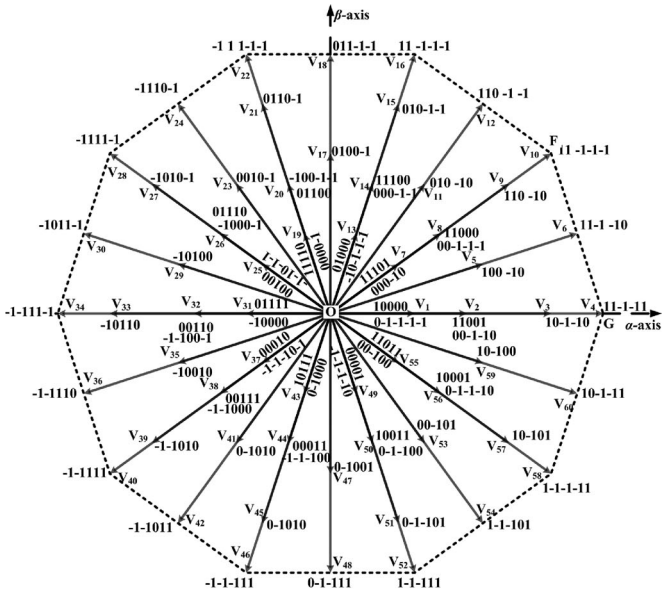
A method to eliminate the nonpotential switching states to reduce the number of switching states was proposed in [15] and [38]. Switching states whose pole voltage order contradict the order of reference voltage in a particular sector are discarded. Based on this concept out of 243, 113 switching states are selected for space vector modulation technique of five-phase TL-NPC inverter [15]. In this paper the switching states given in [15] has been considered for the DTC operation of FPIM.

B. Concept of VV

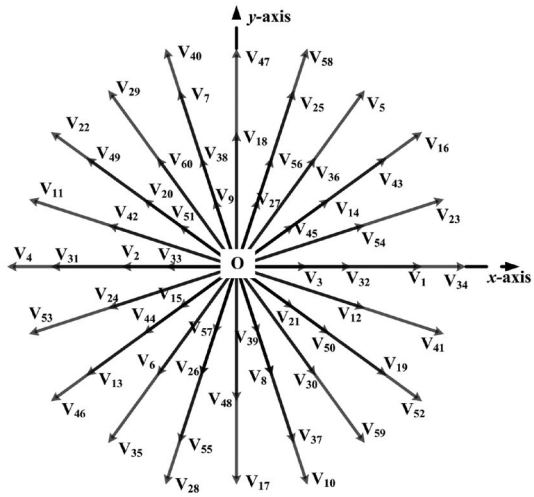
The operation of FPIM with distributed winding requires the flux of third harmonic plane (xy plane) to be zero. For this the resultant voltage of xy plane should be eliminated. If this voltage is not eliminated, it will cause distortion in the stator current [36]. The DTC operation of FPIM using two-level inverter as

TABLE I
MAGNITUDE OF VERTEX AND NONVERTEX VECTORS IN $\alpha\beta$ AND xy SPACE

Vertex vector	
$\alpha\beta$ space vector magnitude	xy space vector magnitude
0.647 V_d	0.076 V_d
0.524 V_d	0.124 V_d
0.447 V_d	0.20 V_d
0.40 V_d	0.247 V_d
0.324 V_d	0.324 V_d
0.247 V_d	0.40 V_d
0.20 V_d	0.447 V_d
0.124 V_d	0.524 V_d
0.076 V_d	0.647 V_d
Nonvertex vector	
0.615 V_d	0.145 V_d
0.380 V_d	0.235 V_d
0.235 V_d	0.380 V_d
0.145 V_d	0.615 V_d



(a)



(b)

Fig. 2. Space vectors of five-phase TL-NPC in (a) $\alpha\beta$ and (b) xy plane used for DTC operation.

reported in [34] and [35] have used the concept of VV, where the VVs are generated using two switching states in such a way that the resultant voltage in xy plane is zero. In [30], Zhang *et al.* have advocated that for DTC operation of three-phase IM using TL-NPC inverter, the technique of two-level inverter cannot be directly extended to TL-NPC inverter case as it requires two issues to be taken care of. First, the switching should be done in such a way that the dv/dt should be low. Second, the dc-link capacitor voltages should be balanced. So, the DTC technique for FPIM using TL-NPC inverter is developed considering following points:

1) the resultant voltage in xy plane should be zero;
2) the switching transitions should have low dv/dt;
3) the dc-link capacitor voltages should be balanced.

For this the concept of VV is utilized, where they are synthesized considering first two requirements. The balancing of dc-link capacitor voltage is addressed in the next section. The operation of TL-NPC inverter requires that the voltage level of a particular phase should not change from the lowest level to the highest level, *i.e.,* the voltage jump should be smooth. Say, if the pole voltage is $-\frac{V_d}{2}$ then it should not go directly to $+\frac{V_d}{2}$. Rather, it should go from $-\frac{V_d}{2}$ to 0 then it should go to $+\frac{V_d}{2}$. This will maintain low dv/dt change and lower stress on the power semiconductor switches.

The voltage vectors in $\alpha\beta$ plane should be selected such that the resultant voltage vectors in xy plane is zero. Out of 113 switching states, 61 switching states in $\alpha\beta$ plane are selected for the synthesis of VVs. The voltage vectors corresponding to these switching states are the vertex vectors and they are in total 41 in numbers. The selected vectors in $\alpha\beta$ plane and corresponding vectors in xy plane are shown in Fig. 2(a) and (b). The switching states and the vector numbers have been marked for $\alpha\beta$ plane. For xy plane only vector number has been shown for simplicity. The magnitude of the voltage vectors used for the DTC operation in $\alpha\beta$ plane and xy plane are given in Table II.

In the proposed DTC scheme, only two vertex vectors of magnitude $0.6472\,V_d$ and $0.5236\,V_d$ in one sample time are used to synthesize the large VVs. And two vertex vectors of magnitude $0.3236\,V_d$ and $0.20\,V_d$ are used for small VVs. Consider the sector OFG in $\alpha\beta$ plane shown in Fig. 3(a). Voltage vectors V_1 and V_2 are in opposite direction in xy plane. Similarly, V_3 and V_4 are in opposite direction in xy plane as shown in Fig. 3(b). Using the volt–second balance technique, the dwell time of switching states is calculated. Selection of voltage vectors V_1 and V_2 in one sample time gives resultant VV V_{S1} of smaller magnitude in $\alpha\beta$ plane. Similarly V_3 and V_4 produces VV V_{L1} of larger magnitude in $\alpha\beta$ plane and zero resultant voltage vector in xy plane. The resultant VVs in $\alpha\beta$ plane of all vertex vectors is shown in Fig. 4.

1) Dwell Time Calculation: Using volt–second balance technique the resultant voltage vector in xy plane is made zero. The dwell time for the switching states corresponding to voltage

TABLE II
MAGNITUDE OF VERTEX VECTOR IN $\alpha\beta$ AND xy PLANE USED FOR DTC OPERATION

$\alpha\beta$ space vector magnitude	xy space vector magnitude
0.6472 V_d	0.2472 V_d
0.5236 V_d	0.0764 V_d
0.3236 V_d	0.1236 V_d
0.20 V_d	0.20 V_d

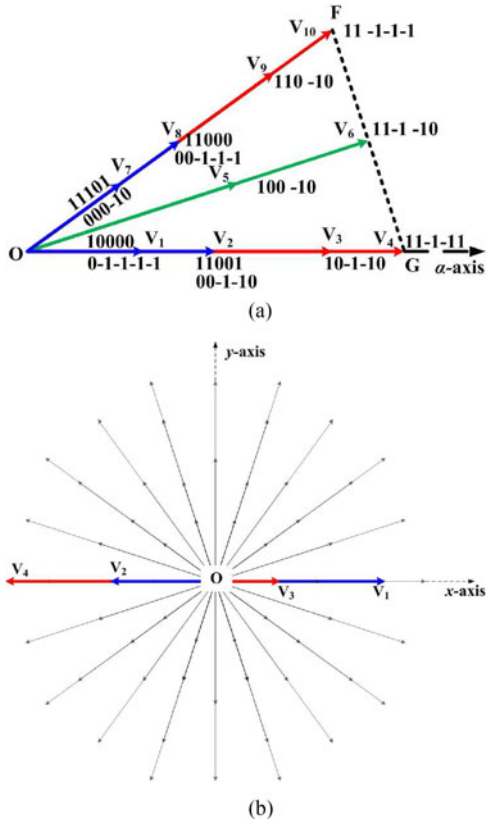


Fig. 3. (a) Sector OFG of $\alpha\beta$ plane and (b) corresponding voltage vectors in xy plane of TL-NPC inverter for the proposed DTC scheme.

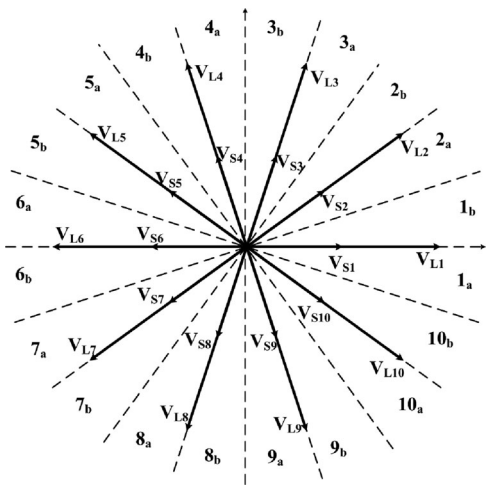


Fig. 4. Resultant VVs in $\alpha\beta$ plane for the proposed DTC scheme.

vectors V_1 and V_2 can be derived as

$$T_{\text{dtc}}\overrightarrow{V}^{\text{res}}_{\alpha\beta} = T_1\overrightarrow{V}_{1\alpha\beta} + T_2\overrightarrow{V}_{2\alpha\beta} \tag{4}$$

$$T_{\text{dtc}}\overrightarrow{V}^{\text{res}}_{xy} = T_1\overrightarrow{V}_{1xy} + T_2\overrightarrow{V}_{2xy} \tag{5}$$

$$T_{\text{dtc}} = T_1 + T_2 \tag{6}$$

where $\overrightarrow{V}^{\text{res}}_{\alpha\beta}$ and $\overrightarrow{V}^{\text{res}}_{xy}$ are the resultant voltage vectors in $\alpha\beta$ and xy plane, respectively. T_1 and T_2 are the dwell time for switching states corresponding to V_1 and V_2, respectively and T_{dtc} is the sample time. In (5), the $\overrightarrow{V}^{\text{res}}_{xy} = 0$ as resultant voltage vector in xy plane should be zero. Since time being a scalar quantity, can be derived as

$$\frac{T_1}{T_2} = \frac{|V_{2xy}|}{|V_{1xy}|}. \tag{7}$$

Since $|V_{1xy}| = 0.20\,V_d$ and $|V_{2xy}| = 0.1236\,V_d$, where, V_d is the dc-link voltage. From (6) and (7), we get

$$T_1 = 0.3820\,T_{\text{dtc}} \tag{8}$$

$$T_2 = 0.6180\,T_{\text{dtc}}. \tag{9}$$

By putting the values of T_1 and T_2 and magnitude and direction of voltage vectors V_1 and V_2 in (4), the resultant voltage vector in $\alpha\beta$ plane is found to be

$$\overrightarrow{V}^{\text{res}}_{\alpha\beta} = 0.2764\,V_d\angle 0^\circ. \tag{10}$$

Similarly, the dwell time for switching states corresponding to V_3 and V_4 is calculated and is given by (11) and (12). The resultant voltage vector is given by (13)

$$T_3 = 0.7639\,T_{\text{dtc}} \tag{11}$$

$$T_4 = 0.2361\,T_{\text{dtc}} \tag{12}$$

$$\overrightarrow{V}^{\text{res}}_{\alpha\beta} = 0.5528\,V_d\angle 0^\circ \tag{13}$$

From (10) and (13) it is observed that the resultant voltage vector in $\alpha\beta$ plane synthesized from V_1 and V_2 is of the magnitude of $0.2764\,V_d$ and that of V_3 and V_4 is $0.5528\,V_d$. The smaller resultant vector is numbered as V_{Sj} and larger one as V_{Lj} as shown in Fig. 4 where, j varies from 1 to 10.

2) Switching Transitions: The switching transitions are selected such that there is smooth transition of pole voltage and line voltage from one state to other and there is only one level jump in the phase and line voltage. The switching transitions for the synthesis of large VV V_{L1} is shown in Fig. 5. From Fig. 5, it can be observed that in a sample time two switching states are symmetrically distributed in such a way that there is no direct jump from 0 level to $\pm V_d$ in the line voltages (see line voltage V_{BC} and V_{DE}). The switching transitions for the large VV for the proposed DTC scheme is given in Table III.

III. NEUTRAL POINT VOLTAGE BALANCING

In five-phase TL-NPC inverter, the vertex vector of magnitude $0.2\,V_d$ and $0.3236\,V_d$ are having redundant switching states. The switching states are of P-types or N-types. P-type means the phases are connected to positive dc rail and neutral point. While

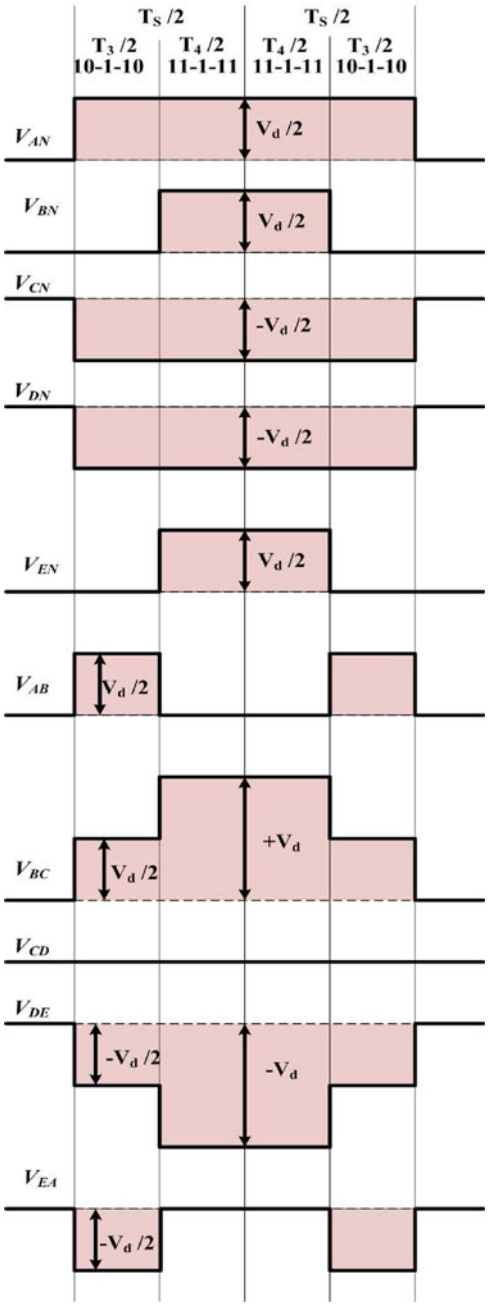


Fig. 5. Switching transitions for the synthesis of VV V_{L1}.

TABLE III
SWITCHING STATES CORRESPONDING TO LARGE VVS FOR PROPOSED DTC SCHEME

Large VV	Switching states
V_{L1}	10-1-10 → 11-1-11
V_{L2}	110-10→11-1-1-1
V_{L3}	010-1-1→11-1-1-1
V_{L4}	0110-1→ -111-1-1
V_{L5}	-1010-1→-1111-1
V_{L6}	-10110→-1-111-1
V_{L7}	-1-1010→-1-1111
V_{L8}	0-1010→-1-1-111
V_{L9}	0-1-101→1-1-111
V_{L10}	10-101→1-1-1-11

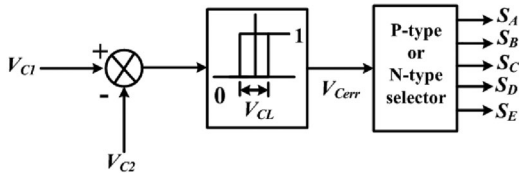


Fig. 6. Schematic for balancing the dc-link capacitor voltage.

TABLE IV
SWITCHING STATES CORRESPONDING TO SMALL VVS FOR THE PROPOSED DTC SCHEME

Small VV	DC-link capacitor voltage	Switching states
V_{S1}	$V_{\mathrm{Cerr}} = 1$	10000→11001
	$V_{\mathrm{Cerr}} = 0$	0-1-1-1-1 →00-1-10
V_{S2}	$V_{\mathrm{Cerr}} = 1$	11101 → 11000
	$V_{\mathrm{Cerr}} = 0$	000-10 → 00-1-1-1
V_{S3}	$V_{\mathrm{Cerr}} = 1$	01000 → 11100
	$V_{\mathrm{Cerr}} = 0$	-10-1-1-1 → 000-1-1
V_{S4}	$V_{\mathrm{Cerr}} = 1$	11110 → 01100
	$V_{\mathrm{Cerr}} = 0$	0000-1→-100-1-1
V_{S5}	$V_{\mathrm{Cerr}} = 1$	00100 → 01110
	$V_{\mathrm{Cerr}} = 0$	-1-10-1-1→-1000-1
V_{S6}	$V_{\mathrm{Cerr}} = 1$	01111 → 00110
	$V_{\mathrm{Cerr}} = 0$	-10000→-1-100-1
V_{S7}	$V_{\mathrm{Cerr}} = 1$	00010 → 00111
	$V_{\mathrm{Cerr}} = 0$	-1-1-10-1→-1-1000
V_{S8}	$V_{\mathrm{Cerr}} = 1$	10111→00011
	$V_{\mathrm{Cerr}} = 0$	0-1000→-1-1-100
V_{S9}	$V_{\mathrm{Cerr}} = 1$	00001→10011
	$V_{\mathrm{Cerr}} = 0$	-1-1-1-10→0-1-100
V_{S10}	$V_{\mathrm{Cerr}} = 1$	11011→10001
	$V_{\mathrm{Cerr}} = 0$	00-100→0-1-1-10

N-type switching state means that phases are connected to neutral point and the negative dc rail. P-type and N-type switching states mostly causes the neutral point voltage deviation. P-type states increase the lower dc-link capacitor voltage V_{C2}, whereas the N-type states decreases the lower dc-link capacitor voltage in motoring mode [39]. One of the modulation techniques for neutral point voltage balancing is to incorporate both type of switching states for equal time duration in one sample time [39]. But this increases the switching frequency.

In [40] and [41], Choudhury *et al.* have used the redundant switching states for three-phase NPC inverter depending upon the top and bottom dc-link capacitor voltages. If upper dc-link capacitor voltage V_{C1} is higher than the lower dc-link capacitor voltage V_{C2} then P-type switching states are applied and if $V_{C1} < V_{C2}$ then N-type switching states are applied for motoring mode. By using this technique the switching frequency is maintained at lower value as compared with techniques where neutral point is balanced using the both the redundant switching states for half of the duration in one sampling time.

For DTC operation, the smaller VVs used by the proposed DTC scheme are generated based on the technique proposed in [40] with little modification. The schematic of the proposed technique for balancing the dc-link capacitor voltage is shown

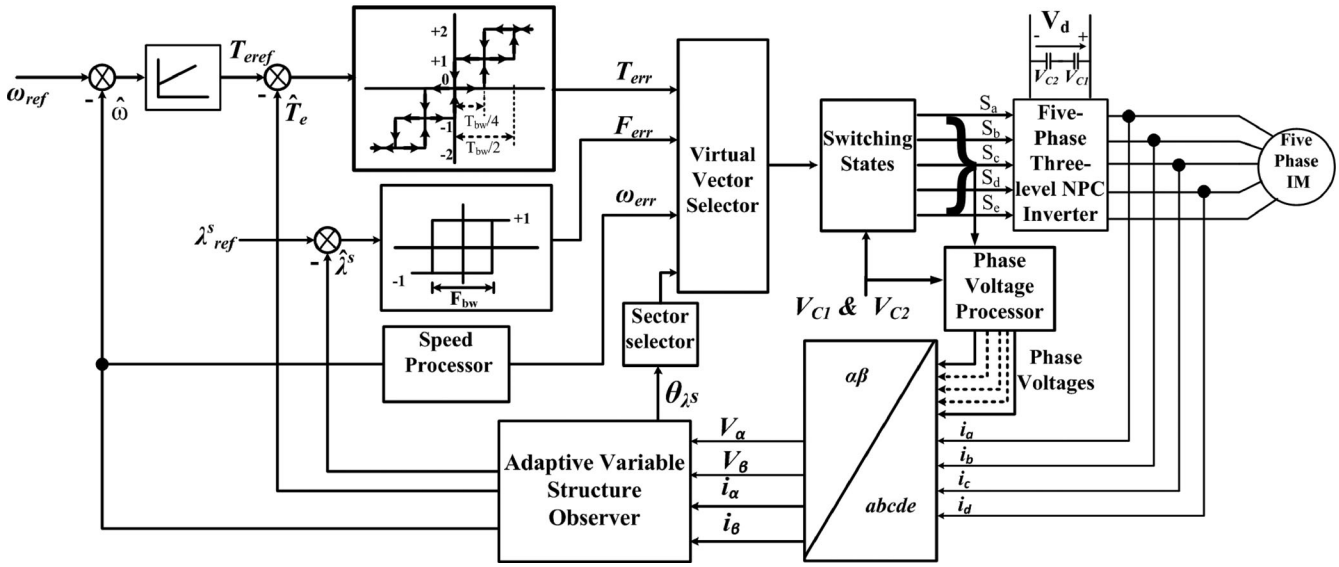


Fig. 7. Sensorless DTC scheme of FPIM using TL-NPC inverter.

in Fig. 6. In the proposed technique, the P-type and N-type switching states are selected based on the difference of the dc-link capacitor voltages. If the $|V_{C1} - V_{C2}|$ is greater than the limit of the difference in the capacitor voltage V_{CL}, then $V_{\rm Cerr}$ is either 1 or 0 depending upon the difference value. Otherwise the value of $V_{\rm Cerr}$ is retained. By doing this the switching frequency would be less as compared with the proposed technique of [40]. Now if $V_{\rm Cerr} = 1$ then P-type switching states are used else if $V_{\rm Cerr} = 0$ then N-type switching states are used for the motoring mode. In braking mode if $V_{\rm Cerr} = 1$ then N-type switching states are used else if $V_{\rm Cerr} = 0$ then P-type switching states are used. The switching states corresponding to small VVs for the proposed DTC scheme for motoring mode are given in Table IV.

IV. DTC of FPIM Using Three-Level NPC Inverter

DTC technique is used for the high-performance operation of FPIM drive. The DTC of FPIM using TL-NPC inverter is equally important because of the suitability of TL-NPC topology for high-power applications and other inherent advantages. The sensorless DTC operation of FPIM drive using TL-NPC inverter is shown in Fig. 7. Depending upon the stator flux angle θ_{λ^s}, sector is identified as per the Table V. The VVs are selected as per speed, torque, and flux error command. Two-level hysteresis flux band and five-level hysteresis torque band is used for the flux and torque control of FPIM drive. Speed adaptive variable structure observer given in [35] is used to observe the speed, flux, and torque of the FPIM. The details of variable structure observer is given in the Appendix. The logic for implementation of flux error is given by

$$\begin{aligned} \lambda^s_{\rm ref} - \lambda^s \geq F_{\rm bw} \quad F_{\rm err} = +1 \\ \lambda^s_{\rm ref} - \lambda^s \leq F_{\rm bw} \quad F_{\rm err} = -1 \end{aligned} \tag{14}$$

where $\lambda^s_{\rm ref}$, λ^s, $F_{\rm bw}$, and $F_{\rm err}$ are reference , actual stator flux of FPIM, flux hysteresis band width, and flux error signal, respectively. $F_{\rm err} = +1$ means flux has to be increased, whereas

TABLE V
Angle Corresponding to Sectors for the Proposed DTC Scheme

Sector	Subsector	$\theta_{\lambda s}$ corresponding to sector
1	a	$-18^\circ \leq \theta_{\lambda s} < 0^\circ$
	b	$0^\circ \leq \theta_{\lambda s} < 18^\circ$
2	a	$18^\circ \leq \theta_{\lambda s} < 36^\circ$
	b	$36^\circ \leq \theta_{\lambda s} < 54^\circ$
3	a	$54^\circ \leq \theta_{\lambda s} < 72^\circ$
	b	$72^\circ \leq \theta_{\lambda s} < 90^\circ$
4	a	$90^\circ \leq \theta_{\lambda s} < 108^\circ$
	b	$108^\circ \leq \theta_{\lambda s} < 126^\circ$
5	a	$126^\circ \leq \theta_{\lambda s} < 144^\circ$
	b	$144^\circ \leq \theta_{\lambda s} < 162^\circ$
6	a	$162^\circ \leq \theta_{\lambda s} < 180^\circ$
	b	$-180^\circ \leq \theta_{\lambda s} < -162^\circ$
7	a	$-162^\circ \leq \theta_{\lambda s} < -144^\circ$
	b	$-144^\circ \leq \theta_{\lambda s} < -126^\circ$
8	a	$-126^\circ \leq \theta_{\lambda s} < -108^\circ$
	b	$-108^\circ \leq \theta_{\lambda s} < -90^\circ$
9	a	$-90^\circ \leq \theta_{\lambda s} < -72^\circ$
	b	$-72^\circ \leq \theta_{\lambda s} < -54^\circ$
10	a	$-54^\circ \leq \theta_{\lambda s} < -36^\circ$
	b	$-36^\circ \leq \theta_{\lambda s} < -18^\circ$

$F_{\rm err} = -1$ means flux has to be decreased. The logic for torque is given by

$$\begin{aligned} T_{\rm eref} - T_e \geq +\frac{T_{\rm bw}}{2} \quad & T_{\rm err} = +2 \\ +\frac{T_{\rm bw}}{4} \leq T_{\rm eref} - T_e < +\frac{T_{\rm bw}}{2} \quad & T_{\rm err} = +1 \\ -\frac{T_{\rm bw}}{4} < T_{\rm eref} - T_e < \frac{T_{\rm bw}}{4} \quad & T_{\rm err} = 0 \\ -\frac{T_{\rm bw}}{4} \geq T_{\rm eref} - T_e > -\frac{T_{\rm bw}}{2} \quad & T_{\rm err} = -1 \\ T_{\rm eref} - T_e \leq -\frac{T_{\rm bw}}{2} \quad & T_{\rm err} = -2 \end{aligned} \tag{15}$$

TABLE VI
LOOKUP TABLE FOR DTC OPERATION OF FPIM USING PROPOSED DTC SCHEME

$\omega_{\rm err}$	$F_{\rm err}$	$T_{\rm err}$	Sector 1		2		3		4		5		6		7		8		9		10	
			a	b	a	b	a	b	a	b	a	b	a	b	a	b	a	b	a	b	a	b
1	1	2	V_{L2}	V_{L3}	V_{L3}	V_{L4}	V_{L4}	V_{L5}	V_{L5}	V_{L6}	V_{L6}	V_{L7}	V_{L7}	V_{L8}	V_{L8}	V_{L9}	V_{L9}	V_{L10}	V_{L10}	V_{L1}	V_{L1}	V_{L2}
		1	V_{S2}	V_{S3}	V_{S3}	V_{S4}	V_{S4}	V_{S5}	V_{S5}	V_{S6}	V_{S6}	V_{S7}	V_{S7}	V_{S8}	V_{S8}	V_{S9}	V_{S9}	V_{S10}	V_{S10}	V_{S1}	V_{S1}	V_{S2}
		0	V_0	V_0	V_0	V_0	V_0	V_0	V_0	V_0	V_0	V_0	V_0	V_0	V_0	V_0	V_0	V_0	V_0	V_0	V_0	V_0
		−1	V_{S9}	V_{S10}	V_{S10}	V_{S1}	V_{S1}	V_{S2}	V_{S2}	V_{S3}	V_{S3}	V_{S4}	V_{S4}	V_{S5}	V_{S5}	V_{S6}	V_{S6}	V_{S7}	V_{S7}	V_{S8}	V_{S8}	V_{S9}
		−2	V_{L9}	V_{L10}	V_{L10}	V_{L1}	V_{L1}	V_{L2}	V_{L2}	V_{L3}	V_{L3}	V_{L4}	V_{L4}	V_{L5}	V_{L5}	V_{L6}	V_{L6}	V_{L7}	V_{L7}	V_{L8}	V_{L8}	V_{L9}
	−1	2	V_{L4}	V_{L4}	V_{L5}	V_{L5}	V_{L6}	V_{L6}	V_{L7}	V_{L7}	V_{L8}	V_{L8}	V_{L9}	V_{L9}	V_{L10}	V_{L10}	V_{L1}	V_{L1}	V_{L2}	V_{L2}	V_{L3}	V_{L3}
		1	V_{S4}	V_{S4}	V_{S5}	V_{S5}	V_{S6}	V_{S6}	V_{S7}	V_{S7}	V_{S8}	V_{S8}	V_{S9}	V_{S9}	V_{S10}	V_{S10}	V_{S1}	V_{S1}	V_{S2}	V_{S2}	V_{S3}	V_{S3}
		0	V_0	V_0	V_0	V_0	V_0	V_0	V_0	V_0	V_0	V_0	V_0	V_0	V_0	V_0	V_0	V_0	V_0	V_0	V_0	V_0
		−1	V_{S7}	V_{S8}	V_8	V_{S9}	V_{S9}	V_{S10}	V_{S10}	V_{S1}	V_{S1}	V_{S2}	V_{S2}	V_{S3}	V_{S3}	V_{S4}	V_{S4}	V_{S5}	V_{S5}	V_{S6}	V_{S6}	V_{S7}
		−2	V_{L7}	V_{L8}	V_{L8}	V_{L9}	V_{L9}	V_{L10}	V_{L10}	V_{L1}	V_{L1}	V_{L2}	V_{L2}	V_{L3}	V_{L3}	V_{L4}	V_{L4}	V_{L5}	V_{L5}	V_{L6}	V_{L6}	V_{L7}
−1	1	2	V_{L2}	V_{L3}	V_{L3}	V_{L4}	V_{L4}	V_{L5}	V_{L5}	V_{L6}	V_{L6}	V_{L7}	V_{L7}	V_{L8}	V_{L8}	V_{L9}	V_{L9}	V_{L10}	V_{L10}	V_{L1}	V_{L1}	V_{L2}
		1	V_{S2}	V_{S3}	V_{S3}	V_{S4}	V_{S4}	V_{S5}	V_{S5}	V_{S6}	V_{S6}	V_{S7}	V_{S7}	V_{S8}	V_{S8}	V_{S9}	V_{S9}	V_{S10}	V_{S10}	V_{S1}	V_{S1}	V_{S2}
		0	V_0	V_0	V_0	V_0	V_0	V_0	V_0	V_0	V_0	V_0	V_0	V_0	V_0	V_0	V_0	V_0	V_0	V_0	V_0	V_0
		−1	V_{S9}	V_{S10}	V_{S10}	V_{S1}	V_{S1}	V_{S2}	V_{S2}	V_{S3}	V_{S3}	V_{S4}	V_{S4}	V_{S5}	V_{S5}	V_{S6}	V_{S6}	V_{S7}	V_{S7}	V_{S8}	V_{S8}	V_{S9}
		−2	V_{L9}	V_{L10}	V_{L10}	V_{L1}	V_{L1}	V_{L2}	V_{L2}	V_{L3}	V_{L3}	V_{L4}	V_{L4}	V_{L5}	V_{L5}	V_{L6}	V_{L6}	V_{L7}	V_{L7}	V_{L8}	V_{L8}	V_{L9}
	−1	2	V_{L4}	V_{L5}	V_{L5}	V_{L6}	V_{L6}	V_{L7}	V_{L7}	V_{L8}	V_{L8}	V_{L9}	V_{L9}	V_{L10}	V_{L10}	V_{L1}	V_{L1}	V_{L2}	V_{L2}	V_{L3}	V_{L3}	V_{L4}
		1	V_{S4}	V_{S5}	V_{S5}	V_{S6}	V_{S6}	V_{S7}	V_{S7}	V_{S8}	V_{S8}	V_{S9}	V_{S9}	V_{S10}	V_{S10}	V_{S1}	V_{S1}	V_{S2}	V_{S2}	V_{S3}	V_{S3}	V_{S4}
		0	V_0	V_0	V_0	V_0	V_0	V_0	V_0	V_0	V_0	V_0	V_0	V_0	V_0	V_0	V_0	V_0	V_0	V_0	V_0	V_0
		−1	V_{S8}	V_{S8}	V_{S9}	V_{S9}	V_{S10}	V_{S10}	V_{S1}	V_{S1}	V_{S2}	V_{S2}	V_{S3}	V_{S3}	V_{S4}	V_{S4}	V_{S5}	V_{S5}	V_{S6}	V_{S6}	V_{S7}	V_{S7}
		−2	V_{L8}	V_{L8}	V_{L9}	V_{L9}	V_{L10}	V_{L10}	V_{L1}	V_{L1}	V_{L2}	V_{L2}	V_{L3}	V_{L3}	V_{L4}	V_{L4}	V_{L5}	V_{L5}	V_{L6}	V_{L6}	V_{L7}	V_{L7}

where $T_{\rm eref}$, T_e, $T_{\rm bw}$, and $T_{\rm err}$ are reference, actual torque of FPIM, hysteresis band width for torque, and torque error signal, respectively. $T_{\rm err} = +2$ and $T_{\rm err} = +1$ means torque has to be increased. And $T_{\rm err} = -2$ and $T_{\rm err} = -1$ implies torque has to be decreased, whereas $T_{\rm err} = 0$ means that no change in torque is required. The VVs are selected depending upon the sector, speed, torque, and stator flux for the proposed scheme. Depending upon the direction of rotation, the speed processor block generates the speed error ($\omega_{\rm err}$) command. $\omega_{\rm err} = +1$ implies anticlockwise rotation of stator flux and $\omega_{\rm err} = -1$ implies clockwise rotation.

For a particular location of stator flux, an appropriate VV is selected to control the torque and flux of the IM. The VVs are selected in such a way that the effect of it on the torque and flux response of the IM is as per $T_{\rm err}$ and $F_{\rm err}$. The entire vector space is divided into ten sectors and each sector is further divided into two subsectors as shown in Fig. 4. Dividing of each sector into subsectors helps in the proper selection of VVs for efficient control of torque and flux of IM. Say, for anticlockwise rotation of stator flux ($\omega_{\rm err} = +1$), when $T_{\rm err} = +2$ and $F_{\rm err} = +1$ and stator flux is leaving sector 10_b and entering 1_a, the application of vector V_{L3} will have very little impact on the flux change. But, V_{L2} will increase the flux and torque of IM. Once the stator flux moves to subsector 1_b then V_{L3} will increase the both the torque and flux of the FPIM. Similarly, for other conditions of $T_{\rm err}$ and $F_{\rm err}$ VVs can be decided. When torque lies between the torque band of $+\frac{T_{\rm bw}}{4}$ and $+\frac{T_{\rm bw}}{2}$ or $-\frac{T_{\rm bw}}{4}$ and $-\frac{T_{\rm bw}}{2}$, *i.e.,* $T_{\rm err} = \pm 1$ smaller VVs are selected. Smaller VVs (V_{Sj}) have same effect as that of larger VVs (V_{Lj}) on the torque and flux response of the FPIM but of smaller magnitude. Depending upon the conditions of dc-link capacitor voltage V_{C1} and V_{C2}, the signal $V_{\rm Cerr}$ is decided and the switching states corresponding to Table IV is generated. This ensures the balancing of dc-link capacitor voltage without any additional hardware. The entire lookup table formed for the DTC operation is presented in Table VI.

The DTC scheme for FPIM using TL-NPC inverter is developed by *Tatte and Aware* in [37]. In that paper five-level hysteresis torque band and two-level hysteresis flux band was used to control the torque and flux of the FPIM. However, *Tatte and Aware* have not used the concept of VV, rather they have used the voltage vectors of magnitude $0.6472\,V_d$ and $0.3236\,V_d$ for $T_{\rm err} = \pm 2$ and $T_{\rm err} = \pm 1$, respectively, [like V_2 and V_4 and similar voltage vectors shown in Fig. 2(a)]. And for the vector of magnitude $0.3236\,V_d$ only one switching state is utilized, which does not ensure the balancing of dc-link capacitor voltage. In the coming section initially the DTC technique proposed in [37] is simulated and subsequently simulation and experiment of the proposed DTC scheme is presented.

V. SIMULATION AND EXPERIMENTAL VERIFICATIONS

The DTC of FPIM using TL-NPC inverter is carried out through simulation in MATLAB/Simulink environment and the results are verified experimentally on a 5 hp IM. The sampling time of 50 μs is taken for the DTC operation. The FPIM specifications and parameters are given in the Table VII.

A. Simulation Results

1) Tatte and Aware DTC Scheme: First, the simulation results based on the technique proposed by *Tatte and Aware* in [37] for DTC operation of FPIM using TL-NPC inverter is presented. For this scheme the lookup table given in [37] is utilized. The speed and corresponding torque of IM is shown in Fig. 8.

TABLE VII
SPECIFICATIONS AND PARAMETERS OF THE FPIM

Parameters/specifications	Value
FPIM rating	5 hp
Voltage	220 V per phase
Rated torque	23 N·m
Number of poles	4
Rated flux linkage	0.99 Wb
Frequency	50 Hz
Stator resistance (R_s)	7.2 Ω
Rotor resistance (R_r)	6.4 Ω
Stator leakage inductance (L_{ls})	0.043 H
Rotor leakage inductance (L_{lr})	0.043 H
Mutual inductance (L_m)	1.013 H
Inertia (J)	0.08 kg·m^2

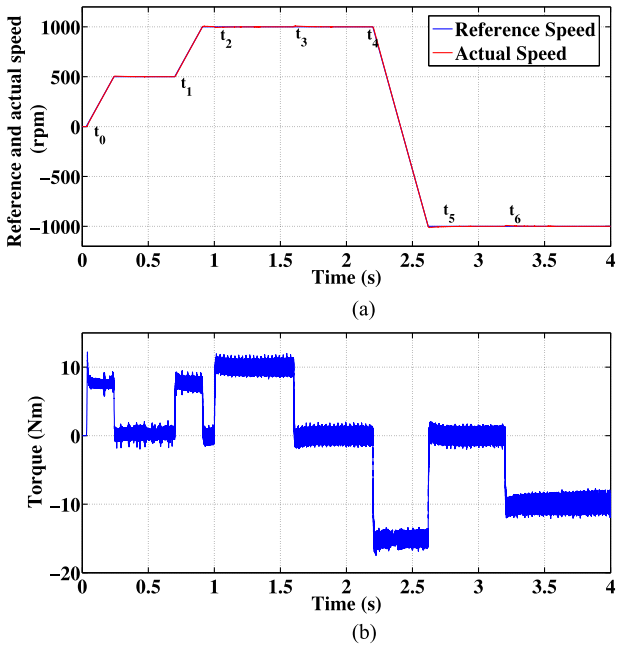


Fig. 8. Simulation results of (a) speed and (b) torque of IM for the control strategy proposed by *Tatte and Aware*.

At $t_0 = 0.03$ s a speed ramp from 0 to 500 r/min is applied with a rising rate of 1000 r/min·s. Again at $t_1 = 0.7$ s a ramp speed from 500 r/min is applied. At $t_2 = 1$ s a load torque of 10 N·m is applied, which is removed at $t_3 = 1.6$ s. At $t_4 = 2.2$ s a speed ramp from $+1000$ to -1000 r/min with a slope of -2000 r/min·s is given. At $t_5 = 3.2$ s, a load torque of -10 N·m is applied. It is observed that the actual speed of the FPIM follows the reference speed. The torque ripple is about 2.8 N·m. The $\alpha\beta$ and xy stator flux trajectories are shown in Fig. 9. The magnitude of $\alpha\beta$ flux is equal to the rated flux of 0.99 Wb as shown in Fig. 9(a). However, the magnitude of xy flux is 0.18 Wb, which is about 20% of the rated flux as observed from Fig. 9(b). The xy flux is not eliminated because no volt–second balance technique was applied by *Tatte and Aware* to cancel the resultant voltage vector in xy plane. From Fig. 10, it is observed that the dc-link capacitor voltages are not balanced as it was not considered in the DTC scheme proposed by *Tatte and Aware*.

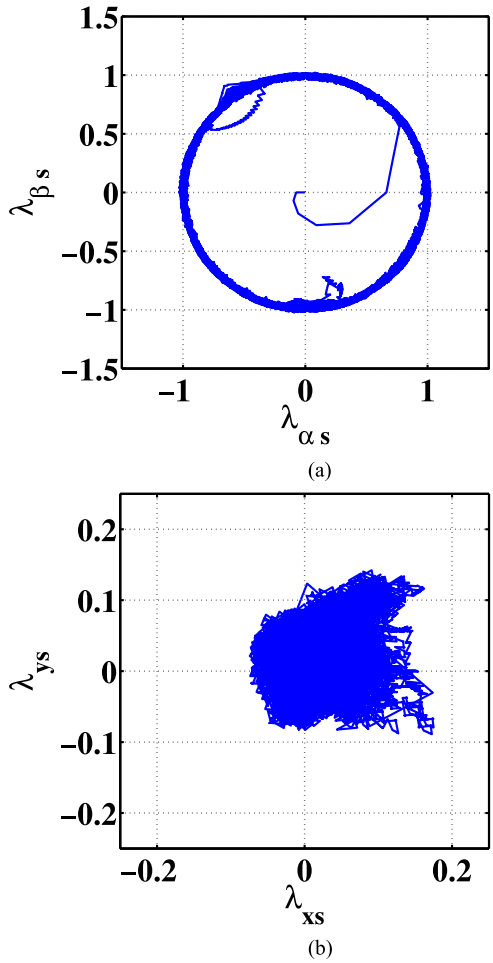


Fig. 9. Simulation results of stator (a) $\alpha\beta$ flux and (b) xy flux trajectory of IM for the DTC scheme proposed by *Tatte and Aware*.

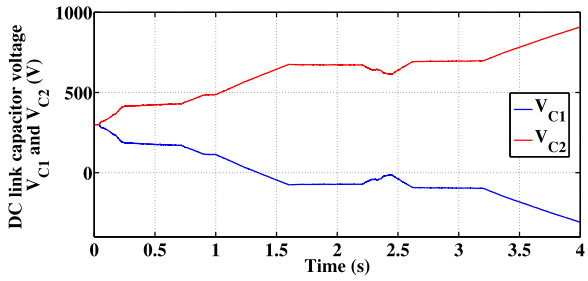


Fig. 10. Simulation results of dc-link capacitor voltages for the scheme proposed by *Tatte and Aware*.

2) Proposed DTC Scheme: The similar speed profile as shown in Fig. 8(a) is obtained for the proposed DTC scheme. The actual speed of the FPIM follows the reference speed. The corresponding torque of the FPIM is shown in Fig. 11. The torque ripple is about 1.6 N·m, which is about 42% lesser than torque ripple of the scheme proposed by *Tatte and Aware* [37].

Fig. 12 shows the stator $\alpha\beta$ and xy flux trajectory in the stationary reference frame of the IM for the proposed DTC scheme. It can be observed that the $\alpha\beta$ flux is maintained at its

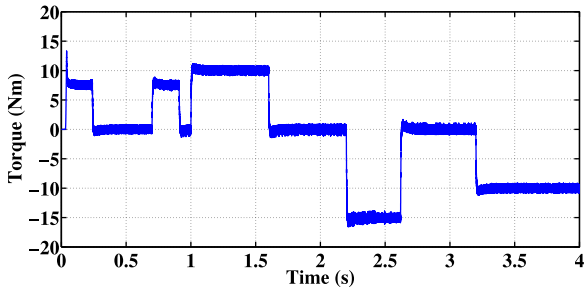


Fig. 11. Simulation results of torque profile of IM for the proposed DTC scheme.

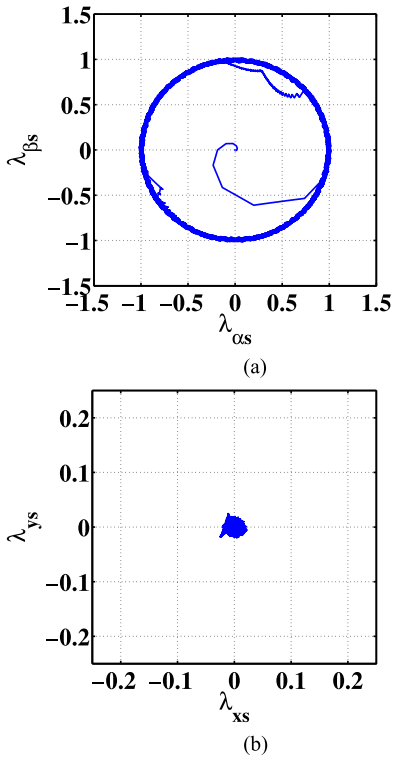


Fig. 12. Simulation results of stator (a) $\alpha\beta$ flux and (b) xy flux trajectory of IM for proposed DTC scheme.

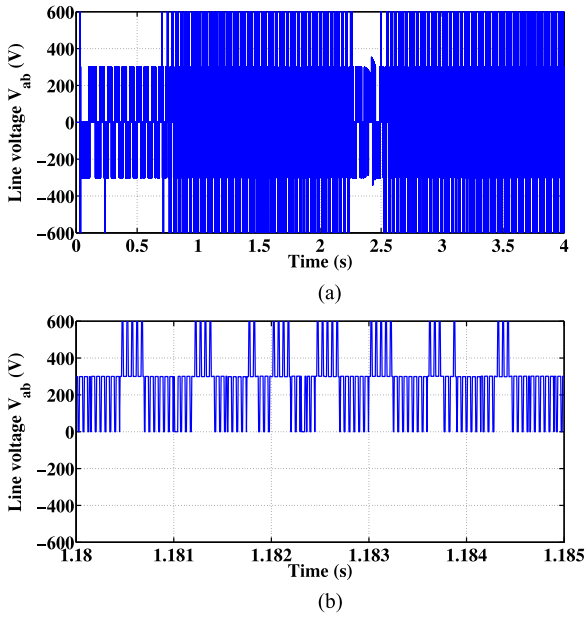


Fig. 13. Simulation results of (a) line voltage V_{ab} and (b) is zoomed in view of it for proposed DTC scheme.

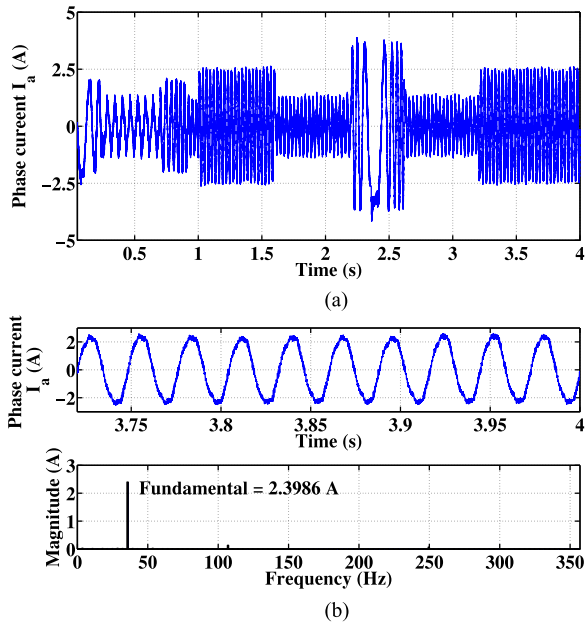


Fig. 14. Simulation results of (a) phase current I_a for entire cycle and its (b) harmonic spectrum for the proposed DTC scheme under loading condition.

rated value of 0.99 Wb. It can also be observed that the resultant xy flux has the magnitude lesser than 0.02 Wb, which is less than 2% of the reference stator flux.

Fig. 13 shows the line voltage V_{ab} and its zoomed in waveform for the proposed DTC scheme. From Fig. 13(b), it can be observed that there is smooth transition of voltage form one level to another. This maintains the low dv/dt stress on the power semiconductor switches. The current for the entire cycle and its harmonic spectrum for last ten cycles are shown in Fig. 14. The total harmonic distortion (THD) of the current is 5.19%. The dc-link capacitor voltage is shown in Fig. 15. It can be observed that the upper dc-link capacitor voltage V_{C1} and lower dc-link capacitor voltage V_{C2} are balanced. However, at the time of braking they deviates but once the FPIM comes in motoring mode, they are once again brought back to balance state. The dc-link capacitor voltages for the proposed DTC scheme is shown in Fig. 15. It is observed that the both the capacitor voltages are balanced even during the loading conditions. The variation in the dc-link capacitor voltage is about ± 2.5 V, which is less than $1\,\%$ of the half of the rated dc-link capacitor voltage.

B. Experimental Results

The proposed DTC scheme is validated through experimental investigations. The schematic of experimental setup is shown

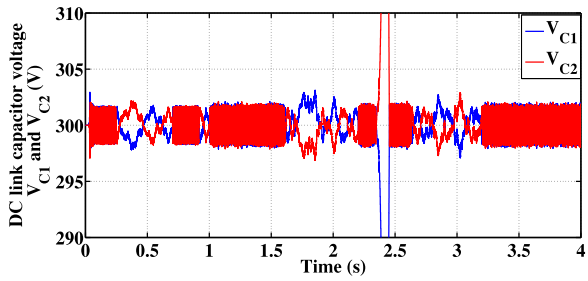


Fig. 15. Simulation results of dc-link capacitor voltage for proposed DTC scheme.

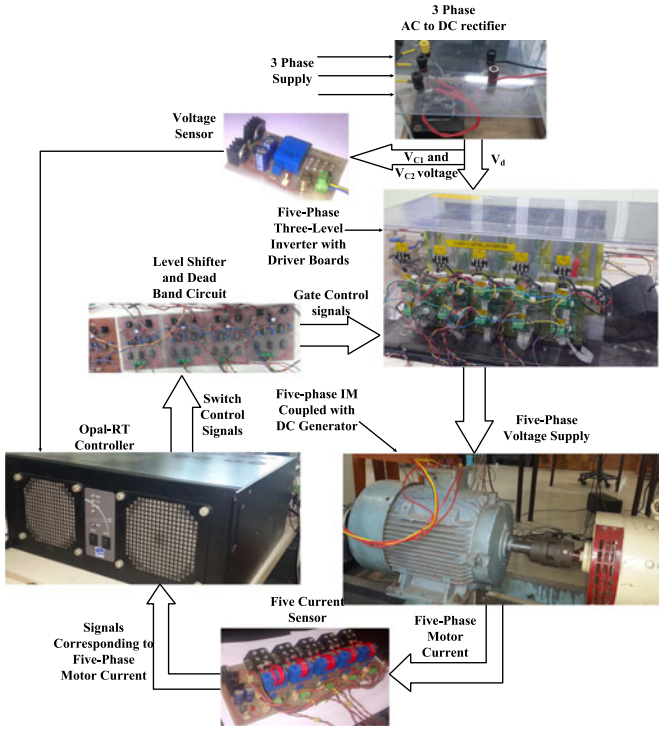


Fig. 16. Experimental schematic for DTC of FPIM using TL-NPC inverter.

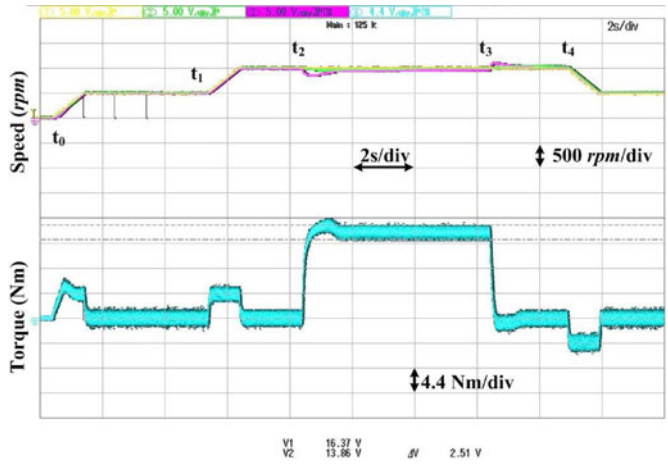


Fig. 17. Experimental results of speed and torque of the FPIM using proposed DTC scheme.

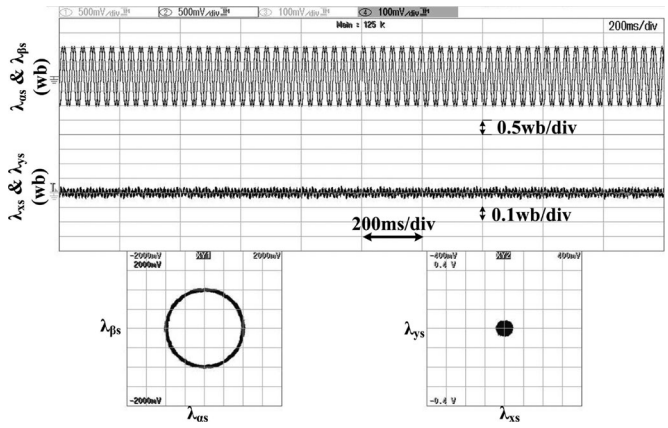


Fig. 18. Estimated stator flux of $\alpha\beta$ and xy plane and their trajectories for the proposed DTC scheme at 1000 r/min.

in Fig. 16. Five-phase TL-NPC inverter is developed using Semikron 150-MLI066-TAT IGBT modular switches. The controller is developed in OPAL-RT system. The FPIM currents and dc-link capacitor voltages of TL-NPC inverter are sensed using LEM current sensor (LA55P) and voltage sensor (LV25P), respectively. The dc-link capacitor voltages along with the switching states are used to generate the phase voltages. The phase voltages and currents are used by the speed adaptive variable structure observer to estimate the speed, torque, and stator flux. Depending upon the sector location of the stator flux in stationary reference frame, motor's speed, flux, and torque error command, the VVs are selected from the lookup table. And finally switching signals are generated corresponding to the VV. A dead time of 1.5 μs is incorporated at the rising edge of each gate signals generated by the controller to avoid the shoot through of the complementary switches. Also the control signals are made compatible as per the requirement of the driver circuit.

A dc generator of 3 kW coupled to the FPIM is used for loading purpose. Fig. 17 shows the speed and torque response of the FPIM. A reference speed ramp at different time instant is given and it is observed that the estimated and actual speed has same dynamic response. At time $t = t_2$ a load torque of 15 N·m is applied and it is removed at $t = t_3$. At the time of loading speed dips momentarily and it is regained after 1 s. After the load is removed there is speed jump but the controller brings back the FPIM speed to its reference value. The torque ripple observed is 2.5 N·m, which is almost 10% of the nominal torque of the FPIM. The FPIM was not loaded to its full capacity because of the limitations of the dc generator coupled with the FPIM.

The estimated stator $\alpha\beta$ and xy flux and its trajectories are shown in Fig. 18. It is observed that the stator $\alpha\beta$ flux linkage is maintained at its rated value of 0.99 Wb. The xy flux is almost eliminated and its magnitude is less than 0.05 Wb, which is slightly higher than the simulated results. This is because of the non linearities introduced by the introduction of dead time and transportation delay of the controller. The line voltage V_{ab} and its zoomed waveform is shown in Fig. 19. It is observed

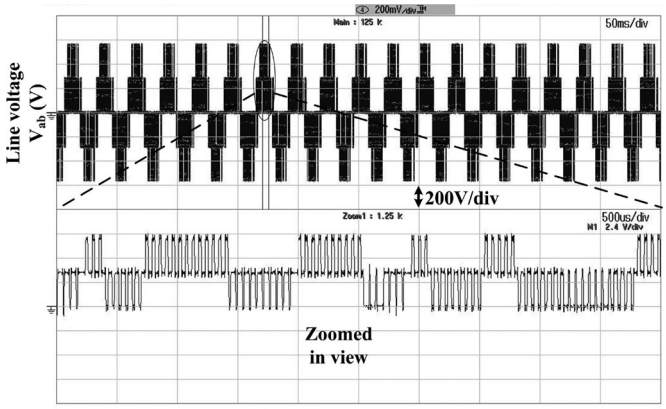


Fig. 19. Experimental results of line voltage V_{ab} and its zoomed waveform.

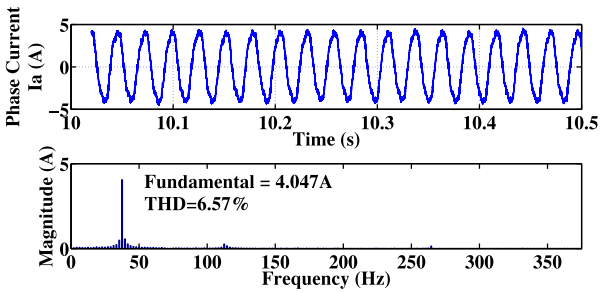


Fig. 20. Experimental phase current and its harmonics spectrum.

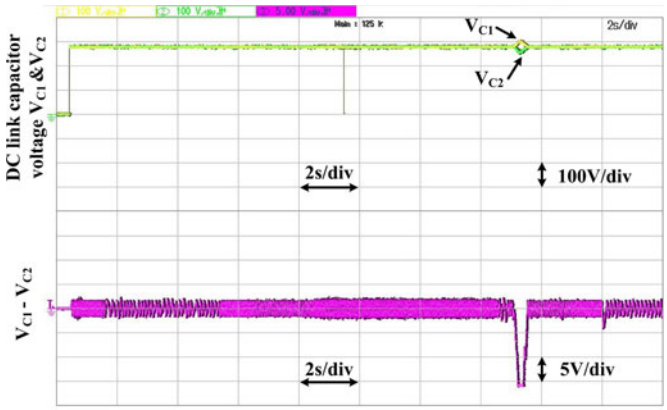


Fig. 21. Experimental results of dc-link capacitor voltage V_{C1} and V_{C2} and $V_{C1} - V_{C2}$.

from the waveform that there is no direct jump from zero to highest voltage level rather the jump is from zero to the mid of the voltage and then from mid to the upper level. This maintains the advantages of TL-NPC inverter of low dv/dt transition and lower stress on the power semiconductor switches. This maintains the advantages of TL-NPC inverter of low dv/dt transition and lower stress on the power semiconductor switches. The harmonic spectrum of the phase current of FPIM I_a is shown in Fig. 20. The data of current are imported into MATLAB and then its harmonic spectrum is plotted. The THD of the stator current is 6.57%, which is almost near to its simulated result.

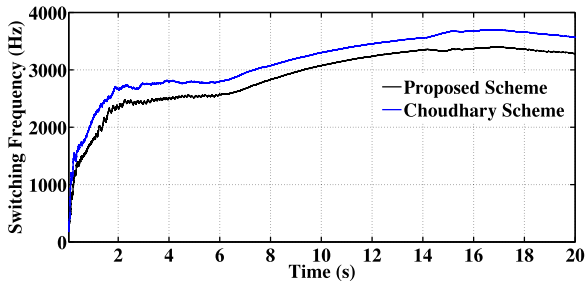


Fig. 22. Switching frequency of a switch corresponding to speed profile.

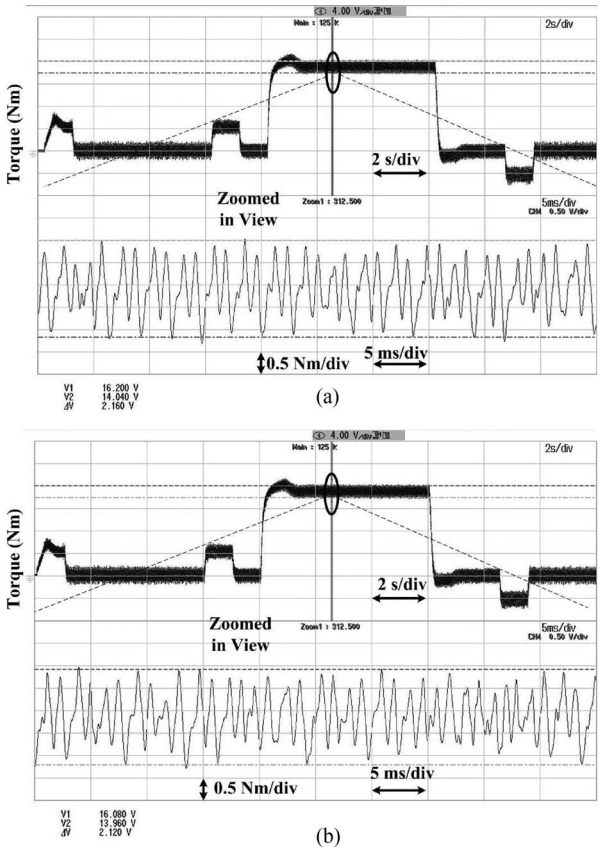


Fig. 23. Experimental results of torque and its zoomed in view, when (a) Choudhury *et al.* and (b) proposed neutral point voltage balancing scheme is incorporated in the DTC implementation of FPIM using TL-NPC.

Fig. 21 shows the dc-link capacitor voltages V_{C1}, V_{C2}, and there difference $V_{C1} - V_{C2}$. It can be observed from Fig. 21 that the dc-link capacitor voltages are almost balanced in the transition as well as steady-state condition. Also at low speed $(500\,\text{r/min})$ and no load the dc-link capacitor voltage is having ripple of lower frequency. This is because only smaller VVs are used to balance the dc-link capacitor voltages. At lower speed, the zero vector is applied for more duration as compared to smaller VV. Hence, the ripple is available in the neutral point voltage. It is also observed from $V_{C1} - V_{C2}$ waveform that the difference of magnitude lies between $\pm 3\,\text{V}$ which is around $1\,\%$ of half of the rated dc-link voltage. And this is within the limit of the designed controller. Fig. 22 shows the switching

frequency of a particular switch for the entire speed cycle of the proposed and the technique given by Choudhury *et al.* in [40] to balance the dc-link capacitor voltage. It can be observed that the switching frequency with the proposed dc link balancing scheme is around $8\,\%$ lower as compared with the scheme given by Choudhury *et al.*

Fig. 23(a) shows the experimental torque response when Choudhury *et al.* scheme for balancing the dc-link capacitor voltage is incorporated in the DTC scheme while Fig. 23(b) shows torque response for the proposed neutral point voltage scheme. By comparing both the figures of Fig. 23, it can be observed that both the neutral point voltage balancing scheme produce almost equal torque ripple. This is because the neutral point voltage balancing scheme comes into effect only when smaller VVs are selected and torque ripple in DTC technique mainly depends upon the hysteresis torque band and DTC sample time. The magnitude of vector decides the slope of torque ripple.

VI. Conclusion

In this paper, the DTC scheme of FPIM using TL-NPC inverter is presented. For the implementation of DTC technique using TL-NPC inverter, concept of VV is utilized. The VVs are synthesized using volt–second balancing technique such that the resultant voltage in xy plane is zero. The proposed scheme for DTC operation uses two voltage vectors to generate the large VVs and two for small VVs. The smaller VVs are generated from voltage vectors that have redundant switching states and there redundancy are used in a novel way to balance the dc-link capacitor voltage. The simulation results of one of the existing paper related to DTC of FPIM using TL-NPC inverter is carried out to show the superiority of the proposed DTC scheme. The proposed DTC scheme was verified using simulation in MATLAB/Simulink environment. And finally the simulation results were validated through experimental results. The proposed DTC scheme gave the lower dv/dt transitions, thus, having lower stress on the power semiconductor switches. The deviation in dc-link capacitor voltages was also within limit of 1% of the half of the rating of dc-link voltage. Also the proposed scheme to balance the dc-link capacitor voltage gave around 8% lower switching frequency as compared with one of the recently proposed technique.

Appendix

The state-space model of the fundamental space harmonic of FPIM is given in (16). *s* and *r* used as subscript or superscript are referred to stator and rotor variables, respectively. p is used as the first time derivative of a variable. The underlined variables are the matrices

$$\begin{aligned} p\underline{i}^s_{\alpha\beta} &= \left(-\frac{1}{T_s\sigma}-\frac{1-\sigma}{T_r\sigma}\right)\underline{i}^s_{\alpha\beta}+\frac{1-\sigma}{L_m\sigma}\left(\frac{1}{T_r-\omega j}\right)\underline{\lambda}_{\alpha\beta}\\ &\quad+\frac{1}{L_s\sigma}\underline{v}^r_{\alpha\beta}\\ p\underline{\lambda}^r_{\alpha\beta} &= \frac{L_m}{T_r}\underline{i}^s_{\alpha\beta}-\left(\frac{1}{T_r-\omega j}\right)\underline{\lambda}^r_{\alpha\beta} \end{aligned} \tag{16}$$

where $T_s = L_s/r_s$, $T_r = L_r/r_r$, and $\sigma = (L_sL_r - {L_m}^2/L_sL_r)$. The speed adaptive variable structure observer is formed as

$$\begin{aligned} p\hat{\underline{i}}^s_{\alpha\beta} &= \left(-\frac{1}{T_s\sigma 1}-\frac{1-\sigma}{T_r\sigma_1}\right)\hat{\underline{i}}^s_{\alpha\beta}+\frac{1-\sigma_1}{L_m\sigma}\left(\frac{1}{T_r-\omega j}\right)\hat{\underline{\lambda}}^r_{\alpha\beta}\\ &\quad+\frac{1}{L^s\sigma}\underline{v}^s_{\alpha\beta}+G_1\mathrm{sgn}(\underline{i}^s_{\alpha\beta}-\hat{\underline{i}}^s_{\alpha\beta})\\ p\hat{\underline{\lambda}}^r_{\alpha\beta} &= \frac{L_m}{T_r}\hat{\underline{i}}^s_{\alpha\beta}-\left(\frac{1}{T_r-\hat{\omega}j}\right)\hat{\underline{\lambda}}^r_{\alpha\beta}+\underline{G_2}G_1\mathrm{sgn}(\underline{i}^s_{\alpha\beta}-\hat{\underline{i}}^s_{\alpha\beta}). \end{aligned} \tag{17}$$

where $\underline{G_2}$ is a complex gain. The error dynamic equation is given by subtracting (17) from (16) as

$$\begin{aligned} p\Delta\underline{i}^s_{\alpha\beta} &= \left(-\frac{1}{T_s\sigma}-\frac{1-\sigma}{T_r\sigma}\right)\Delta\underline{i}^s_{\alpha\beta}\\ &\quad+\frac{1-\sigma}{L_m\sigma}\left(\frac{1}{T_r-\omega j}\right)\Delta\underline{\lambda}^r_{\alpha\beta}\\ &\quad-\frac{1-\sigma}{L_m\sigma}\Delta\omega j\hat{\underline{\lambda}}^r_{\alpha\beta}-G_1\mathrm{sgn}(\Delta\underline{i}^s_{\alpha\beta})\\ p\Delta\underline{\lambda}^r_{\alpha\beta} &= \frac{L_m}{T_r}\Delta\underline{i}^s_{\alpha\beta}-\left(\frac{1}{T_r-\omega j}\right)\Delta\underline{\lambda}^r_{\alpha\beta}+\Delta\omega j\hat{\underline{\lambda}}^r_{\alpha\beta}\\ &\quad-\underline{G_2}G_1\mathrm{sgn}(\Delta\underline{i}^s_{\alpha\beta}). \end{aligned} \tag{18}$$

To compensate for dynamic uncertainty, the gain G_1 should be large enough. In this condition the low frequency component of the current will converge to zero, i.e., $\Delta\underline{i}^s_{\alpha\beta} = p\Delta\underline{i}^s_{\alpha\beta} = 0$. The flux error dynamics is given by

$$\begin{aligned} \Delta\underline{\lambda}^r_{\alpha\beta} &= \left(\Delta\omega j\hat{\underline{\lambda}}^r_{\alpha\beta}+\frac{L_m\sigma}{1-\sigma}G_1\mathrm{sgn}(\Delta\underline{i}^s_{\alpha\beta})|_{\mathrm{eq}}\right)\\ &\quad\times\left(\frac{1}{T_r}-\omega j\right)^{-1} \end{aligned} \tag{19}$$

$$p\Delta\underline{\lambda}^r_{\alpha\beta} = \left(-\frac{L_m\sigma}{1-\sigma}-\underline{G_2}\right)G_1\mathrm{sgn}(\Delta\underline{i}^s_{\alpha\beta})|_{\mathrm{eq}}. \tag{20}$$

For stable operation the positive definite Lyapunov candidate function V is chosen in the form given by (21). The first derivative of V should be negative definite

$$V = \frac{1}{2}(\Delta{\lambda^r}^2_\alpha+\Delta{\lambda^r}^2_\beta)+\frac{\Delta\omega^2}{2\rho}\geq 0,\quad \rho>0. \tag{21}$$

The time derivative of V is given by (22). The dot represents the dot products of two vectors

$$pV = \Delta\underline{\lambda}^r_{\alpha\beta}.p\Delta\underline{\lambda}^r_{\alpha\beta}+\frac{\Delta\omega p\Delta\omega}{\rho}<0. \tag{22}$$

Substituting (20) and (21) in (22) gives

$$\begin{aligned} pV &= pV_1 + pV_2 \\ pV_1 &= \left(\frac{L_m\sigma}{1-\sigma}G_1\operatorname{sgn}(\Delta\underline{i}^s_{\alpha\beta})|_{\text{eq}}\left(\frac{1}{T_r-\omega j}\right)^{-1}\right) \\ &\quad \left(\left(-\frac{L_m\sigma}{1-\sigma}-\underline{G_2}\right)G_1\operatorname{sgn}(\Delta\underline{i}^s_{\alpha\beta})|_{\text{eq}}\right), pV_1<0 \\ pV_2 &= \frac{\Delta\omega p\Delta\omega}{\rho}+\left(\Delta\omega j\hat{\underline{\lambda}}^r_{\alpha\beta}\left(\frac{1}{T_r-\omega j}\right)^{-1}\right) \\ &\quad \left(\left(-\frac{L_m\sigma}{1-\sigma}-\underline{G_2}\right)G_1\operatorname{sgn}(\Delta\underline{i}^s_{\alpha\beta})|_{\text{eq}}\right), pV_2=0. \end{aligned} \tag{23}$$

For pV_1 to be negative definite the condition of (24) should be satisfied. The imaginary part of (24) should be zero to avoid oscillations during error convergence. Speed-dependent complex gain G_2 can be found by solving (24) by replacing the actual speed with the estimated speed

$$\frac{1-\sigma}{L_m\sigma}\left(-\frac{L_m\sigma}{1-\sigma}-\underline{G_2}\right)\left(\frac{1}{T_r}-\omega j\right)=\mu,\quad \mu<0. \tag{24}$$

The real and imaginary part of $\underline{G_2}$ is given by (25)

$$\begin{aligned} G_{2\text{real}} &= -\frac{L_m\sigma}{1-\sigma}\left(1+\frac{\mu T_r}{1+\hat{\omega}^2T^{r\,2}}\right) \\ G_{2i} &= -\frac{L_m\sigma}{1-\sigma}\left(\frac{\mu\hat{\omega}^rT^{r\,2}}{1+\hat{\omega}^2T^{r\,2}}\right) \end{aligned} \tag{25}$$

From (23) the speed adaptive equation can be found by solving $pV_2=0$. And the observed speed is given by

$$p\hat{\omega}^r = K_\omega\left(\operatorname{sgn}(i^s_\alpha-\hat{i}^s_\alpha)\hat{\lambda}^r_\beta-\operatorname{sgn}(i^s_\beta-\hat{i}^s_\beta)\hat{\lambda}^r_\alpha\right)+\frac{\hat{T}_e-\hat{T}_L}{J} \tag{26}$$

where $K_\omega>0$. The estimated electromagnetic torque T_e is given by

$$\hat{T}_e=\frac{5}{2}\frac{P}{2}\frac{L_m}{L^r}(\hat{\lambda}^r_\alpha\hat{i}_\beta)-(\hat{\lambda}^r_\beta\hat{i}^s_\alpha). \tag{27}$$

The adaptation mechanism is used to find the load torque and is given by

$$p\hat{T}_L=-K_t\left(\operatorname{sgn}(i^s_\alpha-\hat{i}^s_\alpha)\hat{\lambda}^r_\beta-\operatorname{sgn}(i^s_\beta-\hat{i}^s_\beta)\hat{\lambda}^r_\alpha\right) \tag{28}$$

where $K_t>0$. The stator flux components are estimated from the observed rotor flux obtained from (17) and is given by

$$\hat{\underline{\lambda}}^s_{\alpha\beta}=\frac{L_m}{L_r}\hat{\underline{\lambda}}^r_{\alpha\beta}+\sigma L_s\hat{\underline{i}}^s_{\alpha\beta}. \tag{29}$$

The resultant magnitude of the stator flux is given by

$$|\hat{\lambda}^s|=\sqrt{\left(\hat{\lambda}^s_\alpha\right)^2+\left(\hat{\lambda}^s_\beta\right)^2}. \tag{30}$$

REFERENCES

[1] E. Ward and H. Hrer, "Preliminary investigation of an invertor-fed 5-phase induction motor," *Proc. Inst. Electr. Eng.,*, vol. 116, no. 6, pp. 980–984, Jun. 1969.

[2] S. Williamson and S. Smith, "Pulsating torque and losses in multiphase induction machines," *IEEE Trans. Ind. Appl.*, vol. 39, no. 4, pp. 986–993, Jul. 2003.

[3] J. Apsley, S. Williamson, A. Smith, and M. Barnes, "Induction motor performance as a function of phase number," *IEE Proc. Electr. Power Appl.,* vol. 153, no. 6, pp. 898–904, Nov. 2006.

[4] H. Toliyat, T. Lipo, and J. White, "Analysis of a concentrated winding induction machine for adjustable speed drive applications. ii. motor design and performance," *IEEE Trans. Energy Convers.*, vol. 6, no. 4, pp. 684–692, Dec. 1991.

[5] R. O. C. Lyra and T. Lipo, "Torque density improvement in a six-phase induction motor with third harmonic current injection," *IEEE Trans. Ind. Appl.*, vol. 38, no. 5, pp. 1351–1360, Sep. 2002.

[6] D. Dujic, M. Jones, and E. Levi, "Analysis of output current ripple RMS in multiphase drives using space vector approach," *IEEE Trans. Power Electron.*, vol. 24, no. 8, pp. 1926–1938, Aug. 2009.

[7] E. Levi, "Multiphase electric machines for variable-speed applications," *IEEE Trans. Ind. Electron.*, vol. 55, no. 5, pp. 1893–1909, May 2008.

[8] E. Levi, R. Bojoi, F. Profumo, H. Toliyat, and S. Williamson, "Multiphase induction motor drives—A technology status review," *IET Electr. Power Appl.,*, vol. 1, no. 4, pp. 489–516, Jul. 2007.

[9] M. Jones and E. Levi, "A literature survey of state-of-the-art in multiphase ac drives," in *Proc. 37th Int. Univ. Power Eng. Conf.*, 2002, pp. 505–510.

[10] Q. Song, X. Zhang, F. Yu, and C. Zhang, "Research on PWM techniques of five-phase three-level inverter," in *Proc. Int. Symp. Power Electron., Electr. Drives, Autom. Motion, 2006*, May 2006, pp. 561–565.

[11] S. Kouro *et al.*, "Recent advances and industrial applications of multilevel converters," *IEEE Trans. Ind. Electron.*, vol. 57, no. 8, pp. 2553–2580, Aug. 2010.

[12] L. Franquelo, J. Rodriguez, J. Leon, S. Kouro, R. Portillo, and M. Prats, "The age of multilevel converters arrives," *IEEE Ind. Electron. Mag.,*, vol. 2, no. 2, pp. 28–39, Jun. 2008.

[13] J. Rodriguez, S. Bernet, B. Wu, J. Pontt, and S. Kouro, "Multilevel voltage-source-converter topologies for industrial medium-voltage drives," *IEEE Trans. Ind. Electron.*, vol. 54, no. 6, pp. 2930–2945, Dec. 2007.

[14] S. Lu and K. Corzine, "Multilevel multi-phase propulsion drives," in *Proc. 2005 IEEE Electr. Ship Technol. Symp.*, Jul. 2005, pp. 363–370.

[15] L. Gao and J. Fletcher, "A space vector switching strategy for three-level five-phase inverter drives," *IEEE Trans. Ind. Electron.*, vol. 57, no. 7, pp. 2332–2343, Jul. 2010.

[16] O. Lopez, J. Alvarez, J. Doval-Gandoy, and F. Freijedo, "Multilevel multiphase space vector PWM algorithm with switching state redundancy," *IEEE Trans. Ind. Electron.*, vol. 56, no. 3, pp. 792–804, Mar. 2009.

[17] S. Payami, R. K. Behera, A. Iqbal, and R. Al-Ammari, "Common-mode voltage and vibration mitigation of a five-phase three-level NPC inverter-fed induction motor drive system," *IEEE J. Emerg. Sel. Topics Power Electron.*, vol. 3, no. 2, pp. 349–361, Jun. 2015.

[18] O. Dordevic, M. Jones, and E. Levi, "A comparison of PWM techniques for three-level five-phase voltage source inverters," in *Proc. 2011-2014th Eur. Conf. Power Electron. Appl.*, Aug. 2011, pp. 1–10.

[19] O. Dordevic, M. Jones, and E. Levi, "A comparison of carrier-based and space vector PWM techniques for three-level five-phase voltage source inverters," *IEEE Trans. Ind. Informat.*, vol. 9, no. 2, pp. 609–619, May 2013.

[20] B. Sakthisudhursun, J. K. Pandit, and M. V. Aware, "Simplified three-level five-phase SVPWM," *IEEE Trans. Power Electron.*, vol. 31, no. 3, pp. 2429–2436, Mar. 2016.

[21] A. Iqbal, H. Abu-Rub, S. K. M. Ahmed, P. Cortes, and J. Rodriguez, "Model predictive current control of a three-level five-phase NPC VSI using simplified computational approach," in *Proc. 2014 IEEE Appl. Power Electron. Conf. Expo.*, Mar. 2014, pp. 2323–2330.

[22] A. Iqbal, H. Abu-Rub, S. M. Ahmed, P. Cortes, and J. Rodriguez, "Finite state model predictive current control of a three-level five-phase npc voltage source inverter," in *Proc. 36th Annu. Conf. IEEE Ind. Electron. Soc.*, Nov. 2010, pp. 2953–2958.

[23] I. Takahashi and Y. Ohmori, "High-performance direct torque control of an induction motor," *IEEE Trans. Ind. Appl.*, vol. 25, no. 2, pp. 257–264, Mar. 1989.

[24] M. Denpenbrock, "Direct self-control of inverter fed induction machine," *IEEE Trans. Power Electron.*, vol. 3, no. 4, pp. 420–429, Oct. 1986.

[25] Y.-S. Lai and J.-H. Chen, "A new approach to direct torque control of induction motor drives for constant inverter switching frequency and torque ripple reduction," *IEEE Trans. Energy Convers.*, vol. 16, no. 3, pp. 220–227, Sep. 2001.
[26] D. Casadei, F. Profumo, G. Serra, and A. Tani, "FOC and DTC: Two viable schemes for induction motors torque control," *IEEE Trans. Power Electron.*, vol. 17, no. 5, pp. 779–787, Sep. 2002.
[27] B. El Badsi, B. Bouzidi, and A. Masmoudi, "Bus-clamping-based DTC: An attempt to reduce harmonic distortion and switching losses," *IEEE Trans. Ind. Electron.*, vol. 60, no. 3, pp. 873–884, Mar. 2013.
[28] R. Zaimeddine and T. Undeland, "DTC control schemes for induction motor fed by three-level NPC-VSI using space vector modulation," in *Proc. 2010 Int. Symp. Power Electron. Electr. Drives Autom. Motion*, Jun. 2010, pp. 966–971.
[29] K.-B. Lee, J.-H. Song, I. Choy, and J.-Y. Yoo, "Torque ripple reduction in DTC of induction motor driven by three-level inverter with low switching frequency," *IEEE Trans. Power Electron.*, vol. 17, no. 2, pp. 255–264, Mar. 2002.
[30] Y. Zhang, J. Zhu, Z. Zhao, W. Xu, and D. G. Dorrell, "An improved direct torque control for three-level inverter-fed induction motor sensorless drive," *IEEE Trans. Power Electron.*, vol. 27, no. 3, pp. 1502–1513, Mar. 2012.
[31] H. Xu, H. Toliyat, and L. Petersen, "Five-phase induction motor drives with DSP-based control system," *IEEE Trans. Power Electron.*, vol. 17, no. 4, pp. 524–533, Jul. 2002.
[32] L. Parsa and H. A. Toliyat, "Five-phase permanent-magnet motor drives," *IEEE Trans. Ind. Appl.*, vol. 41, no. 1, pp. 30–37, Jan. 2005.
[33] L. Parsa and H. A. Toliyat, "Sensorless direct torque control of five-phase interior permanent-magnet motor drives," *IEEE Trans. Ind. Appl.*, vol. 43, no. 4, pp. 952–959, Jul. 2007.
[34] L. Gao, J. E. Fletcher, and L. Zheng, "Low-speed control improvements for a two-level five-phase inverter-fed induction machine using classic direct torque control," *IEEE Trans. Ind. Electron.*, vol. 58, no. 7, pp. 2744–2754, Jul. 2011.
[35] L. Zheng, J. Fletcher, B. Williams, and X. He, "A novel direct torque control scheme for a sensorless five-phase induction motor drive," *IEEE Trans. Indu. Electron.*, vol. 58, no. 2, pp. 503–513, Feb. 2011.
[36] A. Iqbal and E. Levi, "Space vector PWM techniques for sinusoidal output voltage generation with a five-phase voltage source inverter," *Electr. Power Compon. Syst.*, vol. 34, no. 2, pp. 119–140, 2006.
[37] Y. N. Tatte and M. V. Aware, "Torque ripple minimization in five-phase three-level inverter fed direct torque control induction motor drive," in *Proc. 17th Eur. Conf. Power Electron. Appl.*, Sep. 2015, pp. 1–6.
[38] O. Dordevic, E. Levi, and M. Jones, "A vector space decomposition based space vector PWM algorithm for a three-level seven-phase voltage source inverter," *IEEE Trans. Power Electron*, vol. 28, no. 2, pp. 637–649, Feb. 2013.
[39] B. Wu, *High-power converters and AC drives*. New York, NY, USA: Wiley, 2006.
[40] A. Choudhury, P. Pillay, and S. S. Williamson, "Dc-link voltage balancing for a three-level electric vehicle traction inverter using an innovative switching sequence control scheme," *IEEE J. Emerg. Sel. Topics Power Electron.*, vol. 2, no. 2, pp. 296–307, Jun. 2014.
[41] A. Choudhury and P. Pillay, "Reduced common mode voltage based DC-bus voltage balancing algorithm for three-level neutral point clamped (NPC) inverter drive," in *Proc. IEEE Energy Convers. Congr. Expo.*, Montreal, QC, Canada, Sep. 2015, pp. 4496–4501.

Saifullah Payami received the B. Tech. degree in electrical engineering and the M.Tech. degree in power system and drives from Aligarh Muslim University, Aligarh, India, in 2007 and 2010, respectively, and the Ph.D. degree in electrical engineering from Indian Institute of Technology Patna, Patna, India, in 2016.

He is currently working as a Research Fellow in Rolls Royce@NTU Corporate Laboratory, Nanyang Technological University, Singapore. His principal research interest includes power electronic converters, control of multi-phase motor drives, and renewable energy sources.

Ranjan Kumar Behera (SM'13) received the B.Eng. degree in electrical engineering from the Regional Engineering College (now NIT) Rourkela, Rourkela, India, and the M. Tech. and Ph.D. degrees in electrical engineering from Indian Institute of Technology Kanpur, Kanpur, India, in 1998, 2003, and 2009, respectively.

He worked at Hindustan Aeronautic Limited, Sunabeda, India, as a Trainee Engineer. Since May 2009, he is a faculty member in the Department of Electrical Engineering, IIT Patna, where he became the Head of the Department in January 2016. During July 2008–Feb. 2009, he was as a Visiting Scholar in the Energy Systems Research Center, Tennessee Technological University, USA, and also as a visiting research collaborator at ECE department, University of Pretoria, South Africa during July 2016. He published 50 articles in different national international journals and conference proceedings. His current research interests include power electronics, electric motor drives, and nonlinear control applications.

Dr. Behera received several national and international awards such as Young scientists award in engineering sciences, from DST, Government of India, in 2001, selected as the featured engineer of the globe 2015, and Bhaskara Advanced Solar Energy Indo-U.S. Science and Technology Forum, 2014.

Atif Iqbal (SM'09) received the B.Sc. (Gold Medal) degree in electrical engineering and M.Sc. Engineering degree in power system and drives from the Aligarh Muslim University (AMU), Aligarh, India, in 1991 and 1996, respectively, and the Ph.D. degree from Liverpool John Moores University, Liverpool, U.K., in 2006.

Since 1991, he has been employed as a Lecturer in the Department of Electrical Engineering, AMU, Aligarh, where he served as Full Professor until August 2016. He is currently an Associate Professor in the Department of Electrical Engineering, Qatar University, Doha, Qatar, and Former Full Professor in the Department of Electrical Engineering, AMU. He has published widely in International Journals and Conferences his research findings related to power electronics and renewable energy Sources. He has authored/coauthored more than 280 research papers and one book and two chapters in two other books. He has supervised several large R&D projects. His principal research interests include modeling and simulation of power electronic converters, control of multiphase motor drives and renewable energy sources.

Dr. Iqbal received the Maulana Tufail Ahmad Gold Medal for standing first at B.Sc. Eng. Exams in 1991 from AMU, Outstanding Faculty Merit Award AY 2014-2015 and Research excellence award at Qatar University. He has received best research papers awards at IEEE ICIT-2013 and IET-SESICON-2013. He is a Fellow of IE (India) and an Associate Editor of the IEEE TRANSACTION ON INDUSTRY APPLICATION.