Current Ripple Mechanism with Quantization in Digital *LLC* Converters for Battery Charging Applications

Zhiliang Zhang, *Senior Member, IEEE*, Ya-Qi Wu, Dong-Jie Gu, and Qianhong Chen, *Member, IEEE*

***Abstract*—The mechanism of current ripple propagation in a digital controlled *LLC* converter is investigated from three aspects: battery load, quantization error, and double line frequency perturbation at the input. With conventional frequency modulation (FM), every modulation step is accompanied by quantization error due to limited resolution of digital controllers. Large current ripple is propagated to the output due to poor FM and extremely low internal impedance of batteries, which hurts battery health seriously. The analytical model of output current oscillation is proposed considering the quantization effects and double line frequency input voltage perturbation. The synchronous frequency dither (FD) is proposed to improve quantization resolution and reduce current ripple further. A 2-kW Li-ion battery charger was built to verify the proposed current oscillation model and effectiveness of synchronous FD control. Good agreement is verified between analytical derivations and experimental results. The quantization current ripple is significantly attenuated by around 45% over entire charging range.**

***Index Terms*—Battery chargers, current ripple, digital control, frequency dither (FD), frequency modulation (FM), Li-ion batteries, *LLC* resonant converter, quantization resolution.**

I. Introduction

LITHIUM battery storage and charging issues become hot topics with fast development of electrical vehicles (EVs) [1], [2]. Recently, the charging current ripple problem has attracted more attention. The long-term impact of current ripple on the battery performance degradation is investigated in [3]. The experimental reports show that an increased level of capacity fade and power fade existed among the cells due to high frequency charging and discharging current ripple. Meanwhile, the surface temperature rising of the cells is noticeable due to ac coupled current ripple. For long cycle life of the Li-ion batteries, the constant current (CC) method was reported in [4] more suitable for slow charging. During the CC phase, it is important to reduce charging current ripple especially with high frequency to increase the battery life.

Various methods to reduce the charging current ripple are presented in [5] and [6]. However, these methods has not been effective to reduce the quantization current ripple since the current ripple under quantization effects in the battery charger has rarely been reported in the literature yet. Digital controllers provide an opportunity for implementing sophisticated control laws such as optimal trajectory control in [7] and universal adaptive synchronous rectification in [8] to improve the efficiency of *LLC* converters. However, it is well known that digital controlled pulse width modulation (PWM) and frequency modulation (FM) converters may exhibit undesirable limit-cycle oscillations (LCO) because of analog-to-digital converter (ADC) and digital PWM (DPWM), respectively. For double line frequency voltage ripple across the dc bus capacitance, the switching frequency of an *LLC* converter is modulated by the DPWM modules to realize well-regulated output current. Unfortunately, the switching frequency is modulated with a tolerance of one least significant bit (LSB).

Models and solutions of LCO are introduced in [9]–[13]. In [9], the static and dynamic models that include quantization effects are derived to explain the LCO root reason. Meanwhile, the resolution effects on digital controlled PWM converters and resonant converters are investigated in [10] and [11]. However, in [9]–[11], the focus was on the derivation of no-limit-cycle conditions associated with ADC and DPWM modules. The analytical results of LCO are based on the assumption that there is no perturbation at input. A PWM and FM hybrid control method is proposed in [12] to enhance the output voltage regulation of a 1-MHz *LLC* converter. However, this method is also limited by the resolution of DPWM modules. Dithering digital ripple correlation control is proposed in [13] to achieve high resolution and fast maximum power point tracking. However, these benefits are obtained by using additional hardware configuration.

In this paper, the current ripple propagation mechanism is investigated from three aspects: battery load, quantization error, and double line frequency perturbation at input. Then, the analytical model of output current oscillation is explored considering quantization effects and double line frequency perturbation at input. Synchronous frequency dither (FD) is proposed to improve the effective quantization resolution and further reduce

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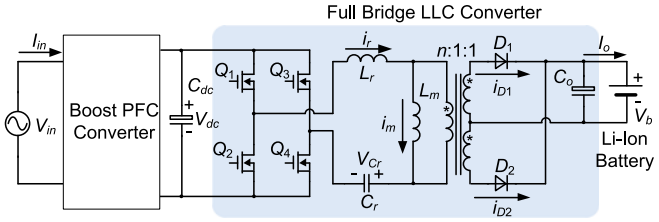


Fig. 1. Battery charger comprised of a boost PFC stage and a full bridge *LLC* stage.

TABLE I
EV ON-BOARD CHARGER SPECIFICATIONS

Input voltage	90–265 V (AC)	DC-link voltage	390 V
Output current	25 A	Power rating	2 kW
Battery cell voltage	3.0–4.2 V	Battery cell capacity	200 Ah
Battery pack voltage	64–80 V (20 cells)	Battery cell Type	Li (NiCoMn) O2

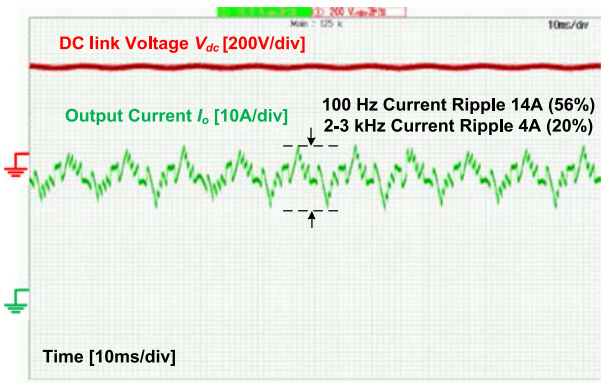


Fig. 2. Waveforms of the dc-link voltage and the charging current.

current ripple. A 2-kW on-board EV charger comprised of a boost PFC converter with a full bridge *LLC* converter was built to validate the analytical results of current oscillation and the effectiveness of the proposed synchronous FD.

II. MECHANISM OF CURRENT RIPPLE PROPAGATION

A typical two-stage battery charger is shown in Fig. 1. The battery charger specifications are listed in Table I. Fig. 2 shows the dc-link voltage and output current of the battery charger. It is observed that the average value of output current is 25 A. The large output current ripple is the superposition of current ripple at twice line frequency and unpredictable high-frequency current ripple due to quantization resolution.

A. Low Internal Impedance of Li-Ion Batteries

The equivalent circuit model of Li-Ion batteries is shown in Fig. 3. The classified sections in the battery model can be represented as follows:

1) the internal ohmic resistance $R_{\rm o}$;
2) the time constant formed by $R_D C_D$ and $R_T C_T$;
3) the open-circuit voltage $U_{\rm oc}$, which relates with the state of charge directly.

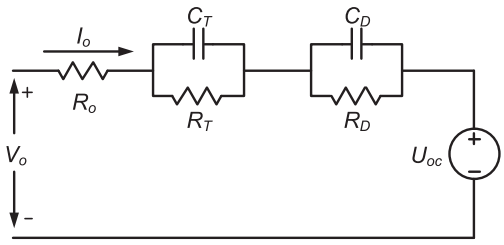


Fig. 3. Equivalent circuit of Li-ion batteries during charging procedure.

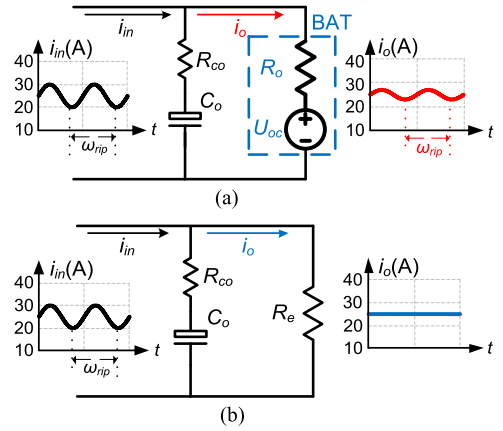


Fig. 4. Filtering performance comparison between battery load and equivalent resistive load. (a) Battery load. (b) Equivalent resistive load.

In this experimental testing, internal ohmic resistance R_o is obtained as 85 mΩ through dividing output voltage ripple 94 mV over output current ripple 1.1 A. The measured current ripple and voltage ripple are in phase, so the battery impedance can be modeled as a resistance.

The filter capacitor is often used in the output stage of *LLC* converters to pass the dc component but remove the components at switching frequency and its harmonics. The filtering performance comparison between the battery load and equivalent resistive load is shown in Fig. 4. Large low-frequency current ripple that mainly results from double line frequency pulsation and quantization resolution is contained in the input current of the filter network.

In order to simplify the derivation of output current ripple, following assumptions are made.

1) The ac component of input current is regarded as the superposition of two pure sinusoidal waveforms. One is at double line frequency, and the other is at oscillation frequency.
2) According to the superposition principle, two kinds of current ripple can be calculated separately and similarly. Thus, only one of two waveforms is considered in this analysis.

According to Kirchhoff's circuit laws, the ac component amplitude in the output current $I_{\rm rip}$ is given as

$$I_{\rm rip} = I_{in}\frac{\omega_{\rm rip} C_o R_{co} + 1}{\omega_{\rm rip} C_o (R_{\rm ac} + R_{co}) + 1} \tag{1}$$

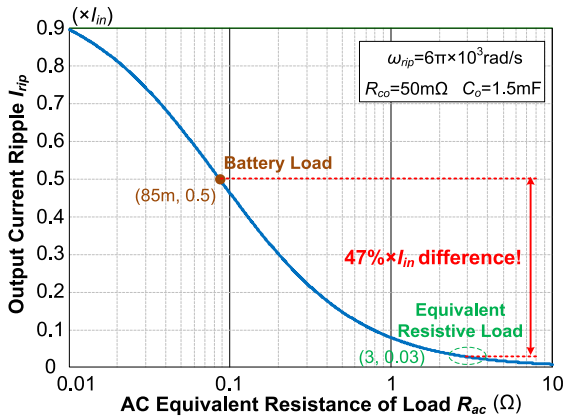


Fig. 5. Output current ripple with ac load resistance.

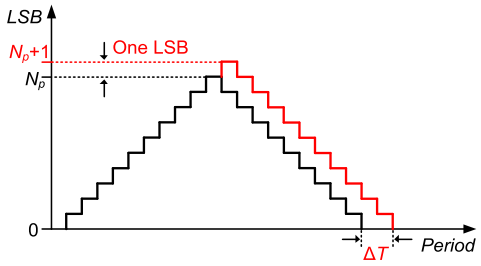


Fig. 6. Quantization effects.

where C_o is the output capacitance, R_{co} is the equivalent series resistance (ESR) of the output capacitor, and $R_{\rm ac}$ represents the load ac equivalent resistance.

It should be emphasized that the ac impedance of the battery load is much lower than the equivalent resistive load normally, which results in high current ripple. For a battery load, the ac resistance $R_{\rm ac}$ is internal impedance R_o. In contrast, the equivalent resistive load $R_{\rm eq} = V_b/I_o + R_o$, where V_b is battery pack voltage and I_o is charging current at the CC phase.

Output current ripple with ac load resistance is illustrated in Fig. 5. Under the same condition, the low battery impedance deteriorates the filtering performance of output capacitance. The current ripple with the battery load is higher as much as 47% of the input current ripple compared to the resistive load.

B. Quantization Resolution

The least regulation step in FM under quantization effects is illustrated in Fig. 6. The frequency generation by DPWM in the center-aligned mode is achieved by a counter incrementing and decrementing at the rate of system's clock $f_{\rm clk}$ (with no divisions). Meanwhile, the direction is switched whenever the counter reaches programmed value N_p or zero.

The least frequency modulation step (LFMS), $\Delta f_{\rm min}$, is regarded as difference between two nearest period settings (N_p) and ($N_p + 1$)

$$\Delta f_{\rm min} = \frac{f_{\rm clk}}{2N_p} - \frac{f_{\rm clk}}{2(N_p+1)} = \frac{f_{\rm clk}}{2N_p(N_p+1)} = \frac{f_s^2}{\frac{f_{\rm clk}}{2}+f_s}. \tag{2}$$

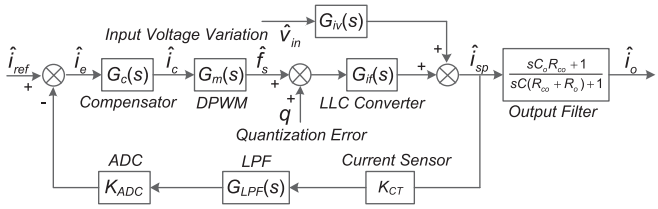


Fig. 7. Small-signal model of current regulator for an *LLC* converter.

According to (2), a 72-MHz clock generating a 100-kHz PWM signal results in a resolution limit of 0.28%.

C. Voltage Ripple at Twice Line Frequency

In [9]–[11], the limit cycle condition is derived assuming that there is no perturbation at input. However, as PFC is required, the input voltage of the *LLC* converter pulsates at double line frequency (for single-phase ac/dc applications) [14]. The limit cycle condition is no longer validated.

The peak-to-peak value of the voltage ripple across the dc-link capacitors is

$$\Delta V_{\rm dc} = \frac{P_o}{\eta \cdot \omega_l \cdot V_{\rm dc} \cdot C_{\rm dc}} \tag{3}$$

where P_o is constant output power, η is the efficiency of the charger, $C_{\rm dc}$ and $V_{\rm dc}$ are the dc-link capacitance and dc-link voltage, respectively, and ω_l is the line frequency in radians.

III. Proposed Analytical Model of Current Oscillation

The small-signal model of current regulator for the *LLC* converter is illustrated in Fig. 7. In the experimental prototype, the rectified current i_{sp} from the center-tapped transformer is sensed by the current transformer with gain K_{CT}. However, a large amount of second harmonics exists in the sensing signal. Therefore, additional low-pass filter (LPF) is added to attenuate the second harmonics. Since the LPF bandwidth is designed higher than the desired closed-loop bandwidth of the *LLC* converter, it will not affect the current ripple analysis. The low-frequency component of the rectified current i_{sp} and output current i_o can be regarded as identical since the output filter only filters high-frequency components of i_o. Thus, we have $\hat{i}_{sp}(s) = \hat{i}_o(s)$. The transfer function of current sampling circuit is denoted as $G_{\rm LPF}(s)$. The sampled output signal is compared with the reference current. The frequency modulator is modeled as $G_m(s)$. $G_c(s)$ is the PI compensator, $G_{iv}(s)$ is input-to-current transfer function, and $G_{if}(s)$ is control-to-current transfer function. All variables in the control circuit diagram are perturbed and linearized around their quiescent points. The *LLC* converter contains two independent inputs: control input variation $\hat{f}_s$, and input voltage variation $\hat{v}_{in}$. The quantization error q is caused by round-off of PI results into digital representation N_p, which further results in large current ripple at the output.

The output current variation can be expressed as a linear combination of two independent inputs:

$$\hat{i}_o(s) = G_{if}(s)(\hat{f}_s(s) + q) + G_{iv}(s)\hat{v}_{in}(s) \tag{4}$$

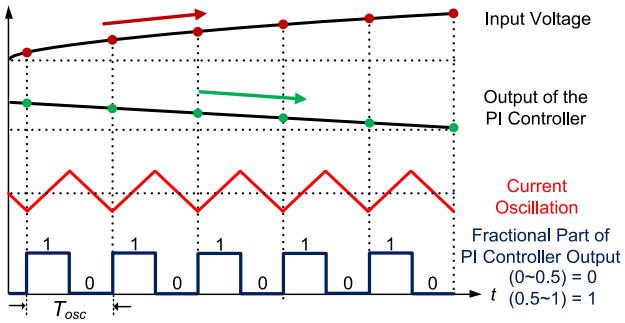


Fig. 8. Behavior of current oscillation by quantization error.

where the control-to-output transfer function $G_{if}(s) = \hat{i}_o(s)/\hat{f}_s(s)|_{\hat{v}_{in}(s)=0}$, and the input-to-output transfer function is $G_{iv}(s) = \hat{i}_o(s)/\hat{v}_{in}(s)|_{\hat{f}_s(s)=0}$.

In the CC phase, the current reference is constant, so $\hat{i}_{\rm ref} = 0$. From the feedback loop in Fig. 7, the control input variation is

$$\hat{f}_s = K_{\rm ADC} G_{\rm LPF}(s) G_c(s) G_m(s) \hat{i}_o \tag{5}$$

where $K_{\rm ADC}$ is the static gain of the ADC modules.

Substituting (5) into (4), the output variation is given as

$$\hat{i}_o(s) = \frac{G_{if}(s)}{1+T(s)} q + \frac{G_{iv}(s)}{1+T(s)} \hat{v}_{in}(s) \tag{6}$$

where the loop gain $T(s) = K_{\rm ADC} G_{\rm LPF}(s) G_c(s) G_m(s) G_{if}(s)$.

The first term in (6) is current variation resulting from quantization error, which is defined as $\hat{i}_q(s)$. Similarly, the second term represents current variation caused by double line frequency voltage variation, which is defined as $\hat{i}_d(s)$. So, we have

$$\hat{i}_d(s) = \frac{G_{iv}(s)}{1+T(s)} \hat{v}_{in}(s) \quad \hat{i}_q(s) = \frac{G_{if}(s)}{1+T(s)} q. \tag{7}$$

From (7), it is found that the transfer function from disturbance to output current is multiplied by a factor $1/[1+T(s)]$. If the loop gain $T(s)$ is large enough in magnitude, the reduction is significant. Hence, the output current variation resulting from input voltage variation is attenuated by the feedback loop.

However, the current variation caused by quantization error cannot be attenuated by high loop gain at oscillation frequency. Because the quantization error is unavoidable, increasing the bandwidth of the controller can lead to large oscillation and even cause system unstable. So, the loop gain at oscillation frequency $\omega_{\rm osc}$ (in rad/s) should be limited by

$$\|T(j\omega_{\rm osc})\| << 1. \tag{8}$$

Assuming that the output current is well regulated, which means $\hat{i}_o = 0$. From (4), the relationship of frequency variation and input voltage disturbances is given as

$$\left.\frac{\hat{f}_s(s)}{\hat{v}_{in}(s)}\right|_{\hat{i}_o(s)=0} = -\frac{G_{iv}(s)}{G_{if}(s)}. \tag{9}$$

The current oscillation behavior is illustrated in Fig. 8. Because the current oscillation frequency is much higher than the double line frequency, it can assume that the input voltage increases linearly in oscillation period $T_{\rm osc}$. In order to realize well-regulated output current, the output of PI controller decreases linearly to compensate input voltage variation. Unfortunately, the effective number of bits that might be used to represent switching period is limited. Therefore, the controller output rounding is unavoidable. If the output fractional part is less than 0.5, this part is truncated. On the contrary, the integral part is increased by 1 when the factional part is larger than 0.5. The current oscillation is induced by output quantization.

The ac component of the dc-link voltage can be regarded as a pure sine wave at double line frequency, which is

$$V_{\rm ac} = \frac{\Delta V_{\rm dc}}{2} \sin(2\omega_l t). \tag{10}$$

From (10), the input voltage variation in one current oscillation period is given as

$$\Delta V_{\rm osc} = \frac{\Delta V_{\rm dc}}{2} \left|\sin(2\omega_l t + 2\omega_l T_{\rm osc}) - \sin(2\omega_l t)\right|. \tag{11}$$

According to (11), the input voltage variation is not constant in double line cycle, which means the current oscillation frequency is not constant. Considering the PI controller in the feedback loop, the low-frequency current ripple is greatly attenuated owing to high loop gain. The current oscillation period can approximately deduced by the average input voltage variation $\overline{\Delta V_{\rm osc}}$, which is given as

$$\overline{\Delta V_{\rm osc}} = \frac{1}{\pi} \int_{-\frac{\pi}{2}-\omega_l T_{\rm osc}}^{\frac{\pi}{2}-\omega_l T_{\rm osc}} \Delta V_{\rm osc} d\theta \approx \frac{2\omega_l T_{\rm osc}}{\pi} \Delta V_{\rm dc}. \tag{12}$$

As shown in Fig. 8, the switching frequency is increased by LFMS in every current oscillation period. Combining (2) and (9), the average input voltage variation is derived as

$$\overline{\Delta V_{\rm osc}} = \frac{\|G_{if}(j2\omega_l)\|}{\|G_{iv}(j2\omega_l)\|} \Delta f_{\rm min}. \tag{13}$$

Thus, the current oscillation period can be obtained by solving (12) and (13) as

$$T_{\rm osc} = \frac{\eta\pi C_{\rm dc} V_{\rm dc} f_s^2}{(2f_s + f_{\rm clk}) P_o} \frac{\|G_{if}(j2\omega_l)\|}{\|G_{iv}(j2\omega_l)\|}. \tag{14}$$

As shown in Fig. 8, maximum quantization error occurs at beginning of every current oscillation period. So, the peak-to-peak value of the current oscillation is given as

$$\Delta I_q = \|G_{if}(j\omega_{\rm osc})\| \cdot q_m \tag{15}$$

where $q_{\rm m}$ is the maximum round-off error in the digital controller, which is one half of LFMS $\Delta f_{\rm min}$.

However, due to the requirement of high loop gain at double line frequency, the loop gain at oscillation frequency cannot completely meet the requirement in (8). Under this circumstance, the integral term responds to accumulated errors from the oscillation. Thus, larger oscillation is caused by LFMS, which is

$$\Delta I_{ql} = \|G_{if}(j\omega_{\rm osc})\| \cdot \Delta f_{\rm min}. \tag{16}$$

A. Oscillation Current Model Derived by Fundamental-Harmonic Approximation (FHA)

The key point of FHA is assuming the fundamental harmonic of the primary current sending power. So, the actual primary current is replaced by a sine wave current for analysis. The normalized dc gain M is given as

$$M = \frac{n \cdot V_o}{V_{\rm dc}} = \frac{1}{\sqrt{\left(1+\frac{1}{\lambda}-\frac{1}{\lambda \cdot {f_n}^2}\right)^2 + Q^2 \cdot \left(\frac{1}{f_n} - f_n\right)^2}} \quad (17)$$

where λ is the inductance ratio, and $\lambda = L_m/L_r$, L_m is the magnetic inductance and L_r is the resonant inductance; f_r is the resonant frequency, $f_r = 1/2\pi\sqrt{L_r C_r}$, C_r is the resonant capacitor; Z_r is the characteristic impedance, $Z_r = \sqrt{L_r/C_r}$; f_n is the normalized switching frequency, $f_n = f_s/f_r$; and Q is the quality factor, $Q = \pi^2 Z_r/8n^2 R_L$, R_L is the load resistance, $R_L = V_o/I_o$, n is the turns ratio.

The small-signal frequency-to-voltage gain of power stage can be calculated by taking the derivative of (17). The frequency-to-voltage gain $\|G_{vf}\|$ is given as

$$\|G_{vf}(f_n)\| = \frac{V_{\rm dc}}{n} \cdot \left|\frac{\partial M}{\partial f_n}\right|$$

$$= \frac{V_{\rm dc}}{n} \cdot \frac{\left(1+\frac{1}{\lambda}-\frac{1}{\lambda \cdot {f_n}^2}\right) \cdot \left(\frac{2}{\lambda \cdot {f_n}^3}\right) - \left(\frac{1}{f_n} - f_n\right) \cdot \left(\frac{1}{{f_n}^2}+1\right) \cdot Q^2}{\left[\sqrt{\left(1+\frac{1}{\lambda}-\frac{1}{\lambda \cdot {f_n}^2}\right)^2 + \left(\frac{1}{f_n} - f_n\right)^2 \cdot Q^2}\right]^3}. \quad (18)$$

It should be noted that (18) is valid under the assumption that response of the resonant network to frequency changes is instantaneous as compared to the control bandwidth and its effect on system dynamic behavior is negligibly small.

Similarly to (18), the input-to-output voltage gain $\|G_{vv}\|$ is

$$\|G_{vv}(f_n)\| = \frac{M}{n} = \frac{1}{n\sqrt{\left(1+\frac{1}{\lambda}-\frac{1}{\lambda \cdot {f_n}^2}\right)^2 + Q^2 \cdot \left(\frac{1}{f_n} - f_n\right)^2}}. \quad (19)$$

According to (2), the normalized LFMS Δf_n is

$$\Delta f_n = \frac{f_n^2}{f_n + \frac{f_{\rm clk}}{2f_r}}. \quad (20)$$

Assuming that output current is well regulated, average input variation in one oscillation period is related with the normalized LFMS in (20), which is

$$\overline{\Delta V_{\rm osc}} = \frac{V_{\rm dc} f_n^2}{f_n + \frac{f_{\rm clk}}{2f_r}} \cdot \frac{\left(1+\frac{1}{\lambda}-\frac{1}{\lambda \cdot {f_n}^2}\right) \cdot \left(\frac{2}{\lambda \cdot {f_n}^3}\right) - \left(\frac{1}{f_n} - f_n\right) \cdot \left(\frac{1}{{f_n}^2}+1\right) \cdot Q^2}{\left(1+\frac{1}{\lambda}-\frac{1}{\lambda \cdot {f_n}^2}\right)^2 + \left(\frac{1}{f_n} - f_n\right)^2 \cdot Q^2}. \quad (21)$$

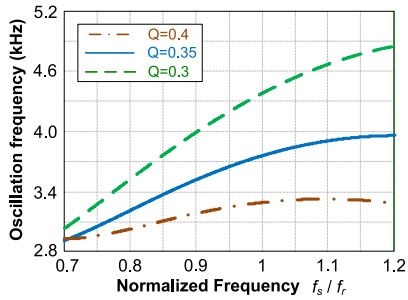


Fig. 9. Oscillation frequency with normalized frequency.

Combining (3), (14), (18)–(20), the current oscillation period is solved by

$$T_{\rm osc} = \frac{\eta\pi C_{\rm dc} V_{\rm dc}^2 f_n^2}{(2f_n + \frac{f_{\rm clk}}{f_r})P_o} \cdot \frac{\left(1+\frac{1}{\lambda}-\frac{1}{\lambda \cdot {f_n}^2}\right) \cdot \left(\frac{2}{\lambda \cdot {f_n}^3}\right) - \left(\frac{1}{f_n} - f_n\right) \cdot \left(\frac{1}{{f_n}^2}+1\right) \cdot Q^2}{\left(1+\frac{1}{\lambda}-\frac{1}{\lambda \cdot {f_n}^2}\right)^2 + \left(\frac{1}{f_n} - f_n\right)^2 \cdot Q^2}. \quad (22)$$

From (22), the oscillation period of quantization current ripple with normalized frequency is illustrated in Fig. 9. As the switching frequency increases, the current ripple oscillation frequency also increases accordingly.

According to the equivalent circuit of Li-ion batteries in Fig. 3, the control-to-current gain $\|G_{if}\|$ is given as

$$\|G_{if}(f_n)\| = \frac{\|G_{vf}(f_n)\|}{R_o}. \quad (23)$$

However, (23) is only valid at low frequency, where control-to-current gain is nearly constant. Due to the filter network impact, the control-to-current gain decreases significantly at middle frequency range. So, it is necessary to calculate current ripple considering the gain attenuation of filter network.

Substituting (1) and (23) into (15), the relationship of charging current ripple and normalized frequency can be expressed by

$$\Delta I_{ql} = \frac{V_{\rm dc} f_n^2}{nR_o(f_n + \frac{f_{\rm clk}}{2f_r})} \cdot \frac{\left(1+\frac{1}{\lambda}-\frac{1}{\lambda \cdot {f_n}^2}\right) \cdot \left(\frac{2}{\lambda \cdot {f_n}^3}\right) - \left(\frac{1}{f_n} - f_n\right) \cdot \left(\frac{1}{{f_n}^2}+1\right) \cdot Q^2}{\left[\sqrt{\left(1+\frac{1}{\lambda}-\frac{1}{\lambda \cdot {f_n}^2}\right)^2 + \left(\frac{1}{f_n} - f_n\right)^2 \cdot Q^2}\right]^3} \cdot \frac{\omega_{osc} C_o R_{co} + 1}{\omega_{osc} C_o (R_o + R_{co}) + 1}. \quad (24)$$

From (24), the peak-to-peak value of quantization current ripple with normalized frequency is illustrated in Fig. 10. As the switching frequency decreases to obtain high voltage gain, the current ripple amplitude increases even higher. According to (24), the parameters of the *LLC* power stage can be tuned to reduce current ripple. However, the tolerance of resonant components may reduce the effectiveness of current ripple reduction.

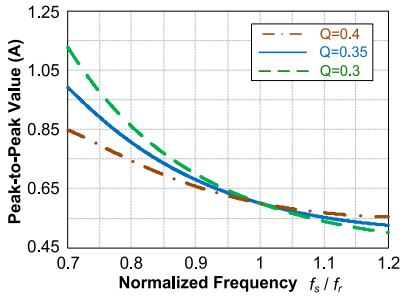


Fig. 10. Peak-to-peak value with normalized frequency.

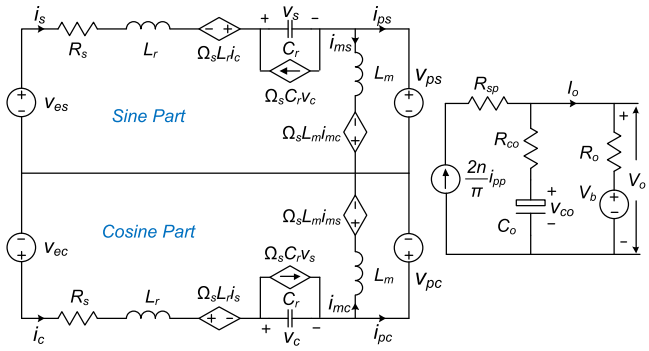


Fig. 11. Large signal model of an *LLC* converter.

B. Oscillation Current Model Derived by Extended Describing Functions (EDF) Considering Damping Effects

The EDF technique is first proposed in [15] to develop small-signal models of a series-resonant converter and a parallel-resonant converter, which combines the time-domain and frequency-domain analysis and extracts the model by dividing modulated waveforms into sine and cosine waveforms. The sine components and cosine components of state variables are slow time-varying components. Therefore, the dynamic behavior of these parameters can be analyzed.

The large signal model of the *LLC* converter is shown in Fig. 11. This model is derived by harmonic balance, which is a frequency domain method used to calculate steady-state response of nonlinear differential equations. Using the sinusoidal approximation, the three state variables i_r, v_{cr}, i_m are decomposed into sine part and cosine part of the fundamental components. The method assumes that the solution can be represented by a linear combination of sinusoids, and then balances current and voltage sinusoids to satisfy Kirchhoff's laws. The ESR of the output capacitor R_{co} is considered to develop this model. The parasitic resistance of the primary side R_s (on resistance of MOSFETs, ESR of the resonant inductor) and secondary side R_{sp} (simulate the secondary wingding loss and the conduction loss of diodes) are introduced for damping effects.

The state-space representation of the *LLC* converter is shown by

$$\frac{d\hat{x}}{dt} = A\hat{x} + B\hat{u} \tag{25}$$

$$\hat{y} = C\hat{x} + D\hat{u} \tag{26}$$

where the states of the system $\hat{x} = (\,\hat{i}_s\ \hat{i}_c\ \hat{v}_s\ \hat{v}_c\ \hat{i}_{ms}\ \hat{i}_{mc}\ \hat{v}_{co}\,)^T$, the control inputs and the disturbance inputs $\hat{u} = (\,\hat{f}_s\ \hat{v}_{in}\ \hat{d}\,)^T$, the output $\hat{y} = \hat{i}_o$. The matrices are defined as eq. (27) shown at bottom of this page.

$$A = \begin{bmatrix}
-\frac{H_{ip}+R_s}{L_r} & -\frac{\Omega_s L_r + H_{ic}}{L_r} & -\frac{1}{L_r} & 0 & \frac{H_{ip}}{L_r} & \frac{H_{ic}}{L_r} & -\frac{H_{vco}}{L_r} \\
\frac{\Omega_s L_r - G_{ip}}{L_r} & -\frac{(G_{ic}+R_s)}{L_r} & 0 & -\frac{1}{L_r} & \frac{G_{ip}}{L_r} & \frac{G_{ic}}{L_r} & -\frac{G_{vco}}{L_r} \\
\frac{1}{C_r} & 0 & 0 & -\Omega_s & 0 & 0 & 0 \\
0 & \frac{1}{C_r} & \Omega_s & 0 & 0 & 0 & 0 \\
\frac{H_{ip}}{L_m} & \frac{H_{ic}}{L_m} & 0 & 0 & -\frac{H_{ip}}{L_m} & -\frac{H_{ic}+L_m\Omega_s}{L_m} & \frac{H_{vco}}{L_m} \\
\frac{G_{ip}}{L_m} & \frac{G_{ic}}{L_m} & 0 & 0 & -\frac{G_{ip}-L_m\Omega_s}{L_m} & -\frac{G_{ic}}{L_m} & \frac{G_{vco}}{L_m} \\
\frac{K_{is}R_p}{C_o R_{co}} & \frac{K_{ic}R_p}{C_o R_{co}} & 0 & 0 & -\frac{K_{is}R_p}{C_o R_{co}} & -\frac{K_{ic}R_p}{C_o R_{co}} & -\frac{R_p}{R_o C_o R_{co}}
\end{bmatrix}$$

$$B = \begin{bmatrix}
-2\pi I_c & 2\pi I_s & -2\pi V_c & 2\pi V_s & -2\pi I_{mc} & 2\pi I_{ms} & 0 \\
K_1/L_r & 0 & 0 & 0 & 0 & 0 & 0 \\
K_2/L_r & 0 & 0 & 0 & 0 & 0 & 0
\end{bmatrix}^T$$

$$C = \begin{bmatrix} \frac{K_{is}R_p}{R_o} & \frac{K_{ic}R_p}{R_o} & 0 & 0 & -\frac{K_{is}R_p}{R_o} & -\frac{K_{ic}R_p}{R_o} & \frac{R_p}{R_o R_{co}} \end{bmatrix} \quad D = 0 \tag{27}$$

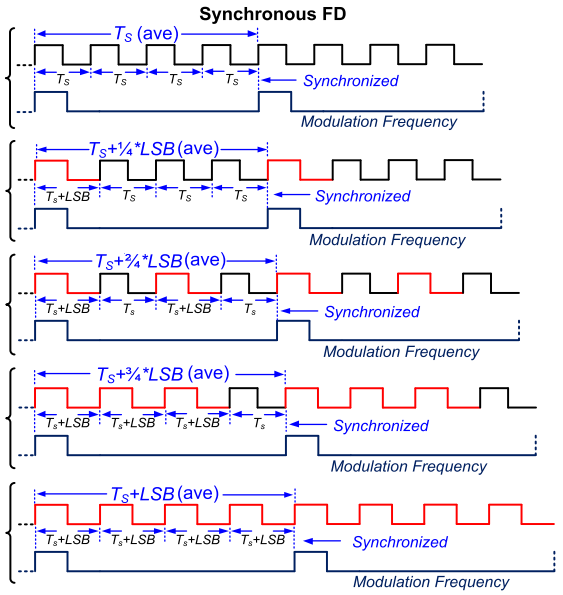


Fig. 12. Synchronous FD patterns realizing high resolution period levels.

where the coefficients are

$$H_{vco} = \frac{4n}{\pi}\frac{I_{ps}}{I_{pp}},\ H_{ip} = \frac{4nV_{co}}{\pi}\frac{{I_{pc}}^2}{{I_{pp}}^3} + \frac{8n^2}{\pi^2}R_{sp},$$

$$H_{ic} = -\frac{4nV_{co}}{\pi}\frac{I_{ps}I_{pc}}{{I_{pp}}^3},\ G_{ip} = -\frac{4nV_{co}}{\pi}\frac{I_{ps}I_{pc}}{{I_{pp}}^3},$$

$$G_{ic} = \frac{4nV_{co}}{\pi}\frac{{I_{pc}}^2}{{I_{pp}}^3} + \frac{8n^2}{\pi^2}R_{sp}, G_{vco} = \frac{4n}{\pi}\frac{I_{pc}}{I_{pp}},$$

$$K_1 = \frac{4}{\pi}\sin\left(\frac{\pi}{2}D\right),\ K_2 = 4V_{in}\cos\left(\frac{\pi}{2}D\right),$$

$$K_{is} = \frac{2n}{\pi}\frac{I_{ps}}{\sqrt{{I_{ps}}^2 + {I_{pc}}^2}},\ \text{and}\ K_{ic} = \frac{2n}{\pi}\frac{I_{pc}}{\sqrt{{I_{ps}}^2 + {I_{pc}}^2}}.$$

For the linearized system, the required transfer functions are

$$\left[G_{if}(s)\ G_{iv}(s)\ G_{id}(s)\right]^T = C(sI - A)^{-1}B. \tag{28}$$

Equation (28) can be solved by MATLAB to obtain the transfer functions that provide accurate expressions for current oscillation analysis and feedback loop design.

IV. Proposed Synchronous Frequency Dither

FD is to vary the period between two adjacent values during several switching periods, so that the average period has a fractional value. Theoretically, with a dither sequence with four switching periods, two more bits of the DPWM resolution can be achieved. The proposed two-bit dither patterns with synchronization are shown in Fig. 12. T_s and T_s + LSB correspond to two adjacent quantized period levels output from DPWM modules. With the dither sequence T_s, $T_s + \text{LSB}$, T_s, $T_s + \text{LSB}$, the average switching period is equal to $(T_s + T_s + \text{LSB} + T_s + T_s + \text{LSB})/4 = T_s + (1/2)\text{LSB}$. Thus, an intermediate (1/2)LSB subbit level is

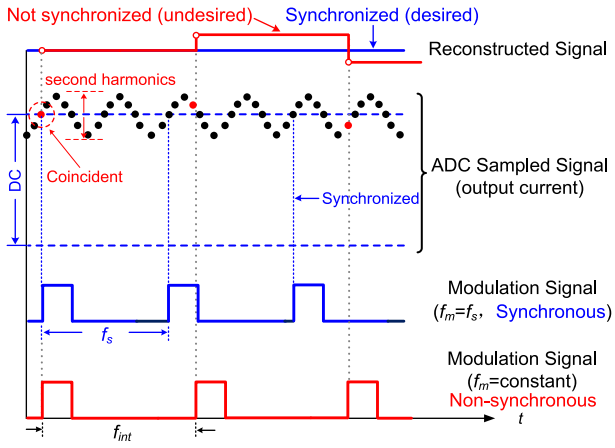


Fig. 13. Synchronization effect in reconstructed signal.

achieved by averaging over four switching periods. It should be emphasized that the modulation frequency should be always synchronized with the dither sequence.

It is necessary to suitably synchronize the modulation frequency and the dither sequence. Taking the dither sequence with one switching period (exactly the conventional FM) as an example, the synchronization effect in the reconstructed signal is illustrated in Fig. 13. At the rising edge of the modulation signal, the previous ADC sampled value is processed in the current regulator. However, given the sampler modeled in the current regulator with sampling rate of modulation frequency f_m ($f_m \le f_s$), the sensing voltage contains the second switching frequency harmonics due to the full-wave rectifier, which is above the Nyquist frequency $\omega_m/2$. As a result, the aliasing effects on the reconstructed signal processed in the current regulator should be considered.

Note that even if the modulation and switching frequencies are set equal ($f_m = f_s$, in blue), there still can be zero frequency error in the reconstruction of average sampled signal, when the modulation instants are not coincident with the zero-crossing of sampled voltage ripple. This can be solved by fine-tuning the current reference to compensate the steady-state error.

Zero-order hold (ZOH) is often introduced as a model for storage register in ADC that maintains a constant signal value between adjacent samples. In this paper, the maximum sampling rate of ADC is 1 MHz. That means ADC can be regarded as an ideal sampler. In contrast, the rate of the equivalent sampler in the current regulator should be selected. According to Franklin *et al.* [16], the desired sampling multiple K_{sam} for a reasonably smooth time response is given as

$$20 < K_{\text{sam}} = \frac{\omega_m}{\omega_b} < 40 \tag{29}$$

where ω_m is the modulation frequency in rad/s and ω_b is the closed-loop bandwidth of the *LLC* converter.

The interpolator function is inherent to DPWM. This is the block where the conversion from the digital-to-analog domain happens. Due to limited modulation frequency ($\le f_s$), the holder effect should be modeled in DPWM modules. The continuous time model of ZOH $G_h(s)$) usually adopted in sampled data

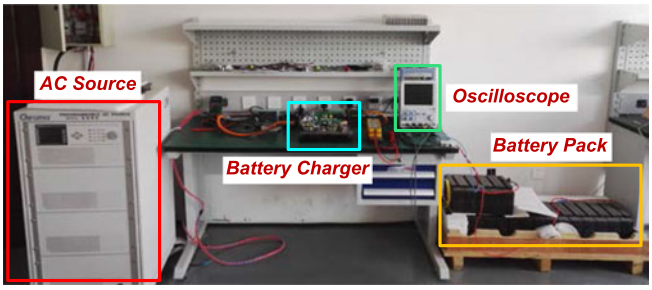


Fig. 14. Experimental testing platform.

TABLE II
CIRCUIT PARAMETERS OF *LLC* CONVERTER

I_o	25 A	C_r	6×10 nF
V_b	64–80 V	n	5.6 (28:5:5)
$V_{\rm dc}$	390 V	$C_{\rm oss}$	800 pF
$C_{\rm dc}$	$3 \times 470\ \mu$F	T_d	200 ns
f_s	80–120 kHz	C_o	$3 \times 470\ \mu\text{F} + 10 \times 10\ \mu$F
f_r	106 kHz	$R_{\rm co}$	50 mΩ
L_r	37 μH	R_s	150 mΩ
L_m	150 μH	$R_{\rm sp}$	40 mΩ

controller design, which is

$$G_h(s) = \frac{1 - e^{-sT_m}}{s} \tag{30}$$

where T_m is the modulation period.

The gain of the equivalent sampler in the current regulator equals to $1/T_m$. Multiplying (30), the continuous time model of sample-and-hold SH(s) is obtained as

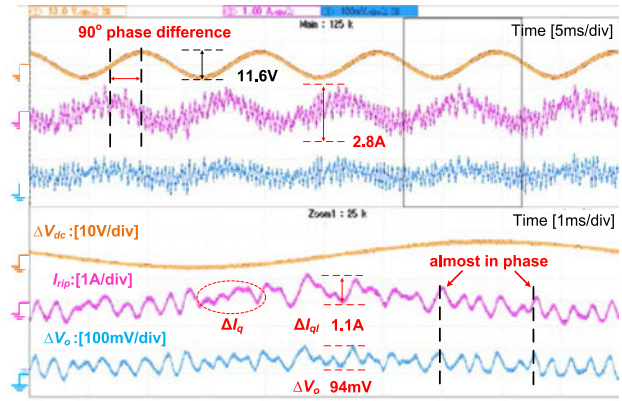
$$\text{SH}(s) = \frac{1 - e^{-sT_m}}{sT_m} \approx \frac{2}{sT_m + 2} \tag{31}$$

According to (31), a low modulation frequency decreases low-frequency loop gain and deteriorates phase margin. For the design tradeoff of the effective DPWM resolution and sample-and-hold effect, one bit dither sequence is adopted in the experiment and synchronized with the modulation frequency.

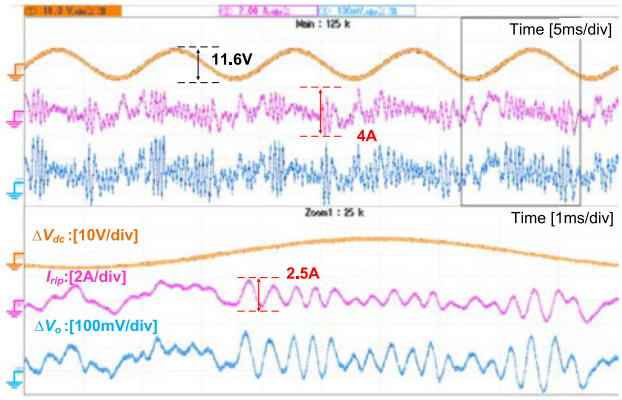
V. EXPERIMENTAL RESULTS AND DISCUSSION

In order to verify the proposed current ripple analysis and synchronous FD control, a 2-kW prototype of battery charger with 90–265 V input and 64–80 V output was built. Fig. 14 shows the photo of testing platform including the battery charger and a battery pack with 20 series-connected 1665132 model laminated Li(NiCoMn)O2 battery cells from Do-Fluoride New Energy Technology Co., Ltd.

The circuit parameters for the digital *LLC* converter are listed in Table II. A split inductor built with EE42-PC40 core is 25 μH as a part of the resonant inductor. With the external 12 μH leakage inductance of the *LLC* transformer (EE65-PC40), the total resonant inductance is 37 μH. The primary side resistance is comprised of on resistance of MOSFETs (2×65 mΩ) and ESR of the resonant inductor (20 mΩ). The forward voltage of secondary diodes is about 1 V, so the secondary side



(a)



(b)

Fig. 15. Battery charging current (FM): $V_{\rm b} = 80$ V, $I_{\rm o} = 25$ A. (a) With synchronization. (b) Without synchronization.

resistance introduced for damping effects is regarded as 40 mΩ (1 V/25 A).

The ac coupled charging current waveforms with conventional FM at 80 V battery voltage are illustrated in Fig. 15. It is observed that the current ripple caused by double line frequency voltage pulsation and the quantization error clearly exist in the output current waveform. As shown in Fig. 15(a), the quantization current ripple is 1.1 A, which accounts for 39% of total current ripple of 2.8 A. In Fig. 15(b), the quantization current ripple is 2.5 A, which is two times more than that with synchronization. It should be noted that the compensator is designed identically with synchronous FM and nonsynchronous FM.

The effectiveness of proposed synchronous FD is verified in Fig. 16. The experiment is carried out under the nominal operating condition at 72 V battery voltage. Fig. 16(a) illustrates ac coupled waveforms of dc-link voltage, output current, and output voltage with FM. The peak-to-peak output current ripple caused by quantization error is 0.85 A. In comparison, Fig. 16(b) shows the results with synchronous FD. It can be seen that the current ripple is 0.45 A (a reduction of 47%). Due to nonlinearity of the frequency-to-current gain, the FD effectiveness is less than theoretical value as 50%.

Note that two different kinds of quantization current ripple can be observed in charging current waveforms. ΔI_q with small

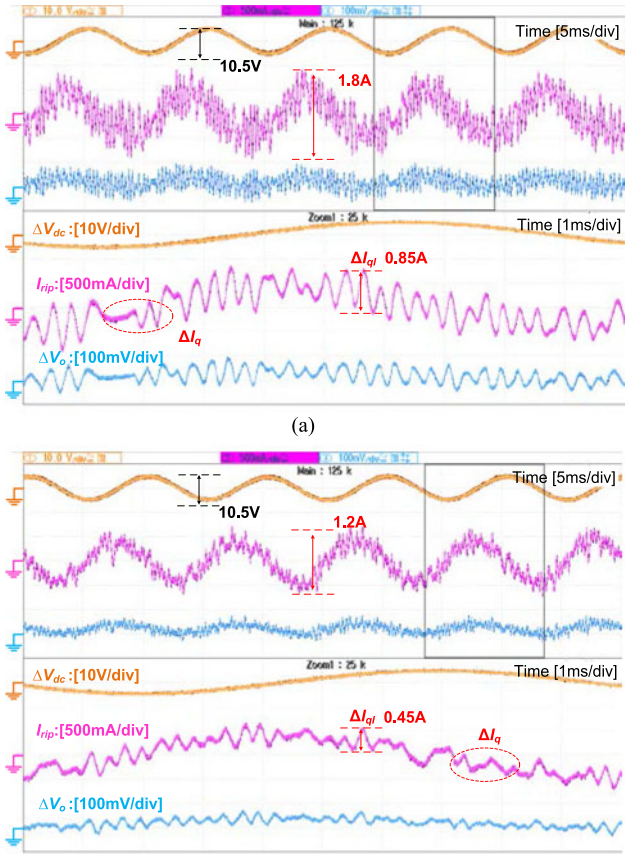


Fig. 16. Battery charging current: $V_{\rm b} = 72$ V, $I_{\rm o} = 25$ A. (a) Conventional FM. (b) With synchronous FD.

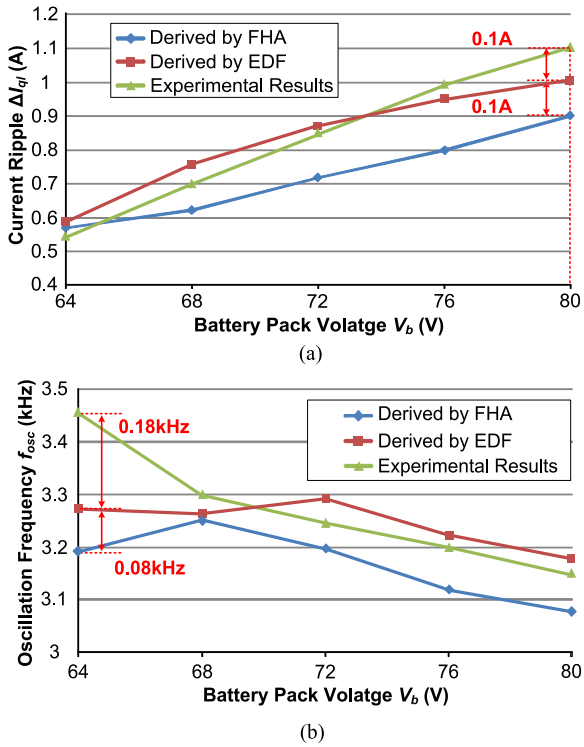


Fig. 17. Current oscillation model verification. (a) Peak-to-peak value of current oscillation at different battery voltages. (b) Frequency of current oscillation at different battery voltages.

amplitude is caused by the rounding-off error. Because the actual bandwidth of the current loop is not far lower than the oscillation frequency, ΔI_{ql} with large amplitude is caused by LFMS.

To verify proposed analytical model of current oscillation, Fig. 17(a) and (b) shows comparison of the peak-to-peak value and oscillation frequency between the modeling results and experimental results under different battery voltages. The oscillation frequency is estimated by counting wave peaks of quantization current ripple in one double line cycle. Thus, the oscillation frequency can be obtained as $N_{\rm q}$/10 kHz, where $N_{\rm q}$ represents the number of wave peaks in one double line cycle. From Fig. 17(a) and (b), the results derived by EDF are more accurate than by FHA. The maximum difference between EDF results and experimental results is 9.1% in the peak-to-peak value and 5.2% in oscillation frequency, respectively. In contrast, the maximum difference increases to 21.7% in the peak-to-peak value and 7.5% in oscillation frequency, respectively, for FHA results and experimental results. As the small-signal gain derived by EDF is more accurate than FHA especially at high frequency, the EDF results match better with the experimental data.

VI. Conclusion

Following the current ripple propagating mechanism, an analytical model of current oscillation under quantization effects is proposed. The analytical expressions of current oscillation frequency and peak-to-peak value can be derived by FHA, which provides practical design guidelines for current ripple reduction and stable current feedback loop. Compared with FHA, EDF can only provide numerical solutions. However, the small-signal gain derived by EDF is more accurate than FHA especially at high frequency. Less than 9% deviation is found between the derived results by EDF and the experimental results.

Synchronous FD is proposed to reduce quantization error and attenuate current oscillation. With a two-period dither sequence, one more bits of DPWM resolution is achieved. Synchronization with switching frequency is to prevent low-frequency aliased components created in the reconstructed signal. Compared with FM, the synchronous FD can reduce the quantization current ripple from 1.1 to 0.6 A (a reduction of 45%) at 80 V battery voltage, from 0.85 to 0.45 A (a reduction of 47%) at 72 V battery voltage, and 0.55–0.3 A (a reduction of 45%) at 64 V battery voltage. A current ripple reduction of around 45% is achieved over the entire charging procedure.

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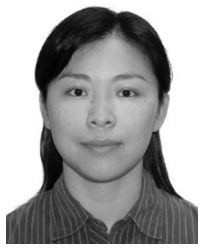

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