Current Flow Controlling Hybrid DC Circuit Breaker

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***Abstract*—This paper proposes a new device by combining features of an interline dual H-bridge current flow controller with the core idea of a hybrid HVdc circuit breaker for meshed HVdc grid application. The proposed device can substitute two dc circuit breakers at a dc bus with at least two adjacent transmission lines. In addition to the current interruption action, the current in one of the adjacent lines can be controlled by the embedded current flow controller. The system-level behavior of the proposed current flow controlling hybrid dc circuit breaker is similar to that of the typical hybrid dc circuit breaker and the interline dual H-bridge current flow controller. The operation principles of the proposed device are introduced and analyzed in this work. The component ratings are compared to the existing solution, and the functionality of the proposed device is verified by simulation.**

***Index Terms*—Current flow controller (CFC), dc circuit breaker (DCCB), fault protection, meshed dc grid.**

I. Introduction

DC POWER transmission technology was revived since the middle of the 20th century by realization of the first dc cable link between mainland Sweden and Gotland island in 1953 [1], [2]. Recent advances in the converter technology and the need for transmitting bulk amount of electrical energy over long distances have brought about the HVdc technology as a cost-efficient and reliable solution [2]. Nowadays, the multiterminal HVdc (MT-HVdc) grid concept is widely considered by both academia and industry due to the increasing demand for collecting the offshore wind energy [1].

While the MT-HVdc grid offers several advantages, its operation faces a few drawbacks. The MT-HVdc gird protection against a dc short-circuit fault has been identified as the major difficulty due to inability of most of the VSC topologies in blocking the dc fault current [2]–[4]. Even for voltage-source converter (VSC) technologies able to block the fault current (employing full-bridge cells), there is a need to use additional protective devices when complex MT-HVdc grids with more than one protection zones are considered [1]. Moreover, the interruption of dc current is technically difficult due to the lack of natural zero crossing [5], [6]. In addition to the protection problem, a meshed HVdc (M-HVdc) grid as a complex form of the MT-HVdc grid may face power flow control problems. Typically, the power flow in the M-HVdc grid is controlled by regulating the converters' dc-side voltage considering the transmission line impedance. Due to the M-HVdc grid topology, there are multiple paths for the current to circulate between two different nodes. Consequently, some of the transmission lines can be overloaded because of their lower impedances [7].

Over the last decade, the dc current interruption problem has been addressed by the introduction of several dc circuit breaker (DCCB) topologies [5], [8]–[11]. Among the proposed devices, the hybrid dc circuit breaker (HCB) merges the fast turn-off feature of semiconductor switches with the low-loss performance of metallic contacts and hence is technically highly attractive [12], [13]. The HCB requires hundreds of semiconductor switches in its main breaker (MB) branch to tolerate the system voltage [14], [15]; hence, its implementation cost is expected to be high. The number of required semiconductor switches for protection of a dc bus with two adjacent lines would be comparable to that of a modular multilevel converter station [14].

Furthermore, several current flow controller (CFC) devices have been introduced to solve the power flow problem in the M-HVdc grid [16]–[21]. The series CFCs demonstrate less power losses and reduced cost due to their lower voltage requirement and hence the fewer number of switches. The interline dual H-bridge CFC with a reduced number of switches can be considered as one of the most efficient CFCs [18].

The coordinated operation of HCBs and CFCs is expectable in the future M-HVdc grids. As an alternative solution, this paper proposes a new device, which benefits from the core idea of the typical HCB [12] and possesses an embedded CFC [18] and, therefore, can be named as a current flow controlling circuit breaker (CFCCB). The CFCCB has three ports and can connect a dc bus to two adjacent transmission lines. The CFCCB can regulate the current in one of the adjacent lines and upon receiving a trip command can interrupt the fault current and isolate the faulty line from the dc bus. The proposed approach requires fewer number of semiconductor switches as compared to the typical approach. Moreover, the ratings of required surge arresters (SAs) in the DCCB part can be reduced remarkably by employing the proposed device.

This paper is organized as follows. The CFCCB topology and operation principles are detailed in Section II. The case study model is explained in Section III, and Section IV provides

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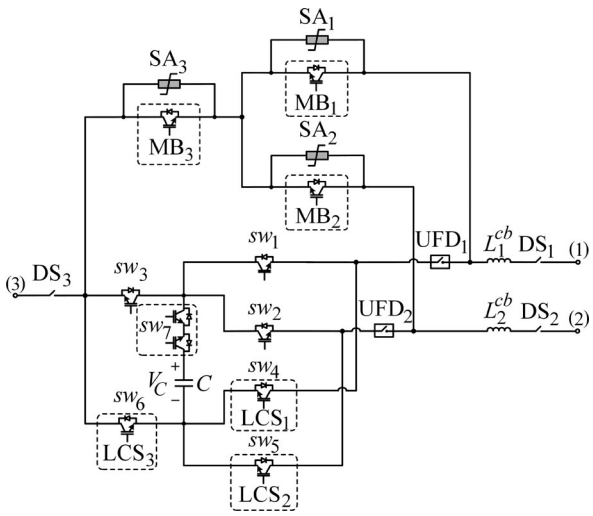

Fig. 1. Current flow controlling DCCB topology.

the analysis of CFCCB operation. The simulation results are presented and discussed in Section V. A comparison between the typical approach and the proposed CFCCB is included in Section VI, and this paper is concluded in Section VII.

A. CFCCB Topology

The topology of the proposed CFCCB is shown in Fig. 1. The CFCCB has three terminals and can connect a dc bus to two adjacent transmission lines.

II. Current Flow Controlling DCCB

The CFCCB consists of main breaker (MB_i) units, ultrafast disconnectors (UFD_i), surge arresters (SA_i), disconnectors (DS_i), seven semiconductor valves, and one capacitor. Moreover, (L_1^{cb}) and (L_2^{cb}) are employed as current-limiting inductors. The MB units consist of several semiconductor switches with antiparallel diodes in series connection. The semiconductor switches are connected in one direction, and hence, the MB units are unidirectional. UFD_1–UFD_3 are assumed to be similar to the UFDs in typical HCB [12]. DS_1–DS_3 are standard high-voltage disconnectors to provide the electrical isolation after CFCCB action. As shown in Fig. 1, sw_1–sw_6 together with capacitor C form an interline dual H-bridge CFC with a reduced number of switches [18]. However, sw_4–sw_6 are also exploited as load commutation switches (LCSs). Therefore, sw_4–sw_6 are also referred as LCS_1–LCS_3 in this paper.

A. Operation Principles

1) CFC Bypassed Mode: In this mode, the CFCCB does not control the current and only maintain the power flow between the dc bus and the adjacent lines. The equivalent representation of the CFCCB in the CFC bypassed mode is depicted in Fig. 2(a). Note that the semiconductor switches are represented by ideal switches in Fig. 2. In this mode, sw_1–sw_3 and sw_7 are opened, whereas sw_4–sw_6 are closed. DS_1–DS_3 and UFD_1–UFD_2 are closed, while MB_1–MB_3 are opened. It can be seen in the figure

TABLE I
Switching States for Positive and Negative Current Scenarios [7]

Positive Currents					
Set	sw_1	sw_6	sw_2	V_{31}	V_{32}
1	0	0	0	$-V$	$-V$
2	0	0	1	$-V$	0
3	0	1	0	0	$-V$
4	0	1	1	0	0
5	1	0	0	0	0
6	1	0	1	0	$+V$
7	1	1	0	$+V$	0
8	1	1	1	$+V$	$+V$
Negative Currents					
Set	sw_3	sw_4	sw_5	V_{31}	V_{32}
9	0	0	0	$+V$	$+V$
10	0	0	1	$+V$	0
11	0	1	0	0	$+V$
12	0	1	1	0	0
13	1	0	0	0	0
14	1	0	1	0	$-V$
15	1	1	0	$-V$	0
16	1	1	1	$-V$	$-V$

that the current can flow between the terminals of the CFCCB irrespective of its direction.

2) Active CFC Mode: The equivalent representation of the CFCCB in the active CFC mode is depicted in Fig. 2(b). In this mode, the CFCCB controls the current in one of the adjacent lines by operating its embedded dual H-bridge CFC. Depending on the current direction, the desired voltage can be generated by selecting a suitable set of states of switches. Table I illustrates the switching states for both negative and positive currents. The capacitor voltage is represented by V in Table I. The current can be controlled using a PI and second-order compensator. The linearized average model of the CFC represented by a couple of voltage sources can be used to design the current control system [7]. The embedded CFC operation modes and control scheme have been extensively investigated in [7] and [18]. As shown in Fig. 2, i_1, i_2, and i_3 are the currents flowing through terminals 1, 2, and 3 of the CFCCB, respectively. Based on the switching states in Table I, i_2 can be controlled only by applying pulse width modulation signal to sw_6 assuming the following scenario:

1) i_3 is incoming current into the CFCCB, and i_2 and i_1 are outgoing currents;
2) the currents are positive;

3) fault mode: the CFCCB can receive three independent trip commands including two line faults and one dc-bus fault trip commands. Upon receiving a trip command, the corresponding terminal(s) of the CFCCB must interrupt(s) its(their) current(s). Note that the CFCCB may enter to the fault mode either when it operates in the CFC bypassed or in the active CFC modes.

a) Fault on adjacent transmission line: Assume a permanent short-circuit fault happens on the line connected to terminal 1 of the CFCCB. Hence, terminal 1 of the CFCCB should trip and interrupt the fault current. It is assumed that the fault incepts at time t_f, and the trip command is received by the CFCCB at time t_1. At time t_1, sw_1–sw_3 should be opened, and consequently,

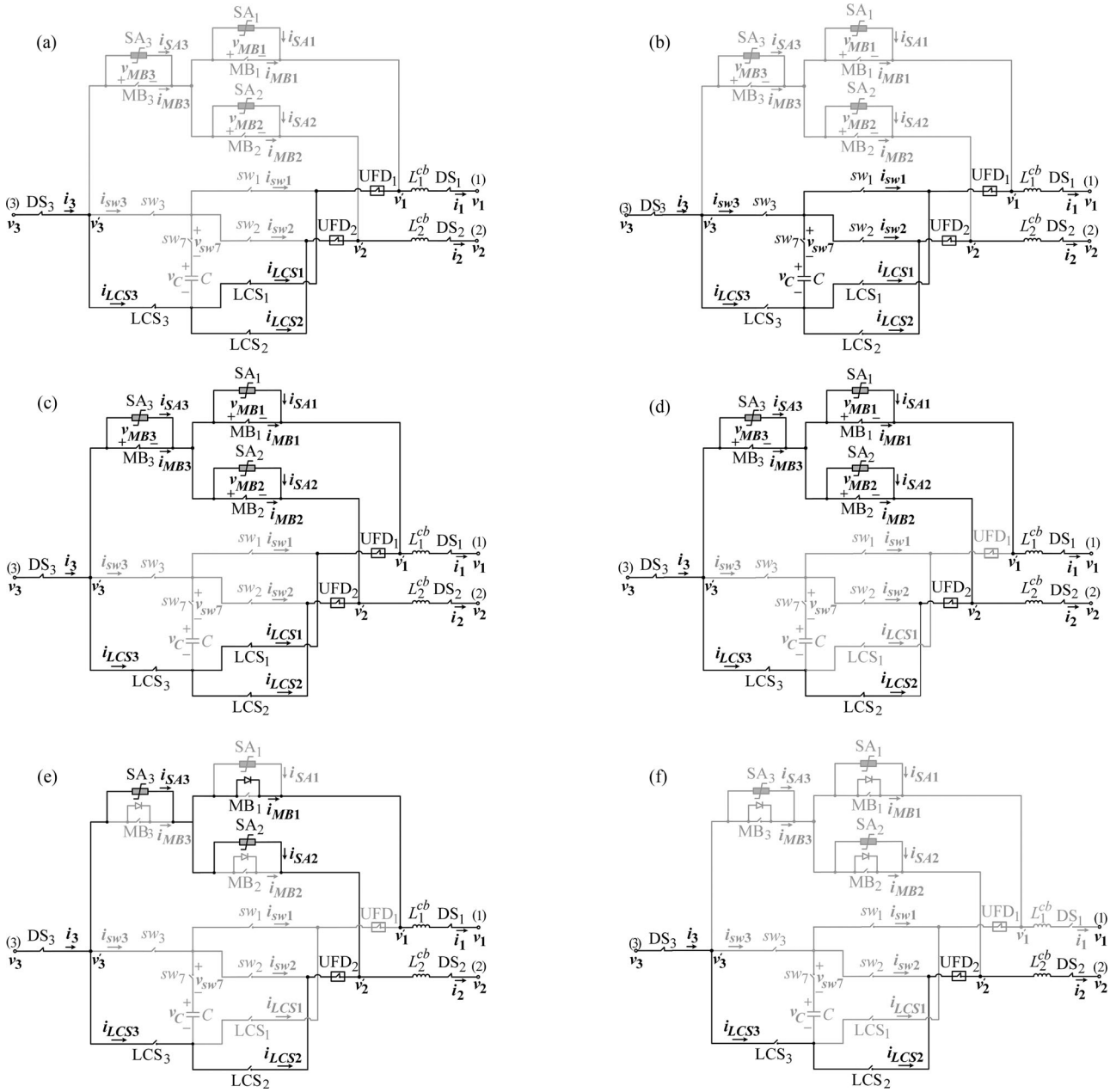

Fig. 2. Operation stages of current flow controlling HCB.

sw_4–sw_6 must be closed at time t_2. This action redirects the fault current path into the LCS units and prevents the capacitor from charging or discharging by reducing its current to zero. Thereafter, sw_7 can be opened at time t_3 in zero current to ensure that the capacitor is disconnected from the system. Upon opening of sw_7, MB_1–MB_3 must be closed at time t_4. The equivalent representation of this stage is shown in Fig. 2(c). As can be seen in the figure, the fault current is shared between MB and LCS units. At time t_5, sw_4–sw_6 should be opened and commutate the current into the MB units. At this stage, the current in UFD units is almost zero. Therefore, UFD_1 can be opened at time t_6 in order to isolate terminal 1 of the CFCCB (faulty line corresponding terminal) from the dc bus and the other adjacent line. Consequently, sw_4–sw_6 should be closed at time t_7. Fig. 2(d) shows the equivalent representation of the CFCCB at time t_7. Note that the current cannot flow through LCS_1 due to the open state of UFD_1. Finally, MB_1–MB_3 open and redirect the currents into the SA_1–SA_3 at t_{br}. The time period between t_7 and t_{br} is named as the current-sharing stage. The current in SA_1 will be zero due to the conduction of antiparallel diodes of MB_1. Fig. 3 illustrates the sequential operation of the CFCCB in the line fault mode. The operation sequence for a fault on the line connected to terminal 2 of the CFCCB is similar to the explained case. However, in the latter scenario, UFD_2 must be opened instead of UFD_1. To provide the electrical isolation, the corresponding terminal disconnector (DS) can be opened.

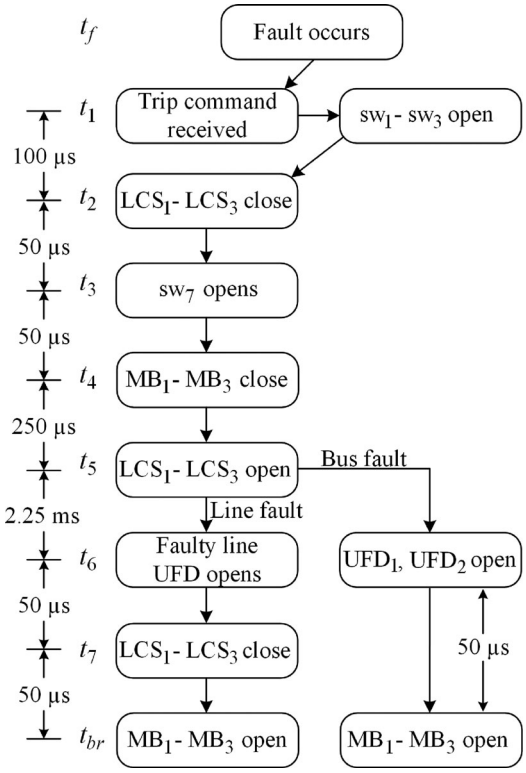

Fig. 3. Line and bus fault isolation process.

b) Fault at dc bus: Upon detection of a permanent dc-bus fault, all adjacent lines must be isolated from the dc bus. The operation sequence for a bus fault interruption is illustrated in Fig. 3. As shown in the figure, the operation sequences for line and bus faults are the same until time t_5. To interrupt a dc-bus fault, it is necessary to open both UFD_1 and UFD_2 at time t_6. For the bus fault interruption, there is no current-sharing stage and MB_1–MB_3 can be directly opened at time t_{br} to interrupt the fault current and redirect it into the SAs. Note that the current in SA_3 will be zero due the conduction of the antiparallel diodes of MB_3. The bus fault current interruption is expected to be faster than the line fault scenario due to the lack of current-sharing stage. Finally, the electrical isolation can be provided by opening DS_1– DS_3.

c) Recloser mode: The recloser mode might be required before completely opening of the CFCCB. The CFCCB can be reclosed by reclosing MB_1–MB_3 after opening the faulty line corresponding UFD. The equivalent circuits of the reclosing mode are equal to Fig. 2(d) and (f). Finally, in the case of a nonpermanent fault, the faulty line corresponding UFD can be again closed and the CFCCB shifts to its normal conduction state by closing sw_4–sw_6 and opening MB_1–MB_3.

III. Case Study Model

The current interruption operation of the CFCCB does not depend on the grid topology. Therefore, an average model of a three-terminal meshed grid is selected for performing the analysis and simulation. The three-terminal grid model is shown in Fig. 4. The transmission lines are modeled using lumped

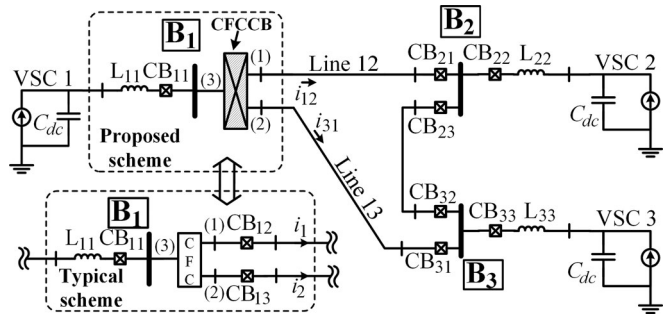

Fig. 4. Average model of the three-terminal grid.

T-equivalent model. The parameters of test system are illustrated in Table V. The analysis and simulations are carried out for both the proposed and typical schemes. As illustrated in Fig. 4, in the typical scheme, a CFC is installed at bus B_1 to regulate the current in line 12. In addition, two HCBs are installed between two adjacent lines (12 and 13) and the CFC. In this study, the HCBs from [12] are considered. A detailed schematic of the HCB is illustrated in Fig. 5. In the proposed scheme, the CFC and the HCBs are substituted by the CFCCB (see Fig. 4). The CFC control system is designed based on [7] for both the typical and proposed schemes. The parameters of CFC are the same for both mentioned schemes and are illustrated in Table V.

IV. Analysis

The operation of the embedded CFC has been analyzed in [7] and [18]. Therefore, only the current interruption mode of the CFCCB is considered in this section. In order to clarify the differences between the proposed and the typical methods, the analysis is simplified by considering the following aspects:

1) the permanent dc fault and prompt fault interruption strategy are considered [15], [22];
2) voltage at dc buses is assumed to be constant during the DCCB operation time [23];
3) transmission line and dc-bus short-circuit faults are modeled by a voltage source, whose value is equal to the system steady-state voltage value in the normal condition, and it changes to 0 V as soon as a fault happens.

Considering the aforementioned assumptions, the grid model can be simplified by eliminating the connection between buses B_2 and B_3. The simplification can be done due to assumed constant dc-bus voltage during the fault condition. The simplified model for analysis is depicted in Fig. 5.

A. Impact of the Embedded CFC on the Fault Current

The embedded CFC is composed of six switches with their antiparallel diodes and one bidirectional switch. Due to arrangement of the switches and the capacitor, the CFC cannot block the fault current until the capacitor is charged up to the nominal line voltage. The voltage rating of the capacitor lies in the range of few kilovolts. Therefore, the CFC capacitor must be disconnected from the fault current path to prevent it from being charged or discharged. The capacitor can be retained by opening sw_1–sw_3, while closing sw_4–sw_6 and then opening sw_7.

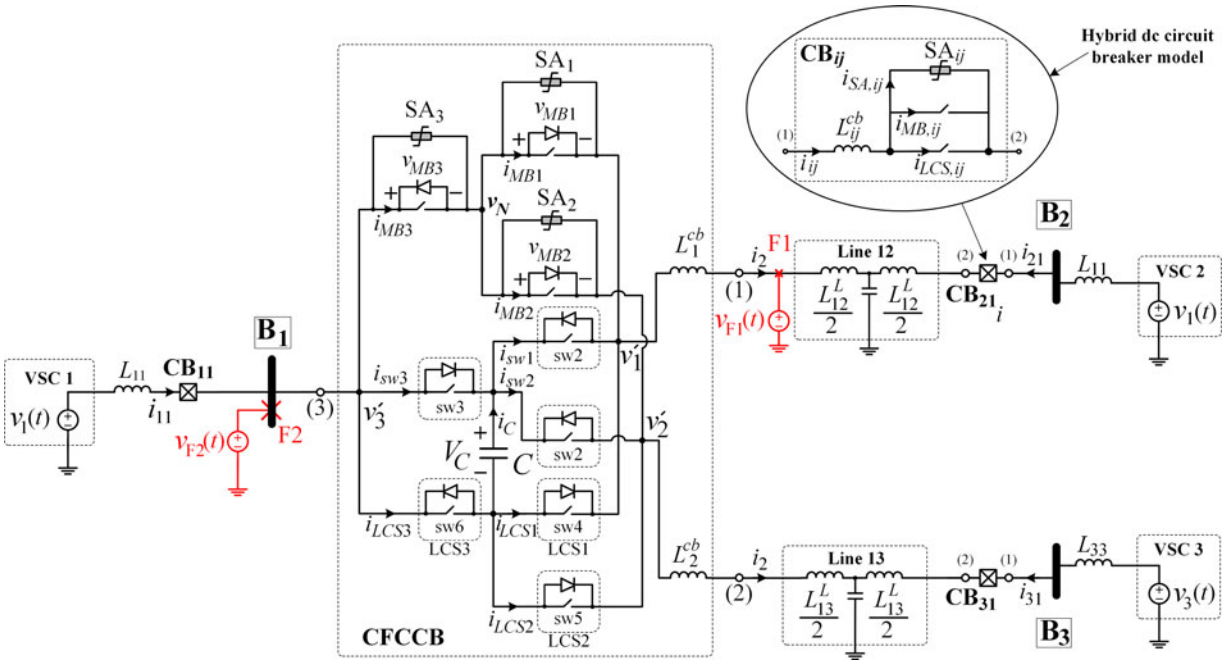

Fig. 5. Equivalent circuit of the test system in presence of the CFCCB.

Considering the embedded CFC structure, it can be found out that all the switching states may only change the fault current path inside the CFC and the fault current may charge or discharge the capacitor. Hence, during the fault clearing time period (which lies in range of few milliseconds), the CFC has almost no impact on the fault current. When $0 < t \leq t_2$, the current flows through sw_1–sw_7 depending on their state. Therefore, considering the scope of paper, the analysis considers the current equations for $t_2 < t \leq t_{br}$.

B. Transmission Line Fault F_1 and the CFCCB

A low-impedance ($R_{\mathrm{fault}} \approx 0\,\Omega$) pole-to-ground fault occurs on line 12 at point F_1 at $t = 0$ s. The voltage at fault location (v_{F1}) becomes zero after the fault occurs. The following equations can be given considering the initial conditions and assumptions:

$$\begin{aligned} v_{F1}(0) &= V_{\mathrm{dc}} \\ v_{F1}(0^+) &= 0 \\ v_j(t) &= V_{\mathrm{dc}}, \quad 0 < t \leq t_{br}, \quad j = 1,2,3 \\ i_j(0) &= I_{\mathrm{pre},j}, \quad j = 1,2,3. \end{aligned} \tag{1}$$

In (1), $v_{F1}(t)$, $v_j(t)$, and $I_{\mathrm{pre},j}$ represent the voltage at fault location, dc-bus B_j voltage, and prefault current of port j of the CFCCB. t_{br} represents the current interruption instant. The current at port 3 can be given as follows:

$$i_3(t) = \begin{cases} i_{\mathrm{LCS3}}(t), & t_2 < t \leq t_5 \\ i_{\mathrm{MB3}}(t), & t_5 < t \leq t_7 \\ i_{\mathrm{MB3}}(t) + i_{\mathrm{LCS3}}(t), & t_7 < t \leq t_{br} \\ i_{\mathrm{SA3}}(t) + i_{\mathrm{LCS3}}(t), & t_{br} < t \leq t_e \end{cases} \tag{2}$$

and for port 1

$$i_1(t) = \begin{cases} i_{\mathrm{LCS1}}(t), & t_2 < t \leq t_5 \\ i_{\mathrm{MB1}}(t), & t_5 < t \leq t_7 \\ i_{\mathrm{MB1}}(t), & t_7 < t \leq t_{br} \\ i_{\mathrm{MB1}}(t), & t_{br} < t \leq t_e \end{cases} \tag{3}$$

and for port 2

$$i_2(t) = \begin{cases} i_{\mathrm{LCS2}}(t), & t_2 < t \leq t_5 \\ i_{\mathrm{MB2}}(t), & t_5 < t \leq t_7 \\ i_{\mathrm{MB2}}(t) + i_{\mathrm{LCS2}}(t), & t_7 < t \leq t_{br} \\ i_{\mathrm{SA2}}(t) + i_{\mathrm{LCS2}}(t), & t_{br} < t \leq t_e. \end{cases} \tag{4}$$

We replace the sum of half of line $1j$ inductance (L^L_{1j}) and corresponding port current-limiting inductor value (L^{cb}_{j-1}) by L'_{1j}:

$$\begin{aligned} L'_{1j} &= L^{cb}_{j-1} + \frac{1}{2}L^L_{1j} \quad \text{for} \quad j = 1,2 \\ L'_{11} &= L_{11} + L^{cb}_{11}. \end{aligned} \tag{5}$$

Therefore, considering the impact of transmission line lumped T-equivalent model capacitance during the short fault clearing time period, the initial rate of rise of current at port 1, which is equal to that of fault current, can be given by

$$\frac{di_1(0^+)}{dt} = \frac{V_{\mathrm{dc}}}{\left((L'_{11} \parallel L'_{13}) + L^{cb}_1 + L^f_{12}\right)} \tag{6}$$

where L^f_{12} represents the inductance between the CFCCB and the fault location. The current derivative at the other ports of the

CFCCB can be given as

$$\left|\frac{di_2\left(0^+\right)}{dt}\right| = \frac{L'_{11}}{\left(L'_{11}+L'_{13}\right)}\left|\frac{di_1\left(0^+\right)}{dt}\right|$$
$$\left|\frac{di_3\left(0^+\right)}{dt}\right| = \frac{L'_{13}}{\left(L'_{11}+L'_{13}\right)}\left|\frac{di_1\left(0^+\right)}{dt}\right|. \quad (7)$$

The current in MB and LCS units can be obtained using (2)–(4), (6), and (7).

1) MB Units: When $t_4 < t < t_{br}$, MB_1–MB_3 are closed. Therefore, assuming instantaneous current commutation at $t = t_5$, the current in MB_1 can be given as

$$i_{\mathrm{MB1}}\left(t\right) = I_{\mathrm{pre},1} + \left|\frac{di_1\left(0^+\right)}{dt}\right| t. \quad (8)$$

The maximum current in MB_1 ($I_{\max}^{MB1}$) happens at $t = t_{br}$. The current in MB_2 and MB_3 when $t_4 < t < t_7$ can be given by

$$i_{\mathrm{MBi}}\left(t\right) = I_{\mathrm{pre},i} + \mathrm{sgn}\left(i-2.5\right)\left|\frac{di_i\left(0^+\right)}{dt}\right| t, \quad i = 2,3. \quad (9)$$

The maximum current in MB_2 and MB_3 is reached at $t = t_7$. When $t_7 < t < t_{br}$, the current is shared between two mentioned MBs and their current will be decreased.

2) LCS Units: As was explained, the LCS switches conduct the current in two periods of time: 1) $t_2 < t < t_5$; and 2) $t_7 < t < t_{br}$. In the first stage (when $t_2 < t < t_5$), the current in LCS_j for $j = 1$ and for $j = 2,3$ holds the same equations as (8) and (9), respectively. The maximum current in the first stage in the LCS units happens at $t = t_5$. The second maximum of current in the LCS units occurs at time t_{br}. Fig. 2(d) shows the equivalent circuit of the CFCCB when $t_5 < t \le t_{br}$. The MBs have several insulated-gate bipolar transistors (IGBTs) in series, whereas the LCSs have only few IGBTs. The on-state voltage drop on an MB can be hundred times larger than the on-state voltage drop of an LCS. Hence, the voltage drop on the LCSs can be neglected against that of MB units. Therefore, the following equation can be given considering Fig. 2(d):

$$v'_2 \approx v'_3. \quad (10)$$

v'_1–v'_3 are illustrated in Fig. 2. Based on (10), MB_2 and MB_3 can be considered as parallel branches during the mentioned time period and their currents will be almost equal. The absolute value of the current in MB_j at $t = t_7^+$ can be given by

$$\left|i_{\mathrm{MB}j}\left(t_7^+\right)\right| = \frac{\left|i_{\mathrm{MB3}}\left(t_7^-\right)\right| + \left|i_{\mathrm{MB2}}\left(t_7^-\right)\right|}{2}, \quad j = 2,3. \quad (11)$$

Using (2), the current in LCS_n can be given as follows:

$$i_{\mathrm{LCS3}}\left(t_7^+\right) = i_{\mathrm{LCS1}}\left(t_7^+\right) = \frac{\left|i_{\mathrm{MB3}}\left(t_7^-\right)\right| - \left|i_{\mathrm{MB2}}\left(t_7^-\right)\right|}{2}. \quad (12)$$

The time $t_{br} - t_7$ lies in the range of tens of microseconds. However, using the obtained current derivative in (6), the second maximum of current in LCS_j for $j = 2,3$ can be obtained as

$$I_{\mathrm{max2}}^{\mathrm{LCS}j} = i_{\mathrm{LCS}j}\left(t_7^+\right) + \frac{\mathrm{d}i_1\left(0^+\right)}{\mathrm{d}t}\cdot\frac{t_{br}-t_7}{2}. \quad (13)$$

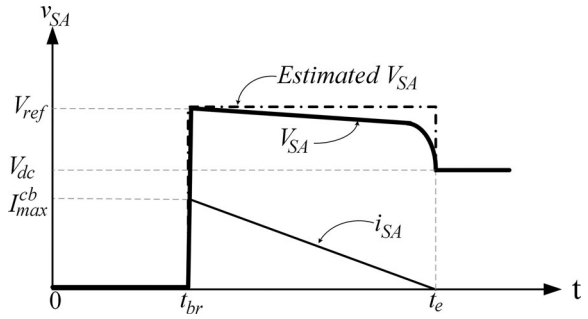

Fig. 6. SA approximated current and voltage.

3) Surge Arresters: SAs have a nonlinear voltage–current characteristic. Only for comparison purposes, SA's parameters are approximated by assuming its voltage to be constant until its current falls to zero for both the proposed and typical schemes. Fig. 6 illustrates the voltage and current approximation method used for the SAs. It is assumed that the SA current reaches its maximum instantaneously and then decreases linearly. This method is used to identify the maximum possible energy absorption in the SAs. Neglecting the practical mismatch between V–I characteristics of SAs, the current can be given as

$$\left|i_{\mathrm{SA}j}\right| = \left|\frac{i_{\mathrm{MB1}}}{2}\right| \quad j = 2,3$$
$$\left|i_{\mathrm{SA1}}\right| = 0. \quad (14)$$

The current in SA_1 is zero due to the conduction of antiparallel diodes in MB_1. Considering (10), it can be assumed that SA_2 and SA_3 operate in parallel connection. The rated voltage of each SA is assumed to be equal to V_r. The transient interruption voltage (TIV) across MB_2 and MB_3 can be given by

$$\mathrm{TIV} = V_{\mathrm{dc}} + \left(\left(L'_{11} \parallel L'_{13}\right) + L_1^{cb} + L_{12}^{f}\right)\frac{I_{\max}^{\mathrm{MB1}}}{t_e - t_{br}}. \quad (15)$$

The current in SA reaches zero when its voltage falls below its rated voltage. The maximum required time for SA current to fall to zero $(t_e - t_{br})$ can be given as

$$\left(t_e - t_{br}\right) \le \left(\left(L'_{11} \parallel L'_{13}\right) + L_1^{cb} + L_{12}^{f}\right)\frac{I_{\max}^{\mathrm{MB1}}}{V_r - V_{\mathrm{dc}}}. \quad (16)$$

The maximum absorbed energy in all the SAs holds

$$E_{\mathrm{SA},T} = \int_{t_{br}}^{t_e} V_r \cdot i_1\left(t\right) dt. \quad (17)$$

Consequently, the maximum absorbed energy in SA_j can be given as

$$E_{\mathrm{SA}j} = \frac{V_r I_{\max}^{\mathrm{MB1}}\left(t_e - t_{br}\right)}{4}, \quad j = 2,3$$
$$E_{\mathrm{SA1}} = 0. \quad (18)$$

C. DC-Bus Fault F_2 and the CFCCB

As shown in Fig. 5, a low-impedance pole-to-ground fault ($R_{\mathrm{fault}} \approx 0\ \Omega$) occurs at dc bus B_1 at time 0 s. The initial conditions and study assumptions are similar to (1), and also,

a similar approach to Section IV-B is used for analysis. The current at port j for various time periods can be given by

$$i_j(t) = \begin{cases} i_{\mathrm{LCS}j}(t), & t_2 < t \le t_5 \\ i_{\mathrm{MB}j}(t), & t_5 < t \le t_{br} \\ i_{\mathrm{SA}j}(t), & t_{br} < t \le t_e, \end{cases} \quad j = 1,2,3. \tag{19}$$

The current derivative at ports of the CFCCB can be given by

$$\frac{di_3(0^+)}{dt} = V_{\mathrm{dc}} \frac{L'_{12} + L'_{13}}{L'_{12} L'_{13}}$$
$$\left| \frac{di_i(0^+)}{dt} \right| = \frac{V_{\mathrm{dc}}}{L'_{1(i+1)}}, \quad i = 1,2. \tag{20}$$

1) MB Units: The currents in MB units when $t_5 < t \le t_{br}$ can be given as

$$i_{\mathrm{MB}i}(t) = \begin{cases} I_{\mathrm{pre},i} - \dfrac{V_{\mathrm{dc}}}{L'_{1(i+1)}} t, & i = 1,2 \\ I_{\mathrm{pre},i} - V_{\mathrm{dc}} \dfrac{L'_{12} + L'_{13}}{L'_{12} L'_{13}} t, & i = 3. \end{cases} \tag{21}$$

The maximum current in MB_j ($I_{\max}^{\mathrm{MB}j}$) is reached at $t = t_{br}$.

2) LCS Units: Despite the line fault scenario, the current in LCS units has one maximum at $t = t_5$ and can be given as

$$I_{\max}^{\mathrm{LCS}i}(t) = \begin{cases} I_{\mathrm{pre},i} - \dfrac{V_{\mathrm{dc}}}{L'_{1(i+1)}} t_5, & i = 1,2 \\ I_{\mathrm{pre},i} - V_{\mathrm{dc}} \dfrac{L'_{12} + L'_{13}}{L'_{12} L'_{13}} t_5, & i = 3. \end{cases} \tag{22}$$

3) Surge Arresters: The SA current can be given as

$$|i_{\mathrm{SA}j}| = \left| \frac{i_{\mathrm{MB3}}}{2} \right|, \quad j = 1,2$$
$$|i_{\mathrm{SA3}}| = 0. \tag{23}$$

Depending on the length of adjacent lines, the absorbed energy in the SAs of the CFCCB and also the energy absorption time ($t_{ej} - t_{br}$) can be different for each SA. The range of energy absorption time can be given as

$$t_{ej} - t_{br} \le \frac{L'_{1(j+1)} I_{\max}^{\mathrm{MB}j}}{V_r - V_{\mathrm{dc}}}, \quad j = 1,2 \tag{24}$$

where t_{ej} is the time when the current in SA_j becomes zero. Due to conduction of antiparallel diode D_3, the current in SA_3 remains zero, and consequently, the absorbed energy in SA_3 is also zero. The absorbed energy in SA_j can be given by

$$E_{\mathrm{SA}j} = \frac{V_r I_{\max}^{\mathrm{MB}j} (t_{ej} - t_{br})}{2}, \quad j = 1,2. \tag{25}$$

D. Typical Scheme

In the typical scheme, after receiving a trip command by the corresponding HCB at time t_1, its MB unit is closed. Thereafter, the LCS unit opens at time t_2, and consequently, the MB unit opens at time t_3 [24]. Similar line and bus fault scenarios to Section IV-B to Sections IV-B and IV-C are considered. For the sake of brevity, only the most relevant equations are included in this section.

1) Transmission Line Fault and the HCB: a) LCS units: The LCS current in CB_{12} reaches its maximum at $t = t_2$, whereas the current in the LCS unit of CB_{13} reaches its maximum at $t = t_{br}$. The maximum current in the LCS unit of CB_{12} can be given by

$$I_{\max}^{\mathrm{LCS12}}(t) = I_{\mathrm{pre},12} + \left| \frac{di_{12}(0^+)}{dt} \right| t_2 \tag{26}$$

and for the LCS unit of CB_{13}

$$I_{\max}^{\mathrm{LCS13}}(t) = I_{\mathrm{pre},13} - \left| \frac{di_{13}(0^+)}{dt} \right| t_{br}. \tag{27}$$

b) MB units: It is assumed that only the MB unit of the corresponding HCB of the faulty line is activated. Therefore, the current in MB]units of other HCBs remains zero. The current in the MB unit of CB_{12} for $t_2 < t \le t_{br}$ can be given as

$$I_{\max}^{\mathrm{MB12}}(t) = I_{\mathrm{pre},12} + \left| \frac{di_{12}(0^+)}{dt} \right| t. \tag{28}$$

The maximum current in the MB unit in CB_{12} ($I_{\max}^{\mathrm{MB12}}$) is reached at time t_{br}.

c) Surge arresters: The currents in SAs of all the HCBs are zero except the faulty line HCB (SA_{12}). The absorbed energy in the SA can be given by

$$E_{\mathrm{SA12}} = \frac{V_r I_{\max}^{\mathrm{MB12}} (t_e - t_{br})}{2}. \tag{29}$$

2) DC-Bus Fault and the HCB

a) LCS units: During the bus fault, all the adjacent HCBs of the faulty dc bus are activated. The maximum current in the LCS unit of all adjacent HCBs ($I_{\max}^{\mathrm{LCS1}i}$) can be given as

$$I_{\max}^{\mathrm{LCS1}i} = I_{\mathrm{pre},li} - \frac{V_{\mathrm{dc}}}{L'_{1i}} t_2, \quad i = 2,3. \tag{30}$$

b) MB units: The currents of MB units for $t_2 < t \le t_{br}$ can be given as

$$i_{\mathrm{MB1}i}(t) = I_{\mathrm{pre},li} - \frac{V_{\mathrm{dc}}}{L'_{1i}} t, \quad i = 2,3. \tag{31}$$

The maximum current in the MB unit ($I_{\max}^{\mathrm{MB1}i}$) is reached at $t = t_{br}$.

c) Surge arresters: The absorbed energy in SA_{1j} can be given by

$$E_{\mathrm{SA1}j} = V_r I_{\max}^{\mathrm{MB1}j} (t_{ej} - t_{br}), \quad j = 2,3. \tag{32}$$

V. Simulation Results

In this section, the simulation results of the three-terminal grid (see Fig. 4) for line 12 and dc-bus fault scenarios are presented and compared to the obtained numerical values from the analysis of the simplified grid model in Section IV. The simulations are carried out using PSCAD. The nonlinear V–I characteristics of SAs are also considered. The transmission lines are protected by the standard overcurrent protection scheme. The line fault trip command is sent to the CFCCB or the corresponding HCB when the line current exceeds 2.8 kA. The dc buses are protected

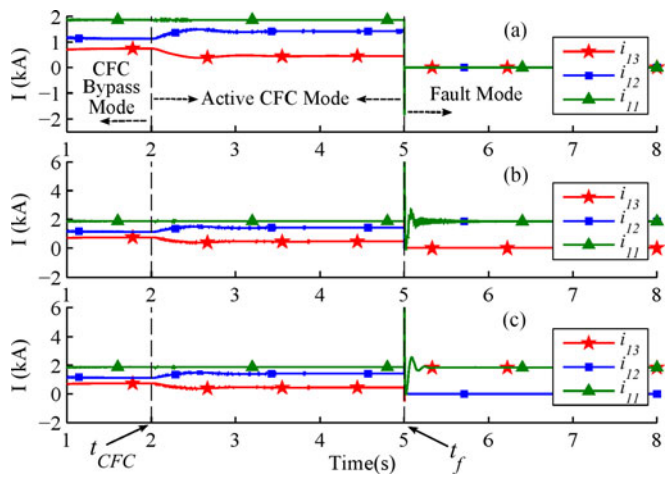

Fig. 7. Transmission lines and dc-bus currents during fault at (a) dc bus B_1, (b) line 13, and (c) line 12.

by the differential protection scheme. In this scheme, when the sum of incoming and outgoing currents at a dc bus becomes nonzero, the dc-bus trip signal is activated.

A. Power Flow

The currents flowing from the dc bus and the transmission lines in presence of the CFCCB are depicted in Fig. 7. Fig. 7(a)–(c) depicts the currents for dc bus B_1, line 13 and 12 fault scenarios, respectively. The CFCCB operates in the CFC bypassed mode for $0 < t < 2$ s. Thereafter, the CFCCB changes its operation mode to active CFC mode at time $t_{\rm CFC} = 2$ s. In all scenarios, the fault happens at time $t_f = 5$ s. The behavior of the CFCCB has been found out to be similar to the typical scheme during normal operation and fault condition from the grid point of view.

B. Transmission Line Fault

To consider the most severe scenario, a low-impedance pole-to-ground fault (100 mΩ) is placed very close to the CFCCB (distance from the CFCCB is equal to 0 km.) on line 12 at $t = 0$ s. In the typical approach, CB_{12} and CB_{21} and, in the case of the proposed CFCCB, CB_{21} and port 1 of the CFCCB should trip. Figs. 8 and 9 show different waveforms for the proposed and typical schemes, respectively. The important numerical values obtained from simulation and analysis are also illustrated in Table II. The interrupted current in the CFCCB is almost 5% larger than the interrupted current in the typical scheme due to the additional time that is considered in the modeling of the current-sharing stage in the CFCCB. As shown in Figs. 8(b) and 9(b), the current in sw_1–sw_3 in both schemes is almost equal. However, a large difference in the current of sw_4–sw_6 can be observed in Figs. 8(c) and 9(c). The absolute value of the current in sw_4 and sw_6 in the typical scheme reaches almost 10 kA, whereas in sw_5 and sw_6 in the proposed scheme, it does not exceed 5 kA. Fig. 8(d) depicts the CFCCB capacitor voltage and current and also the voltage across sw_7. The absolute value of the voltage across sw_7 does not exceed 2.5 kV. As shown in Figs. 8(f) and 9(f), the fault current is redirected into two SAs (SA_2 and SA_3) in the CFCCB, whereas it is handled by one SA in the typical method. Since the rated voltage of SAs in the CFCCB is equal to that of HCBs, the maximum voltage across MB units in both methods is equal [see Figs. 8(g) and 9(g)]. Figs. 8(h) and 9(h) show the absorbed energy in the SAs in both methods. The amount of absorbed energy in each SA in the CFCCB reaches almost 7.2 MJ, whereas it reaches approximately 14 MJ in the typical scheme. The results confirm that the absorbed energy in the SA in the typical scheme is almost equal to twice the absorbed energy in each SA in the proposed scheme.

C. DC-Bus Fault

A low-impedance pole-to-ground fault (100 mΩ) is placed at bus B_1. In the typical scheme, CB_{11}, CB_{12}, and CB_{13} and, in the proposed scheme, CB_{33} and all the ports of the CFCCB should trip. Figs. 10 and 11 depict the results for the proposed and the typical schemes, respectively. The most relevant numerical values obtained from analysis and simulation are illustrated in Table III. The obtained approximated values from analysis are close to the values obtained from simulation. Figs. 10(a) and 11(a) show that the behavior of both schemes from the system point of view are similar. As can be seen in Figs. 10(b) and 11(b), the current in sw_1–sw_3 for both schemes is equal. Figs. 10(c) and 11(c) show that the current in sw_4–sw_6 in the typical scheme may reach higher values as compared to the proposed scheme. The maximum current in MB_{12} and MB_1 and also in MB_{13} and MB_2 is equal [see Figs. 10(e) and 11(e)]. The absolute value of the current in MB_3 of the CFCCB reaches almost 1.8 kA, which is higher than the current in MB units of CB_{12} and CB_{13}. However, this does not necessarily mean that the antiparallel diodes of MB_3 should be rated for higher current than the antiparallel diodes of MB_1 and MB_2. In fact, MB_1 and MB_2 may be required to carry higher currents during a line fault and should be rated for that. Figs. 10(f) and 11(f) illustrate that the maximum current in the SAs of both schemes is equal. In contrary with MB_1 and MB_2, the current in MB_3 does not redirected to the SA due to the explained reason in Section IV. The absorbed energy in the SAs in the CFCCB and the typical scheme is depicted in Figs. 10(h) and 11(h), respectively.

VI. Comparison

The proposed scheme is compared to the typical scheme in this section. As shown in Fig. 4, to fully protect a dc bus with two adjacent lines and one converter station with an asymmetric monopole HVdc configuration, three HCBs are required in the typical scheme. The number of HCBs can be doubled in symmetric monopole and bipole configurations. Although the comparison study is done for asymmetric monopole configuration, it is valid for other mentioned configurations. The HCBs and the CFC can be replaced by the CFCCB. The converter station HCB (CB_{11}) will not be removed. Therefore, the requirements of CB_{11} in both cases are equal and will not be compared and included in calculations. Table IV compares different aspects of both the proposed and typical devices assuming $t_6 \approx t_{br}$.

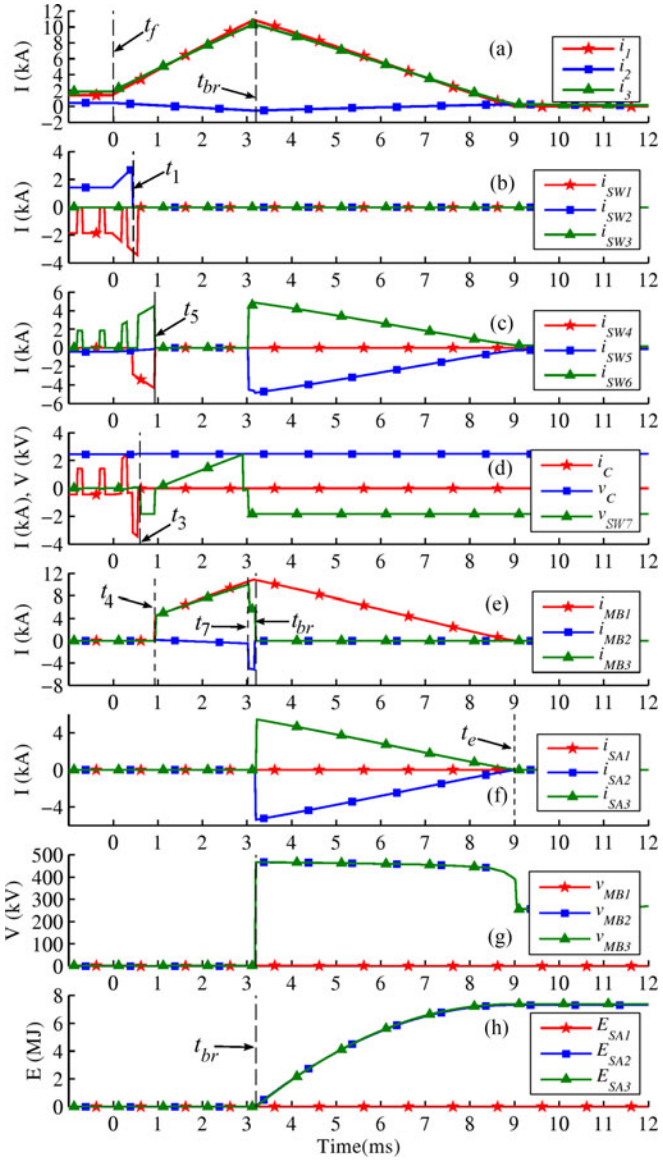

Fig. 8. CFCCB waveforms for fault on line 12.

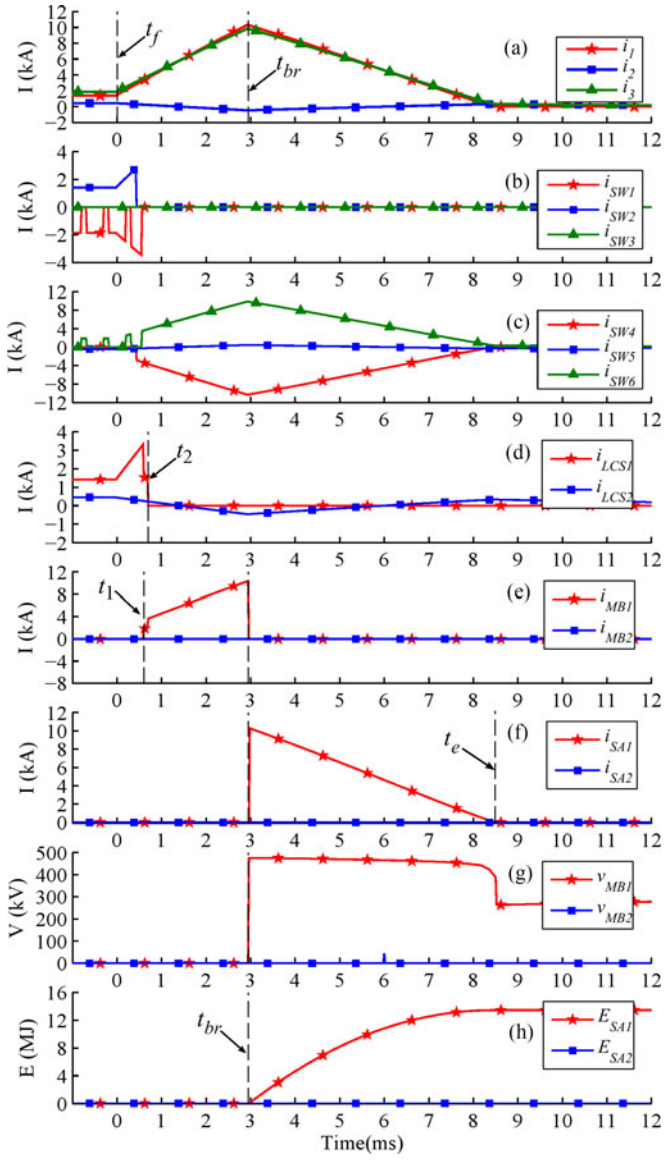

Fig. 9. Typical scheme waveforms for fault on line 12.

CFC: The CFC can be bypassed during the fault either by the explained method in Section IV-A or using bypass valves. Considering the method from Section IV-A, sw_4–sw_6 are required to carry the fault current till the corresponding HCBs interrupt the fault (at time t_{br}). In contrary, the same switches in the embedded CFC of the CFCCB are only required to carry the fault current till the LCS units are opened (at time t_5). In addition, sw_4–sw_6 are closed at time t_7 and share the fault current with the MB units in the line fault scenario. Comparing (30) and (13) implies that sw_4–sw_6 should be rated for higher current in the typical scheme than the proposed scheme.

TABLE II
CFCCB AND HCB PARAMETERS DURING LINE FAULT

Parameters CFCCB (HCB)	CFCCB		HCB	
	Analysis	Simulation	Analysis	Simulation
I^{LCS1}_{max1} (I^{LCS12}_{max}) [kA]	4.18	4.28	3.20	3.28
I^{LCS1}_{max2} [kA]	4.48	4.62	–	–
I^{MB1}_{max} (I^{MB12}_{max})[kA]	11.10	10.9	10.43	10.33
E_{SA1} (E_{SA12})[MJ]	0	0	16.98	13.69
E_{SA2} (E_{SA13})[MJ]	8.99	7.31	0	0
E_{SA3} [MJ]	8.99	7.38	–	–

A. Load Commutation Switches

The CFCCB uses sw_4–sw_6 of the embedded CFC as the LCSs. In fact, the CFCCB saves all the IGBTs, which are required for implementing the LCS units (N_{LCS}) in the HCBs. The maximum current in the LCS unit of HCB_{1j} is equal to the first maximum current in LCS_j of the CFCCB for the line fault scenario. Depending on the grid topology, the second maximum current in LCS units of the CFCCB might be greater as compared to the typical HCB. During the dc-bus fault condition, the current in LCS_2 and LCS_3 of the CFCCB is equal to the current in LCS units of HCB_{11} to HCB_{12}. The current in LCS_1

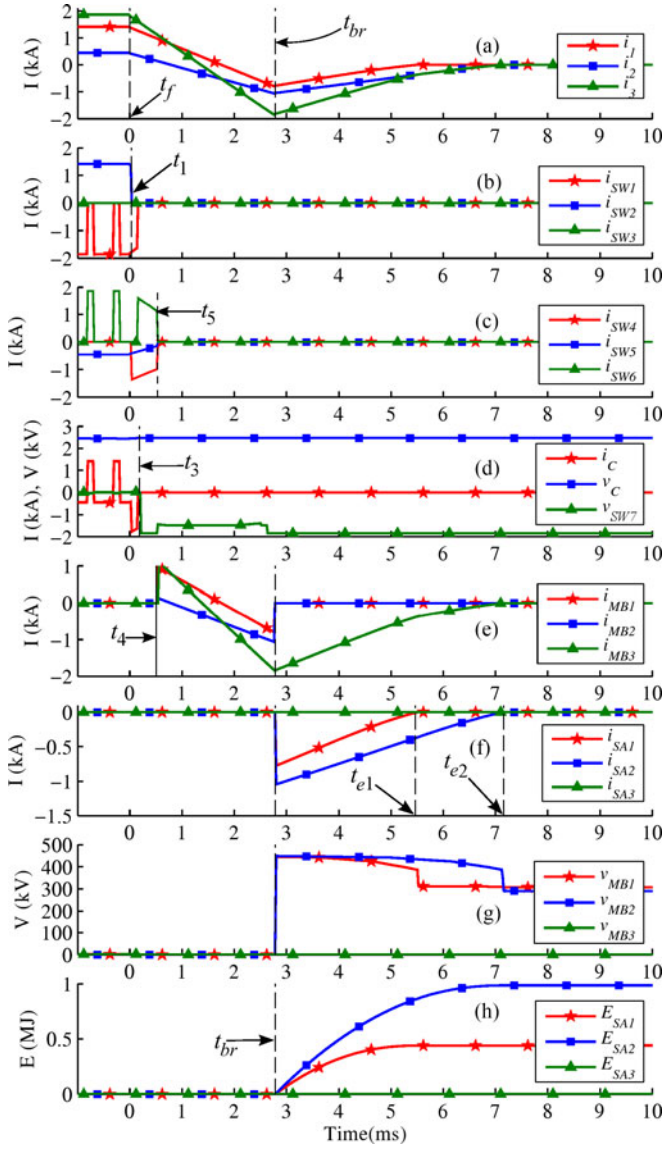

Fig. 10. CFCCB waveforms for fault at bus B_1.

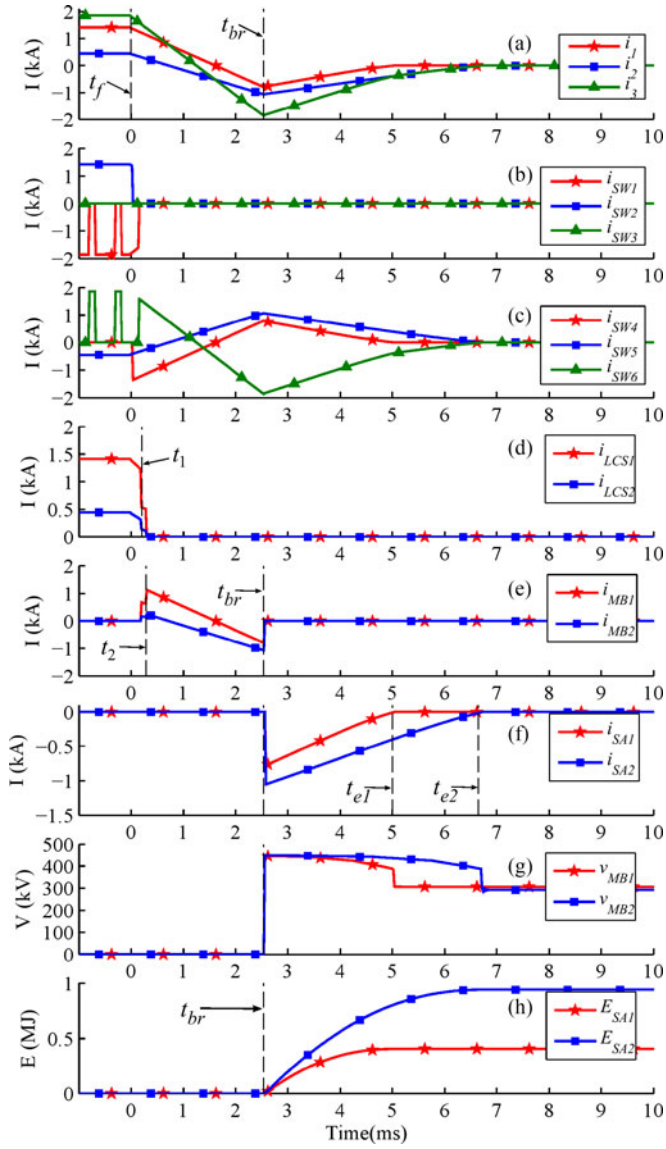

Fig. 11. Typical scheme waveforms for fault at bus B_1.

is equal to sum of currents in LCS_2 and LCS_3 of the CFCCB and, therefore, is higher than the currents in other units. Note that the current in LCS_1 flows through its antiparallel diodes during the bus fault. Hence, the current rating of the IGBTs is equal.

B. MB Units

During the line fault, the current in corresponding MB units of the CFCCB and the HCB is equal. Similar to the previous subsection, the antiparallel diodes of MB_1 in the CFCCB may need to be able to carry higher current as compared to the other units depending on the fault identification time and the grid topology. As illustrated in Table IV, the typical approach requires a larger number of IGBTs in MB units of HCBs as compared to the proposed CFCCB. V_{CES} represents the collector–emitter blocking voltage of IGBTs in Table IV.

C. Surge Arresters

1) Rated Voltage: The rated voltage for the SA of the HCB would lie in range of $1.4V_{\rm dc} - 1.5V_{\rm dc}$ [13], [14]. The rated voltage of SAs of the CFCCB is also assumed to lie in the same range.

2) Discharge Current: Equation (14) illustrates that the maximum discharge current in the SAs of the CFCCB in the line fault scenario is almost half of the fault current at the interruption instance. However, the maximum discharge current in the SA in the typical HCB is almost equal to the interrupted current. Therefore, the maximum discharge current in the SAs of the CFCCB is almost 50% smaller than that of the typical scheme.

3) Energy: Transmission line fault: In the typical scheme and during the line fault, only the faulty line HCB interrupts the current and its SA absorbs the energy. When using the CFCCB, the faulted line corresponding SA does not absorb the energy

TABLE III
CFCCB AND HCB PARAMETERS DURING BUS FAULT

Parameters CFCCB (HCB)	CFCCB		HCB	
	Analysis	Simulation	Analysis	Simulation
$I_{\max}^{\mathrm{LCS1}}$ ($I_{\max}^{\mathrm{LCS12}}$) [kA]	– 0.96	– 0.98	– 1.19	– 1.24
$I_{\max}^{\mathrm{LCS2}}$ ($I_{\max}^{\mathrm{LCS13}}$) [kA]	– 0.133	– 1.151	– 0.29	– 0.33
$I_{\max}^{\mathrm{LCS3}}$ (-) [kA]	– 1.103	– 1.13	–	–
$I_{\max}^{\mathrm{MB1}}$ ($I_{\max}^{\mathrm{MB12}}$) [kA]	– 0.933	– 0.81	– 0.75	– 0.78
$I_{\max}^{\mathrm{MB2}}$ ($I_{\max}^{\mathrm{MB13}}$) [kA]	– 1.19	– 1.056	–1.059	– 1.06
$I_{\max}^{\mathrm{MB3}}$ (-) [kA]	– 2.12	– 1.84	–	–
E_{SA1} (E_{SA12}) [MJ]	0.534	0.442	0.452	0.406
E_{SA2} (E_{SA13}) [MJ]	1.249	0.995	1.056	0.941
E_{SA3} [MJ]	0	0	–	–

TABLE IV
CFCCB- AND HCB-BASED METHODS PARAMETER COMPARISON

Parameter	HCB	CFCCB
Number of UFDs	2	2
Number of limiting ind.	2	2
Number of surge arresters	2	3
Surge arresters energy	E	$\frac{E}{2}$
Surge arresters voltage	V_r	V_r
Number of IGBTs in LCS	$2N_{\mathrm{LCS}}$	0
Number of IGBTs in MB	$\frac{4V_r}{V_{\mathrm{CES}}}$	$\frac{3V_r}{V_{\mathrm{CES}}}$

and the energy absorption is shared between two SAs. Using (18) and (29) and assuming identical current at the interruption instant in both schemes, the ratio of the total absorbed energy in both schemes can be given as

$$\frac{E_{\mathrm{SA},T}^{\mathrm{CFCCB}}}{E_{\mathrm{SA},T}^{\mathrm{HCB}}} = \frac{1}{2} \tag{33}$$

where $E_{\mathrm{SA},T}^{\mathrm{CFCCB}}$ and $E_{\mathrm{SA},T}^{\mathrm{HCB}}$ represent the total absorbed energy in the SAs of the CFCCB and the HCB, respectively. Equation (33) implies that the energy rating of SAs in the CFCCB is almost 50% smaller than that of the HCB.

b) DC-bus fault: The CFCCB performance during the dc-bus fault was found to be similar to the typical method. Therefore, equal amount of energy is absorbed in the SAs in both schemes.

D. Ultrafast Disconnector

Each HCB has an UFD. As shown in Fig. 1, the CFCCB has two UFDs. Therefore, there is no difference in the number of required UFD units for both the typical and proposed schemes.

E. Current-Limiting Inductors

The number of current-limiting inductors in both schemes is same. Also, the inductances of current-limiting inductors for the proposed and typical devices are equal.

VII. CONCLUSION

In this paper, a novel current flow controlling dc circuit breaker (CFCCB) has been proposed and analyzed. The proposed CFCCB has three ports and can connect a dc bus to two adjacent transmission lines. Each port of the CFCCB can interrupt its current, independent of the other ports and irrespective of the current direction. Furthermore, the proposed device possesses an embedded interline dual H-bridge CFC, which can regulate the current in one of the adjacent transmission lines.

While the proposed device shows similar behavior compared to the typical scheme from the system-level view, it can reduce the requirements of different elements of the system. The analysis and simulations imply that the proposed CFCCB requires fewer IGBTs compared to the typical approach. For a dc bus with two adjacent transmission lines, the CFCCB needs at least 25% fewer IGBTs as compared to the typical scheme.

Moreover, the proposed device requires smaller size SAs due to the less energy absorption in its SAs. In addition, the maximum current discharge in the SAs in the proposed method is smaller to that of the typical method. The results from this study confirm that the energy and discharge current ratings of the SAs can be reduced by almost 50%. Considering the improvements by applying the proposed device, its implementation cost is expected to be remarkably lower than the cost of the typical scheme. The future work will concern with the cost benefit and reliability studies of the proposed device.

TABLE V
THREE-TERMINAL TEST GRID AND CFC PARAMETERS

Transmission Lines Parameters			
Lumped T-model Parameters	R [Ω/km]	L [mH/km]	C [μ F/km]
0.01105	3.245	0.382	
Length [km]	Line 12	Line 13	Line 23
	200	300	200
VSC Parameters			
Bus	**1**	**2**	**3**
Capacitance [μ F]	1000	1000	1000
Power [MW]	600	–	–
V_i^* [kV]	–	300	300
Droop Constant k_i [A/V]	–	0.05	0.5
Voltage [kV]	320	320	320
Filter reactor [mH]	10	10	10
CFC Parameters			
Nominal Voltage [kV]	4		
Capacitor [mF]	10		
Switching Frequency [kHz]	2		
PI	$0.012 + \frac{0.398}{s}$		
Compensator	$\frac{0.3421s^2 + 1.2978s + 21.5213}{s^2 + 120.5323s + 3207.9071}$		
Filter	$\frac{1}{0.08s + 1}$		

REFERENCES

[1] D. V. Hertem, O. Gomis-Bellmunt, and J. Liang, *HVDC GRIDS For Offshore and Supergrid of the Future*. New York, NY, USA: Wiley, 2016.

[2] B. C. N. Chaudhuri, R. Majumder, and A. Yazdani, *Multi-Terminal Direct-Current Grids: Modeling, Analysis, and Control*. New York, NY, USA: Wiley, 2014.

[3] A. Mokhberdoran, N. Silva, H. Leite, and A. Carvalho, "Unidirectional protection strategy for multi-terminal HVDC grids," *Trans. Environ. Elect. Eng.*, vol. 1, no. 4, pp. 58–65, 2016.

[4] A. Mokhberdoran and A. Ajami, "Symmetric and asymmetric design and implementation of new cascaded multilevel inverter topology," *IEEE Trans. Power Electron.*, vol. 29, no. 12, pp. 6712–6724, Dec. 2014.

[5] C. M. Franck, "Hvdc circuit breakers: A review identifying future research needs," *IEEE Trans. Power Del.*, vol. 26, no. 2, pp. 998–1007, Apr. 2011.
[6] A. Mokhberdoran, A. Carvalho, H. Leite, and N. Silva, "A review on HVDC circuit breakers," in *Proc. 3rd Renew. Power Gener. Conf.*, Sep. 2014, pp. 1–6.
[7] J. Sau-Bassols, E. Prieto-Araujo, and O. Gomis-Bellmunt, "Modelling and control of an interline current flow controller for meshed HVDC grids," *IEEE Trans. Power Del.*, vol. 32, no. 1, pp. 11–22, Feb. 2017.
[8] K. A. Corzine, "A new-coupled-inductor circuit breaker for dc applications," *IEEE Trans. Power Electron.*, vol. 32, no. 2, pp. 1411–1418, Feb. 2017.
[9] D. Keshavarzi, T. Ghanbari, and E. Farjah, "A z-source based bidirectional dc circuit breaker with fault current limitation and interruption capabilities," *IEEE Trans. Power Electron.*, vol. PP, no. 99, p. 1, doi: 10.1109/TPEL.2016.2624147
[10] A. Maqsood, A. Overstreet, and K. A. Corzine, "Modified z-source dc circuit breaker topologies," *IEEE Trans. Power Electron.*, vol. 31, no. 10, pp. 7394–7403, Oct. 2016.
[11] A. Mokhberdoran, A. Carvalho, N. Silva, H. Leite, and A. Carrapatoso, "A new topology of fast solid-state HVDC circuit breaker for offshore wind integration applications," in *Proc. 17th Eur. Conf. Power Electron. Appl.*, Sep. 2015, pp. 1–10.
[12] J. Hafner and B. Jacobson, "Proactive hybrid HVDC breakers—A key innovation for reliable HVDC grids," in *Proc. Electr. Power Syst. Future—Integr. Supergrids Microgrids Int. Symp.*, 2011, pp. 1–9.
[13] A. Hassanpoor, J. Hafner, and B. Jacobson, "Technical assessment of load commutation switch in hybrid HVDC breaker," *IEEE Trans. Power Electron.*, vol. 30, no. 10, pp. 5393–5400, Oct. 2015.
[14] G. Liu, F. Xu, Z. Xu, Z. Zhang, and G. Tang, "Assembly HVDC breaker for HVDC grids with modular multilevel converters," *IEEE Trans. Power Electron.*, vol. 32, no. 2, pp. 931–941, Feb. 2017.
[15] A. Mokhberdoran, A. Carvalho, N. Silva, H. Leite, and A. Carrapatoso, "Application study of superconducting fault current limiters in meshed hvdc grids protected by fast protection relays," *Electr. Power Syst. Res.*, vol. 143, pp. 292–302, 2017.
[16] C. D. Barker and R. S. Whitehouse, "A current flow controller for use in HVDC grids," in *Proc. 10th IET Int. Conf. AC DC Power Transmiss.*, Dec. 2012, pp. 1–5.
[17] D. Jovcic, M. Hajian, H. Zhang, and G. Asplund, "Power flow control in dc transmission grids using mechanical and semiconductor based dc/dc devices," in *Proc. 10th IET Int. Conf. AC DC Power Transmiss.*, Dec. 2012, pp. 1–6.
[18] S. Balasubramaniam, J. Liang, and C. E. UgaldeLoo, "Control, dynamics and operation of a dual h-bridge current flow controller," in *Proc. IEEE Energy Convers. Congr. Expo.*, Sep. 2015, pp. 2386–2393.
[19] V. Hofmann, A. Schn, and M. M. Bakran, "A modular and scalable HVDC current flow controller," in *Proc. 17th Eur. Conf. Power Electron. Appl.*, Sep. 2015, pp. 1–9.
[20] M. Ranjram and P. W. Lehn, "A multiport power-flow controller for dc transmission grids," *IEEE Trans. Power Del.*, vol. 31, no. 1, pp. 389–396, Feb. 2016.
[21] W. Chen *et al.*, "A novel interline dc power-flow controller (IDCPFC) for meshed HVDC grids," *IEEE Trans. Power Del.*, vol. 31, no. 4, pp. 1719–1727, Aug 2016.
[22] W. Leterme and D. V. Hertem, "Classification of fault clearing strategies for HVDC grids," in *Proc. Lund Symp., Cigre*, Lund, Sweden, 2015.
[23] D. Jovcic and K. Ahmed, *High Voltage Direct Current Transmission: Converters, System and DC Grid*. New York, NY, USA: Wiley, 2015.
[24] W. Lin, D. Jovcic, S. Nguefeu, and H. Saad, "Modelling of high-power hybrid dc circuit breaker for grid-level studies," *IET Power Electron.*, vol. 9, no. 2, pp. 237–246, 2016.

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