A Novel Method Based on Self-Power Supply Control for Balancing Capacitor Static Voltage in MMC

Longfei Luo, Yanbin Zhang, *Member, IEEE*, Lixin Jia, *Member, IEEE*, and Ningning Yang

***Abstract*—The modular multilevel converter is one of the most attractive converter topologies for high-voltage dc transmission systems, but it needs at least 10 min during the system uncontrolled precharge stage to verify the stability and reliability of submodules (SMs), making the capacitor static voltage balancing a key issue. This paper proposes a novel method based on self-power supply control for balancing capacitor static voltage. Because of the influence of self-power supplies on capacitor voltages, the method can keep the capacitor static voltage balanced by controlling the input characteristic of SMs self-power supplies. The control signals of self-power supplies have a fixed frequency and duty ratio, and they can be determined based on capacitor voltage sorting results and self-power supply output support capacitor. Compared with previous works, this method has less computation, and it does not rely on IGBTs and additional complex circuits except for the self-power supplies. This can save on the software and hardware costs. The proposed method also leads to improved equalizing resistances and reduced active power losses of the SMs. Simulations and experimental studies were conducted, and the results confirm the effectiveness of the proposed method.**

***Index Terms*—Capacitor static voltage balancing, equalizing resistance, high-voltage dc transmission (HVDC), modular multilevel converter (MMC), self-power supply control.**

I. Introduction

MODULAR multilevel converter (MMC) is a potential candidate for medium or high-power applications, specifically for high-voltage direct current (HVDC) transmission systems because of its scalability, higher power-handling capability, modular structure, common dc-bus, distributed dc capacitors, etc. [1]–[5].

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Capacitor voltage imbalance is a serious threat to the reliable operation of HVDC systems based on MMC. During the system controlled precharge and normal operation stages, the nonideal drive pulses of submodules (SMs) cause this capacitor voltage imbalance. During the system uncontrolled precharge stage, the differences in power electronic device parasitic parameters are closely related to the capacitor static voltage imbalance. In particular, the losses differences of self-power supplies that obtain energy from SM capacitors are the main factor causing capacitor static voltage imbalances. Keeping the SM capacitor voltages balanced at their nominal values has become one of the main technical challenges for MMC [6]–[9]. To date, many papers on voltage balancing control methods have been published, and they can be roughly categorized into two groups: distributed voltage closed loop control methods and centralized SM selection control methods [10]. They both involve controlling capacitor voltages based on the control of insulated-gate bipolar transistors (IGBTs) during the controlled precharge and normal operation stages of the HVDC system [11]–[15]. The existing methods in both groups can control the capacitor voltage balancing well, but during the uncontrolled precharge stage of systems, the IGBTs are always locked, leaving the capacitor voltages in an uncontrollable state. Therefore, the existing methods in the two groups cannot be used for MMC systems.

According to the minimum dc voltage test requirements of the international standard IEC62501, the capacitor voltages need to be maintained in a good balanced state for not less than 10 min during the system uncontrolled precharge stage to verify the correct performance of SM designs [16]. Because IGBTs are locked in this stage, the capacitor voltage balancing can be achieved by adding equalizing resistances to the SM capacitors [23]. However, the equalizing resistances are relatively small, and they will be connected to the capacitors during the whole working process of MMC systems, leading to more active power losses in the systems. Methods for voltage balancing by using additional circuits were proposed in [17]–[19]. Ajami *et al.* [17] presented a parallel switch-based chopper circuit for voltage balancing, and the capacitor voltages were efficiently controlled by a switching scheme. When the method is applied in MMC, it requires a large number of switching devices and increases the costs and losses of SMs. Ewanchuk and Salmon, [18] presented a modular balancing bridge for series-connected voltage sources, where the voltage balancing is achieved across N cells using cascaded transformers with coupled windings. This method may be used

in MMC systems, but it requires a large number of transformers and increases the complexity of the SM designs. A voltage balancing circuit consisting of two unidirectional choppers and a single coupled inductor with two Galvanically isolated windings was proposed in [19], where the phase-shift control is used to adjust the balancing circuit. For MMC systems, the hardware costs and the complexity of the system control for this method are significantly increased.

Because of the limitations of the methods mentioned above, this paper proposes a simple and low-loss capacitor static voltage balancing method. By taking into consideration the influence of self-power supplies on capacitor voltages, this method can keep the capacitor static voltage balanced by controlling the input characteristic of the self-power supplies. The control signals of self-power supplies have a fixed frequency and duty ratio, and they can be generated based on SM capacitor voltage sorting results and self-power supply output support capacitor. Based on the control signals, the input current of self-power supply with the lowest SM capacitor voltage is decreased, and the voltage and input current of corresponding capacitor will be increased. Therefore, the capacitor voltage balancing can be controlled indirectly by using the control signals. Compared with previous works, this novel method has a simple control strategy and hardware circuit. In particular, this method has less computation, and it does not rely on IGBTs and additional complex circuits other than the self-power supplies. This leads to significant savings for software and hardware.

Another main contribution of this paper is that the equalizing resistances of SMs are improved based on the proposed voltage balancing method. Although the proposed method can balance the capacitor static voltage well without equalizing resistances, it still needs suitable resistances to discharge the SMs when the systems stop working. The calculated discharge resistance is much larger than the conventional equalizing resistance. The equalizing resistances are improved, and the active power losses of SMs are reduced.

The paper is organized as follows. In Section II, the basic structure and capacitor static voltage imbalance phenomenon of MMCs are described. Section III proposes the capacitor static voltage balancing method for the MMC. Sections IV and V describe system simulations and experimental tests, respectively, to show the effectiveness of the proposed method. Finally, Section VI presents the conclusions.

II. Structure and Voltage Imbalance Phenomenon of MMCs

A. Structure of an MMC

The topologies of an MMC and SM unit are shown in Fig. 1. The upper arm and the lower arm in the same phase comprise a phase leg. Each arm has *N* identical SMs and one smoothing inductor *L*. Each SM in an engineering application is composed of a bypass switch (S), a thyristor (VT), two power semiconductor switches (VT1 and VT2) with antiparallel diodes (VD1 and VD2) representing two IGBTs with freewheeling diodes (or other types), a dc capacitor (C), an equalizing resistance (R), and a self-power supply. There are two functions of the bypass switch in an SM: It protects the SM when the SM fails, and it ensures the continuity of the arm current for the MMC. The thyristor in an SM is used to protect the diode VD2 when a short-circuit fault occurs in an MMC system [20]. A self-power supply, which obtains energy from a capacitor, is used to supply power for the driving and control circuits of the SM [21]. In order to reduce the influence of capacitor failure on the SM driving and control circuits, the flyback topology with isolated two-stage transformers is adopted in the design of the self-power supply. The equalizing resistance in the SM is used to keep the capacitor static voltage balanced.

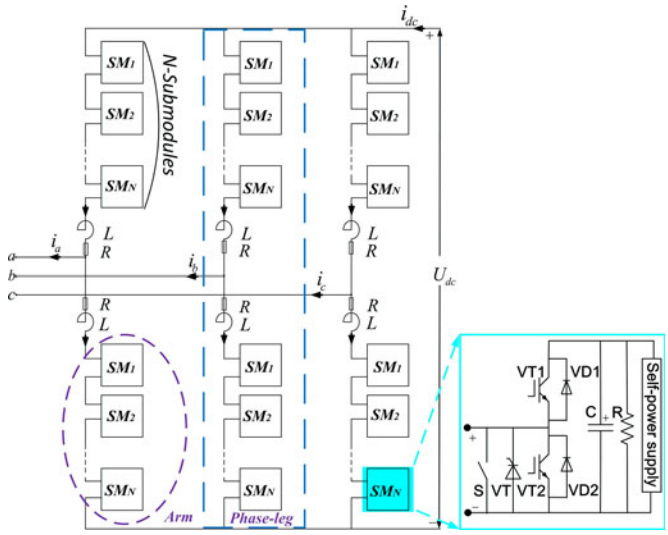

Fig. 1. Block diagram of an MMC and SM unit.

B. Capacitor Static Voltage Imbalance Phenomenon

The MMC can be precharged by two methods during start-up processes: the ac system precharge method and the dc line precharge method. Both of these methods can be divided into two stages: the uncontrolled precharge stage and controllable precharge stage [11]. Due to the IGBTs are locked during the uncontrolled precharge stage, the capacitor static voltage imbalance is obvious in this stage. In particular, when the dc line is selected to precharge the MMC, the SM capacitor will have a 50% voltage difference away from the rated value [22], and the voltage imbalance becomes serious.

Taking one phase of an MMC as an example, the system uncontrolled precharge process based on dc line is shown in Fig. 2. The arm current i_{pa} can be described as follows:

$$i_{pa} = i_{ck} + i_{dk} + i_{pk} \tag{1}$$

with

$$i_{pa} = c\frac{du_{ck}}{dt} + \frac{u_{ck}}{R_d} + i_{pk} \tag{2}$$

where $k = 1, 2, 3 \ldots .2N$, u_{ck} indicates capacitor voltage, i_{ck} is the current flowing into the capacitor, i_{dk} is the current that flows through the R_d, and i_{pk} is the current flowing into the self-power supply.

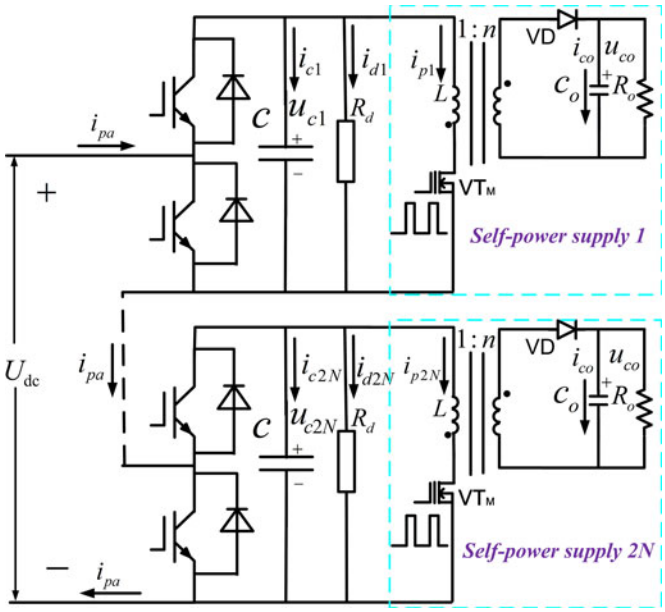

Fig. 2. One phase of an MMC with dc line uncontrolled precharge.

In equations (1) and (2), the i_{pk} difference between self-power supplies is the main factor causing the capacitor voltage imbalance. To further analyze the self-power supply, the self-power supply average model in a switching cycle T can be described as follows:

$$\begin{cases} L\dfrac{di_{pk}}{dt} = u_{ck}D - \dfrac{u_{co}}{n}(1-D) \\ c_o\dfrac{du_{co}}{dt} = \dfrac{i_{pk}}{n}(1-D) - \dfrac{u_{co}}{R_o} \end{cases} \tag{3}$$

where D is the duty cycle of the self-power supply, n is the turns ratio of transformer, u_{co} is the output voltage of self-power supply, and R_o is the equivalent resistance of SM driving and control circuits.

According to the relationships between i_{pk} and u_{ck} in (2) and (3), when the R_o is smaller than the equivalent resistances of the other SM driving and control circuits, the u_{co} will be decreased. In order to maintain the stability of u_{co}, the i_{pk} needs to be increased, and the u_{ck} needs to be decreased. In order to meet the input power requirements of the self-power supply, the decrease of u_{ck} will lead to the increase of the duty cycle D, and it will also lead to the increase of i_{pk} again. In this process, the degree of capacitor voltage imbalance will be more serious with the accumulation of time.

In order to reduce the effect of the self-power supply on the capacitor voltage, the basic voltage balancing method selects a suitable R_d to minimize the effect of current i_{pk}. According to (1) and (2), the i_{ck} can also be written as follows:

$$i_{ck} = i_{pa} - \frac{u_{ck}}{R_d} - i_{pk}. \tag{4}$$

Based on the principles of automatic control, when the capacitor voltages are maintained at capacitor average voltage $\bar{u}_c$, (4) needs to meet the following conditions [23]:

$$\frac{di_{ck}}{du_{ck}} = \frac{d}{du_{ck}}\left[i_{pa} - \frac{u_{ck}}{R_d} - i_{pk}\right]\Big|_{u_{ck}=\bar{u}_c} < 0. \tag{5}$$

The i_{pk} in (5) can be approximately expressed as

$$i_{pk} = \frac{p_s}{u_{ck}}. \tag{6}$$

The R_d can be calculated as follows:

$$R_d < \frac{\bar{u}_c^2}{p_s} \tag{7}$$

where p_s is the input power of the self-power supply. Although (7) provides a range of R_d, the resistance is relatively small, and it will cause more losses to the SMs.

III. Proposed Capacitor Voltage Balancing Method

A. Proposed Capacitor Static Voltage Balancing Schemes

Taking one arm of an MMC as an example, several schemes of capacitor static voltage balancing are proposed by the analysis of capacitor static voltage imbalance phenomenon, and they can be shown as Fig. 3.

Scheme 1: Fig. 3(a) shows the capacitor static voltage balancing scheme based on self-power supply load switching circuit. In Fig. 3(a), the self-power supply load switching circuit is composed of a MOSFET and a resistor R_s, and it can regulate the capacitor voltages by the control of the MOSFET. The control process of capacitor voltages can be divided into three steps. The first step involves sorting the capacitor voltages from low to high when the voltage sorting control signal is logic high, and the second step is to calculate the maximum voltage difference of SM capacitors. The third step is to select the self-power supply load switching circuit with highest capacitor voltage when the maximum voltage difference is greater than the set value. Based on the three steps, the self-power supply load switching circuit with highest capacitor voltage is controlled by using a control signal with fixed frequency and duty ratio, and the other load switching circuits remain stopped. The essence of this scheme is to control the voltage balancing indirectly by increasing the load of the self-power supply with highest capacitor voltage.

Scheme 2: The voltage balancing scheme based on self-power supply mutual providing energy circuit is shown as Fig. 3(b). In Fig. 3(b), each self-power supply not only provides energy to its load, but also provides energy to other self-power supply loads. The VDs is the diode that prevents circulating current between self-power supplies. The voltage balancing control can be divided into three steps, and the first two steps of this scheme are same with that of scheme 1. In this scheme, when the maximum voltage difference is greater than the set value, the self-power supply with lowest capacitor voltage is forced to stop working, and other self-power supplies work normally. This scheme focuses on improving input impedance of the self-power supply by stopping the self-power supply with lowest capacitor voltage, and thus the capacitor voltage balancing can be controlled indirectly.

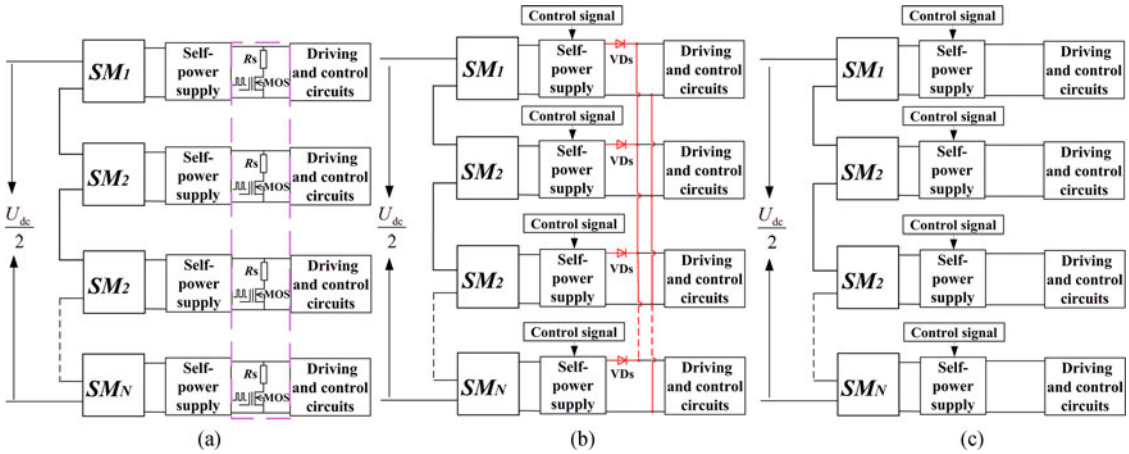

Fig. 3. Schemes of capacitor static voltage balancing. (a) Voltage balancing based on self-power supply load switching circuit. (b) Voltage balancing based on self-power supply mutual providing energy circuit. (c) Voltage balancing based on self-power supply input characteristic regulation.

TABLE I
SUMMARY OF THREE VOLTAGE BALANCING SCHEMES

Items	Advantages	Disadvantages
Voltage Balancing in Fig. 3(a)	Independent of main circuit. Flexible control.	High number of switching devices. High device losses
Voltage Balancing in Fig. 3(b)	Reliable power supply for driving and controlling circuits. Simple control strategy.	Circuit connection is complicated. Need more diodes.
Voltage Balancing in Fig. 3(c)	Simple control strategy and structure. No external switching devices. No need extra diodes.	There are small fluctuations in the output voltage of self-power supply

Scheme 3: Fig. 3(c) shows the voltage balancing scheme based on self-power supply input characteristic regulation. This scheme does not need any external accessory circuits other than self-power supplies. This capacitor voltage balancing control can also be divided into three steps, and the first two steps of this scheme are same with that of schemes 1 and 2. In this scheme, when the maximum voltage difference is greater than the set value, a control signal with fixed frequency and duty ratio is used to regulate the input characteristic of self-power supply with lowest capacitor voltage, and other self-power supplies work normally. When the control signal begins to work, the input impedance and input current of self-power supply with lowest capacitor voltage will be improved and decreased, respectively. In this manner, the voltage and input current of corresponding capacitor will be increased, and the capacitor voltage balancing can be controlled indirectly.

The advantages and disadvantages of the three capacitor voltage balancing schemes are summarized in Table I. According to the Table I, the following section will focus on the voltage balancing scheme based on self-power supply input characteristic regulation (scheme 3).

B. Principles of Voltage Balancing Based on Self-Power Supply Input Characteristic Regulation

In the proposed scheme in Fig. 3(c), the load (driving and control circuits) of a self-power supply can be considered as a constant power load, and the self-power supply with a constant power load can also be considered as an approximately constant power load to the SM capacitor. Due to the u_{ck} and i_{pk} are closely related to the approximately constant power p_s and the capacitor voltage balancing control based on self-power supply input characteristic regulation, the relationships between u_{ck} and i_{pk} need to be studied. There are three steps to do that.

1) Equivalent Transformation of the SM Capacitor Branch: The u_{ck} in Fig. 2 can also be written as follows:

$$u_{ck} = \frac{1}{c}\int_{-\infty}^{t} i_{ck}d\tau. \tag{8}$$

During the voltage change time ΔT, the u_{ck} in (8) can be described as follows:

$$u_{ck} = \underbrace{\frac{1}{c}\int_{-\infty}^{t-\Delta T} i_{ck}d\tau}_{\text{part1}} + \underbrace{\frac{1}{c}\int_{t-\Delta T}^{t} i_{ck}d\tau}_{\text{part2}}. \tag{9}$$

The part 1 of u_{ck} represents the capacitor voltage u_{ck} (t–ΔT) at time t–ΔT, and part 2 can be solved by the integral of the trapezoidal area. Therefore, the (9) can be simplified to

$$u_{ck} = u_{ck}(t-\Delta T) + \frac{i_{ck}(t)+i_{ck}(t-\Delta T)}{2c}\Delta T \tag{10}$$

with

$$u_{ck} = R_c i_{ck}(t) + u_{ck\text{eq}} \tag{11}$$

where the R_c is equal to $\Delta T/2c$, and the $u_{ck\text{eq}}$ can be expressed as follows:

$$u_{ck\text{eq}} = R_c i_{ck}(t-\Delta T) + u_{ck}(t-\Delta T). \tag{12}$$

Based on (11) and (12), the equivalent transformation of SM capacitor branch is shown as Fig. 4(a).

2) Equivalent Transformation of the SM Self-power Supply Branch: Assuming that the input characteristic of power supply meets the function $i = f(u)$, based on Newton–Raphson method, the Taylor approximate expansion of $i = f(u)$ at

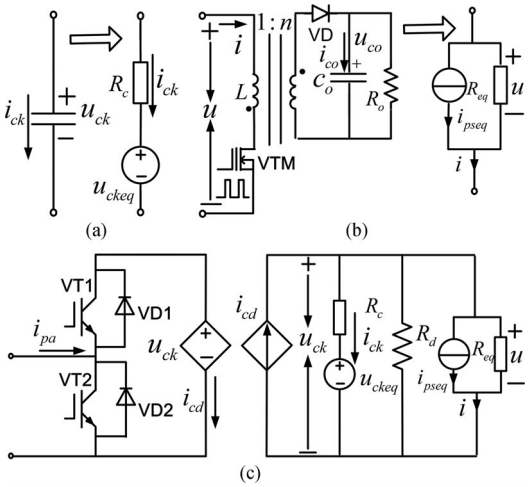

Fig. 4. Equivalent transformation of the SM. (a) Equivalent transformation of capacitor branch. (b) Equivalent transformation of self-power supply branch. (c) Equivalent transformation of the SM by the controlled voltage source and current source.

$(u_{ck},\, i_{pk})$ can be written as follows:

$$i = f(u_{ck}) + f'(u_{ck})(u - u_{ck}) + \sum_{n=2}^{\infty} \frac{1}{n!} f^{(n)}(u_{ck})(u - u_{ck})^n. \tag{13}$$

Ignoring the higher-order terms in (13), it can be simplified to

$$i \approx f(u_{ck}) + f'(u_{ck})(u - u_{ck}) \tag{14}$$

with

$$i \approx i_{pseq} + G_{\rm eq} u \tag{15}$$

where the i_{pseq} and $G_{\rm eq}$, respectively, are expressed as follows:

$$i_{pseq} = i_{pk} - f'(u_{ck}) u_{ck} \tag{16}$$

$$G_{\rm eq} = \frac{1}{R_{\rm eq}} = f'(u_{ck}). \tag{17}$$

Based on (15) to (17), the equivalent transformation of the SM self-power supply branch is shown in Fig. 4(b).

3) Equivalent Transformation of the SM: Separating the IGBTs branch and SM capacitor branch by using the controlled voltage source and current source, the equivalent transformation of the SM is shown in Fig. 4(c).

In Fig. 4(c), the u_{ck} and i_{ck} can be expressed as follows:

$$u_{ck} = \frac{R}{R + R_c}(u_{ckeq} - R_c i_{pseq} + R_c i_{cd}) \tag{18}$$

$$i_{ck} = \frac{u_{ck} - u_{ckeq}}{R_c}. \tag{19}$$

The *R* and i_{cd} in (18) can be expressed as follows:

$$R = \frac{R_d R_{\rm eq}}{R_d + R_{\rm eq}} \tag{20}$$

with

$$i_{cd} = i_{pa}. \tag{21}$$

Based on the (15) to (21), the capacitor voltage u_{ck} and input characteristic of self-power supply can be changed by controlling i_{pseq}, and the i_{pseq} can be regulated by i_{pk}. If the i_{pk} in (16) is decreased, the i_{pseq} will also be decreased because the u_{ck} cannot suddenly change. When a control signal with fixed frequency and duty ratio is used to improve the input impedance of self-power supply with the lowest SM capacitor voltage, the current i_{dk} of R_d is almost not change, while the i_{pk} of self-power supply will be decreased. Based on the (1), (2), and (4), the decrease of i_{pk} will lead to the increase of capacitor current i_{ck}. Accordingly, the u_{ck} will be increased according to the (8) to (12). The increase of u_{ck} will also meet the requirements of self-power supply constant power input. In this paper, control signals with fixed frequency and duty ratio are used to regulate the input characteristic of self-power supplies. Depending on the control signals, the i_{pk} of the self-power supply with the lowest SM capacitor voltage is decreased, and the i_{ck} and u_{ck} of the corresponding capacitor are increased. In this way, the capacitor voltage balance can be controlled indirectly.

C. Voltage Balancing Method

Fig. 5(a) shows the capacitor static voltage balancing control framework. The arm controller in Fig. 5(a) is used to select the self-power supply with lowest SM capacitor, and SM controllers are used to generate the control signals of corresponding self-power supplies. The selection process of self-power supplies can be divided into four steps: 1) calculating the frequency and duty ratio of voltage sorting control signal, 2) generating the voltage sorting control signal, 3) sorting the capacitor voltages from low to high when the voltage sorting control signal is logic high, and 4) calculating the maximum capacitor voltages difference. Based on this selection process, when the maximum capacitor voltages difference is greater than the set value, the control signal generated by the SM controller is used to stop the self-power supply with lowest SM capacitor voltage. Other self-power supplies continue to work normally.

The block diagram of self-power supply with two-stage transformers isolated is shown in Fig. 5(b), and the logic of the capacitor voltage balancing control is shown in Fig. 6. In Fig. 6, to control the voltage balancing, the first step is to calculate the frequency f_p and duty ratio D_p of voltage sorting control signal d_s:

$$\begin{cases} f_p = \dfrac{1}{2T_p} \\ D_p = 0.5 \end{cases} \tag{22}$$

where T_p is the time it takes for self-power supply output voltage u_{co} to decrease to the load minimum working voltage $u_{\rm com}$.

For the self-power supply described in Fig. 5(b) to work properly in the case of $f_p = 1/2T_p$, ignoring the effect of transformer inductance on the voltage output support capacitor c_o, the approximate T_p can be calculated from

$$\left(\frac{p_{so}}{u_{\rm com}} + \frac{p_{so}}{u_{co}}\right)\frac{T_p}{2} = (u_{co} - u_{\rm com})c_o$$

$$T_p = \frac{2c_o(u_{co} - u_{\rm com})u_{\rm com}u_{co}}{(u_{co} + u_{\rm com})p_{so}} \tag{23}$$

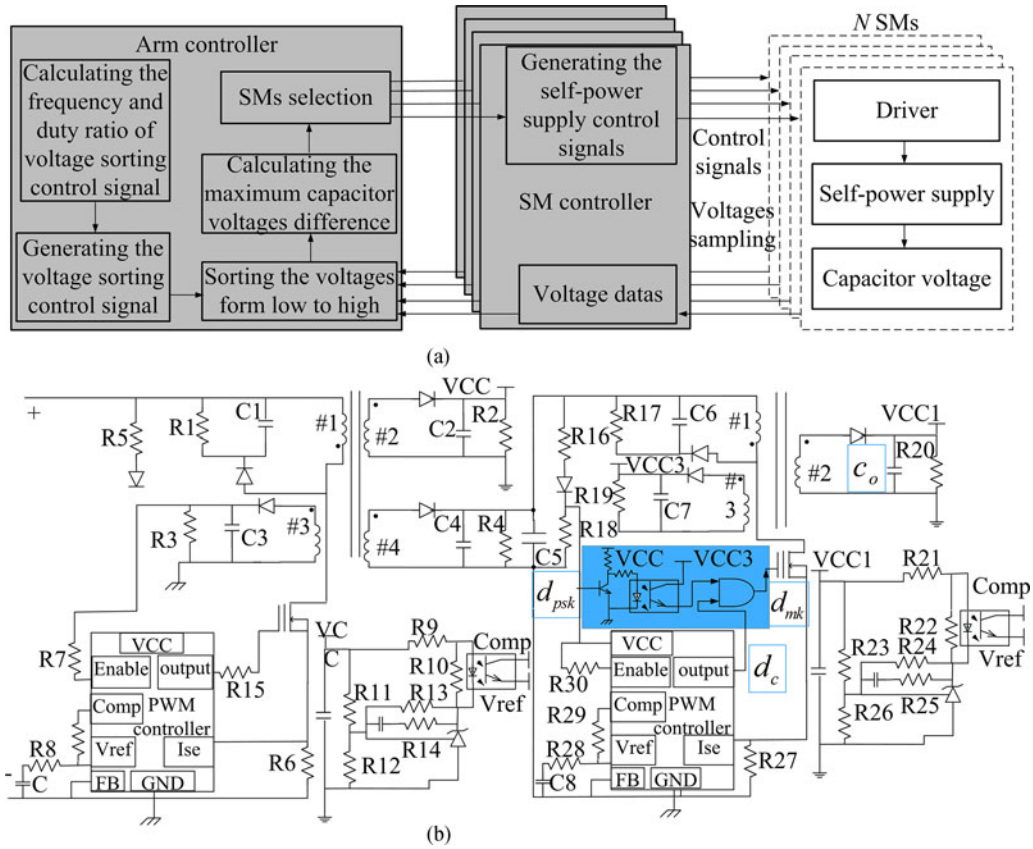

Fig. 5. Capacitor voltage balancing method. (a) Voltage balancing control framework. (b) Block diagram of self-power supply.

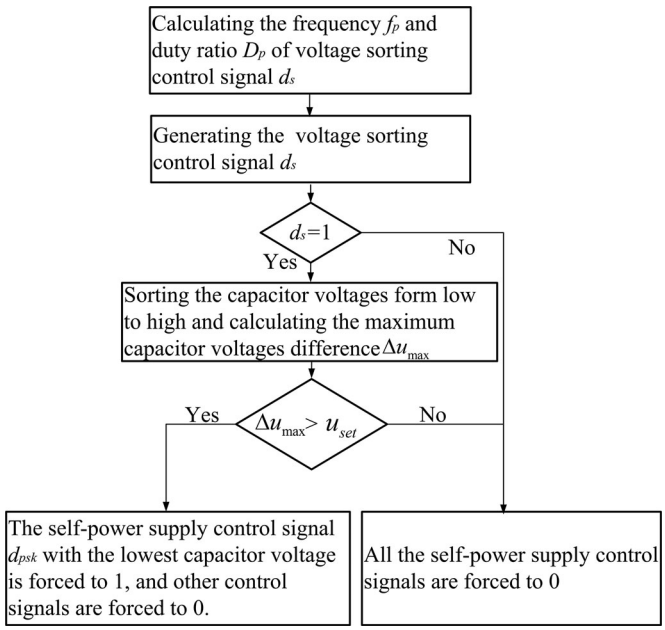

Fig. 6. Logic of capacitor voltage balancing control.

where p_{so} is the power of the SM driving and control circuits.

According to (22) and (23), the voltage sorting control signal d_s will be generated. A $d_s = 1$ indicates that the voltage sorting control signal is logic high, and $d_s = 0$ means that the voltage sorting control signal is logic low. When $d_s = 1$, the capacitor voltages will be sorted form low to high, and the maximum capacitor voltage difference $\Delta u_{\max}$ is calculated. If $\Delta u_{\max} > u_{\text{set}}$ (u_{set} is the set value of capacitor voltages difference), the self-power supply control signal d_{psk} with the lowest capacitor voltage is forced to 1, and other control signals are forced to 0. In contrast, if $\Delta u_{\max} \leq u_{\text{set}}$, all the self-power supply control signals are forced to 0. When $d_s = 0$, all the self-power supply control signals are also forced to 0. A $d_{psk} = 1$ indicates that the self-power supply has stopped working, and the $d_{psk} = 0$ means that the self-power supply is working normally.

Due to the self-power supply control signal d_{psk} is determined by the voltage sorting control signal d_s, when $d_s = 1$ and $\Delta u_{\max} > u_{\text{set}}$, the frequency f_{ps} and duty ratio D_{ps} of self-power supply control signal d_{psk} with the lowest capacitor voltage can be written as

$$\begin{cases} f_{ps} = 1/2T_p \\ D_{ps} = 0.5 \end{cases}. \tag{24}$$

When $d_s = 0$ or $\Delta u_{\max} \leq u_{\text{set}}$, the frequency f_{ps} and duty ratio D_{ps} of self-power supply control signal d_{psk} can be written as follows:

$$\begin{cases} f_{ps} = 0 \\ D_{ps} = 0 \end{cases}. \tag{25}$$

According to the (24) and (25), the gate signal d_{mk} of self-power supply MOSFET in Fig. 5(b) can be obtained by the logic "and" operation of d_c and $\overline{d_{psk}}$. Hence, the d_{mk} can be

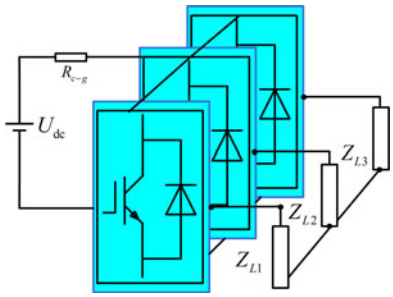

Fig. 7. MMC system with uncontrolled precharge from the dc line.

TABLE II
MAIN PARAMETERS

Items	values
DC Line Voltage	8.8 kV
Number of SMs Per Arm	4
SM Capacitor	0.015 F
SM Capacitor Rated Voltage	2.2 kV
Arm Inductance	3 mH
Self-Power Supply Rated Output Voltage	15 V
Self-Power Supply Load Minimum Working Voltage	12 V
Self-Power supply Load Equivalent Resistor	50 Ω
Self-Power Supply Output Support Capacitor	0.00225 F
Voltage Sorting Control Frequency f_p	25 Hz

described as

$$d_{mk} = \overline{d_{psk}} \cdot d_c \tag{26}$$

where d_c is the output signal of PWM controller, $\overline{d_{psk}}$ indicates the logic "not" operation of d_{psk}.

Based on (24)–(26), the input current i_{pk} of the self-power supplies can be regulated, and the capacitor static voltage u_{ck} can be controlled. When the uncontrolled precharge process of the MMC is over, the arm current and IGBTs can be used to control capacitor voltage balancing, so all of the control signals of self-power supplies are forced to zero, and all of the self-power supplies will be controlled working normally.

IV. Simulation Verification

To verify the proposed method, a self-power supply based on a 300–2700 V input range was used to build the self-power supply model. Its input characteristic is shown in Fig. 14 of Appendix A. An MMC system with uncontrolled precharge from the dc line is modeled with the simulation tool MATLAB/Simulink, as shown in Fig. 7. The main parameters of the self-power supply and MMC system are summarized in Table II.

A. Simulation Verification of Voltage Balancing With Equalizing Resistance

To validate the voltage balancing method based on equalizing resistance, the value of the equalizing resistor needs to be calculated. Using (7) and the self-power supply input characteristic in (29) of the Appendix, the equalizing resistance R_d can be calculated as

$$R_d < \frac{\bar{u}_c^2}{p_s} = \frac{1100^2}{19.91} = 60.8\ \text{k}\Omega.. \tag{27}$$

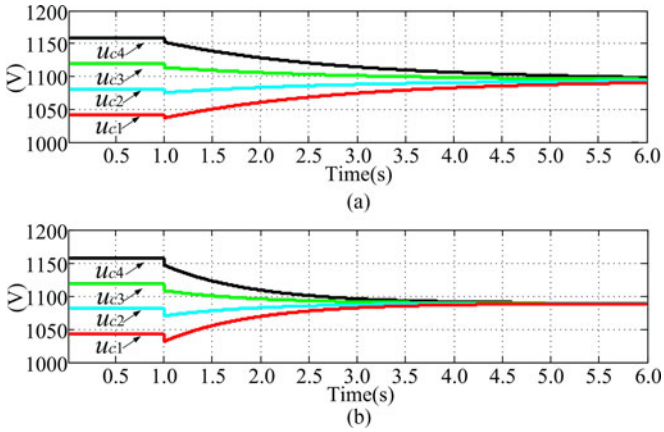

Fig. 8. Simulation waveforms of the voltage balancing method based on equalizing resistance. (a) Voltage balancing with $R_d = 40\ \text{k}\Omega$. (b) Voltage balancing with $R_d = 20\ \text{k}\Omega$.

$R_d = 40\ \text{k}\Omega$ and $R_d = 20\ \text{k}\Omega$ are selected to verify the basic method. The basic voltage balancing control with $R_d = 40\ \text{k}\Omega$ is shown in Fig. 8(a). When $R_d = 40\ \text{k}\Omega$ is used to connect the capacitor circuit at 1 s, the capacitor voltages begin to convergence, and the maximum voltage difference between the capacitors is about 10 V at 6 s. The voltage balancing control with $R_d = 20\ \text{k}\Omega$ is shown in Fig. 8(b), and the voltages almost completely coincide at 5 s. Comparing the capacitor voltages in Fig. 8(a) and (b), the smaller R_d will yield better voltage balancing effect, but it will also bring greater active power losses.

B. Simulation Verification of Proposed Voltage Balancing Method

Fig. 9 shows the performance of the proposed voltage balancing method. In Fig. 9(a), the proposed method begins to regulate the capacitor voltages at 1 s, and they have achieved voltage balancing at 5.25 s. Here, all equalizing resistances are cut out during the control process.

In Fig. 9(b), the proposed method with $R_d = 100\ \text{k}\Omega$ also begins to work at 1 s, and the voltages are balanced at about 4.9 s. Here $R_d = 100\ \text{k}\Omega$ is used to discharge the capacitor when the MMC system stops working, and it can be calculated using (35) in the Appendix. A comparison of the capacitor voltages in Fig. 9(a) and (b) shows that the $R_d = 100\ \text{k}\Omega$ can improve the response speed of the capacitor voltage balancing to a certain extent.

A comparison of the capacitor voltages in Figs. 9(b) and 8(a) shows that the R_d of proposed method is 2.5 times that of basic method. It shows that the losses of R_d in the proposed method are reduced by 60%.

The control signals $d_{ps1} \sim d_{ps4}$ and output voltages $u_{co1} \sim u_{co4}$ for the SM self-power supplies are shown in Fig. 9(c) to (f). When d_{ps1} with 25 Hz begins to control the self-power supply at 1 s, the $d_{ps2} \sim d_{ps4}$ are still kept to zero, and when u_{co1} begins to fluctuate at 1 s, $u_{co2} \sim u_{co4}$ are still kept stable, which indicates that the u_{c1} is the minimum capacitor voltage in Fig. 9(b) at 1 s.

In Fig. 9(d), the d_{ps2} begins to control the self-power supply at 1.2 s, and u_{co2} also begins to fluctuate at 1.2 s, which shows

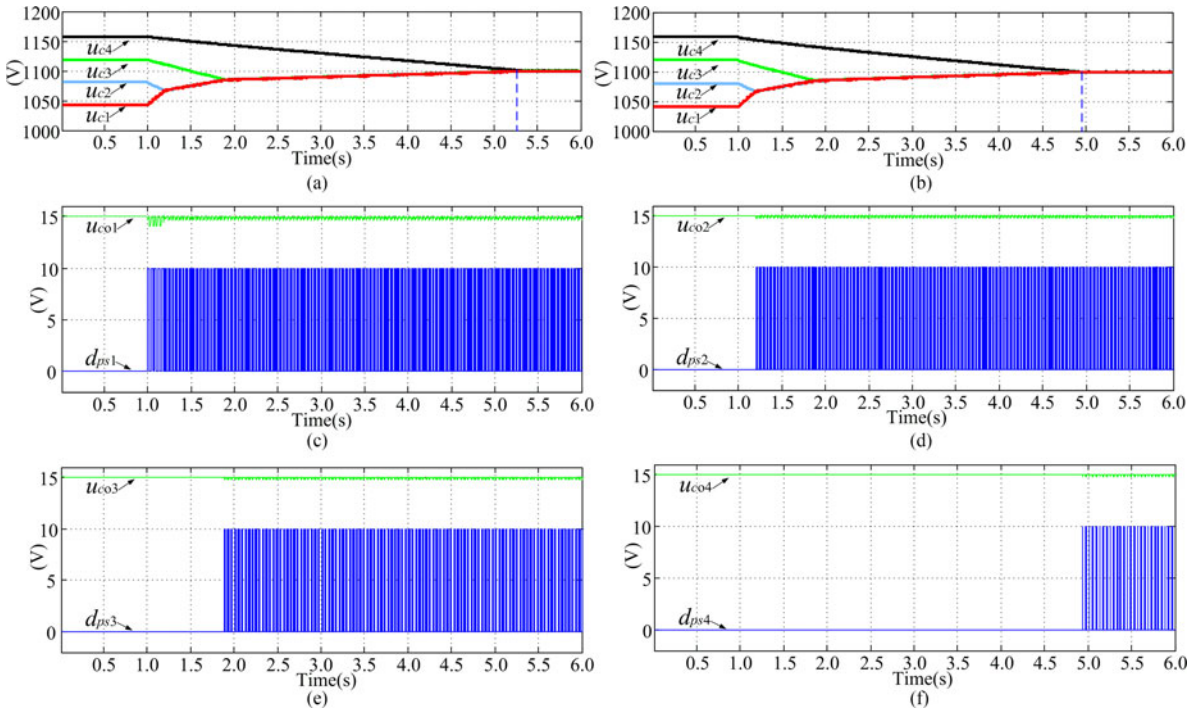

Fig. 9. Simulation waveforms of the proposed voltage balancing method. (a) Voltage balancing without equalizing resistance. (b) Voltage balancing with $R_d = 100$ kΩ. (c)–(f) Control signals $d_{ps1} \sim d_{ps4}$ and output voltages $u_{co1} \sim u_{co4}$ of SM self-power supplies.

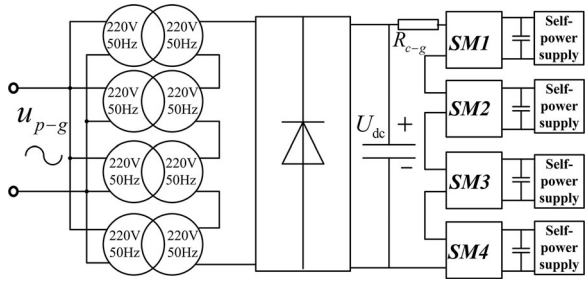

Fig. 10. Block diagram of the experimental circuit.

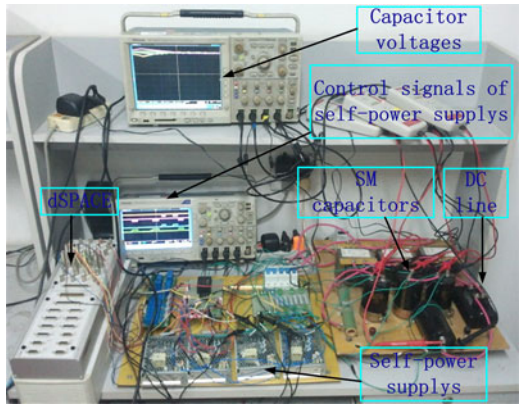

Fig. 11. Photograph of experiment circuit

that the capacitor voltages u_{c2} and u_{c1} start to overlap at 1.2 s. The minimum capacitor voltage will shift between u_{c2} and u_{c1} after 1.2 s.

In Fig. 9(e), the d_{ps3} begins to control the self-power supply at 1.85 s, and u_{co3} also begins to fluctuate at 1.85 s, which shows that the capacitor voltages u_{c3}, u_{c2} and u_{c1} start to overlap at 1.85 s. The minimum capacitor voltage will shift between u_{c3}, u_{c2}, and u_{c1} after 1.85 s. In Fig. 9(f), the self-power supply begins to be controlled by d_{ps4} at about 4.9 s, and u_{co4} also begins to fluctuate at this moment, which indicates that all the capacitor voltages begin to overlap at about 4.9 s. All the capacitor voltages have achieved voltage balancing after 4.9 s.

V. Experimental Verification

The MMC with one arm prototype was built in the laboratory. The circuit configuration and photograph are shown in Figs. 10 and 11, respectively. The arm has four SMs. The system control algorithm is implemented in dSPACE1103, and the self-power supplies control signals from the dSPACE1103 are transferred to the driving circuit of each self-power supply. The main parameters of MMC prototype and self-power supply are described as the Table III.

A. Experimental Verification of Voltage Balancing With Equalizing Resistance

Fig. 12 shows the experimental waveforms of the voltage balancing based on equalizing resistance. Using (7) and the self-power supply input characteristic in (30) of Appendix, the equalizing resistance R_d can be calculated as

$$R_d < \frac{\bar{u}_c^2}{p_s} = \frac{233^2}{5.796} = 9.37 \text{ k}\Omega. \tag{28}$$

TABLE III
MAIN PARAMETERS

Items	Values
DC Line	933 V
Number of SMs	4
SM Capacitor	0.0086 F
SM Capacitor Rated Voltage	466 V
Self-Power Supply Load Rated Voltage	15 V
Self-power Supply Load Minimum Working Voltage	12 V
Self-power supply Load Equivalent Resistor	51 Ω
Self-power Supply Output Support Capacitor	0.0056 F
Voltage Sorting Control Frequency f_p	10 Hz

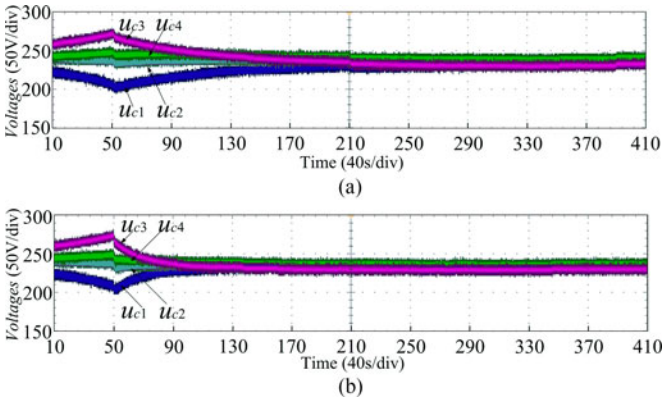

Fig. 12. Experimental waveforms of the voltage balancing method based on equalizing resistance. (a) Voltage balancing with $R_d = 8.2\ \text{k}\Omega$. (b) Voltage balancing with $R_d = 4.1\ \text{k}\Omega$.

$R_d = 8.2\ \text{k}\Omega$ and $R_d = 4.1\ \text{k}\Omega$ were selected to verify the basic method. In Fig. 12(a), the $R_d = 8.2\ \text{k}\Omega$ is used to connect the capacitor circuit at 50 s. The capacitor voltages have achieved voltage balancing at about 210 s, and the maximum voltage difference between the capacitors is about 10 V at 410 s. In Fig. 12(b), the $R_d = 4.1\ \text{k}\Omega$ is also used to connect the capacitor circuit at 50 s. The capacitor voltages have achieved voltage balancing at 130 s, and maximum voltage difference between the capacitors is less than 10 V at 410 s.

Comparing the capacitor voltages in Fig. 12(a) and (b), the voltage balancing for $R_d = 4.1\ \text{k}\Omega$ is better than that of the voltage balancing for $R_d = 8.2\ \text{k}\Omega$, but it leads to greater active power losses.

B. Experimental Verification of Proposed Voltage Balancing Method

The experimental waveforms of the proposed voltage balancing method are shown in Fig. 13. In Fig. 13(a), the capacitor voltages begin to be controlled by the proposed method at 50 s, and the voltages acquire the balancing at 250 s. In this control process, all the equalizing resistances are cut out. In Fig. 13(b), the proposed method with $R_d = 120\ \text{k}\Omega$ is used to control the capacitor voltages, and the voltages acquire a better balance at 226 s. Here, the R_d is used to discharge the capacitor when the MMC system stops working, and it can be calculated using (36) in the Appendix. Comparing the voltages in Fig. 13(a) and

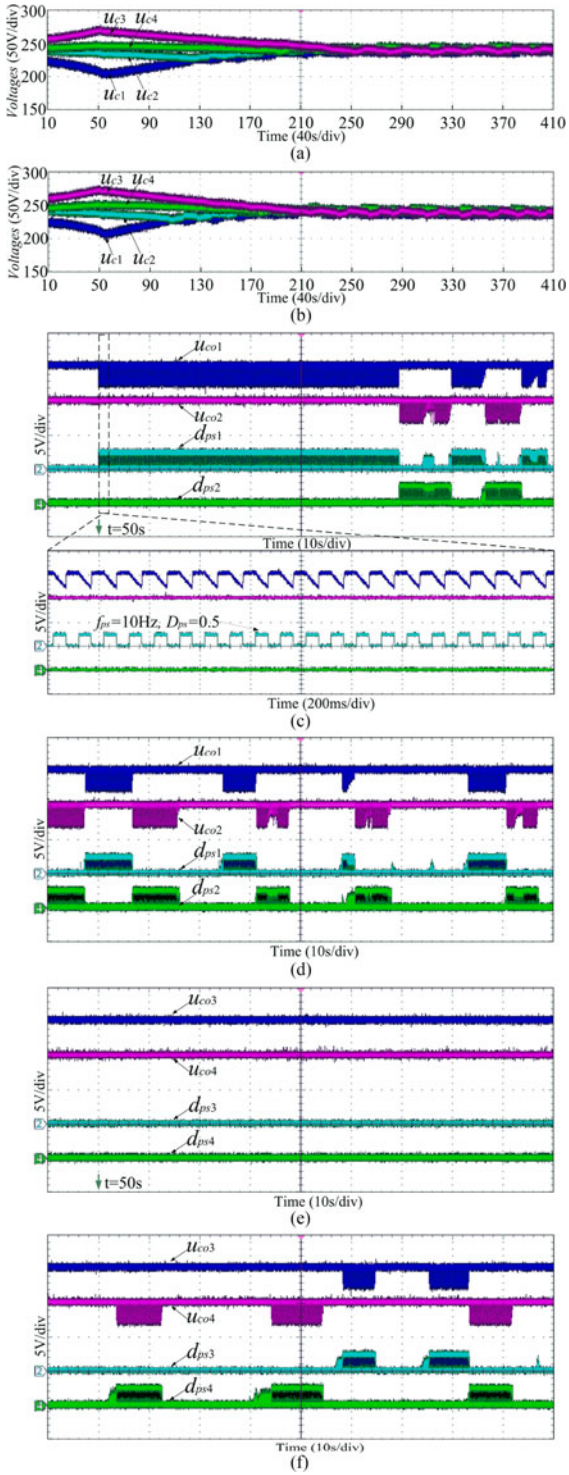

Fig. 13. Experimental waveforms of the proposed voltage balancing method. (a) Voltage balancing without equalizing resistance. (b) Voltage balancing with $R_d = 120\ \text{k}\Omega$. (c)–(f) Control signals $d_{ps1} \sim d_{ps4}$ and output voltages $u_{co1} \sim u_{co4}$ of SM self-power supplies.

(b), the R_d can be seen to improve the response speed of the capacitor voltage balancing to a certain extent. Comparing the capacitor voltages in Figs. 13(b) and 12(a), the R_d of proposed method is about 15 times better than of basic method, which

shows that the losses of R_d in the proposed method are reduced by 93.3%.

During the time periods of 40 to 140 s and 170 to 270 s, the control signals $d_{ps1} \sim d_{ps4}$ and output voltages $u_{co1} \sim u_{co4}$ of the SM self-power supplies are shown in Fig. 13(c)–(f). In Fig. 13(c) and (e), when the d_{ps1} of 10 Hz begins to control the self-power supply at 50 s, the $d_{ps2} \sim d_{ps4}$ are still kept to zero, and when the u_{co1} begins to fluctuate at 50 s, the $u_{co2} \sim u_{co4}$ are still kept stable, which indicates that the u_{c1} is the minimum capacitor voltage in Fig. 13(b) at 50 s. In Fig. 13(c) and (d), the d_{ps2} begins to control the self-power supply at 109.5 s, and the u_{co2} also begins to fluctuate. It shows that capacitor voltages u_{c2} and u_{c1} start to overlap at 109.5 s, and the minimum capacitor voltage will shift between u_{c2} and u_{c1} after 109.5 s. In Fig. 13(e), the d_{ps3} and d_{ps4} are kept to zero, and the u_{co3} and u_{co4} are kept stable, which shows that the capacitor voltages u_{c3} and u_{c4} are greater than the minimum capacitor voltage (u_{c2} or u_{c1}) from 40 to 140 s. In Fig. 13(f), the d_{ps4} begins to control the self-power supply at 183.5 s, and the u_{co4} also begins to fluctuate. It shows that capacitor voltages u_{c1}, u_{c2}, and u_{c4} start to overlap at 183.5 s, and the minimum capacitor voltage will shift between u_{c1}, u_{c2}, and u_{c4} after 183.5 s. The d_{ps3} in Fig. 13(f) begins to control the self-power supply at 226 s, which indicates that all the capacitor voltages begin to overlap at 226 s, and all the capacitor voltages have achieved voltage balancing after 226 s.

VI. Conclusion

In this paper, a novel method based on self-power supply control for balancing capacitor static voltage is proposed. The proposed method can control the capacitor static voltage balancing indirectly by regulating the input characteristic of the self-power supplies. Based on the SM capacitor voltage sorting results and self-power supply output support capacitor, the capacitor static voltage balancing control signals with fixed frequency and duty ratio can be generated. The input impedance and input current of self-power supply with lowest SM capacitor voltage can be regulated by using the control signal, and the capacitor voltage balancing can be controlled indirectly. Compared with previous works, the proposed method has less computation, and it does not rely on IGBTs and additional complex circuits except for the self-power supplies. This can save on the software and hardware costs. The method can also improve the equalizing resistances and reduce the active power losses of SMs. An MMC system was modeled and simulated with MATLAB/Simulink, and a small-scale MMC prototype was built and tested in the laboratory. The results show the effectiveness of the proposed voltage balancing control method.

Appendix

A. Research on Input Characteristic of Self-Power Supply

To build the input characteristic model of a self-power supply based on 300—2700 V input range, the self-power supply needs to be tested. The test data and fitting curve of the self-power supply input voltage and current are shown in Fig. 14.

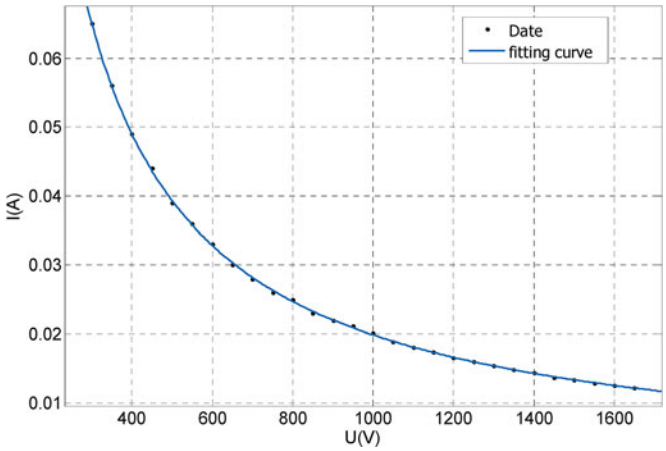

Fig. 14. Input voltage and current test data and fitting curve of the self-power supply based on 300–2700 V input range.

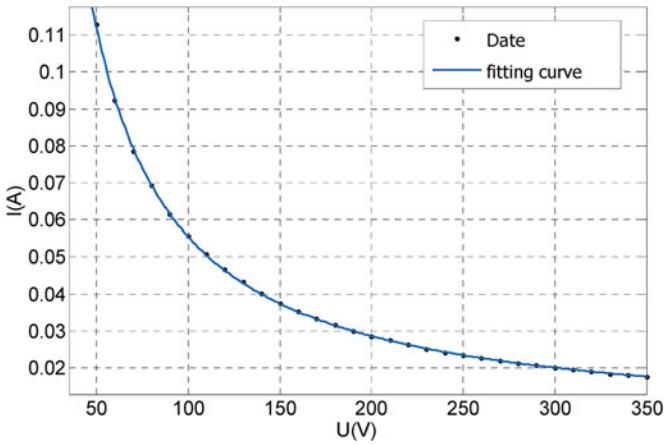

Fig. 15. Input voltage and current test data and fitting curve of the self-power supply based on 50–350 V input range.

The fitting curve in Fig. 14 can be determined by

$$i_{pk} = 2.87 \times 10^{-7} u_{ck} + \frac{19.57}{u_{ck}}. \tag{29}$$

To build the input characteristic model of the self-power supply based on 50—350 V input range, the self-power supply also needs to be tested. The test data and fitting curve are shown in Fig. 15.

The fitting curve in Fig. 15 can be determined by

$$i_{pk} = 4.649 \times 10^{-6} u_{ck} + \frac{5.543}{u_{ck}}. \tag{30}$$

B. Calculation the Discharge Resistance of the SM

After the MMC stops working, the R_d in the SM is used to discharge the capacitor, and the current relationships in (2) can be expressed as

$$c\frac{du_{ck}}{dt} + \frac{u_{ck}}{R_d} + i_{pk} = 0. \tag{31}$$

According to (29) and (30), the input characteristics of self-power supply can be described as

$$i_{pk} = k_1 u_{ck} + \frac{k_2}{u_{ck}} \tag{32}$$

where k_1 and k_2 are the ratio coefficients.

Substituting (32) into (31), (31) can be rewritten as

$$c\frac{du_{ck}}{dt} + \frac{u_{ck}}{R_d} + k_1 u_{ck} + \frac{k_2}{u_{ck}} = 0. \tag{33}$$

To simplify and solve the (33), the capacitor discharge model can be expressed as

$$u_{ck}(t) = \sqrt{(U_{ck}^2 + k_2 R_d)e^{-\frac{2+2k_1 R_d}{cR_d}t} - k_2 R_d} \tag{34}$$

where U_{ck} is capacitor rate voltage, and t is the capacitor discharge time, which is usually less than or equal to 10 min.

According to Table II, substituting $U_{ck} = 2200$ V, $c = 0.015$ F, $t = 600$ s, $k_1 = 2.87 \times 10^{-7}$, $k_2 = 19.57$, and $u_{ck}(t) = 300$ V into (34), the R_d for discharge of capacitor can be calculated as

$$R_d = 107\ \text{k}\Omega. \tag{35}$$

$R_d = 100\ \text{k}\Omega$ was selected to discharge the capacitor in the simulation verification.

According to Table III, substituting $U_{ck} = 466$ V, $c = 0.0086$ F, $t = 90$ s, $k_1 = 4.649 \times 10^{-6}$, $k_2 = 5.543$, and $u_{ck}(t) = 50$ V into (34), the R_d for discharge of capacitor can be calculated as

$$R_d = 133.2\ \text{k}\Omega. \tag{36}$$

$R_d = 120\ \text{k}\Omega$ was selected to discharge the capacitor in the experimental verification.

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