A New Class of Single-Phase High-Frequency Isolated Z-Source AC–AC Converters With Reduced Passive Components

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***Abstract*—In this paper, a class of single-phase Z-source (ZS) ac–ac converters is proposed with high-frequency transformer (HFT) isolation. The proposed HFT isolated (HFTI) ZS ac–ac converters possess all the features of their nonisolated counterparts, such as providing wide range of buck-boost output voltage with reversing or maintaining the phase angle, suppressing the in-rush and harmonic currents, and improved reliability. In addition, the proposed converters incorporate HFT for electrical isolation and safety, and therefore can save an external bulky line frequency transformer, for applications such as dynamic voltage restorers, etc. The proposed HFTI ZS converters are obtained from conventional (nonisolated) ZS ac–ac converters by adding only one extra bidirectional switch, and replacing two inductors with an HFT, thus saving one magnetic core. The switching signals for buck and boost modes are presented with safe-commutation strategy to remove the switch voltage spikes. A quasi-ZS-based HFTI ac–ac is used to discuss the operation principle and circuit analysis of the proposed class of HFTI ZS ac–ac converters. Various ZS-based HFTI proposed ac–ac converters are also presented thereafter. Moreover, a laboratory prototype of the proposed converter is constructed and experiments are conducted to produce output voltage of 110 Vrms / 60 Hz, which verify the operation of the proposed converters.**

***Index Terms*—Buck-boost operation, high-frequency transformer (HFT), inverting and noninverting operations, isolation, Z-source (ZS) ac–ac converters.**

I. Introduction

FOR ac–ac applications which require only voltage regulation, the direct PWM ac–ac converters are advanced because of their advantages, such as single-stage conversion, low harmonic current, better power factor and efficiency, smaller size, and low cost [1]. These direct ac–ac converters are derived from the dc–dc converters by replacing the unidirectional switches with bidirectional switching devices [2]. The direct PWM ac–ac converters have widely explored in various researches, covering their control [3], applications [4], [5], and circuit development [6]–[13]. The buck and boost type ac–ac converters are proposed in [6]–[8], respectively. To overcome the limited voltage gain (either step-up or step-down) of these buck and boost type ac–ac converters, single-phase buck-boost ac–ac converters are proposed in [9]. The single-phase Cuk ac–ac converter proposed in [10] and [11] can also provide both step-up and step-down operation of voltage, the same as buck-boost ac–ac converter, with the additional advantage of having both continuous input and output currents. The single-phase multilevel and multicell ac–ac converters are also proposed in [12] and [13], which can reduce switch voltage stresses and improve the output voltage quality. These direct ac–ac converters have been used as dynamic voltage restorer (DVR) [14], [15], to compensate voltage sags and swells, and to compensate static volt-ampere reactive (VAR) in power systems [16].

The Z-Source (ZS) network based concept is proposed by Peng [17], where a ZS inverter is proposed with buck-boost voltage capability, and enhanced reliability. The ZS concept is also extended to ac–ac converters [18]–[23] with various studies performed on single-phase ac–ac converters [18]–[22] and three-phase ac–ac converters [23]. A single-phase ZS ac–ac converter is proposed in [18], with benefits such as buck-boost voltage capability with reversing or maintaining phase-angle, smaller in-rush and harmonic current, and enhanced reliability. A single-phase quasi-Z-source (qZS) ac–ac converter, which retains all the benefits of the ZS ac–ac converter [18], is proposed in [19]. It provides continuous input current, common grounds between input and output, and low voltage stress across capacitor. In [20], a single-phase modified qZS ac–ac converter is proposed, which has reduced number of passive components compared to the ZS and qZS ac–ac converters. The soft-commutation strategies for these ZS ac–ac converters are presented in [20] and [21], to eliminate switch voltage spikes. A coupled-inductor based single-phase gamma ZS ac–ac converter is proposed in [22], which can adjust the voltage gain by varying the turns ratio of coupled-inductor along with the duty ratio of the converter.

When these single-phase ZS ac–ac converters are used as DVRs to compensate utility voltage sags and swells [15], [24], an external bulky line frequency transformer is added to provide electrical isolation between input side (utility grid) and output (sensitive electronics load). This line frequency transformer is very bulky and heavy with high cost and losses, and also has start-up inrush current and saturation problem [25]–[27]. In addition, the impedance of this low frequency transformer results

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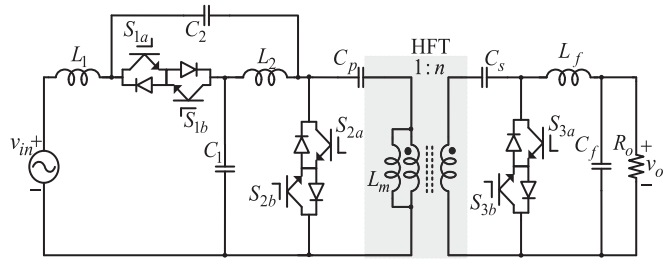

Fig. 1. Circuit topology of the single-phase HFTI qZS ac–ac converter proposed in [28].

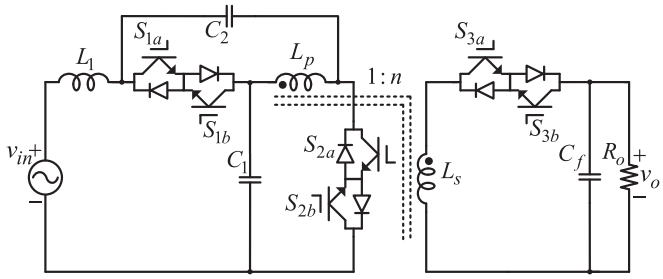

Fig. 2. Proposed single-phase HFTI qZS ac–ac converter.

in voltage drop, and the voltage harmonics become significant with nonlinear loads [27]. To overcome the drawback, new family of HFT isolated (HFTI) ZS ac–ac converters is proposed in [28], which eliminate the external line frequency transformer when used as DVR. However, apart from an additional bidirectional switch, these HFTI ZS ac–ac converters also use extra passive components such as two capacitors C_p, C_s, and an HFT, which increase their cost, volume, and losses.

To overcome aforementioned drawbacks of the conventional non-isolated ZS ac–ac converters [18]–[22] and HFTI ZS ac–ac converters [28], a new class of single-phase ZS ac–ac converters is proposed with HFT isolation and reduced passive components. In addition to retaining all the features of the conventional ZS ac–ac converters, the proposed converters incorporate HFT for electrical isolation and safety. Therefore, they can save a large and costly external line frequency transformer, for applications such as DVRs, etc. The proposed HFTI ZS ac–ac converters use only one additional bidirectional switch compared to their conventional nonisolated counterparts, and have the same or less passive components requirement, as they add one HFT by eliminating two inductors (saving one magnetic core) from their nonisolated counterparts. The proposed converters save two capacitors and two inductors compared to the isolated ZS converters in [28], thus, reduce the cost, volume and losses. The switching strategies for buck and boost modes are presented with safe-commutation to remove the switch voltage spikes. A laboratory prototype of the proposed converter is also constructed and experiments are conducted to produce output voltage of 110 Vrms / 60 Hz, which verify the operation of the proposed converters.

II. Proposed Single-Phase HFTI Quasi-ZS AC–AC Converter

Fig. 1 shows the HFTI single-phase qZS ac–ac converter introduced in [28]. It is obtained from its nonisolated counterpart by adding two capacitors C_p, C_s, an HFT, and a bidirectional switch S_3. Although the converter does not require external bulky line frequency transformer when used for DVR applications, it does require extra passive components (two capacitors C_p, C_s, and an HFT), which increase its size, cost, and losses. Fig. 2 shows the proposed single-phase HFTI qZS ac–ac converter obtained by adding one bidirectional switch S_3 to the conventional nonisolated qZS ac–ac converter [19], and replacing two inductors L_2 and L_f with an HFT; thus, saving one magnetic core. Therefore, the passive component requirement of the proposed converter is almost the same or less than that of its conventional nonisolated counterpart. When compared to the converter in Fig. 1, the proposed converter can save two capacitors (C_p,C_s) and two inductors (L_2,L_f), which result in smaller size, cost, and losses.

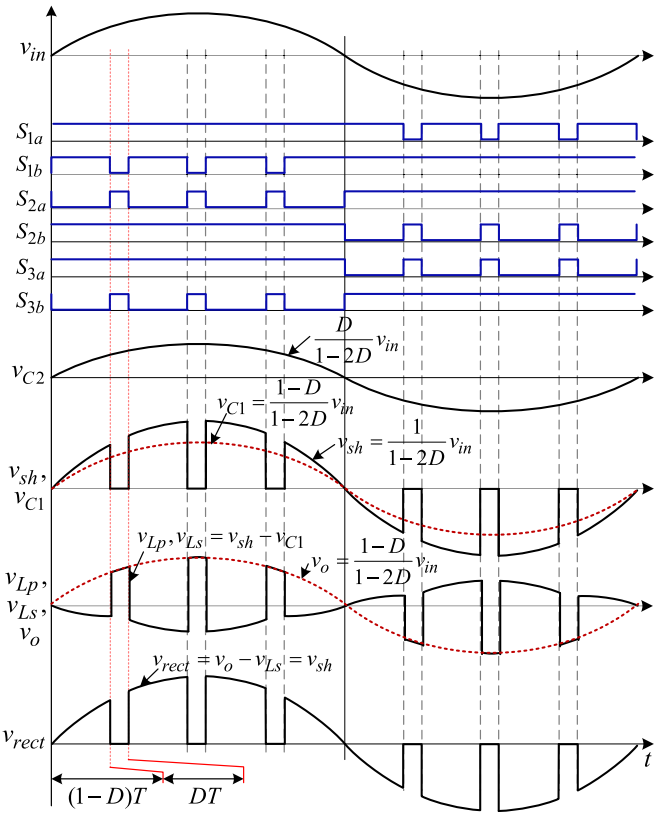

Fig. 3. Gating signals with soft-commutation strategy and key waveforms for boost mode when $n = 1$.

Similar to the nonisolated qZS converter in [19] and the HFTI qZS ac–ac converters in [28], the proposed converter also has the commutation problem. In this paper, soft-commutation strategy is presented for the proposed converter to avoid switches voltage spikes without using snubber circuits.

A. Boost Mode Operation

The gating signals with soft-commutation strategy and key waveforms during boost mode of the proposed converter are depicted in Fig. 3 for $n = 1$. During the positive half-cycle of

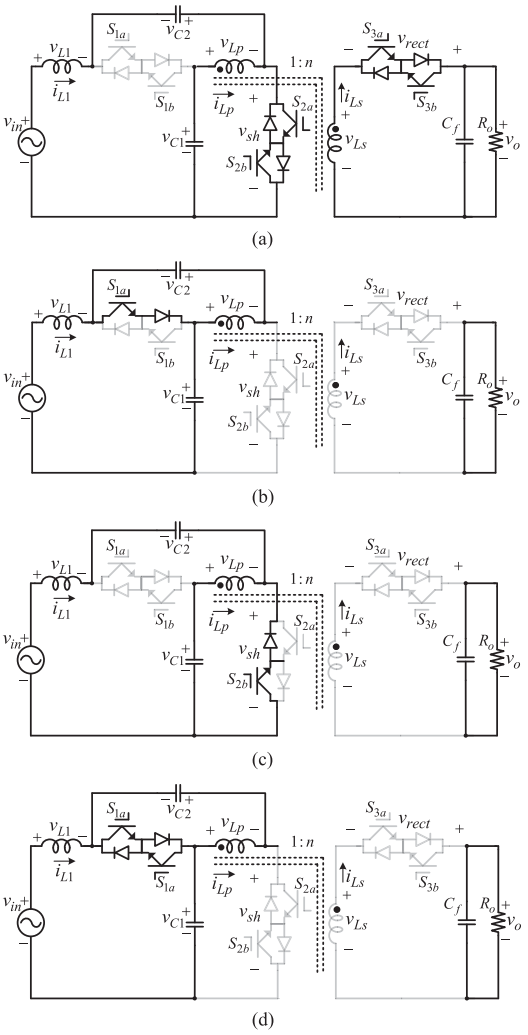

Fig. 4. Equivalent circuits of the proposed converter for boost mode. (a) DT interval. (b) Commutation state I. (c) Commutation state II. (d) (1-D)T interval.

input voltage ($v_{\rm in} > 0$), switches S_{2a}, S_{3b} are switched simultaneously at high frequency, complementary to switch S_{1b}, with small dead-time between them. Whereas, switches S_{1a},S_{2b}, and S_{3a} are completely turned-ON for safe-commutation purpose. The equivalent circuits of the proposed converter during the boost mode are shown in Fig. 4.

The equivalent circuit for DT interval is shown in Fig. 4(a), in which switches S_{2a}, S_{3b}, are turned-ON, whereas switch S_{1b} is turned-OFF. In this interval, capacitors C_1 and C_2 discharge while inductor L_1 stores energy. The output capacitor C_f charges through secondary winding L_s of HFT. Applying Kirchhoff's voltage law (KVL), we get

$$\begin{cases} -v_{\rm in} + v_{L_1} - v_{C_2} = 0 \\ -v_{C_1} + v_{Lp} = 0 \\ -v_{Ls} + v_o = 0 \\ v_{sh}, v_{\rm rect} = 0 \\ v_{Ls} = nv_{Lp} = v_o = nv_{C_1}. \end{cases} \tag{1}$$

At the end of DT interval, dead-time occurs in which switches S_{2a} and S_{3b} are turned-OFF, whereas switch S_{1b} is not turned-ON yet. There are two possible commutation states in this dead-time as shown in Fig. 4(b) and (c). The commutation state I, as shown in Fig. 4(b), occurs if the currents i_{L_1} and i_{Lp} are positive, in which the switch S_{1a} and body diode of switch S_{1b} conduct. The commutation state II, as shown in Fig. 4(c), can occur if the currents i_{L_1} and i_{Lp} are negative, in which the switch S_{2b} and body diode of switch S_{2a} conduct.

After the end of dead-time, (1-D)T interval begins as shown in Fig. 4(d), in which switches S_{2a}, S_{3b} are turned-OFF, whereas switch S_{1b} is turned-ON. In this interval, inductor L_1 releases energy while capacitors C_1 and C_2 are charged. The output capacitor C_f releases its energy to load in this interval.

By applying KVL, we get

$$\begin{cases} -v_{\rm in} + v_{L_1} + v_{C_1} = 0 \\ -v_{C_2} - v_{Lp} = 0 \\ -v_{C_1} - v_{C_2} + v_{sh} = 0 \\ -v_{Ls} - v_{\rm rect} + v_o = 0 \\ v_{Ls} = nv_{Lp} = v_o - v_{\rm rect} = -nv_{C_2}. \end{cases} \tag{2}$$

By applying flux (volt-sec) balance condition on inductors L_1, L_p, the voltages across capacitors C_1 and C_2 can be obtained as follows:

$$v_{C_1} = \frac{1-D}{1-2D} v_{\rm in} \tag{3}$$

$$v_{C_2} = \frac{D}{1-2D} v_{\rm in}. \tag{4}$$

Substituting (3) and (4) into (2), we get

$$v_{sh} = \frac{1}{1-2D} v_{\rm in}. \tag{5}$$

By solving (1)–(4), the $v_{\rm rect}$ and v_o can be obtained as follows:

$$v_{\rm rect} = \frac{1}{1-2D} n v_{\rm in} \tag{6}$$

$$v_o = \frac{(1-D)}{1-2D} n v_{\rm in}. \tag{7}$$

From (7), the voltage gain G (v_o/$v_{\rm in}$) of the proposed converter is $n(1-D)/(1-2D)$, and boost mode occurs when $0 < {\rm D} < 0.5$.

B. Buck Mode Operation

The gating signals with soft-commutation strategy and key waveforms during buck mode are shown in Fig. 5. During the positive half-cycle of input voltage $v_{\rm in} > 0$, switches S_{1b}, S_{3a} are turned-ON or turned-OFF simultaneously, complementary to switch S_{2a}, with small dead-time between them. Whereas, switches S_{1a}, S_{2b}, and S_{3b} are completely turned-ON for safe-commutation purpose. The equivalent circuits of the proposed converter during buck mode are shown in Fig. 6.

The equivalent circuit for DT interval is shown in Fig. 6(a), in which switches S_{1b}, and S_{3a} are turned-ON while switch S_{2a} is turned-OFF. In this interval, capacitors C_1 and C_2 charge while inductor L_1 releases energy. The output capacitor C_f charges through winding L_s.

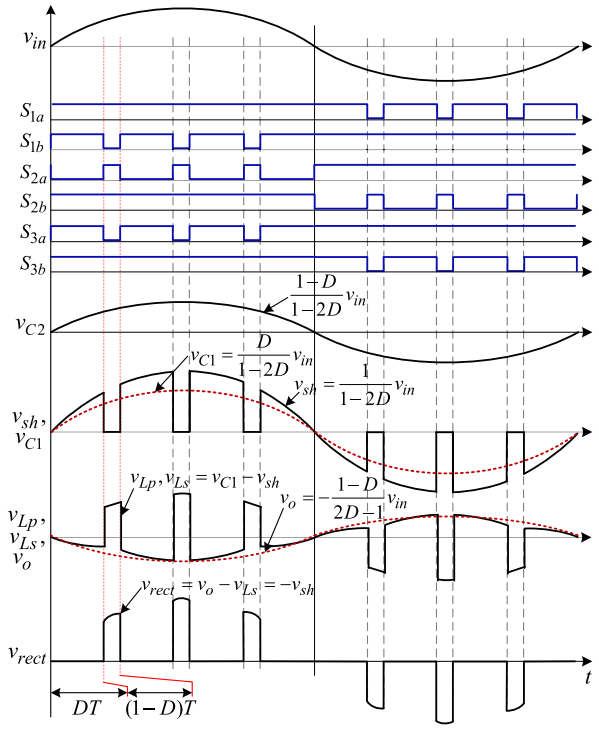

Fig. 5. Gating signals with soft-commutation strategy and key waveforms for buck mode when $n = 1$.

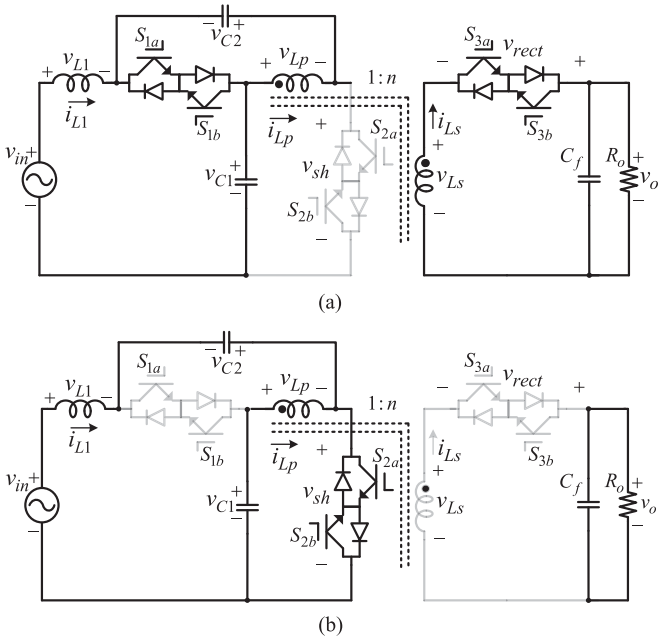

Fig. 6. Equivalent circuits of the proposed converter for buck mode. (a) DT interval. (b) (1-D)T interval.

Applying KVL, we get

$$\begin{cases} -v_{\text{in}} + v_{L_1} + v_{C_1} = 0 \\ -v_{C_2} - v_{Lp} = 0 \\ -v_{C_1} - v_{C_2} + v_{sh} = 0 \\ -v_{Ls} + v_o = 0 \\ v_{Ls} = nv_{Lp} = v_o = -nv_{C_2}. \end{cases} \tag{8}$$

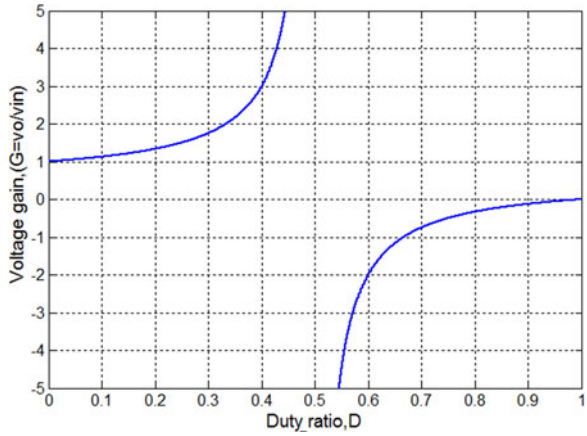

Fig. 7. Voltage gain (G) versus duty ratio (D) for $n = 1$.

After the end of the DT interval, during dead-time, two possible commutation states I or II occurs, as shown in Fig. 4 (b) and (c), respectively, depending on the direction of inductors i_{L_1} and i_{Lp} currents.

After the end of dead-time, (1-D)T interval begins, as shown in Fig. 6(b), in which switches S_{1b}, and S_{3a} are turned-OFF, whereas switch S_{2a} is turned-ON. In this interval, inductor L_1 stores energy while capacitors C_1, and C_2 are discharged. The output capacitor C_f releases its energy to load in this interval.

By applying KVL, we get

$$\begin{cases} -v_{\text{in}} + v_{L_1} - v_{C_2} = 0 \\ -v_{C_1} + v_{Lp} = 0 \\ -v_{Ls} - v_{\text{rect}} + v_o = 0 \\ v_{Ls} = nv_{Lp} = v_o - v_{\text{rect}} = nv_{C_1}. \end{cases} \tag{9}$$

By applying volt-sec balance condition on inductors L_1 and L_p, the voltages across capacitors C_1 and C_2 can be obtained as follows:

$$v_{C_1} = \frac{D}{1-2D} v_{\text{in}} \tag{10}$$

$$v_{C_2} = \frac{1-D}{1-2D} v_{\text{in}}. \tag{11}$$

Substituting (10) and (11) into (8), we get

$$v_{sh} = \frac{1}{1-2D} v_{\text{in}}. \tag{12}$$

By solving (8)–(11), the v_{rect} and v_o can be obtained as follows:

$$v_{\text{rect}} = -\frac{1}{2D-1} n v_{\text{in}} \tag{13}$$

$$v_o = -\frac{(1-D)}{2D-1} n v_{\text{in}}. \tag{14}$$

From (14), the voltage gain G (v_o/v_{in}) of the proposed converter is obtained as $-n(1-D)/(2D-1)$, and buck mode occurs when 0.66 < D < 1. The negative signs in (13) and (14) show that the polarity of output voltage is reversed in the buck mode. The voltage gain (G) versus duty ratio (D) of the proposed converter is plotted in Fig. 7 for $n = 1$.

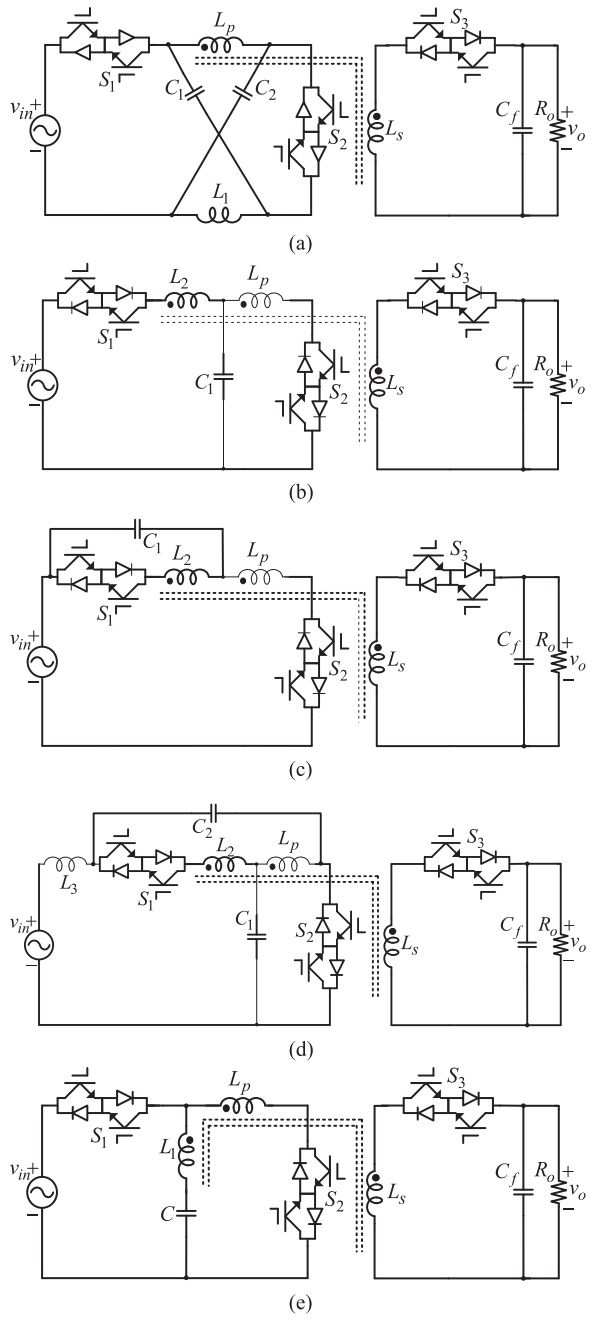

Fig. 8. Various topologies of the proposed HFTI ZS ac–ac converters. (a) HFTI ZS ac–ac converter. (b) HFTI trans-ZS ac–ac converter. (c) HFTI trans-qZS ac–ac converter. (d) HFTI improved trans-ZS ac–ac converter. (e) HFTI gamma-ZS ac–ac converter.

Fig. 8 shows the other types of the proposed single-phase HFTI ZS ac–ac converters, which are obtained from the conventional nonisolated ZS ac–ac converters by replacing two inductors with an HFT, and adding only one bidirectional switch. The component stresses in terms of voltage gain *G* for the proposed class of HFTI ZS ac–ac converters are summarized in Table I. These converters have the same electrical isolation and safety, components stresses, and voltage gain characteristics as the HFTI ZS ac–ac converters in [28]; with the benefits of saving two capacitors C_p and C_s, and two inductors L_2 and L_f. Therefore, the proposed HFTI ZS ac–ac converters have less cost and volume, high power density, and lower losses, compared to their HFTI counterparts in [28].

III. Component Design/Selection of the Proposed HFTI qZS AC–AC Converter

A. Magnetic Components Design

In this section, the design guidelines for the HFT and inductor L_1 of the proposed HFTI qZS ac–ac converter are given based on their current handling capability i_L, allowable current ripple Δi_L, and flux density swing ΔB.

1) For the HFT, the current handling requirement depends on its magnetizing current i_m, which is the difference of primary winding current i_{Lp} and secondary winding current i_{Ls}. From the equivalent circuit of proposed converter in Fig. 4(d), $i_{Ls} = 0$. Therefore, $i_m = i_{Lp}$, and given as

$$i_m = i_{Lp} = \frac{D}{1-D} i_{\text{in}}. \tag{15}$$

The formulas to determine the inductor current ripple Δi_L and flux density swing ΔB are given by

$$\Delta i_L = \frac{v_L}{L} \Delta t \tag{16}$$

$$\Delta B = \frac{v_L}{N A_e} \Delta t \tag{17}$$

where v_L is the voltage applied across inductor during Δt interval, *L* is the inductance value of the inductor, *N* is the number of turns, and A_e is the cross-sectional area of the magnetic core. For the HFT in the proposed converter during DT interval, the voltage v_{Lp} applied across primary winding is v_{C1}[see Fig. 4(a)]. Putting these values in (16) and (17), the magnetizing inductor current ripple Δi_m and flux density swing ΔB of the HFT are given as follows:

$$\Delta i_m = \frac{v_{\text{in}}(1-D)}{L_m(1-2D)} DT \tag{18}$$

$$\Delta B = \frac{v_{\text{in}}(1-D)}{N A_e(1-2D)} DT. \tag{19}$$

From (18), the value of magnetizing inductance L_m can be found corresponding to allowable current ripple Δi_m. Moreover, from (19), the number of turns *N* can be determined corresponding to allowable value of ΔB, for a magnetic core with cross-sectional area of A_e.

2) Since the inductor L_1 is directly connected in series with voltage source v_{in}, the input current i_{in} is continuous, and the current handling requirement of L_1 is the same as i_{in}. During DT interval, the voltage v_{Lp} applied across primary winding is $v_{\text{in}} + v_{C_2}$ [see Fig. 4(a)]. Substituting these values in (16) and (17), the inductor current ripple Δi_{L_1} and flux density swing ΔB of L_1 are given as

$$\Delta i_{L_1} = \frac{v_{\text{in}}(1-D)}{L(1-2D)} DT \tag{20}$$

$$\Delta B = \frac{v_{\text{in}}(1-D)}{N A_e(1-2D)} DT. \tag{21}$$

TABLE I
KEY PARAMETERS OF THE PROPOSED HFTI Z-SOURCE AC–AC CONVERTERS

Parameters	Isolated ZSC Fig. 8(a)	Isolated qZSC Fig. 2	Isolated trans-ZSC Fig. 8(b)	Isolated Trans-qZSC Fig. 8(c)	Isolated Improved Trans-ZSC Fig. 8(d)	Isolated $\Gamma-$ ZSC Fig. 8(e)
D	$\frac{G-n}{2G-n}$	$\frac{G-n}{2G-n}$	$\frac{G-n}{(1+k)G-n}$	$\frac{G-n}{(1+k)G-n}$	$\frac{G-n}{(2+k)G-n}$	$\frac{(k+1)(G-n)}{G(k+2)-n(k+1)}$
v_{C_1}	$\frac{G}{n}v_{\rm in}$	$\frac{G}{n}v_{\rm in}$	$\frac{G}{n}v_{\rm in}$	–	$\frac{G}{n}v_{\rm in}$	$\frac{G}{n}v_{\rm in}$
v_{C_2}	$\frac{G}{n}v_{\rm in}$	$\frac{G-n}{n}v_{\rm in}$	–	$\frac{G-n}{nk}V_{\rm in}$	$\frac{G-n}{(k+1)n}v_{\rm in}$	–
v_{sh}	$\frac{2G-n}{n}v_{\rm in}$	$\frac{2G-n}{n}v_{\rm in}$	$\frac{(k+1)G-n}{nk}v_{\rm in}$	$\frac{(k+1)G-n}{nk}v_{\rm in}$	$\frac{(k+2)G-n}{n(k+1)}v_{\rm in}$	$\frac{G(k+2)-n(k+1)}{n(k+1)}v_{\rm in}$
$v_{\rm rect}$	$(2G-n)v_{\rm in}$	$(2G-n)v_{\rm in}$	$\frac{(k+1)G-n}{k}v_{\rm in}$	$\frac{(k+1)G-n}{k}v_{\rm in}$	$\frac{(k+2)G-n}{(k+1)}v_{\rm in}$	$\frac{G(k+2)-n(k+1)}{(k+1)}v_{\rm in}$
v_o	$\frac{1-D}{1-2D}nV_{\rm in}$	$\frac{1-D}{1-2D}nv_{\rm in}$	$\frac{1-D}{1-(k+1)D}nv_{\rm in}$	$\frac{1-D}{1-(k+1)D}nv_{\rm in}$	$\frac{1-D}{1-(k+2)D}nv_{\rm in}$	$\frac{1-D}{1-D(1+1/(K+1))}nv_{\rm in}$

From (20), the value of inductance L_1 can be found corresponding to allowable current ripple Δi_{L_1}. Moreover, from (21), the number of turns *N* can determined corresponding to allowable value of ΔB, for a magnetic core with area of cross section of A_e.

B. Capacitors Selection

The voltage stresses of capacitors C_1 and C_2 in the proposed HFTI qZS ac–ac converter can be found from (3) and (4), respectively. The formula to determine the capacitor voltage ripple is given by

$$\Delta v_C = \frac{i_C}{C}\Delta t \tag{22}$$

where i_C is the current flowing through capacitor during Δt interval, and *C* is its capacitance value. During DT interval, the currents flowing through capacitors C_1 and C_2 are $i_{\rm in}(1-D)/D$ and $i_{\rm in}$, respectively. Putting these values in (22), the voltage ripples of C_1 and C_2 are given as follows:

$$\Delta v_{C_1} = \frac{i_{\rm in}}{C}(1-D)T \tag{23}$$

$$\Delta v_{C_2} = \frac{i_{\rm in}}{C}DT. \tag{24}$$

From (23) and (24), the capacitance value *C* of the capacitors C_1 and C_2 can be found corresponding to their allowable voltage ripples.

C. Switches Selection

The proposed HFTI qZS ac–ac converter uses six active switches $S_{1(a,b)} - S_{3(a,b)}$. The selection of these switches depends on their maximum voltage and current stresses, and rms currents.

The voltage stresses of these switches are given as

$$v_{S_{1(a,b)}-S_{2(a,b)}} = \frac{v_{\rm in}}{n(1-2D)} \tag{25}$$

$$v_{S_{3(a,b)}} = \frac{v_{\rm in}}{(1-2D)}. \tag{26}$$

The peak current stresses of switches are given as

$$i_{S_{1(a,b)}} = \frac{ni_{\rm in}}{(1-D)} \tag{27}$$

$$i_{S_{2(a,b)}} = \frac{i_{\rm in}nD}{1-D} \tag{28}$$

$$i_{S_{3(a,b)}} = \frac{i_o}{D}. \tag{29}$$

The rms values of current flowing through switches are given as

$$I_{S_{1(a,b)}} = \frac{ni_{\rm in}}{\sqrt{1-D}} \tag{30}$$

$$I_{S_{2(a,b)}} = \frac{i_{\rm in}nD\sqrt{D}}{1-D} \tag{31}$$

$$I_{S_{3(a,b)}} = \frac{i_o}{\sqrt{D}}. \tag{32}$$

From (25)–(32), the voltage and current stresses of the switches in the proposed converter can be determined, and the switches with proper voltage and current ratings can be selected accordingly. The proposed converter has very similar i_{Lp} and i_{Ls} current characteristics as the input current of the switched capacitor converters in [29]–[31]. In such type of converters, a small inductor (leakage inductance of the HFT in the proposed converter) is in series with switched capacitor (C_f in the proposed converter), and create *LC* resonance which yields zero-current switching operation of switches (switch $S_{3(a,b)}$ in the proposed converter). The resonant current peak (i_{Lp} and i_{Ls} in the proposed converter) depends on the value of inductor (leakage inductance of HFT in the proposed converter). The minimum peak current occurs when the leakage inductance value of the HFT is selected such that the positive half-cycle of *LC* resonance is comparable to the DT interval. As these i_{Lp} and i_{Ls} currents pass through switches $S_{2(a,b)}$ and $S_{3(a,b)}$, respectively, the peak current stresses of switches in (28) and (29) holds true only when optimized leakage inductance is used, such as the half *LC* resonance time period is close to DT interval.

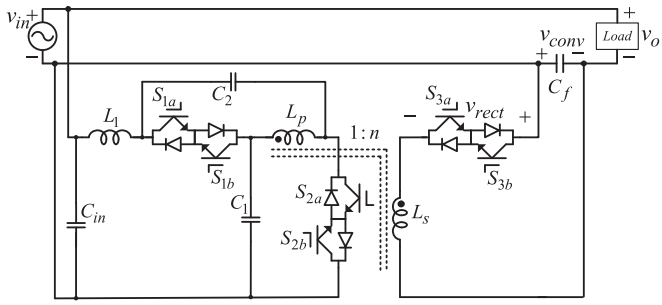

Fig. 9. New DVR topology based on proposed single-phase HFTI qZS ac–ac converter.

IV. Application of the Proposed HFTI qZS AC–AC Converter as DVR

The new DVR topology based on the proposed single-phase HFTI qZS ac–ac converter is shown in Fig. 9. The input of the proposed converter is connected in shunt with the line voltage $v_{\rm in}$, whereas its output $v_{\rm conv}$ is connected in series with line voltage and load. In this way, the proposed converter injects in-phase (boost) or out-of-phase (buck) voltage $v_{\rm conv}$ in series with line voltage $v_{\rm in}$ to regulate the load voltage v_o to a desire value. The proposed converter-based DVR has three operating modes, which are similar to that of the conventional non-isolated ZS ac–ac converters based DVRs in [15] and [24].

A. Bypass Mode

This mode occurs when utility voltage is at normal value (of 110 Vrms). In this mode, the duty ratio of converter is 1. The bidirectional switch $S_{1(a,b)}$ is fully turned-OFF, whereas switches $S_{2(a,b)}$ and $S_{3(a,b)}$ are fully turned-ON. The converter output voltage $v_{\rm conv}$ is zero in this mode, and load voltage v_o is the same as line voltage $v_{\rm in}$.

B. Boost Mode

This mode occurs during voltage sag condition when line voltage $v_{\rm in}$ becomes lower than its normal value. The proposed converter operates in boost in-phase mode (as explained in Section II). By applying KVL on DVR circuit in Fig. 9, and substituting the value of $v_{\rm conv}$ during boost mode operation from (7), we get

$$v_o = v_{\rm in} + v_{\rm in}\frac{1-D}{1-2D},\ 0 < D < 0.5. \tag{33}$$

From (33), $v_o > v_{\rm in}$ in this mode, and therefore voltage sag can be compensated.

C. Buck Mode

This mode occurs during voltage swell condition when utility voltage $v_{\rm in}$ is higher than its normal value. The proposed converter operates in buck out-of-phase mode (as explained in Section II). By applying KVL on DVR circuit in Fig. 9, and substituting the value of $v_{\rm conv}$ during the buck mode operation from (14), we get

$$v_o = v_{\rm in} - v_{\rm in}\frac{1-D}{2D-1},\ 0.66 < D < 1. \tag{34}$$

From (34), $v_o < v_{\rm in}$ in this mode, and therefore voltage swell can be compensated.

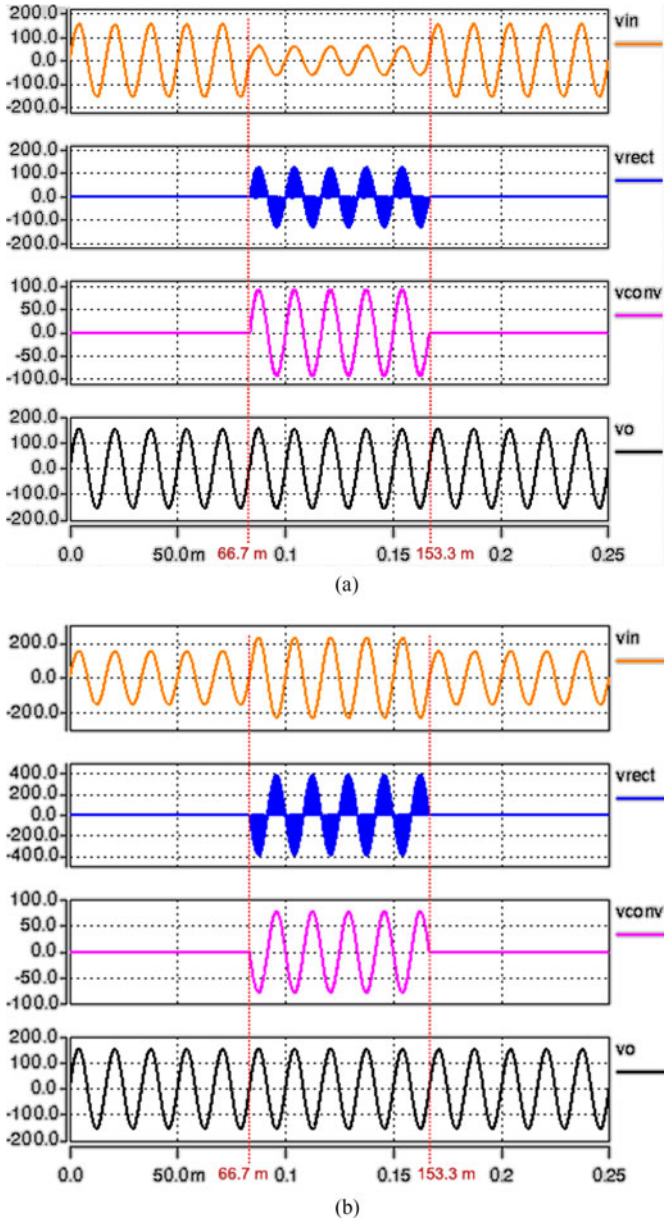

Fig. 10. Simulation waveforms of the proposed HFTI qZS based DVR. (a) Boost operation for voltage sag compensation. (b) Buck operation for voltage swell compensation.

Fig. 10 shows the simulation results of the proposed HFTI qZS ac–ac converter based DVR for voltage sag and swell compensation. Fig. 10(a) shows the waveforms of line voltage $v_{\rm in}$, unfiltered converter voltage $v_{\rm rect}$, converter output voltage $v_{\rm conv}$, and load voltage v_o for voltage sag compensation, as the line voltage $v_{\rm in}$ drops from 110 to 44 Vrms. The converter starts operating in boost (in-phase) mode and load voltage is regulated to normal value of 110 Vrms. Fig. 10(b) shows the

TABLE II
PARAMETERS FOR POWER DENSITY, POWER LOSS, AND EFFICIENCY COMPARISON

IGBTs ($S_{1(a,b)} - S_{3(a,b)}$)	IXGH40N60C2 (600 V / 40 A)
Inductors and HFT cores	PQ5050
Capacitors (C_1, C_2, C_p, C_s, and C_f)	MKP1848560454K2

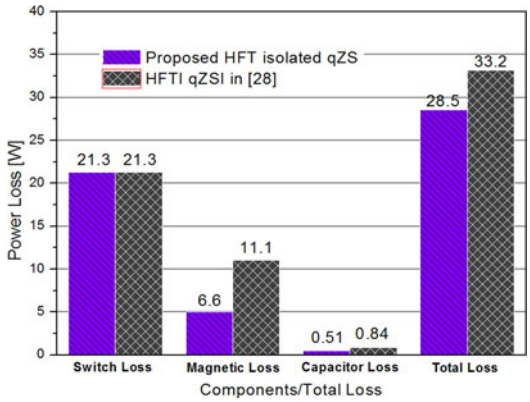

Fig. 11. Comparison of loss distribution in the proposed and conventional HFTI qZS converters for $v_o = 110\,\mathrm{V_{rms}}$, $P_o = 300\,\mathrm{W}$, $D = 0.25$ and $f_s = 20\,\mathrm{kHz}$.

same voltage waveforms during voltage swell compensation when line voltage v_{in} increases from 110 to 165 Vrms. The converter operates in buck (out-of-phase) mode and load voltage is again regulated to normal value of 110 Vrms.

V. COMPARISON OF THE PROPOSED AND EXISTING HFTI QZS AC–AC CONVERTERS

In this section, the proposed HFTI qZS ac–ac converter and its HFTI counterpart converter in [28] are compared in terms of their size, power loss, and efficiency. For this purpose, 300 W prototypes of both the converters are considered using the components as given in Table II. Each converter uses six IXGH40N60C2 IGBTs to form three bidirectional switches $S_{1(a,b)} - S_{3(a,b)}$. The conventional converter in [28] requires four PQ5050 cores, three of them for inductors (L_1,L_2, and L_f) and one for HFT. Whereas the proposed converter uses only two PQ5050 cores, one for inductor L_1 and one for HFT. The conventional converter uses five MKP1848560454K2 film capacitors (C_1,C_2,C_p,C_s, and C_f), whereas the proposed converter uses only three of these capacitors (C_1,C_2, and C_f). From the above discussion, we can conclude that the proposed converter has the same total volume of switches and heatsinks as the conventional converter, whereas its total magnetic and capacitor volumes are reduced by 50% and 30%, respectively, compared to the conventional converter.

In order to compare the power losses and efficiency of the two converters, the winding and core losses of magnetic compensates, and ESR losses of the capacitors are calculated using the parameters in Table II. Moreover, the losses of IGBTs are measured using simulation software for power electronics and motor drive (PSIM) thermal module. Fig. 11 shows comparison of the loss distribution of components and total power loss

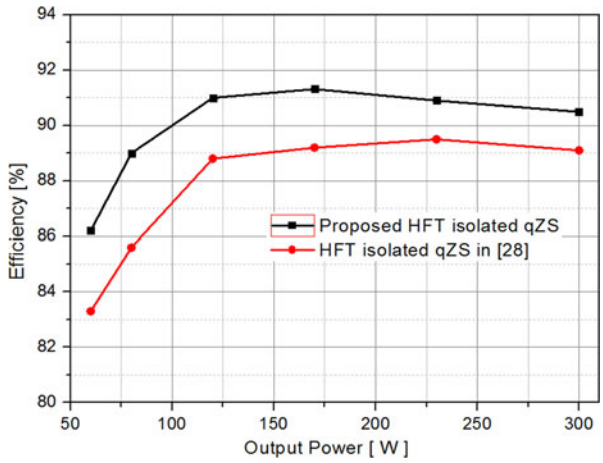

Fig. 12. Comparison of the efficiency for the proposed and conventional HFTI qZS ac–ac converters.

TABLE III
ELECTRICAL SPECIFICATIONS OF THE PROPOSED CONVERTER

Output Voltage	110 VRMS / 60 Hz
Input voltage (Buck operation)	136 VRMS
Input voltage (Boost operation)	73 VRMS
Output power	200 W
Switching frequency	20 kHz
Dead time for commutation	$0.5\,\mu\mathrm{s}$
IGBTs ($S_{1(a,b)} - S_{3(a,b)}$)	FGH40N60CFD
HFT	$L_m = 400\,\mu\mathrm{H}, n = 1$
Capacitors (C_1, C_2)	$6.8\,\mu\mathrm{F}$
Input inductor (L_1)	$800\,\mu\mathrm{H}$
Output filter capacitor (C_o)	$6.8\,\mu\mathrm{F}$

of the proposed and conventional HFTI qZS ac–ac converters for $v_o = 110\,\mathrm{V_{rms}}$, $P_o = 300\,\mathrm{W}$, $D = 0.25$, and $f_s = 20\,\mathrm{kHz}$. From this figure, we can see that the total power loss of the proposed converter is lower than that of the conventional converter, owing to its reduced magnetic (winding and core) and capacitor losses. Fig. 12 shows the efficiency comparison of both the converters for the same operating conditions as the output power is varied.

VI. EXPERIMENTAL RESULTS

To verify the previous analysis, a hardware prototype of the proposed single-phase HFTI qZS ac–ac converter is fabricated and experiments are performed. The component specifications and operating conditions are given in Table III. The input voltage was sensed using an LEM LV-25P voltage transducer and gating signals were generated using TMS320F28335 DSP-kit. The switching frequency was adjusted to 20 kHz and the dead time for safe-commutation was set to 0.5 us. Figs. 13 and 14 show the measured waveforms of input voltage, output voltage, and input current during the boost and buck modes, respectively, for resistive load when $R = 60\,\Omega$. Fig. 15 shows the voltage stresses of switches S_{1b}, S_{2a}, and S_{3b}. Fig. 16 shows the measured voltage waveforms of capacitors C_1, C_2 and primary winding L_p. Fig. 17 shows the voltage waveform across secondary winding L_s, and current waveforms of primary winding L_p, and

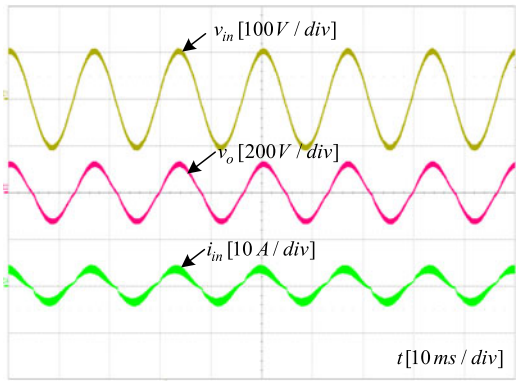

Fig. 13. Measured waveforms of input voltage $v_{\rm in}$, output voltage v_o, and input current $i_{\rm in}$ for noninverting boost mode when $v_{\rm in} = 73\,{\rm V_{rms}}$, and $D = 0.25$.

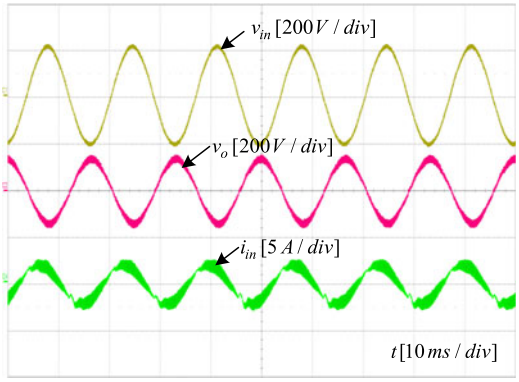

Fig. 14. Measured waveforms of input voltage v_{in}, output voltage v_o, and input current i_{in} for inverting buck mode when $v_{\rm in} = 150\,{\rm V_{rms}}$, and $D = 0.7$.

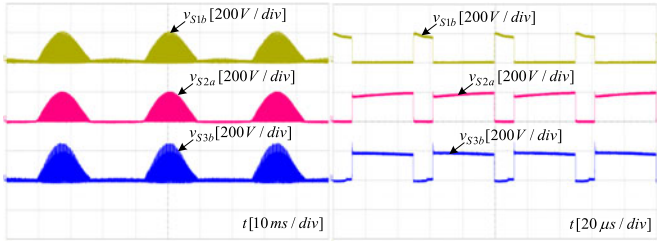

Fig. 15. Measured waveforms of proposed converter when $v_{\rm in} = 73\,{\rm V_{rms}}$, and $D = 0.25$. (a) Switch voltage stresses $v_{S_{1b}}$, $v_{S_{2a}}$, and $v_{S_{3b}}$. (b) Enlarge waveforms of (a).

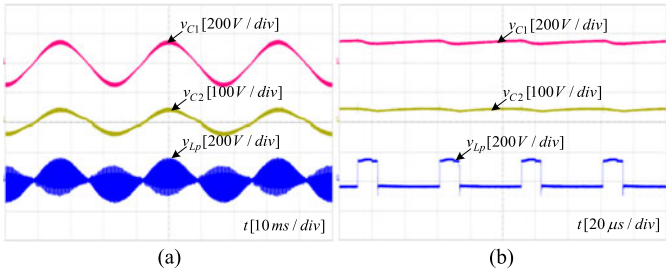

Fig. 16. Measured waveforms when $v_{\rm in} = 73\,{\rm V_{rms}}$, and $D = 0.25$. (a) Voltages v_{C_1}, v_{C_2}, v_{Lp}. (b) Enlarge waveforms of (a).

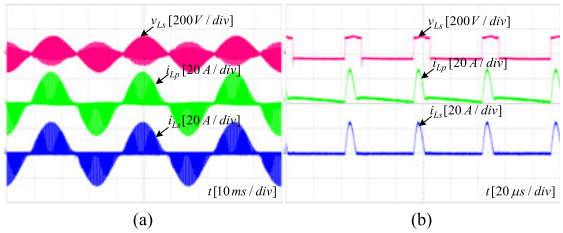

Fig. 17. Measured waveforms when $v_{\rm in} = 73\,{\rm V_{rms}}$, and $D = 0.25$. (a) Voltage v_{Ls} and currents i_{Lp}, i_{Lp}. (b) Enlarge waveforms of (a).

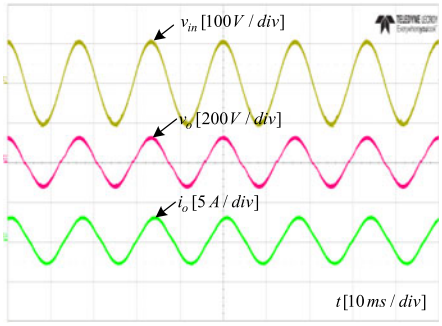

Fig. 18. Measured waveforms of input voltage $v_{\rm in}$, output voltage v_o, and output current i_o during the noninverting boost mode for *RL* load ($R = 50\ \Omega$, $L = 50$ mH) when $v_{\rm in} = 73\,{\rm V_{rms}}$, and $D = 0.25$.

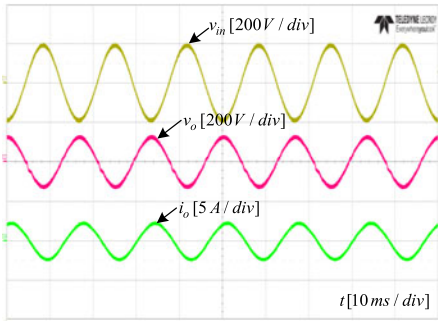

Fig. 19. Measured waveforms of input voltage $v_{\rm in}$, output voltage v_o, and output current i_o during inverting buck mode for *RL* load ($R = 60\ \Omega$, $L = 50$ mH) when $v_{\rm in} = 150\,{\rm V_{rms}}$, and $D = 0.7$.

secondary winding L_s of the HFT. Fig. 18 shows the measured waveforms of input voltage, output voltage, and output current during the boost mode for *RL* load when $R = 50\ \Omega$, $L = 50$ mH with lagging power factor angle of 20.6°. Fig. 19 shows the measured waveforms of input voltage, output voltage, and output current during the buck mode for *RL* load when $R = 60\ \Omega$, $L = 50$ mH with lagging power factor angle of 17.4°. All the experimental results are in close agreement with theoretical analysis and validate the features of the proposed HFTI ZS ac–ac converters.

VII. Conclusion

In this paper, a new class of single-phase ZS ac–ac converters is proposed with HFT isolation. The proposed HFTI ZS ac–ac converters have all the benefits of their conventional nonisolated counterparts such as buck-boost voltage capability, reducing the in-rush and harmonic currents, and enhanced reliability. In addition, the proposed converters have HFT isolation, thus, do not

need bulky external line frequency transformer to provide electrical isolation and safety for application as DVR. The proposed HFTI ZS ac–ac converters are obtained from conventional non-isolated ZS ac–ac converters by replacing two inductors with HFT (saving one magnetic core), and adding only one extra bidirectional switch.

The switching strategies for buck and boost modes are presented with safe-commutation strategy to remove the switch voltage spikes without using snubber circuits. A qZS-based proposed HFTI ac–ac converter is used to discuss the operation principle and circuit analysis of the proposed class of HFTI ZS ac–ac converters. Thereafter, various ZS-based HFTI proposed ac–ac converters are also presented. A laboratory prototype of the proposed converter is also constructed and experiments are conducted to produce output voltage of 110 Vrms / 60 Hz, which verify the operation of the proposed converters.

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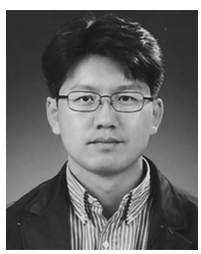

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