A Fixed-Frequency ZVS Integrated Boost Dual Three-Phase Bridge DC–DC LCL-Type Series Resonant Converter

Nagendrappa Harischandrappa, *Member, IEEE*, and Ashoka K. S. Bhat, *Fellow, IEEE*

***Abstract*—A new fixed-frequency controlled three-phase dc–dc LCL-type series resonant converter with integrated boost function is proposed for medium to large power applications with wide input voltage variation that is typical of alternate energy sources. The converter includes a dual three-phase LCL-type resonant bridge inverter modules connected in parallel, thus significantly reducing the component stresses when subjected to medium to large power applications. The fixed-frequency control of the output power is achieved by phase shifting the gating signals of one module with respect to the other, while the rectified voltage at the secondary windings of a three-phase high-frequency transformer connected between the two modules is added to the input voltage to boost the supply voltage to the modules. The zero-voltage-switching of all the switches is accomplished by designing the converter to operate in the lagging PF mode for wide variations in the input voltage and the load. Detailed modeling of the three-phase boost section is done and the steady-state analysis of the proposed converter for three-phase LCL-type dc–dc converter modules using complex ac circuit analysis method is presented. For illustration purpose, a dc–dc converter of 600 W is designed, and its performance is verified using PSIM simulations. An experimental model of the converter is built in the laboratory to verify its performance for wide variations in input voltage and load changes.**

***Index Terms*—DC–DC, dual three-phase bridge, fixed-frequency, integrated boost, LCL-resonant converter.**

I. Introduction

THE power generated using renewable energy sources is highly fluctuating and cannot be used without conditioning. Hence, power converters play an important role in producing usable power from such sources. Many one-phase high-frequency (HF) transformer isolated dc–dc soft-switching resonant converters have been reported in the literature, e.g., [1]–[14]. However, such converters suffer from severe component stresses when subjected to large power applications such as sea wave energy conversion [15]–[16]. To reduce these component stresses, three-phase HF transformer isolated dc–dc converters have been reported in the literature [17]–[29]. Some of the several advantages of the three-phase dc–dc converters over one-phase are: ability to handle higher power, lower current ratings of the switches, reduced input and output current ripple due to an increase in the effective frequency by a factor of three resulting in small size filter requirements, reduced size of the transformer, and better utilization of the transformer core [21], [25], [27]. To increase the converter operating efficiency and reduce its overall size, three-phase HF transformer isolated soft-switching resonant converters capable of operating with much higher switching frequency while keeping the switching losses low are reported in the literature [15], [17]–[28]. These resonant converters were operated with variable frequency control that has the disadvantages such as difficulty in the design of magnetics and filters, increased power losses at higher frequencies (if above resonance mode is used), increase in the size of the magnetics and filters due to very low frequency at light loads (when below resonance operation is used) [1]–[3], [6]. Fixed-frequency control of three-phase resonant converters has the difficulty to operate in zero-voltage-switching (ZVS) mode for wide variations in input voltage and load [23]. Although one-phase HF isolated LCL-type with fixed-frequency gating control can operate in ZVS in such situations [1], [2], [7], [8], three-phase LCL-type converters have been operated only in variable frequency control due to difficulty to maintain ZVS operation in fixed-frequency control [21]. The fixed-frequency controlled three-phase LCL-type dc–dc resonant converter with a capacitive output filter cannot have ZVS for all the switches. Similarly, dual active bridge pulse width modulation (PWM) converter also cannot maintain ZVS for such wide variations in input voltage and load [30], [31]. A variable-frequency controlled one-phase dual half-bridge series-parallel resonant converter with transient-boost function was first proposed in [32]. In [33], a fixed-frequency controlled integrated boost-dual one-phase half-bridge LCL-type series resonant converter (SRC) with a capacitive output filter was proposed. In the present type of application, these types of boost integrated resonant converters are suitable due to wide variations in the input voltage. However, only one-phase versions are proposed in the literature [32], [33]. A three-phase HF transformer isolated dc–dc LCL-type resonant converter with a transient-boost function has not been reported in the literature. In this paper, a fixed-frequency controlled integrated boost dual three-phase bridge LCL-type SRC with capacitive output filter is proposed (see

Manuscript received October 3, 2016; revised January 12, 2017; accepted February 13, 2017. Date of publication March 7, 2017; date of current version November 2, 2017. This work was supported by a grant from Natural Sciences and Engineering Research Council (NSERC) of Canada. Recommended for publication by Associate Editor R.-L. Lin.

N. Harischandrappa is with the National Institute of Technology Karnataka, Mangalore 575025, India (e-mail: nagendrappa@nitk.edu.in).

A. K. S. Bhat is with the University of Victoria, Victoria, BC V8W 2Y2 Canada (e-mail: bhat@ece.uvic.ca).

Color versions of one or more of the figures in this paper are available online at http://ieeexplore.ieee.org.

Digital Object Identifier 10.1109/TPEL.2017.2679041

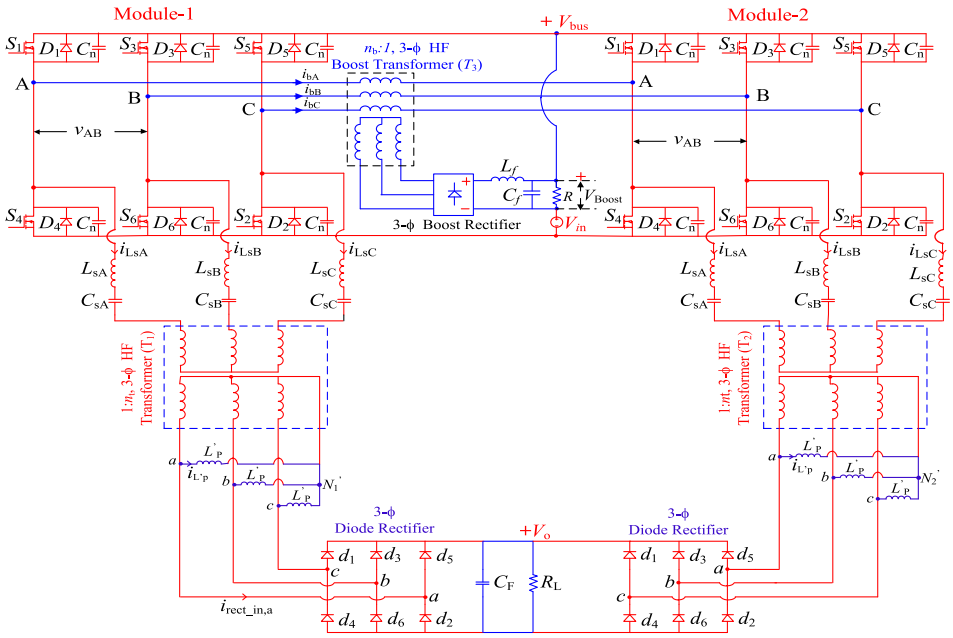

Fig. 1. Fixed-frequency controlled three-phase HF transformer isolated dual three-phase bridge dc–dc LCL-type series resonant converter with capacitive output filter that uses a three-phase boost transformer-rectifier circuit.

Fig. 1). The proposed converter consists of two three-phase inverter bridge modules that are connected in parallel to supply a common load. Each inverter module is provided with 180° wide normal three-phase fixed-frequency gating signals. The fixed-frequency control of regulating the load voltage is achieved by phase shifting the gating signals of module-2 with respect to that of module-1, while the rectified voltage at the secondary windings of the three-phase HF transformer connected between the two modules is added to the input voltage to boost the supply voltage to the modules. This phase-shift is controlled to regulate the output voltage (V_o). The proposed converter has all the advantages aforementioned of the three-phase HF transformer isolated LCC-type and LCL-type of resonant converters while operating in a fixed-frequency ZVS mode. Comparison of existing three-phase dc–dc converter topologies, i.e., Topology-1: thre-phase LCL-type dc–dc resonant power converter with capacitive output filter [21]; Topology-2: three-phase LCC-type dc–dc resonant power converter with capacitive output filter [23], [24]; Topology-3: three-phase PWM dc–dc converter [31] with the proposed converter topology (Topology-4) is presented in Table I. The objectives of this paper are, for the proposed converter,

1) to present the operation;
2) to model the boost transformer–rectifier section;
3) to analyze one of the two LCL inverter modules;
4) to illustrate the design procedure with a design example;
5) to verify the performance using PSIM simulations; and
6) to build an experimental model to verify its performance.

The outline of the paper is as follows: In Section II the circuit details and the operating principle of the proposed converter are described. Modeling of the boost section and the steady-state approximate complex ac circuit analysis of the fixed-frequency three-phase LCL inverter module is presented in Section III.

TABLE I
COMPARISON OF THREE-PHASE DC–DC CONVERTER TOPOLOGIES

Topology	Advantages	Disadvantages
1	A1. Narrow variation in switching frequency for voltage regulation	D1. Variable-frequency control-difficult filter and magnetic design
	A2. Wide ZVS range	D2. Higher component stresses (Due to non-availability of load-sharing modules) for large power applications(> 10 kW)
	A3. Reduced size as the magnetizing inductance of the transformer can be used as part of the parallel inductor.	
2	A1, A3, and A4. Rectifier voltage ratings limited to output voltage.	D1, and D2
3	A5. Simple control.	D2, D3. Hard-switching, and D4. Limited switching frequency range
4	A1 to A5 and A6.Integrated-boost function A7.Reduced component stresses-suitable for use in power rating > 10 kW A8. Fixed frequency control- filter design is simple. A9. Can supply 50% of rated power in case of a fault in one of the modules. A10. Wide input voltage change	D5. Uses more number of components e.g., 12 switches, and 18 diodes.

Design procedure with an illustrative example of a 600-W converter is presented in Section IV. PSIM simulation results are presented in Section V. The experimental results are presented in Section VI. Conclusions are drawn in Section VII.

II. CIRCUIT DETAILS AND THE OPERATING PRINCIPLE

The circuit diagram of the proposed converter is shown in Fig. 1. This circuit consists of two three-phase inverter bridges each having six MOSFETs with antiparallel diodes and a snubber capacitance across it. The output terminals of these

inverters are connected to a three-phase diode rectifier through a three-phase resonant circuit consisting of resonant inductance L_s and resonant capacitance C_s in each phase and a three-phase HF transformer (T_1, T_2) of 1: n_t turns ratio. These modules are connected in parallel and are supplied with V_{bus}. The primary windings of a three-phase HF boost transformer (T_3) of n_b:1 turns ratio is connected between the two modules. Each phase of the primary windings of the boost transformer is connected between the same output phase of the two inverter bridges. The secondary terminals of the boost transformer are connected to a three-phase diode boost rectifier bridge. The boost rectifier bridge output voltage is filtered by L_f and C_f. This filtered output voltage (V_{boost}) of the boost rectifier is connected in series with the input dc source to give V_{bus}, which is applied across the two modules. In the three-phase LCL resonant converter modules, the parallel three-phase Wye connected inductors L'_p in each module are placed on the secondary side of the three-phase HF transformers so that the magnetizing inductance can be used as part of the parallel inductor and the leakage inductance can be used profitably as part of the series resonant inductors L_s [7], [21]. The primary windings of the three-phase boost transformer T_3 are connected between the modules-1 and 2 and secondary windings are shown in Wye connection (they can also be connected in Δ). The six gating signals for the three-phase inverter bridge switches are 180° wide as shown in Fig. 2. These gating signals are applied in an order with a delay of 60° to get a balanced three-phase inverter output voltage. Each switch conducts for 180° and three switches remain on at any point of time in a given interval, devices conducting are shown in Fig. 2. There are six intervals of operation in each cycle and the duration of each interval is 60°. The fixed-frequency control is achieved by phase shifting the gating signals of module-2 with respect to module-1 by an angle δ, which creates a potential difference across the primary windings of the HF boost transformer. The corresponding voltage thus induced in the secondary is rectified and filtered using L_f and C_f to generate V_{boost} and added with input voltage (V_{in}) to create the bus voltage $V_{bus} = V_{in} + V_{boost}$, which is applied across the three-phase inverter bridge modules 1 and 2. At minimum input voltage $V_{in}(\min)$ and full-load, the gating signals of module-2 are shifted by 180° to generate a square wave voltage waveform of pulse width, $\delta = \pi$ in each phase across the primary windings of the three-phase boost transformer. The phase shift is varied to change the pulsewidth δ of quasi-square wave generated across the primary windings of the boost transformer T_3 to regulate V_o for variations in V_{in} and the load. Typical operating waveforms for an arbitrary pulsewidth δ for the boost section and the three-phase resonant converter are shown in Fig. 2. The inverter output voltages (v_{AB}, v_{BC}, v_{CA}) and currents (i_{LsA}, i_{LsB}, i_{LsC}) waveforms are shifted by 120° from each other. The output voltage and current waveforms of module-2 are shifted by an angle δ from that of module-1. It can be noted from Fig. 2 that the widths of the inverter output voltage waveforms v_{AB}, v_{BC}, v_{CA} for each module remains unchanged at 120° as δ is varied. However, the amplitudes of these waveforms change when the load is changed as the V_{bus} changes to keep V_o constant. The resonant current waveforms shown are approximately sinusoidal and they lag the respective voltage waveforms allowing the antiparallel diodes to conduct thereby achieving ZVS.

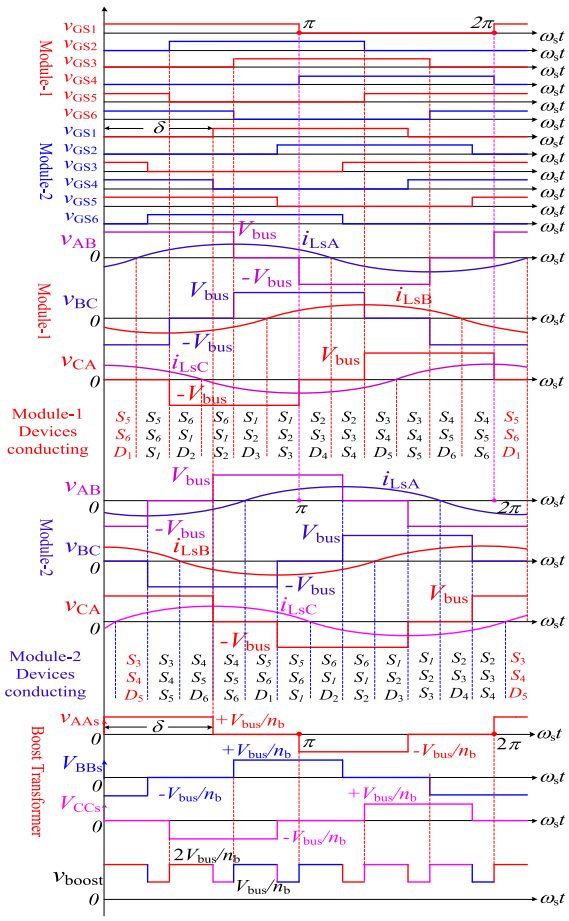

Fig. 2. Typical operating waveforms of the proposed converter shown in Fig. 1: phase-shifted gating signals of modules 1 and 2; output voltages of the three-phase inverter module-1 and module-2 with respective resonant currents; the phase voltage waveforms at the secondary terminals of the boost transformer of n_b:1 turns ratio for an arbitrary pulse-width δ.

III. Modeling and Analysis

In this section, the modeling and analysis of the proposed converter shown in Fig. 1 is presented. The overall modeling of the converter involves modeling the boost section and modeling only one of the two three-phase inverter modules as both the modules are identical. Analysis of the LCL converter part shown in Fig. 1 operating in fixed-frequency mode is done using an approximate complex ac circuit analysis method [8], [21].

A. Assumptions

The following assumptions are made in the analysis:

1) all the switches, diodes, inductors, and capacitors are ideal;
2) the effect of snubbers is neglected;
3) only fundamental components of voltages and currents are considered while analyzing the LCL resonant converter modules;

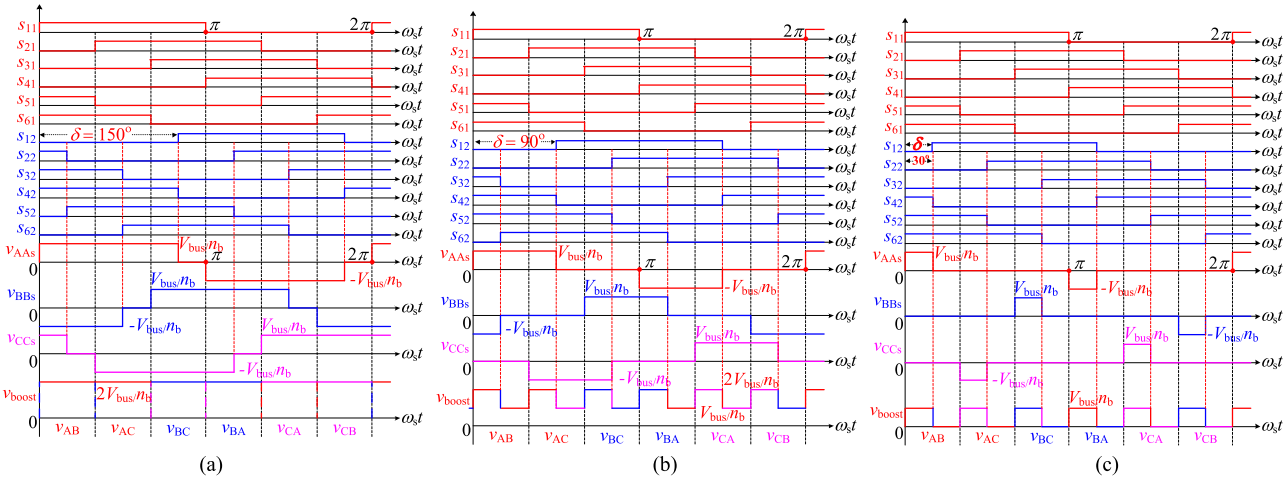

Fig. 3. Typical operating waveforms of the boost transformer–rectifier unit showing the boost transformer secondary-side voltages (v_{AAs}, v_{BBs}, and v_{CCs}) and the rectified boost voltage (v_{boost}) along with the gating signals of modules 1 and 2 for: (a) $\delta = 150°$ in Mode-1 (i.e., $180° \geq \delta \geq 120°$); (b) $\delta = 90°$ in Mode-2 (i.e., $120° \geq \delta \geq 60°$); and (c) $\delta = 30°$ in Mode-3 (i.e., $60° \geq \delta \geq 0°$).

4) the input and output voltages are assumed to be constant without any ripple;
5) all the three phases are identical and balanced;
6) the leakage inductances of the three-phase transformers are taken into account (either as part of resonant inductors for T_1 and T_2 or for use in ZVS in boost section) and the magnetizing inductances of the transformer are considered part of the parallel inductors L'_{p};
7) Module-1 and Module-2 are identical.

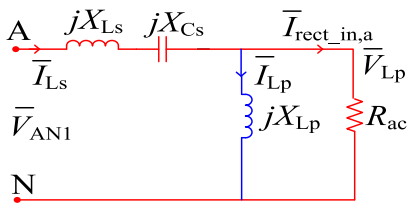

Fig. 4. Phasor equivalent circuit used for analyzing the module-1 of the converter shown in Fig. 1.

B. Modeling and Analysis of the Three-Phase Boost Transformer—Rectifier

The boost section in Fig. 1 comprising the 3-ϕ boost transformer of turns ratio n_{b}:1 and the 3-ϕ boost rectifier operates in three different modes as the input voltage and the load are varied from minimum voltage to maximum and from full-load to the light-load, respectively. For this variation, the phase-shift angle δ is reduced from 180° to the lower values in order to keep the load voltage constant at its full-load value. As δ is reduced, the operation of the boost transformer–rectifier unit changes from mode-1 through mode-3 and is similar to phase-shifted DAB [20].

Mode-1 ($180° \geq \delta \geq 120°$; Uncontrolled mode): The typical operating waveforms in this mode are shown in Fig. 3(a). The rectified boost voltage waveform consists of a constant voltage of value $2V_{\mathrm{bus}}/n_{\mathrm{b}}$. Therefore

$$V_{\mathrm{boost-1}} = \frac{2V_{\mathrm{bus}}}{n_{\mathrm{b}}} \quad (\text{For all } \delta = 180° \text{ to } 120°). \tag{1}$$

Mode-2 ($120° \geq \delta \geq 60°$; Controlled mode): Typical operating waveforms in this mode are shown in Fig. 3(b). The rectified boost voltage waveform consists of pulses of height $2V_{\mathrm{bus}}/n_{\mathrm{b}}$ and $V_{\mathrm{bus}}/n_{\mathrm{b}}$, and V_{boost} can be derived as

$$V_{\mathrm{boost-2}} = \frac{3}{\pi}\frac{V_{\mathrm{bus}}}{n_{\mathrm{b}}}\delta \quad (120° \geq \delta \geq 60°). \tag{2}$$

Mode-3 ($60° \geq \delta \geq 0°$; Controlled mode): The typical operating waveforms in this mode are shown in Fig. 3(c). The rectified boost voltage waveform consists of pulses of height $V_{\mathrm{bus}}/n_{\mathrm{b}}$ and zero. Therefore, V_{boost} can be derived as

$$V_{\mathrm{boost-3}} = \frac{3}{\pi}\frac{V_{\mathrm{bus}}}{n_{\mathrm{b}}}\delta \quad (60° \geq \delta \geq 0°). \tag{3}$$

The widths of the pulses for modes 2 and 3 are the same as the phase-shift angle δ that can be controlled that in turn controls V_{boost}. The V_{bus} applied across the 3-ϕ inverter bridges is given by:

$$V_{\mathrm{bus}} = V_{\mathrm{in}} + V_{\mathrm{boost}}. \tag{4}$$

Hence, for regulating the load voltage when the input voltage and the load changes, the boost transformer–rectifier unit must operate in modes 2 and 3 (i.e., δ has to be reduced below 120°) so that the V_{boost} can be controlled to control V_{bus} thereby regulating the load voltage. The 3-ϕ dc-dc converter modules are designed for the chosen value of V_{bus} corresponding to the minimum input voltage $V_{\mathrm{in}}(\min)$ in (4). Therefore, the boost transformer is designed to give maximum V_{boost} such that (4) is satisfied. The expression for the boost transformer turns ratio (n_{b}:1) is derived by substituting for V_{boost} from (1) in (4)

$$n_{\mathrm{b}} = \frac{2V_{\mathrm{bus}}}{V_{\mathrm{bus}} - V_{\mathrm{in}}}. \tag{5}$$

For ZVS operation, the minimum inductance to be connected in series with each phase of the primary windings of the ideal

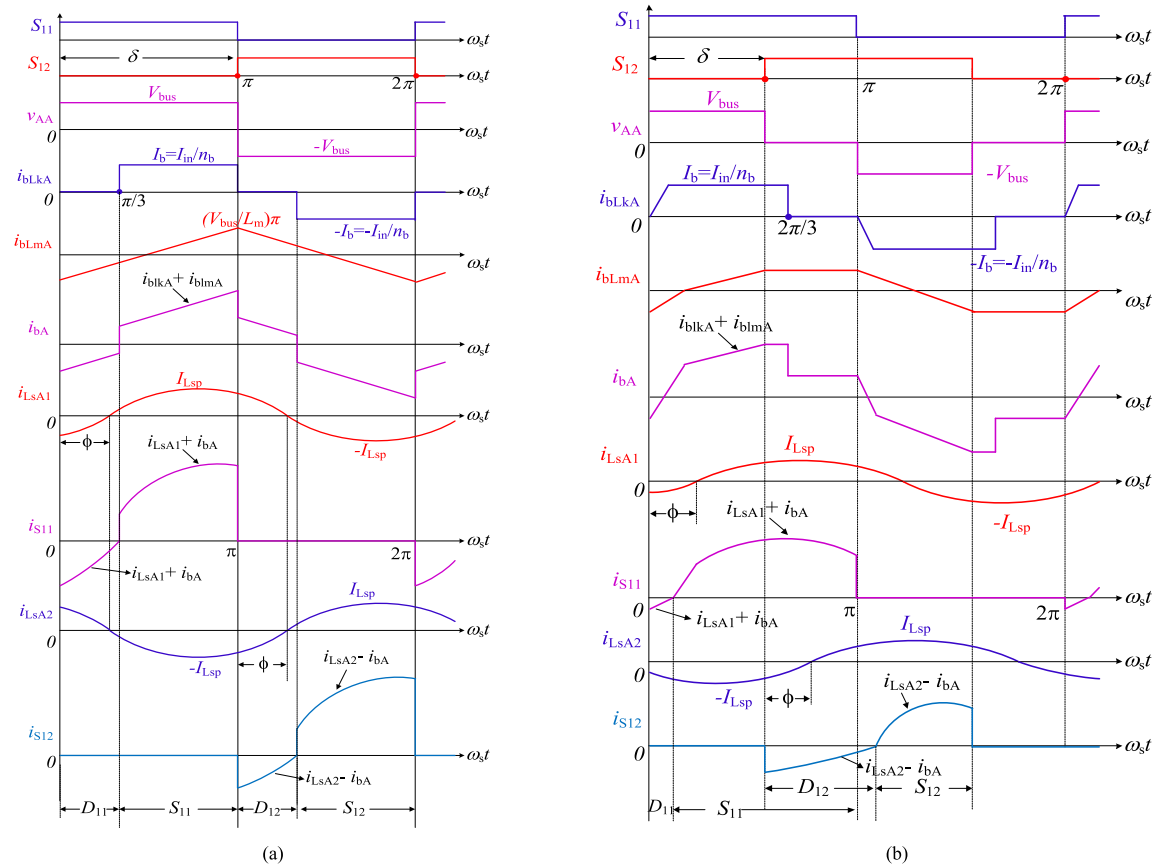

Fig. 5. Waveforms of gating signals (S_{11}, S_{12}), voltage across the primary windings (v_{AA}); reflected input source current (I_{in}) on the primary side of the boost transformer (i_{bLkA}); current through the magnetizing inductance of the boost transformer (i_{bLmA}); approximated primary current in phase-A ($i_{\mathrm{bA}} = i_{\mathrm{bLkA}} + i_{\mathrm{bLmA}}$) of the boost transformer; switch currents, tank currents in phase-A of module-1 (i_{S11}, i_{LsA1}) and module-2 (i_{S12}, i_{LsA2}) for: (a) $\delta = 180°$, used for calculating the switch current ratings, (b) an arbitrary δ in controlled mode-2.

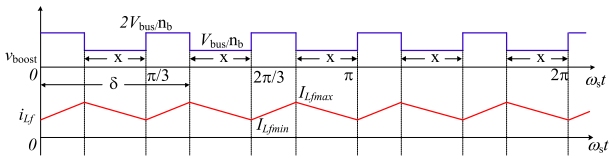

Fig. 6. Waveforms of the boost rectifier output voltage (v_{boost}) and the output current (i_{Lf}) for an arbitrary phase-shift angle of δ in mode-2 (i.e., $120° \geq \delta \geq 60°$), where, $\mathrm{x} = 2\pi/3 - \delta$.

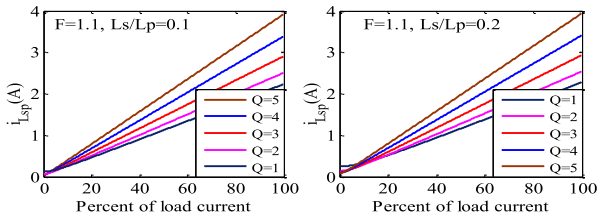

Fig. 7. Variation of peak inverter output current versus percent of full-load current with output voltage held constant at full-load value: for $F = 1.1$ and for various values of full-load Q, (a) $L_{\mathrm{s}}/L_{\mathrm{p}} = 0.1$ and (b) $L_{\mathrm{s}}/L_{\mathrm{p}} = 0.2$; where $Q = \omega_{\mathrm{r}} L_{\mathrm{s}}/R'_{\mathrm{L}}$ is the full-load Q factor of the tank circuit, $F = \omega_{\mathrm{s}}/\omega_{\mathrm{r}} = f_{\mathrm{s}}/f_{\mathrm{r}}$ is the ratio of switching frequency to the resonant frequency.

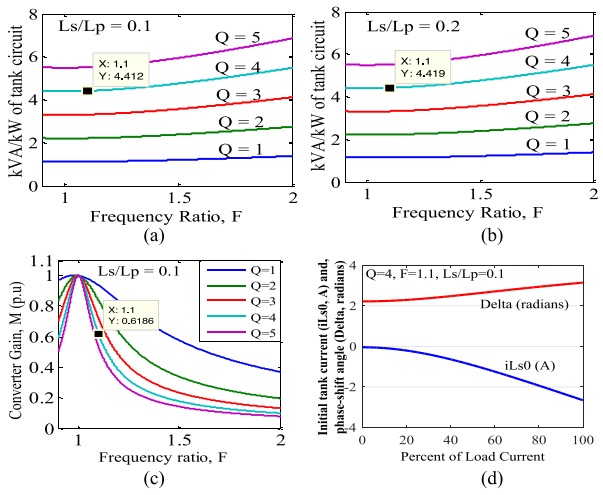

Fig. 8. Variation of tank kVA/kW of rated output power versus frequency ratio F (a) $L_{\mathrm{s}}/L_{\mathrm{p}} = 0.1$; (b) $L_{\mathrm{s}}/L_{\mathrm{p}} = 0.2$; (c) variation of converter gain $M\ (= V'_{\mathrm{o}}/V_{\mathrm{bus}})$ with F for various values of full-load Q; and (d) variation of initial tank current i_{Ls0} (i.e., i_{Ls} at $\omega t = 0$) and variation of phase-shift angle δ, as a function of percent of full-load current for full-load $Q = 4$ and $F = 1.1$. $L_{\mathrm{s}}/L_{\mathrm{p}} = 0.1$ for all the design curves.

three- phase boost transformer (L_{bt}) is obtained using the following expression [34] for the worst operating case of minimum input voltage and the lowest load

$$1/2 L_{bt} I_{\mathrm{b}}^2 > 1/2 (2 C_n V_{\mathrm{bus}}^2) \tag{6}$$

Fig. 9. PSIM simulation waveforms of the voltage across inverter output terminals $(v_{\mathrm{AB}}, v_{\mathrm{BC}}, v_{\mathrm{CA}})$ and the current through phase A of the tank circuit (i_{LsA}) for: (a) module-1 and (b) module-2, and (c) the phase voltages across the secondary terminals of the 3-phase boost transformer $T_3\,(v_{\mathrm{A12s}}, v_{\mathrm{B12s}}, v_{\mathrm{C12s}})$, and the output voltage of the boost rectifier before filtering (vboost); for case-1: $V_{\mathrm{in}}\,(\mathrm{min}) = 50\mathrm{V}$, full-load, $R_{\mathrm{L}} = 60\,\Omega, \delta = 180°$. Waveforms of (a)–(c) repeated: (d)–(f) for case-2: $V_{\mathrm{in}}\,(\mathrm{max}) = 100$ V, full-load, $R_{\mathrm{L}} = 60\,\Omega$, $\delta = 61°$, (g)–(i) for case-3: $V_{\mathrm{in}}\,(\mathrm{min}) = 50$ V, half-load, $R_{\mathrm{L}} = 120\,\Omega$, $\delta = 97°$; and (j)–(l) Case-4: $V_{\mathrm{in}}\,(\mathrm{max}) = 100$ V; half-load, $R_{\mathrm{L}} = 120\,\Omega$; and $\delta = 18°$.

where I_{b} is the amplitude of phase current through the primary windings of the three-phase boost transformer, C_{n} is the snubber capacitance, and V_{bus} is the bus voltage for the given operating point.

C. Modeling of the Three-Phase Inverter Modules

The circuit diagram of module-1 extracted from Fig. 1 is simplified by following the steps described in [21] and a phasor equivalent circuit model as shown in Fig. 4 is obtained. Based on this model, the steady-state analysis of the converter using an approximate complex ac circuit analysis method is done and is summarized in Appendix [21]. Typical operating waveforms of the three-phase inverter modules are given in Fig. 2.

D. Calculation of Device Ratings

(i) MOSFET ratings: Various waveforms associated with the switches S_{11} of module-1 and S_{12} of module-2 for the maximum phase-shift angle of $\delta = 180°$ are given in Fig. 5(a).

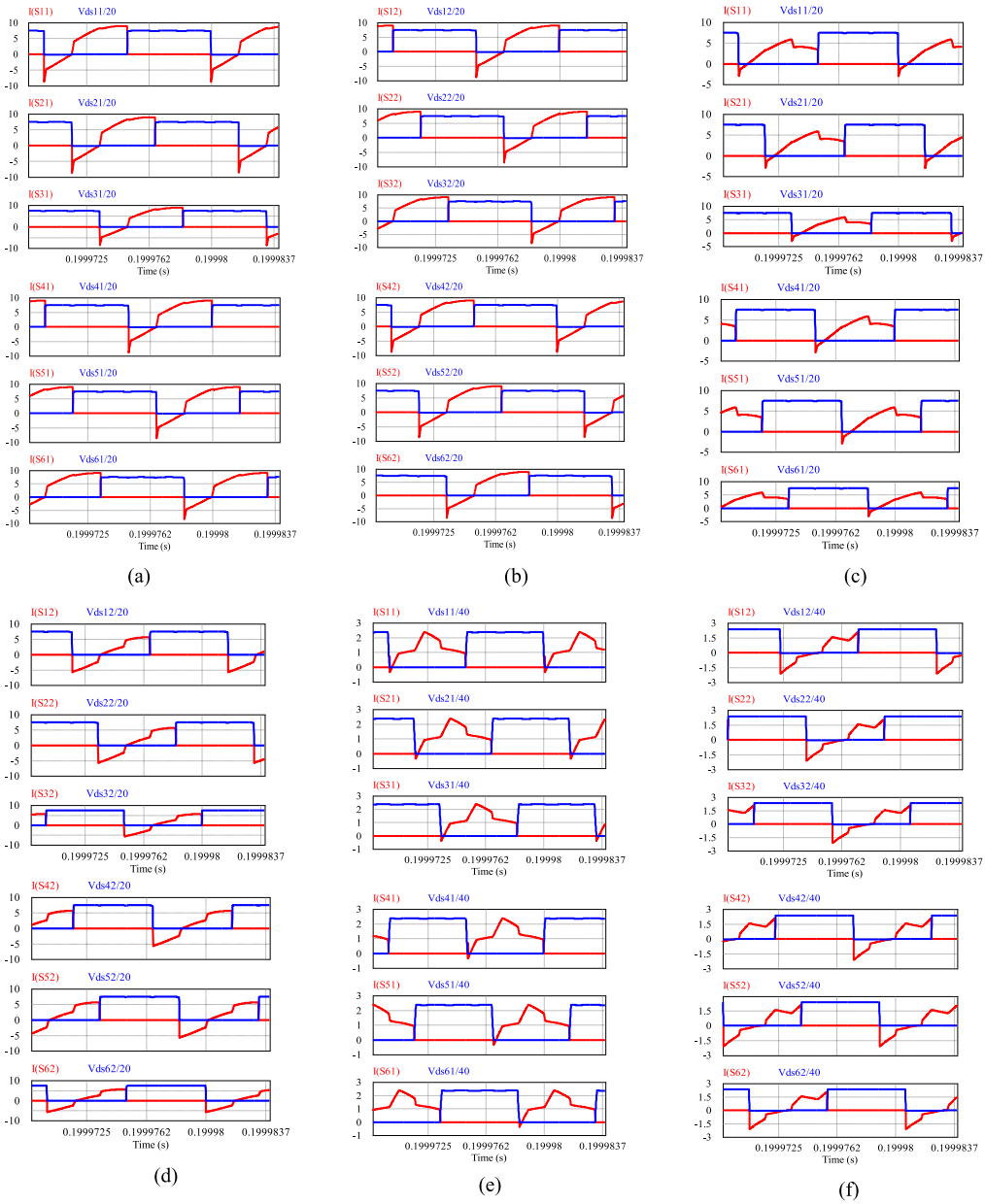

Fig. 10. PSIM simulation waveforms of the voltage across switches (v_{DS}) and the respective current through the switches (i_{S}) to show ZVS of switches $S_1 - S_3$, and $S_4 - S_6$, (a) module-1, and (b) module-2 for case-1: $V_{\mathrm{in}}(\mathrm{min}) = 50$ V, full-load, $R_{\mathrm{L}} = 60\ \Omega$, $\delta = 180°$). Waveforms of (a)–(b) repeated, (c)–(d) for case - 2: $V_{\mathrm{in}}(\mathrm{max}) = 100$ V, full-load, $R_{\mathrm{L}} = 60\ \Omega$, $\delta = 61°$, and (e)–(f) for case - 5: $V_{\mathrm{in}}(\mathrm{min}) = 50$ V, 20% of full-load, $R_{\mathrm{L}} = 300\ \Omega$, $\delta = 84°$.

These waveforms are used in deriving the expressions for the r.m.s and average values of the switch current and the average value of the current in antiparallel diode of the MOSFET. In the derivations, an approximated waveform of the boost transformer primary current (i_{bA}) in phase A is considered. Sample waveforms of these switches for the reduced load in controlled mode-2 (i.e., $120° \geq \delta \geq 60°$) are given in Fig. 5(b). The expressions for different currents are derived [35] by referring to the waveforms given in Fig. 5(a), and are as follows:

1) the r.m.s value of the switch current, $I_{\mathrm{SW}}(\mathrm{rms})$: eqn. (7) shown at the bottom of the page.

$$I_{\mathrm{SW}}\,(\mathrm{rms}) = \sqrt{\frac{1}{2\pi}\left\{I_b^2\left(\pi - \frac{\pi}{3}\right) + \frac{I_{\mathrm{Lsp}}^2}{2}\left(\pi - \frac{\pi}{3} + \frac{\sin 2\Phi}{2} + \frac{\sin\left(2\frac{\pi}{3} - 2\Phi\right)}{2}\right) + 2I_{\mathrm{b}}I_{\mathrm{Lsp}}\left(\cos\Phi + \cos\left(\frac{\pi}{3} - \Phi\right)\right)\right\}} \tag{7}$$

2) the average value of the switch current, $I_{\mathrm{SW}}(\mathrm{av})$

$$I_{\mathrm{SW}}(\mathrm{av}) = \frac{1}{2\pi}\left\{\mathrm{I_b}\left(\pi - \frac{\pi}{3}\right) + \mathrm{I_{Lsp}}\left(\cos\Phi + \cos\left(\frac{\pi}{3} - \Phi\right)\right)\right\} \tag{8}$$

3) the average value of the anti-parallel diode current, $I_{\mathrm{DM}}(\mathrm{av})$

$$I_{\mathrm{DM}}(\mathrm{av}) = \frac{I_{Lsp}}{2\pi}\left(\cos\Phi - \cos\left(\frac{\pi}{3} - \Phi\right)\right) \tag{9}$$

4) the maximum voltage across the switch (MOSFET)

$$v_{\mathrm{DS}}(\max) = V_{\mathrm{bus,max}} \tag{10}$$

where $V_{\mathrm{bus,max}}$ is the rated V_{bus} at full-load.

(ii) Diode ratings: The waveforms of the output voltage (v_{boost}) and the output current (i_{Lf}) of the three-phase boost rectifier are shown in Fig. 6. The average value of the output current (i.e., the current through inductive filter, L_{f}) is derived using the waveform of i_{LF} from Fig. 6. Following expressions for the average current in the diodes of the boost rectifier and the output rectifier are obtained.

1) Boost rectifier average diode current (each diode conducts for 120°)

$$I_{\mathrm{Db}} = I_{\mathrm{Lf}}(\mathrm{av})/3 \tag{11}$$

where

$$I_{\mathrm{Lf}}(\mathrm{av}) = (I_{\mathrm{Lfmin}} + I_{\mathrm{Lfmax}})/2. \tag{12}$$

2) The maximum voltage across the boost rectifier diode

$$V_{\mathrm{Db}} = 2V_{\mathrm{bus}}/n_{\mathrm{b}}. \tag{13}$$

3) Output rectifier average diode current (each diode conducts for 120°, and each rectifier shares the load equally)

$$I_{\mathrm{Do}} = I_{\mathrm{RL}}(\mathrm{av})/(3\times 2) \tag{14}$$

where

$$I_{\mathrm{RL}}(\mathrm{av}) = P_{\mathrm{o}}/V_{\mathrm{o}}. \tag{15}$$

4) The maximum voltage across the output rectifier diodes

$$V_{\mathrm{Do}} = V_{\mathrm{o}}. \tag{16}$$

IV. Design

Based on the analysis presented in Section III, a fixed-frequency ZVS integrated boost dual three-phase bridge dc–dc LCL-type SRC with a capacitive output filter having the following specifications is designed for illustration purpose. Input dc voltage, $V_{\mathrm{in}} = 50$ V (min) to 100 V (max); output dc voltage, $V_{\mathrm{o}} = 190$ V, output power, $P_{\mathrm{o}} = 600$ W; and inverter switching frequency, $f_{\mathrm{s}} = 100$ kHz.

A. Design Tradeoffs

The main objective of the converter is to maintain constant output voltage for variations in the input voltage and the loading conditions. This is achieved by phase-shifting the gating signals of module-2 with respect to that of module-1. The converter is designed to operate in the worst operating condition of minimum input voltage and the maximum load current/power. While designing the converter, zero-voltage switching is targeted by designing the converter to operate in lagging pf mode so that the turn-on losses are minimized. This is taken care by using $F = 1.1$ (which is above 1). Also, the converter is designed to have peak switch currents to reduce as the load current is reduced so that the light load efficiency is good. This is taken care by choosing a proper value of full-load Q from the design curves. The design is made to have lower kVA/kW rating of the tank circuit. This is taken care by using both the lower value of the inductor ratio $L_{\mathrm{s}}/L_{\mathrm{p}}$ and by choosing F marginally above the resonant condition (where the kVA/kW rating is the lowest) for lagging pf operation. Design curves given in Figs. 7 and 8 are used in selecting the optimum values of the design parameters. The worst operating condition of minimum input voltage and maximum output power is used for designing the converter, i.e., under such a condition the converter is operated with a maximum phase-shift of $\delta = \pi$. The converter is designed to operate in the lagging pf or above resonance mode of the tank circuit can be ensured by confirming the negative sign of i_{Ls0} in (37). This along with the phase of the boost transformer primary current decides the ZVS operation of the switches. The variation of peak resonant current "i_{Lsp}" as a function of percent of load current for different values of full-load Q is shown in Fig. 7(a) and (b) for two inductor ratios with the frequency ratio $F = 1.1$. It is observed from Fig. 7(a) and (b) that for decreasing Q, the peak resonant current decreases proportionally with the load. However, this decrease in peak current is not very drastic for Q < 4. Also, for lower values of Q the peak resonant current tends to increase at light load [e.g., $Q = 1$ in Fig. 7(a) and (b)]. It is

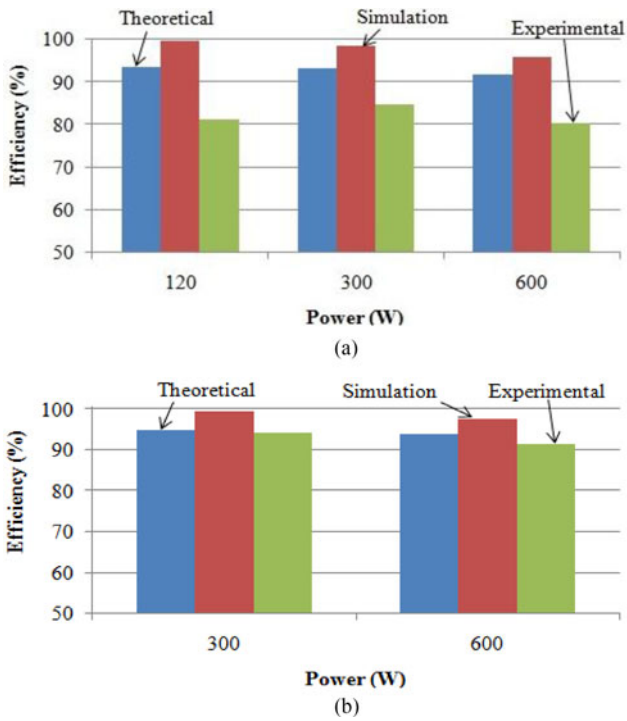

Fig. 11. Theoretical, simulation, and experimental efficiencies of the proposed converter as a function of output power with: (a) $V_{\mathrm{in}}(\min) = 50$ V for full-load (600 W), half-load (300 W), and 20% of full-load (120 W) and (b) $V_{\mathrm{in}}(\max) = 100$ V for full-load (600 W), and half-load (300 W).

TABLE II
COMPARISON OF RESULTS FROM CALCULATIONS, SIMULATION, AND EXPERIMENT

Parameter		Case-1: $V_{\rm in}(\min) = 50$ V, Full load			Case-2: $V_{\rm in}(\max) =$ 100 V, Full load			Case-3: $V_{\rm in}(\min) = 50$ V, half load			Case-4: $V_{\rm in}(\max) =$ 100 V, half load			Case-5: $V_{\rm in}(\rm Min) = 50$ V, 20% load		
		Cal.	Sim.	Expt.	Cal.	Sim.	Expt.	Cal.	Sim.	Expt.	Cal.	Sim.	Expt.	Cal.	Sim.	Expt.
$V_{\rm o}$(V)		190.00	186.21	179.00	190.00	187.65	178.00	190.00	184.50	178.00	190.00	186.10	176.00	190.00	186.66	176.00
$I_{\rm o}$(A)		3.15	3.11	3.01	3.15	3.12	2.98	1.57	1.53	1.50	1.57	1.55	1.50	0.63	0.62	0.60
$V_{\rm bus}$(V)		150.00	150.12	155.00	150.00	151.10	151.00	110.92	109.13	123.00	110.92	110.10	120.00	97.22	95.34	126.00
$V_{\rm boost,DC}$(V)		100.00	100.65	101.00	49.99	51.10	52.00	60.80	59.32	73.00	10.98	10.10	21.00	47.61	45.33	72.00
η(%)		91.75	96.03	80.41	94.02	97.76	91.45	93.17	98.52	84.76	94.93	99.46	94.28	93.70	99.65	81.23
δ(°)		180	180	174	60	61	57	99	97	108	18	18	34	88	84	102
$I_{\rm Lsp}$ ($I_{\rm Lsr}$) (A)	*Mod-1*	3.38 (2.39)	3.39 (2.49)	3.44 (2.29)	3.38 (2.39)	3.41 (2.49)	3.44 (2.30)	1.69 (1.19)	1.70 (1.20)	2.19 (1.41)	1.69 (1.19)	1.71 (1.24)	2.19 (1.43)	0.677 (0.48)	0.69 (0.49)	1.64 (1.03)
	Mod-2	3.38 (2.39)	3.4 (2.49)	3.44 (2.27)	3.38 (2.39)	3.42 (2.37)	3.44 (2.26)	1.69 (1.19)	1.71 (1.20)	2.03 (1.26)	1.69 (1.19)	1.72 (1.24)	2.03 (1.35)	0.677 (0.48)	0.706 (0.48)	1.72 (1.03)
$V_{\rm Csp}$ ($V_{\rm Csr}$) (V)	*Mod-1*	352.73 (249.41)	357.00 (253)	350.00 (247.00)	352.73 (249.41)	359.13 (254.10)	337.00 (246.00)	176.36 (124.71)	176.30 (123.98)	200.00 (139.00)	176.36 (124.71)	177.84 (125.68)	219.00 (148.00)	70.65 (49.95)	70.87 (49.98)	119.00 (83.00)
	Mod-2	352.73 (249.41)	357.00 (253.00)	337.00 (246.00)	352.73 (249.41)	359.60 (254.80)	344.00 (244.00)	176.36 (124.71)	177.30 (126.34)	194.00 (137.00)	176.36 (124.71)	179.06 (126.54)	206.00 (139.00)	70.65 (49.95)	72.76 (51.27)	119.00 (82.50)
$I_{\rm Lab(p)}$ (mA)	*Mod-1*	11.96	12.4	-	11.96	12.37	-	11.96	12.15	-	11.96	12.29	-	11.96	12.29	-
	Mod-2	11.96	12.4	-	11.96	12.15	-	11.96	12.15	-	11.96	12.26	-	11.96	12.29	-

Note: All switches S_1-S_6 are in ZVS for both modules for all the cases shown above.

TABLE III
POWER LOSS BREAK-DOWN OF THE CONVERTER

Case	Inverter (MOSFET) Losses			Rectifier Conduction Losses (W)		Transformer + Q Loss (W) (Assumed 1%)	Total Losses (W)	Efficiency (%)
	Turn-off (W)	Conduction (W)	Diode (W)	Output	Boost			
Case-1: $V_{\rm in} = 50$ V, Full-load	3.12	12.21	2.64	7.89	16.08	12	53.94	91.75
Case-2: $V_{\rm in} = 100$ V, Full-load	1.53	6.03	2.64	7.89	8.04	12	38.13	94.02
Case-3: $V_{\rm in} = 50$ V, Half-load	0.60	3.20	0.20	3.94	8.04	6	21.98	93.17
Case-4: $V_{\rm in} = 100$ V, Half-load	0.26	1.60	0.20	3.94	4.02	6	16.02	94.93
Case-5: $V_{\rm in} = 50$ V, 20% load	0.07	0.51	0.30	1.57	3.21	2.4	8.06	93.70

also observed from Fig. 8(a) and (b) that for increasing Q, the kVA/kW rating of the tank circuit increases. Hence, $Q = 4$ is chosen as a reasonable compromise. In Figs. 8(a) and (b), it can be seen that the kVA/kW rating of the tank circuit is minimum for $F = 1$. However, to give a margin for the current to lag in order to achieve ZVS, a minimum value of $F = 1.1$ is chosen. For the chosen values of $Q = 4$ and $F = 1.1$, it can be observed from Fig. 8(a) and (b) that the kVA/kW rating of the tank circuit is lower for lower value of the inductor ratio. Hence, the inductor ratio of $L_{\rm s}/L_{\rm p} = 0.1$ is chosen. From Fig. 8(d), it can be seen that for the chosen optimum values of Q, F, and $L_{\rm s}/L_{\rm p}$, the sign of $i_{\rm Ls0}$ is negative for the entire load variation, this indicates lagging pf operation of the tank circuit. The criterion for choosing $V_{\rm bus}$ is that $V_{\rm bus} > V_{\rm in}(\min)$ (5). The upper limit on $V_{\rm bus}$ can be decided based on the available voltage ratings of the switching devices. Based on this criterion, $V_{\rm bus} = 150$ V was chosen. This value is used in the design along with $V_{\rm in}(\min) = 50$ V. For full-load, as $V_{\rm in}$ is varied from minimum to maximum, while regulating $V_{\rm o}$, the $V_{\rm bus}$ remains constant at the chosen value of 150 V. However, when the load is changed, $V_{\rm bus}$ happens to go below 150 V to keep $V_{\rm o}$ constant. Since the objective of the converter is to keep $V_{\rm o}$ constant, the fall in the intermediary $V_{\rm bus}$ when the load is changed is insignificant. From Fig. 8(c), for the chosen values of $F = 1.1$, $Q = 4$, and $L_{\rm s}/L_{\rm p} = 0.1$, the converter gain $M = 0.6186$ p.u. The output voltage when reflected on primary side of the HF transformer is $V'_{\rm o} = 92.79$ V. Therefore, the HF transformer turns ratio, $n_{\rm t} = 2.0476$. $R_{\rm L} = V^2{}_{\rm o}/(P_{\rm o}/2) = 120.33\ \Omega$. Since each module equally shares the load, the power output is taken as $P_{\rm o}/2 = 300$ W. The load resistance referred to primary side, $R'_{\rm L} = 28.7\ \Omega$. Tank circuit elements $L_{\rm s}$ and $C_{\rm s}$ are obtained by solving (26) as: $L_{\rm s} = 200.98\ \mu$H and $C_{\rm s} = 15.25$ nF. Since $L_{\rm s}/L_{\rm p} = 0.1$, $L_{\rm p} = 2.1$ mH on the primary side. Therefore, the actual value of $L'_{\rm p}$, connected in each phase on the secondary side of three-phase HF transformer is $L'_{\rm p} = n_{\rm t}^2 L_{\rm p} = 8.4264$ mH. The equivalent impedance using (27)–(32) is $Z_{\rm AB} = 17.45 + {\rm j}22.16\ \Omega$, $|Z_{AB}| = 28.21\ \Omega$, and $\phi = 51.78°$. The peak current through the tank circuit elements $L_{\rm s}$ and $C_{\rm s}$ using (34) is $I_{\rm Lsp} = 3.38$ A. The peak voltage across

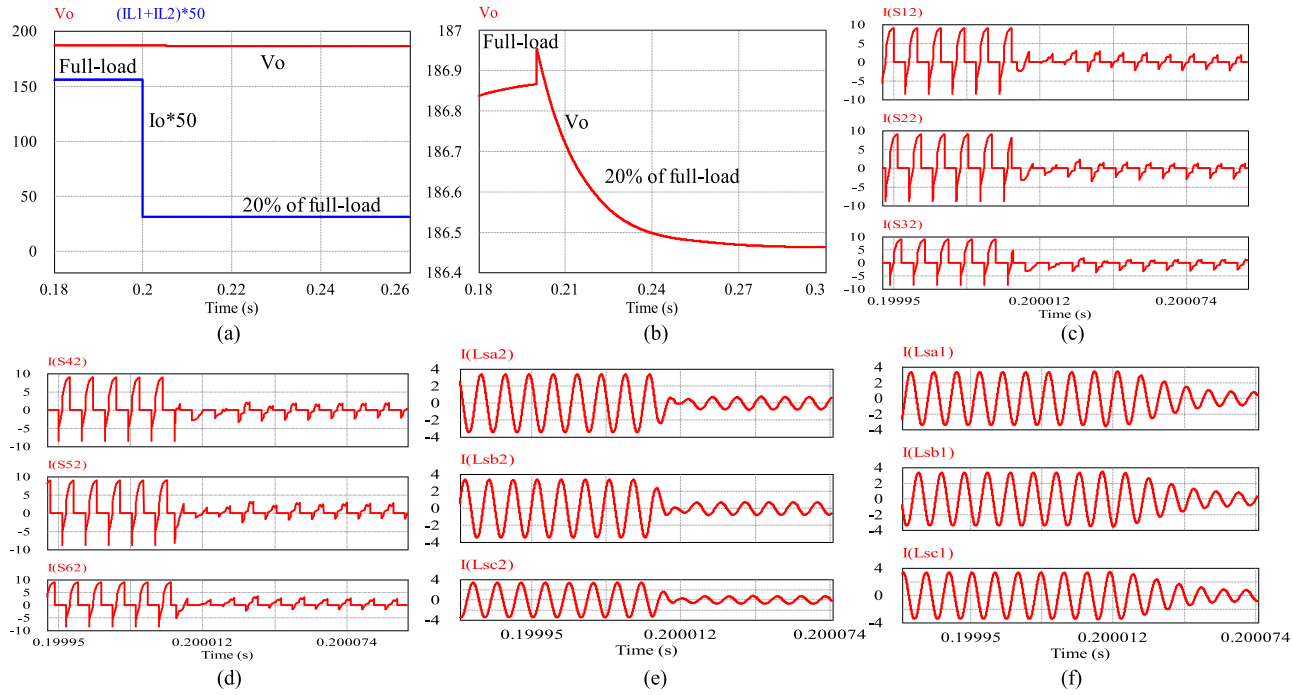

Fig. 12. Simulation waveforms with $V_{\rm in}({\rm min}) = 50$ V for step changes in load current from full-load ($R_{\rm L} = 60\ \Omega$, $\delta = 180°$) to 20% of full-load ($R_{\rm L} = 300\ \Omega$, $\delta = 84°$) at $t = 0.2$ sec: (a) output voltage ($v_{\rm o}$), and the load current ($i_{\rm o}$); (b) expanded waveform of output voltage; (c) switch currents ($i_{\rm s1}$, $i_{\rm s2}$, $i_{\rm s3}$) of module-2; (d) switch currents ($i_{\rm s4}$, $i_{\rm s5}$, $i_{\rm s6}$) of module-2; (e) resonant tank currents ($i_{\rm Lsa}$, $i_{\rm Lsb}$, $i_{\rm Lsc}$) in phases A, B, and C of module-2;, and (f) resonant tank currents ($i_{\rm Lsa}$, $i_{\rm Lsb}$, $i_{\rm Lsc}$) in phases A, B, and C of module-1.

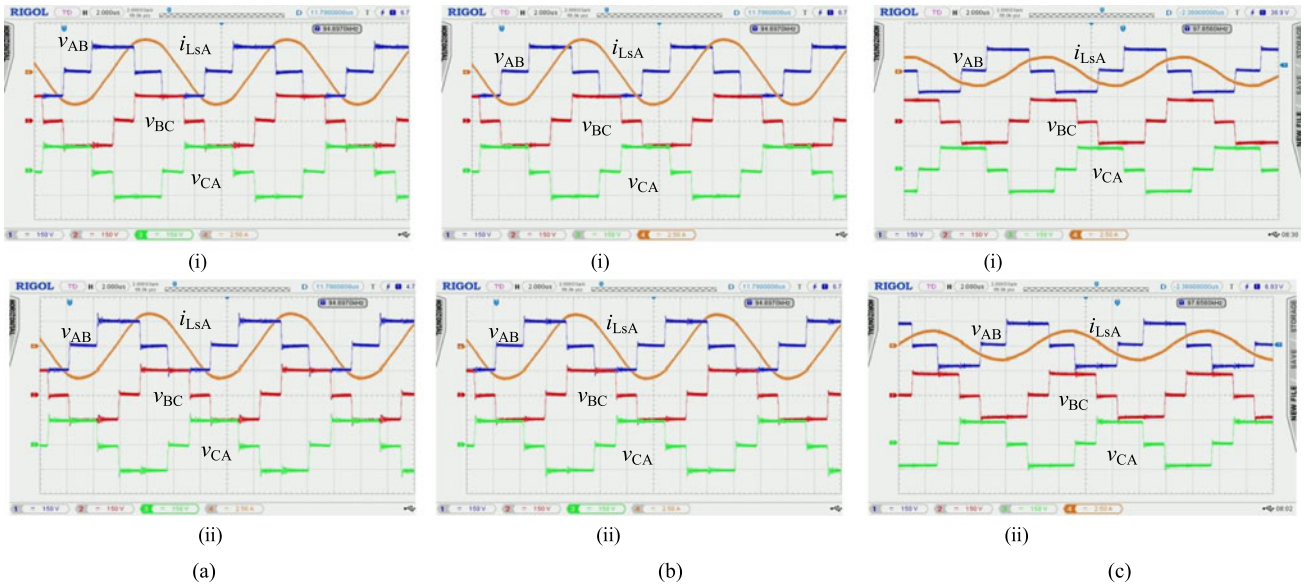

Fig. 13. Experimental waveforms of the voltage across inverter output terminals ($v_{\rm AB}$, $v_{\rm BC}$, $v_{\rm CA}$, 150 V/div.) and current through phase A of the tank circuit ($i_{\rm LsA}$, 2.5 A/div.) for: (a) case-1: $V_{\rm in}({\rm min}) = 50$ V, full-load, $R_{\rm L} = 60\ \Omega$, $\delta = 174°$; (b) case-2: $V_{\rm in}({\rm max}) = 100$ V, full-load, $R_{\rm L} = 60\ \Omega$, $\delta = 57°$; and (c) case-5: $V_{\rm in}({\rm min}) = 50$ V, 20% of full-load, $R_{\rm L} = 300\ \Omega$, $\delta = 84°$: (i) module-1, and (ii) module-2. Time scale: 2 μs/div.

C_s using (35), $V_{\rm Csp} = 352.73$ V. The peak current through Wye connected parallel inductors $L'_{\rm p}$ on secondary side is $I_{\rm L'p,p} = 20.71$ mA. If the parallel inductors are connected in Δ, then the peak current through the Δ connected inductors $L_{\rm ab}$, $L_{\rm bc}$, $L_{\rm ca}$ (on secondary side) is $I_{\rm Lab,p} = 11.96$ mA. The value of the initial tank current using (37), i.e., $i_{\rm Ls0} = -2.655$ A. The negative sign of $i_{\rm Ls0}$ indicates that the tank circuit is operating in lagging pf mode. The boost transformer turns ratio using (5) is $n_{\rm b} = 3$. The per-phase inductance in the primary windings of the three-phase boost transformer calculated using (6) is 4.95 μH. The $L_{\rm f}$ and $C_{\rm f}$ filter components of the three-phase boost rectifier determined are [35]: $L_{\rm f} = 4.83\ \mu$H and $C_{\rm f} = 0.474\ \mu$F. A snubber capacitance of $C_{\rm n} = 443.33$ pF was calculated. The calculated device ratings are [35]: MOSFET: $I_{\rm sw}({\rm rms}) = 3.83$ A, $I_{\rm sw}({\rm av}) =$

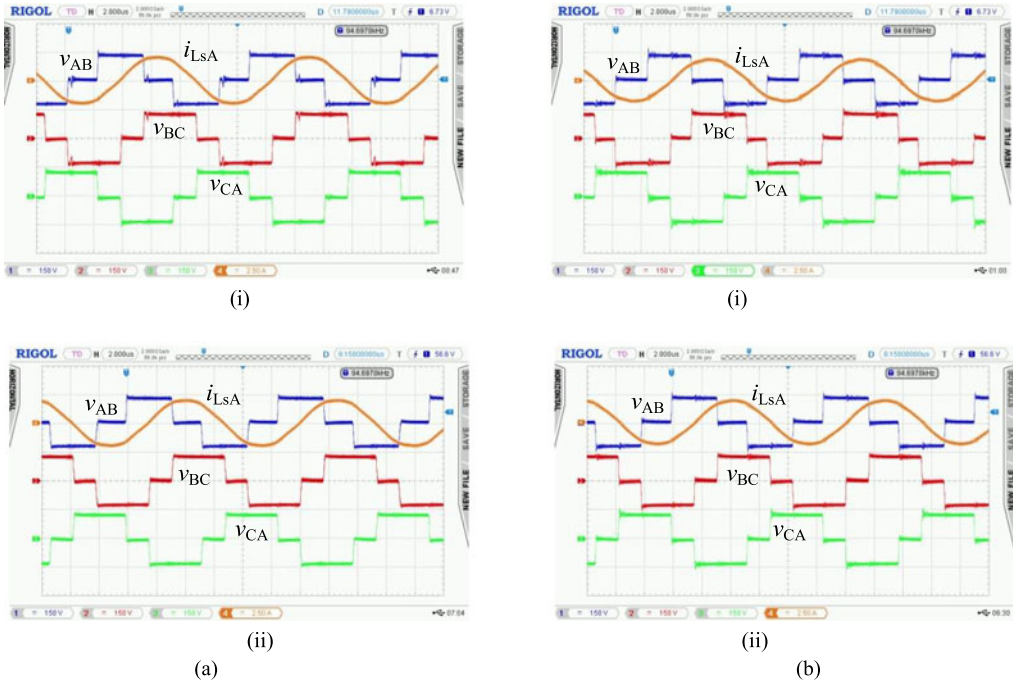

Fig. 14. Experimental waveforms of the voltage across inverter output terminals (v_{AB}, v_{BC}, v_{CA}, 150 V/div.) and current through phase A of the tank circuit (i_{LsA}, 2.5 A/div.) for: (a) case-3: $V_{in}(\min) = 50$ V, half-load, $R_L = 120\ \Omega$, $\delta = 108°$; (b) case-4:$V_{in}(\max) = 100$ V, half-load, $R_L = 120\ \Omega$, $\delta = 34°$: (i) module-1, and (ii) module-2. Time scale: 2 μs/div.

2.2 A, $V_{DS}(\max) = 150$ V, and $I_{DM}(\text{av}) = 0.2$ A; Boost rectifier diodes: $I_{Db}(\text{av}) = 4.515$ A and $V_{Db}(\max) = 100$ V.

V. Simulation Results

A. Steady-State Conditions

Detailed PSIM simulation of the converter designed in Section IV is carried out to verify its performance under steady-state conditions. The following five different cases have been considered for thorough validation of theoretical results [35]. Case-1: $V_{in}(\min) = 50$ V, full-load; Case-2: $V_{in}(\max) = 100$ V, full-load; Case-3: $V_{in}(\min) = 50$ V, half-load; Case-4: $V_{in}(\max) = 100$ V, half-load; Case-5: $V_{in}(\min) = 50$ V, 20% of full-load. The simulation waveforms of cases 1–4 are presented in Figs. 9 and 10. It can be observed from simulation results that all the switches in both modules 1 and 2 operate with ZVS for the entire input voltage variation from $V_{in}(\min)$ to $V_{in}(\max)$ and for the load variation from full-load to 20% of full-load (see Fig. 10). The per-phase peak inverter output current decreases from approximately: 1) Module-1: 3.41 A at $V_{in}(\max) = 100$ V, full-load [see Fig. 9(d)] to 0.689 A at $V_{in}(\min) = 50$ V, 20% of full-load, 2) Module-2: 3.42 A at $V_{in}(\max) = 100$ V, full-load [see Fig. 9(e)] to 0.706 A at $V_{in}(\min) = 50$ V, 20% of full-load. The peak values of the switch currents reduce as the load is reduced. For Module-1: the peak switch current decreases approximately from 9.033 A at $V_{in}(\min) = 50$ V, full-load [see Fig. 10(a)] to 2.39 A at $V_{in}(\min) = 50$ V, 20% of full-load [see Fig. 10(c)]. For Module-2: the peak switch current decreases approximately from 9.038 A at $V_{in}(\min) = 50$ V, full-load [see Fig. 10(a)] to 2.06 A at $V_{in}(\min) = 50$ V, 20% of full-load [see Fig. 10(c)]. It is worth noting here that the peak inverter output currents reduce with the load. A comparison of results obtained from calculations, simulations, and from the experiment is presented in Table II. The results of power loss breakdown analysis of the converter are presented in Table III. Variation of converter efficiency from calculations, simulations, and from experiment is shown in Fig. 11. While comparing the results presented in Table II and in Fig. 11, it is to be noted that in the simulation circuit $R_{DS} = 69\ \text{m}\Omega$ was set for the MOSFETs while all other elements remained ideal. Hence, the efficiency values obtained from simulations are higher than that from the calculations and experiments.

B. Simulation for Step-Changes in Load

The ability of the converter to maintain constant output voltage under transient loading conditions has been simulated using PSIM software. The step change in load from full-load to half-load and then to 20% of full-load was created by operating a load control switch. The phase-shifted gating signals with appropriate phase-shift angle (δ) as given in Table II for corresponding step-changes in load were applied to MOSFETs of module-2. Some of the important sample waveforms obtained through simulations for the step changes in load current from full-load to 20% of full-load (step change given at $t = 0.2$ s, after the steady-state operation at full-load) are presented in Fig. 12. It is observed from Fig. 12(a) and (b) that there is a smooth transition of the output voltage during the step-change in the load while maintaining the output voltage constant at the full-load value. It is also observed from Fig. 12(c) and (d) that the current through the switches does not spike up during the sudden changes in the loading conditions. From Fig. 12(e) and (f) it can be seen that the resonant tank current remains sinusoidal throughout the

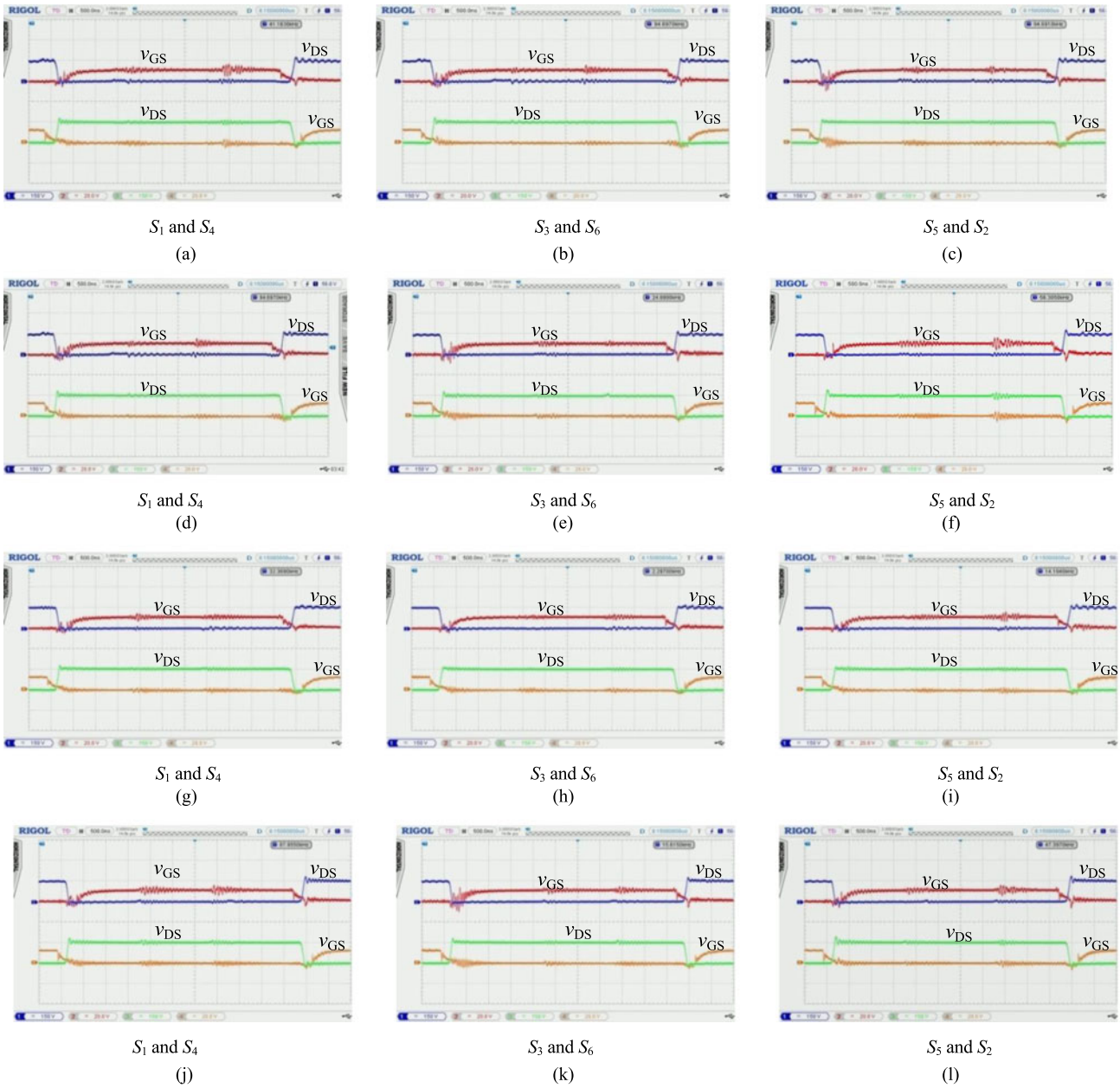

Fig. 15. Experimental waveforms of the voltage across switches (v_{DS}, 150 V/div.) and the gating signals (v_{GS}, 20 V/div.) for respective switches of same leg to demonstrate ZVS for**:** case-1: $V_{\mathrm{in}}(\mathrm{min}) = 50$ V, full-load, $R_{\mathrm{L}} = 60\ \Omega$, $\delta = 174°$: (a)–(c) module-1, and (d)–(f) module-2, case-2: $V_{\mathrm{in}}(\mathrm{max}) = 100$ V, full-load, $R_{\mathrm{L}} = 60\ \Omega$, $\delta = 57°$: (g)–(i) module-1, and (j)–(l) module-2. Time scale: 500 ns/div.

loading conditions. It is also worth noting that all the switches in both the modules remain in ZVS for sudden changes in the loading conditions, e.g., Fig. 12(c) and (d).

VI. Experimental Results

Experimental model of the converter designed in Section IV was built in the laboratory. Rigorous testing of the built converter has been done to verify theoretical predictions in terms of operation and performance by testing the converter for five different cases as mentioned in Section V. Each three-phase HF transformer was built by using two EI-type cores (PC40 EI 60-z). The per-phase leakage (L_l) and the magnetizing (L_{m}) inductances referred to the primary side of the built transformers measured were: 1) Boost transformer: $L_l = 5.0\ \mu$H and $L_{\mathrm{m}} = 170\ \mu$H; 2) Main transformers, T_1: $L_l = 1.0\ \mu$H and $L_{\mathrm{m}} = 45.83\ \mu$H, and T_2:$L_{\mathrm{l}} = 1.4\ \mu$H, and $L_{\mathrm{m}} = 35.46\ \mu$H. The turns ratio of the three-phase boost transformer was reduced to 11:4 instead of 12:4 to compensate for the voltage drop due to leakage inductance. No external L_{p} was used as L_{m} was less than L_{p}. A snubber capacitance of 220 pF was connected externally in addition to the MOSFETs output capacitance of 265 pF. The resonant inductors (built using Iron powder toroidal cores, approximately 200 μH per phase) and the capacitors (WIMA MKP10 Polypropylene film, 16.5 nF per phase) for both modules were used in the laboratory. The switching frequency was

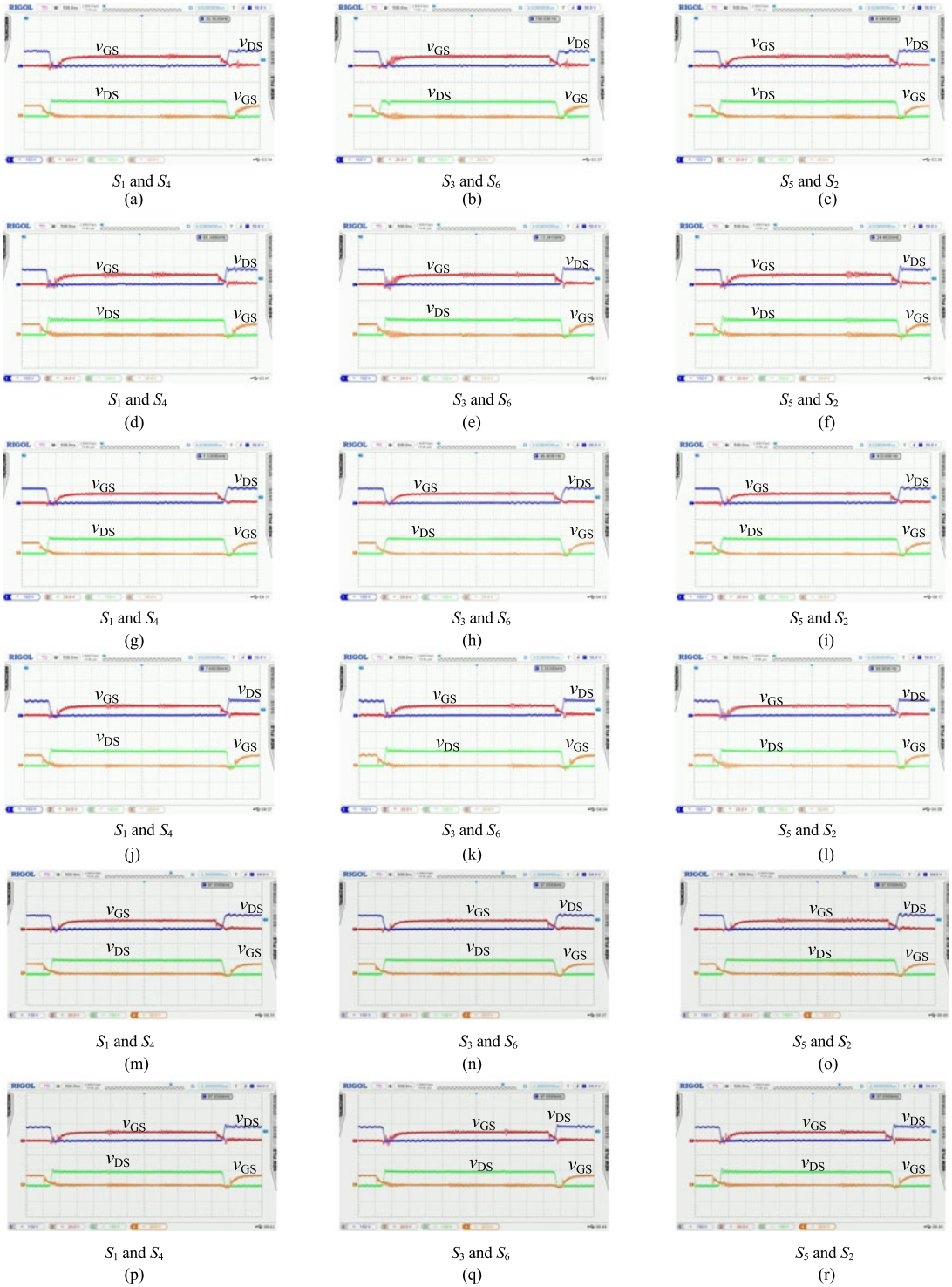

Fig. 16. Experimental waveforms of the voltage across switches (v_{DS}, 150 V/div.) and the gating signals (v_{GS}, 20 V/div.) for respective switches of same leg to demonstrate ZVS for: case-3: $V_{\mathrm{in}}(\min) = 50$ V, half-load, $R_{\mathrm{L}} = 120\ \Omega$, $\delta = 108°$: (a)–(c) module-1, and (d)–(f) module-2, case-4: $V_{\mathrm{in}}(\max) = 100$ V, half-load, $R_{\mathrm{L}} = 120\ \Omega$, $\delta = 34°$: (g)–(i) module-1, and (j)–(l) module-2, case-5: $V_{\mathrm{in}}(\min) = 50$ V, 20% of full-load, $R_{\mathrm{L}} = 300\ \Omega$, $\delta = 84°$: (m)–(o) Module-1, and (p)–(r) Module-2, Time scale: 500ns/div.

reduced to 95 kHz to compensate for the difference in the built tank circuit elements from the designed values. Gating signals were generated by XILINX Spartan-3E FPGA board using VHDL code. Following devices were used in the experiment: MOSFET (IRFB4137), output rectifier diodes (MUR460), and boost rectifier diodes (60CPQ150). The experimental waveforms of all the five cases are presented in Figs. 13 to 17. Following observations are made from the experimental results [35]: 1) In Figs. 15 and 16, the waveforms of gating signals and the voltage across switch for respective switches of same leg are displayed to confirm ZVS operation of the switches. It is found that all the switches in both modules turn-on with

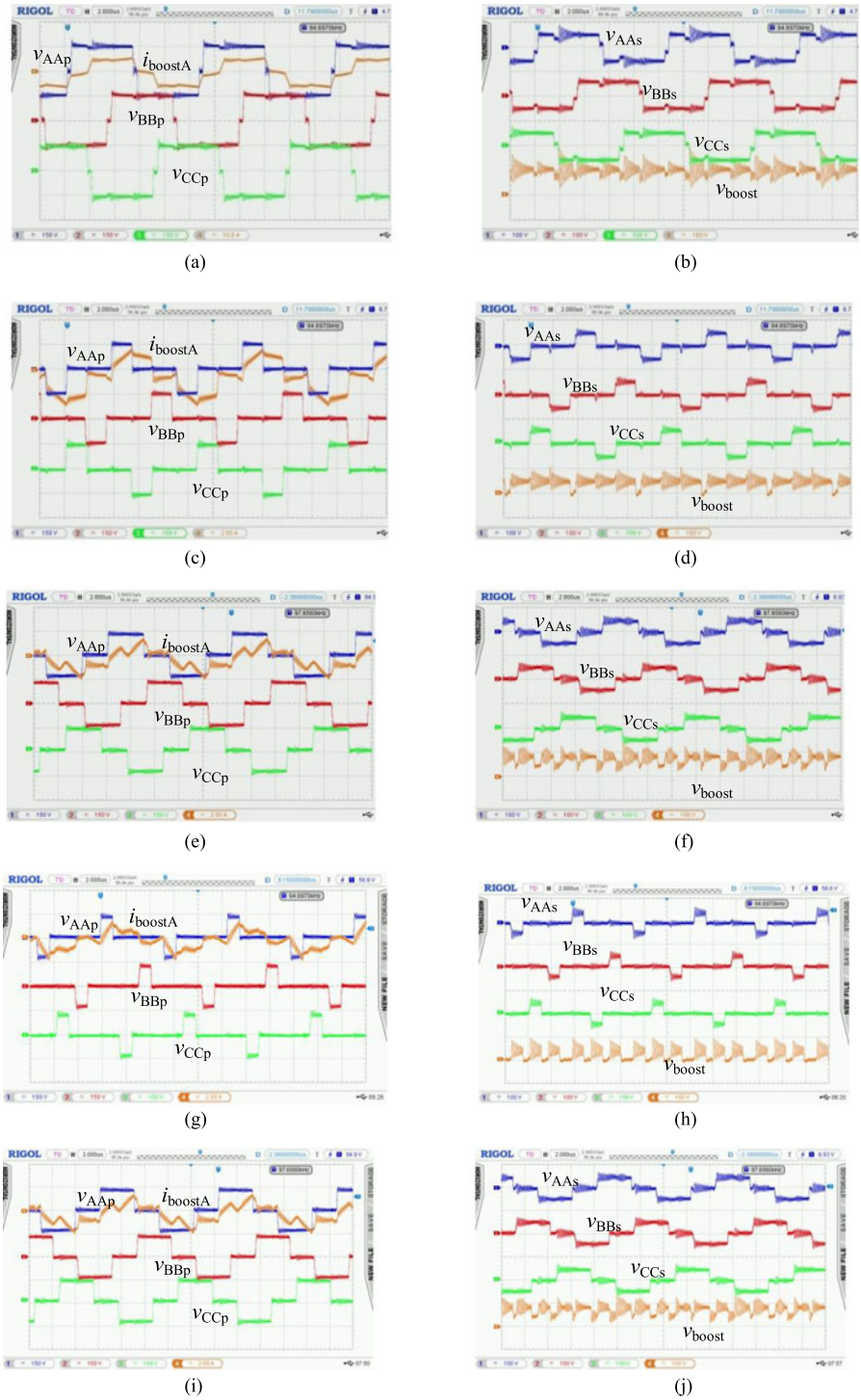

Fig. 17. Experimental waveforms of the 3-ϕ boost transformer, T_3: (a) phase voltages across the primary windings (v_{AAp}, v_{BBp}, v_{CCp}, 150 V/div.) and the current through phase A (i_{boostA}); (b) phase voltages across the secondary terminals (v_{AAs}, v_{BBs}, v_{CCs}, 100 V/div.) and the boost rectifier output voltage before filtering (v_{boost}, 100 V/div.) for case-1: $V_{\mathrm{in(min)}} = 50$ V, full-load, $R_{\mathrm{L}} = 60\ \Omega$, $\delta = 174°$. Waveforms of (a)–(b) repeated, (c)–(d) for case-2: $V_{\mathrm{in}}(\mathrm{max}) = 100$ V, full-load, $R_{\mathrm{L}} = 60\ \Omega$, $\delta = 57°$; (e)–(f) for case-3: $V_{\mathrm{in}}(\mathrm{min}) = 50$ V, half-load, $R_{\mathrm{L}} = 120\ \Omega$, $\delta = 108°$; (g)–(h) for case-4: $V_{\mathrm{in}}(\mathrm{max}) = 100$ V, half-load, $R_{\mathrm{L}} = 120\ \Omega$, $\delta = 34°$; and (i)–(j) for case-5: $V_{\mathrm{in}}(\mathrm{min}) = 50$ V, 20% of full-load, $R_{\mathrm{L}} = 300\ \Omega$, $\delta = 84°$. Time scale: 2 μs/div.

ZVS for the entire input voltage range and the load variation from full-load to 20% of full-load (see Figs. 15 and 16). It can also be verified that the resonant current through phase-A (see Figs. 13 and 14) and the boost transformer primary current in phase-A (see Fig. 17) lag the respective voltages to confirm the lagging pf operation of the converter as designed in Section IV by choosing $F = 1.1$; 2) peak resonant current decreases as the load is reduced. For example, for both modules from 3.44 A in case-1[see Fig. 13(a)(i–ii)] to 1.64 A in case-5 [see Fig. 13(c)(i–ii)]; 3) boost transformer primary current lags the

voltage across it [see Fig. 17(a), (c), (e), (g), and (i)]; 4) output voltage of the boost rectifier $v_{\rm boost}$ follows the theoretical predictions in [see Fig. 17 (b), (d), (f), (h), and (j)]. In Fig. 17(b) for case-1 ($V_{\rm in} = 50$ V, full-load, $\delta = 174°$), $v_{\rm boost}$ remains approximately constant at $2V_{\rm bus}/{\rm n_b}$ confirming the operation in mode-1. For case-5 ($V_{\rm in} = 50$ V, half-load, $\delta = 108°$), the $v_{\rm boost}$ comprises of pulses of heights approximately equal to $2V_{\rm bus}/{\rm n_b}$ and $V_{\rm bus}/{\rm n_b}$ [see Fig. 17(f) and (j)], confirming the operation in mode-2 [35]. For case-2 ($V_{\rm in} = 100$ V, full-load, $\delta = 57°$), the $v_{\rm boost}$ comprises of pulses of heights approximately equal to $V_{\rm bus}/{\rm n_b}$ and zero [see Fig. 17(d) and (h))], confirming the operation in mode-3 [35].

VII. Conclusion

A three-phase fixed-frequency controlled integrated boost dual three-phase bridge dc–dc LCL-type SRC for medium to large power applications has been proposed. The operation and analysis of the proposed converter is done in two parts: 1) The boost transformer and rectifier section has been modeled in detail and the operation in different modes is explained. 2) The LCL converter section has been analyzed using the known approximate complex ac circuit analysis method and used in the design. Various design curves are drawn and used in selecting the optimum design parameters. PSIM simulation for verifying the performance of the proposed converter has been carried out for the variations in the input voltage and the load. The theoretical and simulation results are verified by building an experimental model of the converter. The proposed converter maintains ZVS for all the switches for wide variations in input voltage and load that will be useful in alternate energy applications. The specifications of the prototype were chosen only as an example to illustrate the design procedure of the proposed converter and also to build the experiment converter in the lab. The input voltage of 50–100-V dc (1:2 variations) is considered as the voltage obtained from distributed generation (e.g., sea wave energy, photovoltaics, wind energy, etc.) in general. However, the converter can be designed typically to higher input dc voltages in the ratio 1:2 depending on the ratings of the dc bus supplying the inverter modules and that of the available switching devices. With the recent availability of SiC MOSFETs, the proposed converter can be designed for still higher input voltages varying in the ratio of 1:2 while higher efficiency can be achieved. The effect of thermal distribution on the performance of the converter, the small signal analysis and detailed transient response needs to be studied.

Appendix

The expression for the equivalent resistance $R_{\rm ac}$ shown in Fig. 4, which replaces the rectifier-filter-load block of module-1 in Fig. 1 after referring to primary side, is obtained by following the steps given in [21]. $V_{\rm Lp1}$ is the rms value of the fundamental component of the square–wave voltage across inductor $L_{\rm p}$, and $I_{\rm rect\_in,a}$ is the rms value of the sinusoidal current input to the rectifier, as indicated in the phasor equivalent circuit of Fig. 4. Some of the important expressions are as follows:

$$V_{\rm Lp1} = \left(\sqrt{2}/\pi\right) V_o' \tag{17}$$

$$I_{\rm rect\_in,a} = \left(\pi/3\sqrt{2}\right) I_o'. \tag{18}$$

The equivalent resistance $R_{\rm ac}$ to replace the rectifier-filter-load block is obtained using (17) and (18) as

$$R_{\rm ac} = V_{\rm Lp1}/I_{\rm rect\_in,a} = \left(6/\pi^2\right)\ R_{\rm L}' \tag{19}$$

where,

$$R_{\rm L}' = R_L/n_t^2 \tag{20}$$

i.e., the load resistance referred to primary side of the transformer of ($n_{\rm t}$:1) turns ratio.

A1.1 *Analysis—Derivation of converter gain (M), and Component stresses:*

Based on the phasor equivalent circuit shown in Fig. 4, the r.m.s. value of the fundamental component of the per-phase output voltage of the inverter across terminals AN can be expressed as

$$V_{\rm AN1} = \left(\sqrt{2}/\pi\right) V_{\rm bus}. \tag{21}$$

From (17) and (18),

$$\left|\bar{\rm V}_{\rm Lp1}/\bar{\rm V}_{\rm AN1}\right| = \left({\rm V'_o}/{\rm V_{bus}}\right). \tag{22}$$

Referring to Fig. 4, the following can be obtained:

$$\frac{\bar{V}_{\rm Lp1}}{\bar{V}_{\rm AN1}} = \frac{1}{\left[\left(1 + \frac{X_{\rm Ls}}{X_{\rm Lp}} + \frac{X_{\rm Cs}}{X_{\rm Lp}}\right) + \left(\frac{{\rm j}X_{\rm Ls}}{R_{ac}}\right) + \left(\frac{{\rm j}X_{\rm Cs}}{R_{ac}}\right)\right]}. \tag{23}$$

Further simplification of (23) results in:

$$\left|\bar{V}_{\rm Lp1}/\bar{V}_{\rm AN1}\right| = \frac{1}{\left[\left\{1 + \frac{L_s}{L_P}\left(1 - \frac{1}{F^2}\right)\right\}^2 + \left\{\frac{\pi^2 Q}{6}\left(F - \frac{1}{F}\right)\right\}^2\right]^{1/2}}. \tag{24}$$

Therefore from (22) and (24), the converter gain

$$V_{\rm o}'/V_{\rm bus} = M = \frac{1}{\left[\left\{1 + \frac{L_s}{L_P}\left(1 - \frac{1}{F^2}\right)\right\}^2 + \left\{\frac{\pi^2 Q}{6}\left(F - \frac{1}{F}\right)\right\}^2\right]^{1/2}} \tag{25}$$

where

$$Q = \omega_{\rm r} L_{\rm s}/R'_{\rm L}; F = \omega_{\rm s}/\omega_{\rm r} = f_{\rm s}/f_{\rm r};\ \omega_{\rm s} = 2\pi f_{\rm s}$$

$$\omega_{\rm r} = 2\pi f_{\rm r} = 1/\sqrt{L_{\rm s}C_{\rm s}} \tag{26}$$

$f_{\rm s}$ = switching frequency, $f_{\rm r}$ = resonant frequency, both in hertz.

The equivalent impedance $Z_{\rm AN}$ across AN in Fig. 4 is given by

$$Z_{\rm AN} = R_{\rm AN} + j\ X_{\rm AN} \tag{27}$$

$$|\ Z_{\rm AN}| = \left[R_{\rm AN}^2 + X_{\rm AN}^2\right]^{1/2} \tag{28}$$

$$\Phi = \tan^{-1}\left(\frac{X_{\rm AN}}{R_{\rm AN}}\right) \tag{29}$$

where

$$R_{\mathrm{AN}} = \left(\frac{R_{\mathrm{ac}} X_{\mathrm{LP}}^2}{R_{\mathrm{ac}}^2 + X^2{}_{\mathrm{Lp}}}\right) \tag{30}$$

$$X_{\mathrm{AN}} = \left[(X_{\mathrm{Ls}} + X_{\mathrm{Cs}}) + \left(\frac{R_{\mathrm{ac}}^2 X_{\mathrm{Lp}}}{R_{\mathrm{ac}}^2 + X_{\mathrm{Lp}}^2}\right)\right] \tag{31}$$

$$X_{\mathrm{Ls}} = \omega_{\mathrm{s}} L_{\mathrm{s}};\ X_{\mathrm{Lp}} = \omega_{\mathrm{s}} L_{\mathrm{p}};\ X_{\mathrm{Cs}} = -1/(\omega_{\mathrm{s}} C_{\mathrm{s}}). \tag{32}$$

The expression for current through phase A of the resonant circuit (i.e., the inverter output current in phase-A) is

$$i_{\mathrm{Ls}} = I_{\mathrm{Lsp}} \sin(\omega t - \Phi). \tag{33}$$

The peak inverter output current/peak current through tank circuit elements L_{s} and C_{s} in phase A, peak voltage across the capacitor C_{s}, and the peak current through the parallel inductor L_{p} (on primary side) are given by

$$I_{\mathrm{Lsp}} = V_{\mathrm{AN1}}(\mathrm{peak}) / |Z_{\mathrm{AN}}| \tag{34}$$

$$V_{\mathrm{Csp}} = I_{\mathrm{Lsp}}\, X_{\mathrm{Cs}} \tag{35}$$

$$I_{\mathrm{Lpp}} = I_{\mathrm{La'Np}} = V_{\mathrm{La'Np}}/X_{\mathrm{La'N}} = V_{\mathrm{La'N}}(\mathrm{peak}) / (X_{\mathrm{Lp}}). \tag{36}$$

The value of the initial inverter output current i_{Ls0} (referring to Fig. 2, i.e., i_{Ls} at $\omega t = 0$ in (33)) is given by

$$i_{\mathrm{Ls0}} = I_{\mathrm{Lsp}} \sin(-\Phi). \tag{37}$$

REFERENCES

[1] H. Nagendrappa and A. K. S. Bhat, "A fixed frequency LCL-type series resonant converter with capacitive output filter using a modified gating scheme," in *Proc. IEEE 10th Int. Conf. Power Electron. Drive Syst.*, 2013, pp. 175–180.

[2] A. K. S. Bhat, "Analysis and design of LCL-type resonant converter," *IEEE Trans. Ind. Electron.*, vol. 41, no. 1, pp. 118–124, Feb. 1994.

[3] R. L. Steigerwald, "A comparison of half-bridge resonant converter topologies," *IEEE Trans. Power Electron.*, vol. 3, no. 2, pp. 174–1182, Apr. 1988.

[4] J. Abu-Qahouq and I. Batarseh, "Unified steady-state analysis of soft-switching dc-dc converters," *IEEE Trans. Power Electron.*, vol. 17, no. 5, pp. 684–691, Sep. 2002.

[5] H. A. Kojori, J. D. Lavers, and S. B. Dewan, "Steady-state analysis and design of an inductor-transformer resonant dc-dc converter," *IEEE Trans. Ind. Appl.*, vol. 27, no. 3, pp. 515–522, May 1991.

[6] R. Severns, "Topologies for three element resonant converters," in *Proc. IEEE Applied Power Electron. Conf. Expo.*, 1990, pp. 712–722.

[7] A. K. S. Bhat, "Analysis and design of a fixed-frequency LCL-type series-resonant converter with capacitive output filter," *IEE Trans. Circuits Devices Syst.*, vol. 144, no. 2, pp. 97–103, Apr. 1997.

[8] S. Bronstein and S. Ben-Yaakov, "Approximate analysis of the resonant LCL dc-dc converter," in *Proc. IEEE Elect. Electron. Eng. Israel Conv.*, 2004, pp. 44–47.

[9] F. Musavi, M. Craciun, D. S. Gautam, W. Eberle, and W. G. Dunford, "An LLC resonant DC–DC converter for wide output voltage range battery charging applications," *IEEE Trans. Power Electron.*, vol. 28, no. 12, pp. 5437–5445, Dec. 2013.

[10] W. C. Hsu, J. F. Chen, Y. M. Wu, and Y. P. Hsieh, "Design and steady state analysis of parallel resonant dc-dc converter for HV power generator," *IEEE Trans. Power Electron.*, vol. 32, no. 2, pp. 957–86, Feb. 2017.

[11] Y. K. Lo, C. Y. Lin, M. T. Hsieh, and C. Y. Lin, "Phase-shifted full-bridge series-resonant DC–DC converters for wide load variations," *IEEE Trans. Ind. Electron.*, vol. 58, no. 6, pp. 2572–2575, Jun. 2011.

[12] Y. W. Cho, W. J. Cha, J. M. Kwon, and B. H. Kwon, "High-efficiency bidirectional DAB inverter using a novel hybrid modulation for stand-alone power generating system with low input voltage," *IEEE Trans. Power Electron.*, vol. 31, no. 6, pp. 4138–4147, Jun. 2016.

[13] B. Gu, C. Y. Lin, B. Chen, J. Dominic, and J. S. Lai, "Zero-voltage-switching PWM resonant full-bridge converter with minimized circulating losses and minimal voltage stresses of bridge rectifiers for electric vehicle battery chargers," *IEEE Trans. Power Electron.*, vol. 28, no. 10, pp. 4657–4667, Oct. 2013.

[14] T. Konjedic *et al.*, "DCM-based zero-voltage switching control of a bidirectional DC–DC converter with variable switching frequency," *IEEE Trans. Power Electron.*, vol. 31, no. 4, pp. 3273–3288, Apr. 2016.

[15] C. Meyer and R. W. De Doncker, "Design of a 3-phase SRC for offshore dc grids," in *Proc. IEEE Ind. App. Annu. Meeting*, 2007, pp. 216–223.

[16] S. Hazra *et al.*, "High switching performance of 1700-V, 50-A SiC power MOSFET over Si IGBT/BiMOSFET for advanced power conversion applications," *IEEE Trans. Power Electron.*, vol. 31, no. 7, pp. 4742–4754, Jul. 2016.

[17] H. Nagendrappa and A. K. S. Bhat, "A fixed frequency ZVS integrated boost dual three-phase bridge dc-dc LCL-type series resonant converter," in *Proc. IEEE Energy Convers. Congr. Expo.*, 2015, pp. 2056–2063.

[18] H. M. de Oliveira Filho, D. de Souza Oliveira, and P. P. Praça, "Steady-state analysis of a ZVS bidirectional isolated three-phase DC–DC converter using dual phase-shift control with variable duty cycle," *IEEE Trans. Power Electron.*, vol. 31, no. 3, pp. 1863–1872, Mar. 2016.

[19] L. Chen, F. Liu, Y. Chen, X. Ruan, and C. Wang, "Three-phase three-level LC-type parallel resonant DC/DC converter with variable frequency control," in *Proc. IEEE Energy Convers. Congr. Expo. Conf.*, 2015, pp. 4271–4276.

[20] C. Liu, A. Johnson, and J-S. Lai, "A novel 3-phase high-power soft-switched dc/dc converter for low-voltage fuel cell applications," *IEEE Trans. Ind. Appl.*, vol. 41, no. 6, pp. 1691–1697, Nov./Dec. 2005.

[21] M. S. Almardy and A. K. S. Bhat, "Three-phase (LC)(L)-type series-resonant converter with capacitive output filter," *IEEE Trans. Power Electron.*, vol. 26, no. 4, pp. 1172–1183, Apr. 2011.

[22] S. Akre, M. Egan, and M. J. Willers, "Practical design methodology for a new three-phase dc-dc fully resonant converter employing LCC-type tank circuit," in *Proc. IEE 8th Int. Conf. Power Electron. Variable Speed Drives*, 2000, pp. 340–345.

[23] A. K. S. Bhat and I. Zheng, "Analysis and design of a 3-phase LCC-type resonant converter," in *Proc. 27th Annu. IEEE Power Electron. Spec. Conf.*, 1996, pp. 252–258.

[24] A. K. S. Bhat and R. L. Zheng, "Analysis and design of a three-phase LCC-type resonant converter," *IEEE Trans. Aerosp. Electron. Syst.*, vol. 34, no. 2, pp. 508–519, Apr. 1998.

[25] S. Akre and M. G. Egan, "Analysis and design of a new three-phase resonant dc-dc converter with a capacitive output filter," in *Proc. 32nd Annu. IEEE Power Electron. Spec. Conf.*, 2001, pp. 277–284.

[26] S. S. Tanavade, H. M. Suryawanshi, and M. P. Bhagat, "A three-phase modified series-parallel resonant converter based UPS-analysis, design, simulation & results," in *Proc. EUROCON: Int. Conf. "Computer as a Tool"*, 2007, pp. 2770–2777.

[27] A. K. S. Bhat and R. L. Zheng, "A three-phase series-parallel resonant converter-analysis, design, simulation, and experimental results," *IEEE Trans. Ind. Appl.*, vol. 32, no. 4, pp. 951–960, Jul./Aug. 1996.

[28] D. Cretu, W. G. Dunford, and M. Edmunds, "A comparison of three-phase resonant and PWM converters for high current, high power applications," in *Proc. IEEE Appl. Power Electron. Conf.*, 1997, pp. 631–637.

[29] A. R. Prasad, P. D. Ziogas, and S. Manias, "Analysis and design of a three-phase offline dc-dc converter with high-frequency isolation," *IEEE Trans. Ind. Appl.*, vol. 28, no. 4, pp. 824–832, Jul./Aug. 1992.

[30] R. L. Steigerwald, R. W. De Doncker, and M. H. Kheraluwala, "A comparison of high power dc-dc soft-switched converter topologies," *IEEE Trans. Ind. App.*, vol. 32, no. 5, pp. 1139–1145, Sep./Oct. 1996.

[31] M. N. Kheraluwala, R. W. Gascoigne, D. M. Divan, and E. D. Baumann, "Performance characterization of a high-power dual active bridge DC-to-DC converter," *IEEE Trans. Ind. Applications*, vol. 28, no. 6, pp. 1294–1301, Nov./Dec. 1992.

[32] R. L. Steigerwald, W. Roshen, and C. F. Saj, "A high-density 1 kW resonant power converter with a transient boost function," *IEEE Trans. Power Electron.*, vol. 8, no. 4, pp.431–438, Oct. 1993.

[33] D. S. Gautam and A. K. S. Bhat, "An integrated boost-dual half-bridge LCL SRC with capacitive output filter for electrolyser application," in *Proc. 38th Annu. Ind. Conf. IEEE Electron. Soc.*, 2012, pp. 3376–3381.

[34] J. A. Sabate, V. Vlatkovic, R. B. Ridley, F. Lee, and B. H. Cho, "Design considerations for high-voltage high-power full-bridge zero-voltage-switched PWM converter," in *Proc. 5th Annu. App. Power Electron. Conf. Expo.*, 1990, pp. 275–284.

[35] H. Nagendrappa, "High-frequency transformer isolated fixed frequency dc-dc resonant power converters for alternative energy applications," Ph.D. thesis, Dept. ECE, Univ. Victoria, Victoria, BC, Canada, Jul. 2015.

Nagendrappa Harischandrappa (S'14–M'16) was born in the village Nakaralathanda, Bellary, India, in 1977. He received the B.E. degree in electrical and electronics engineering, in 1999, the M.Tech. degree in power and energy systems, in 2002, both from the National Institute of Technology Karnataka (NITK), Surathkal, India, and the Ph.D. degree in electrical engineering in 2015 from the University of Victoria, Victoria, BC, Canada.

He was an Assistant Lecturer from 2002 to 2004, and as a Teaching Fellow from 2004 to 2006 both in the Department of Electrical Engineering, NITK Surathkal. For a short period, he was an Assistant Engineer (operation and maintenance) in the power distribution utility called Mangalore Electricity Supply Company Ltd. at Ajjampura, Tarikere, India. Since 2006, he has been an Assistant Professor in the Department of Electrical Engineering, NITK Surathkal. He is interested in working on high-frequency soft-switching converters for power generation from renewable energy sources and their grid interfacing applications.

Ashoka K. S. Bhat (S'82–M'85–SM'87–F'98) received the B.Sc. degree in physics and maths from Mysore University, Mysore, India, in 1972. He received the B.E. degree in electrical technology and electronics and the M.E. degree in electrical engineering, both with distinction from the Indian Institute of Science, Bangalore, India, in 1975 and 1977, respectively. He has also received the M.A.Sc. and Ph.D. degrees in electrical engineering from the University of Toronto, Toronto, ON, Canada, in 1982 and 1985, respectively.

From 1977 to 1981, he was a Scientist in the Power Electronics Group of the National Aeronautical Laboratory, Bangalore, and was responsible for the completion of a number of research and development projects. After working as a Postdoctoral Fellow for a short time, he joined the Department of Electrical Engineering, University of Victoria, Victoria, BC, Canada, in 1985, where he is currently a Professor of electrical engineering and is engaged in teaching and conducting research in the area of power electronics. He was responsible for the development of the electromechanical energy conversion and power electronics courses and laboratories in the Department of Electrical Engineering at the University of Victoria.

Dr. Bhat received the "Excellence in Teaching Award" from the Faculty of Engineering during the year 2008 and the "Wighton Fellowship" for the year 2010. He is a Fellow of the Institution of Electronics and Telecommunication Engineers (India), and a registered Professional Engineer in the province of British Columbia, Canada.