The Optimal PWM Modulation and Commutation Scheme for a Three-Phase Isolated Buck Matrix-Type Rectifier

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***Abstract*—This paper first starts with reviewing several commonly practiced PWM schemes for the three-phase isolated buck matrix-type rectifier. Then, an optimal six-segment PWM scheme ("Type A") is proposed. The analysis shows "Type A" PWM scheme has lower duty-cycle loss, maximum output inductor current ripple, and minimum switching loss comparing with other PWM schemes when the MOSFET devices are employed. In addition, a low input current total harmonic distortion (THD) can be achieved with duty-cycle compensation. Finally, the steady-state analysis of duty-cycle loss, inductor current ripple, and THD are all compared and verified by the experimental results for "Type A" PWM and eight-segment PWM ("Type E").**

***Index Terms*—Phase-shifted full-bridge (FB-PS), space-vector modulation (SVM), zero-voltage switching (ZVS).**

I. Introduction

MATRIX rectifier inherits all the advantages of traditional matrix converters and is considered promising in ac–dc applications, such as front-end power converters for high-voltage direct current (HVDC) and telecommunication. Matrix rectifier is designed based on a three-phase to one-phase matrix converter, which has two main topologies: nonisolated matrix rectifier [1]–[5] and isolated matrix rectifier [6]–[12], [14]–[17]. For applications where the isolation is required, the single-stage isolated matrix-type rectifiers are the most favorable in terms of high power density and high efficiency. These single-stage isolated matrix-type rectifiers can be classified into four major categories in [18, Fig. 1]:

1) quasi single-stage (indirect matrix) buck-derived bridge PWM rectifier;
2) single-stage buck-derived matrix-type (direct matrix) PWM rectifier;

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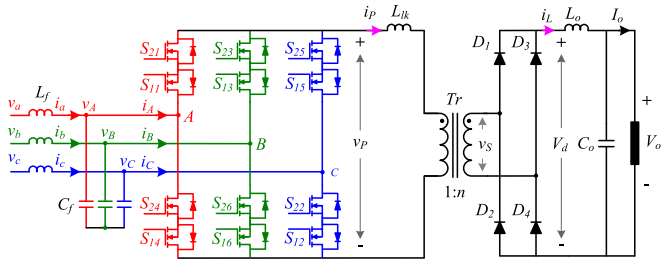

Fig. 1. ZVS three-phase PWM rectifier.

3) quasi-single-stage (indirect matrix) boost-derived bridge PWM rectifier;
4) single-stage boost-derived matrix-type (direct matrix) PWM rectifier.

With them, low total harmonic distortion (THD), power factor correction (PFC), constant power flow, and so minimal filtering component size and cost can be easily achieved. The buck-derived matrix rectifier [6]–[9], [15] can be a choice, especially when the input line voltage is high and so its boost counterpart [18], [19] suffers from high device voltage ratings. The buck-derived matrix-type rectifier is also favorable when the variable output dc voltage is a must, as it is the case for typical telecommunication and HVDC applications where the output is usually connected to a battery bank with large voltage fluctuations. Besides, better dynamic response and no starting problems are among the other advantages of the buck-type topology [20]. A conventional buck-type PFC rectifier in combination with a phase-shift dc/dc converter (indirect matrix) is reported in [15]. However, the conventional buck-type PFC rectifier suffers from high conduction losses in the high-frequency diodes, which are needed in series with the switches [15], [20]. Typically, the single-stage power conversion can be realized with a direct matrix-type rectifier that directly converts the mains-frequency ac voltage into a high-frequency ac voltage which is supplied to a high-frequency isolation transformer and whose secondary voltage is then rectified to the desired dc output voltage [10]. Insulated-gate bipolar transistors (IGBTs) are normally used to realize the bidirectional switches of the matrix converter as reported in the literature [4], [6], [7], [10]–[12], [16]. Compared with MOSFETs, however, the IGBT is a slower device and cannot operate at a higher switching frequency. In addition, the IGBT has a greater conduction loss for medium power. A zero-voltage

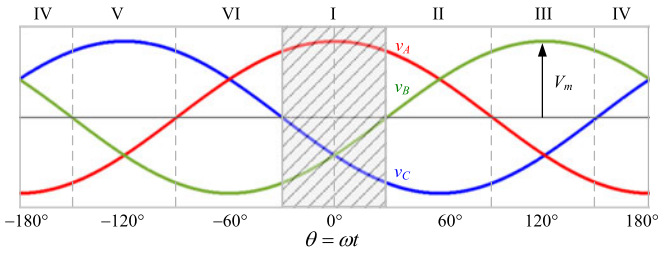

Fig. 2. Input phase voltages.

switched (ZVS) three-phase isolated buck PWM rectifier using MOSFET is proposed in [8] and [9], as shown in Fig. 1. Low switching losses can be achieved due to the ZVS operation with MOSFETs, such that the converter can operate at a higher switching frequency. Within any 60° interval in Fig. 2, the converter is analyzed in [8] and [9] as two full-bridge phase-shifted (FB-PS) converter subtopologies. Therefore, the steady-state operation and ZVS analysis on the three-phase converter can be done in the same way as the FB-PS converter [13]. Same as the FB-PS converter, this converter also utilizes the transformer leakage inductance to achieve ZVS, but at a price of reduction of the effective duty cycle. The duty-cycle loss increases the conduction losses and limits the switching frequency, which results in decreased conversion efficiency and power density of the converter. Unlike the FB-PS converter, where the input dc bus is constant, the dc bus for the two subtopologies vary during every 60° interval, since the dc bus is one of the three line-to-line voltages. These variable operating conditions contribute to a large variation on output inductor current ripple. Then, a large output inductor may be required to limit the ripple current, which results in the reduction of the power density of the converter. Because the switching sequence of the proposed PWM in [8] and [9] contains eight segments in each switching cycle, it is referred as "eight-segment PWM" in this paper. A six-segment PWM scheme is proposed in this paper to overcome the aforementioned drawbacks of large duty cycle loss and large output inductor current ripple with eight-segment PWM. The merit of ZVS operation to use MOSFETs is still maintained in the proposed six-segment PWM. In addition, lower turn-OFF losses are also realized. The rest of the paper is organized as follows: Commonly practiced PWM schemes particularly for three-phase isolated matrix-type rectifier are reviewed and compared in Section II, followed by the principle operation of the proposed six-segment PWM. The steady-state analysis of duty-cycle loss, output inductor current ripple, and input current THD are described in Section III. Experimental results are presented in Section IV, followed by the conclusion in Section V.

II. PWM Schemes for Three-Phase Isolated Buck Matrix-Type Rectifier and Principle of Operation

The three-phase buck matrix-type PWM rectifier is equivalent to a traditional current-source rectifier (CSR), except that all the switches are bidirectional. The space-vector modulation (SVM) for CSR can be adapted to this converter. The space vector of the desired phase current $\vec{I}_{\rm ref}$, the current reference vector, is

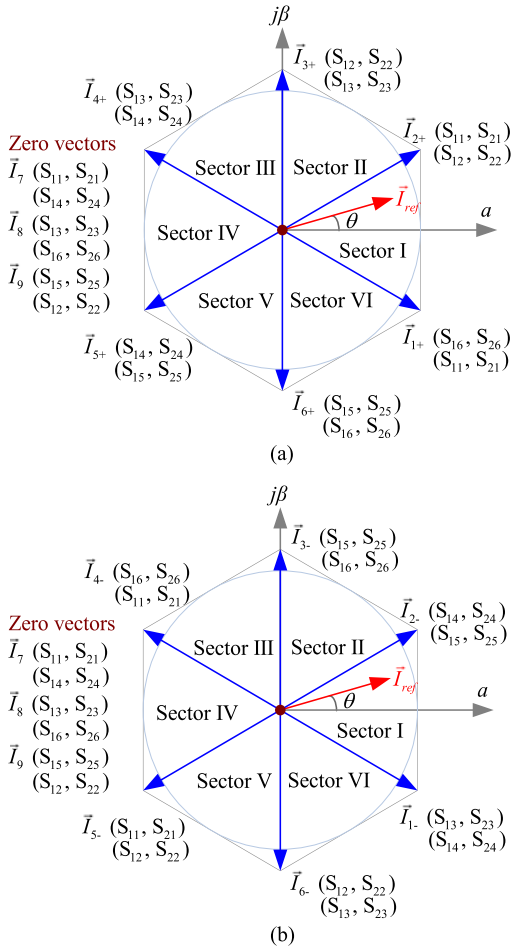

Fig. 3. Current space vector representation. (a) $i_P > 0$. (b) $i_P < 0$.

synthesized by the two adjacent active vectors $\vec{I}_x$, $\vec{I}_y$ and a zero vector $\vec{I}_0$ (here $\vec{I}_x = \vec{I}_1$ and $\vec{I}_y = \vec{I}_2$, when $\vec{I}_{\rm ref}$ is located in sector I), as shown in Fig. 3. In order to use transformer isolation, the primary voltage of the transformer v_P in Fig. 1 must be alternating positive and negative in high frequency to maintain the volt-sec balance. For each active vector, there are two possible switching states depending on the direction of the current in the primary side of the transformer i_P, as shown in Fig. 3. $\vec{I}_{x+}$ and $\vec{I}_{x-}$ represent the switching states of vector $\vec{I}_x$ when $i_P > 0$ and $i_P < 0$, respectively, with equal dwell time. In addition, $\vec{I}_{y+}$ and $\vec{I}_{y-}$ represent switching states of vector $\vec{I}_y$ when $i_P > 0$ and $i_P < 0$, respectively, with equal dwell time.

A. Review of PWM Schemes for a Three-Phase Isolated Buck Matrix-Type Rectifier

For the analysis in this section, it is assumed that the current reference vector $\vec{I}_{\rm ref}$ in Fig. 3 is located at $0° < \theta < 30°$. During this interval the line–line voltage $v_{AB} = v_A - v_B$ is lower than $v_{AC} = v_A - v_C$, as shown in Fig. 2. The SVM and dwell-time calculation are well described in [14]. Depending on how the transformer primary voltage is synthesized by the three-phase input voltages, different switching pattern arrangements can be generated and can be identified by the transformer primary

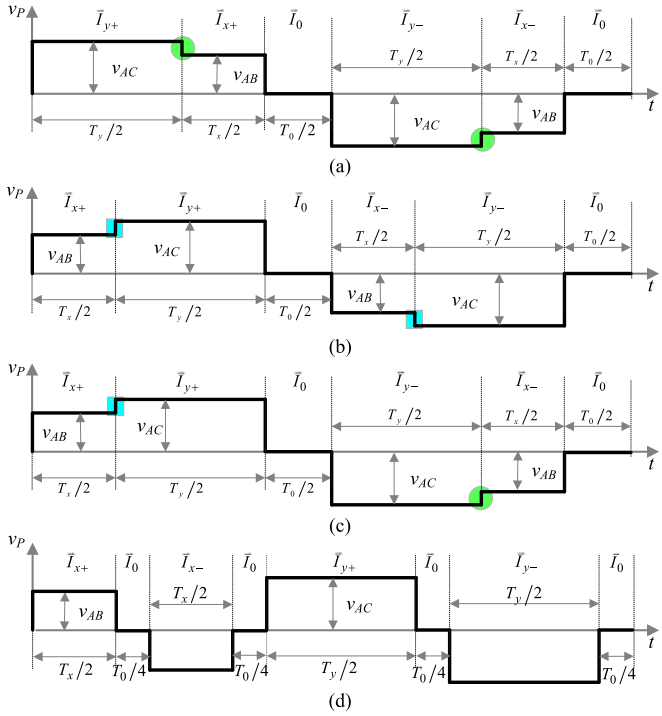

Fig. 4. Transformer primary voltage within a switching cycle with different switching patterns when $\vec{I}_{\rm ref}$ in Fig. 3 is located at $0^\circ < \theta < 30^\circ$. (a) Six-segment PWM with HTL pattern. (b) Six-segment PWM with LTH pattern. (c) Six-segment PWM with Hybrid pattern. (d) Eight-segment PWM pattern.

voltage waveform. Fig. 4 shows the transformer primary voltage waveforms within a switching cycle with the six-segment [6], [7], [11], [12], [14], and eight-segment [8], [9], [10], [15], [16] switching patterns. For the six-segment PWM scheme, the dwell-time of each vector is divided by two ($T_x/2$,$T_y/2$,$T_0/2$), and the active vector $\vec{I}_x$ joints with the active vector $\vec{I}_y$ ($\vec{I}_{x+}$ joints $\vec{I}_{y+}$ in the positive half-cycle and $\vec{I}_{x-}$ joints $\vec{I}_{y-}$ in the negative half-cycle). The switching patterns of the six-segment PWM are identified by the transition between the two attached active vectors. If the vector transition causes a step change in the transformer primary voltage from a higher voltage magnitude to a lower voltage magnitude, the corresponding step change is defined as a high to low (HTL). Fig. 4(a) shows the transformer primary voltage with HTL switching pattern within a switching cycle. It can be observed that there are two HTL step changes (regions with circle) in the positive half-cycle and in the negative half-cycle of the transformer primary voltage, respectively. On the other hand, if the vector transition occurs from a lower voltage magnitude to a higher voltage, the corresponding step change is defined as a low to high (LTH). Fig. 4(b) shows the transformer primary voltage with LTH pattern within a switching cycle. It can be observed that there are two LTH step changes (regions with square) in the positive half-cycle and the negative half-cycle of the transformer primary voltage, respectively. In addition, there is other type of six-segment switching pattern arrangement, which has a different step change in each half-cycle, and it is defined as a hybrid pattern [7], [8], [12], [13]. Fig. 4(c) shows the hybrid PWM pattern with an LTH step change in the positive half-cycle and an HTL in the negative half-cycle. For the eight-segment PWM pattern, the dwell time of $\vec{I}_0$ is equally divided by four and inserted between active vectors, as shown in Fig. 4(d) [8]–[11], [15], [16].

The switching losses corresponding to the transition from zero vector to active vector and from active vector to zero vector should not exhibit significant differences among different switching patterns. However, the switching losses for the transition of HTL are different from the transition of LTH, and will be further discussed and examined below.

1) Switching Transition From Higher Active Vector to Lower Active Vector (HTL): The switching transition for HTL has been discussed thoroughly in [14, Section III-B]. There are two turn-ON actions and one turn-OFF action related to this transition. One of the turn-ON actions is ZVS and the other is non-ZVS. However, the turn-ON loss of the non-ZVS switch is very low, since the MOSFET is turned ON with zero current and very low drain–source voltage. The switching loss contains only the discharging energy stored in $C_{\rm oss}$ of the MOSFET, which is fairly low due to the low drain–source voltage of the switch prior to turn-ON. The turn-OFF loss of the MOSFET is low due to a very small overlapping of the voltage and current during this transition. In addition, the turn-OFF action occurs at low voltage transition.

2) Switching Transition From Lower Active Vector to Higher Active Vector (LTH): The steps involved in this transition are illustrated in Fig. 5, using an example when the current reference vector $\vec{I}_{\rm ref}$ is located at $0^\circ < \theta \leq 30^\circ$, where $v_A > v_B > v_C$. Transition of the active vectors is from vector $\vec{I}_{x+} = \vec{I}_{1+}$ to vector $\vec{I}_{y+} = \vec{I}_{2+}$, and the voltage across the transformer primary is changed from v_{AB} (with lower magnitude) to v_{AC} (with higher magnitude), as shown in Fig. 4(b). Switches S_{21}, S_{14}, S_{15}, and S_{22} were always kept ON during the whole switching cycle to function as a synchronous rectification, since their antiparallel diodes are forward-biased [14]. For the same reason, switches S_{13} and S_{26} also function as a synchronous rectification. However, they should be complementary to S_{25} and S_{12}, respectively, in order to avoid short circuit between phases *B* and *C*, since v_B is higher than v_C. Before the start of this transition, switches S_{11} and S_{16} were ON to generate active vector $\vec{I}_{x+}$, and the transformer primary voltage v_P has the magnitude of v_{AB}. The first step of this transition is to turn OFF S_{26} and the current will commutate from S_{26} to its antiparallel diode D_{26}, as shown in Fig. 5(b), since S_{26} functions as synchronous rectification. This step does not change the state of the vector and is just for preparing the next step to avoid short circuit, as mentioned above. The second step is to turn ON S_{12}. Voltage across S_{12} is v_{BC} prior to turn ON. During the transition of turning ON S_{12}, capacitor across S_{12} is discharged and voltage v_C appears on the cathode of D_{26}. Since $v_A > v_B > v_C$, D_{26} is reverse-biased and the current is forced to commutate from D_{26} to S_{12}. Therefore, there are turn-ON losses due to this hard switching. In addition, a large loss may also be generated due to the reverse recovery of D_{26} if the regular Si MOSFET is employed as the switches. Transition of LTH is completed by the last step of turning OFF S_{16} at zero current. In summary, there are one turn-ON and two turn-OFF actions corresponding to the LTH transition. The turn-ON loss is

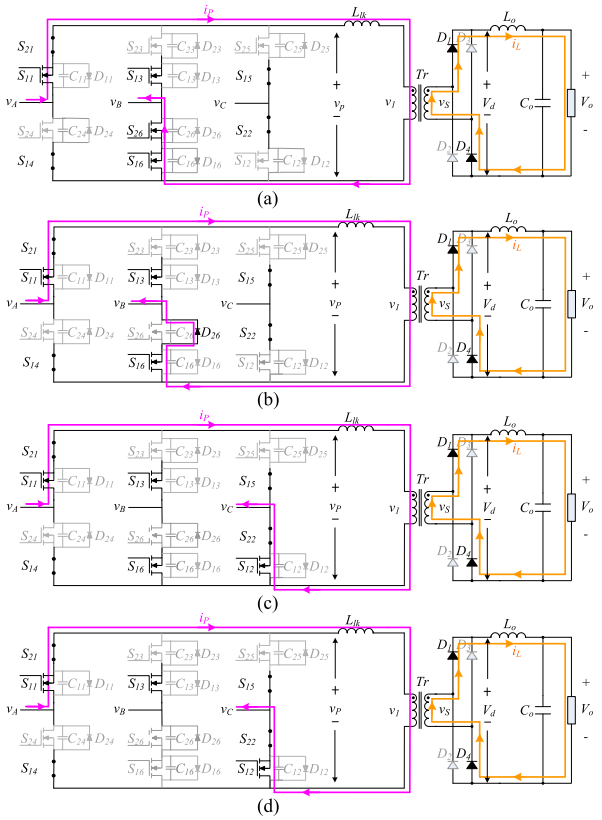

Fig. 5. Switching transition for low-to-high (LTH). (a) Switching state of $\vec{I}_{x+}$. (b) First step of vector transition from $\vec{I}_{x+}$ to $\vec{I}_{y+}$. (c) Second step of vector transition from $\vec{I}_{x+}$ to $\vec{I}_{y+}$. (d) Last step of vector transition from $\vec{I}_{x+}$ to $\vec{I}_{y+}$.

high due to hard switching with full current. This turn-ON loss includes the diode reverse recovery loss, the power loss due to overlapping of drain–source voltage V_{ds} and current I_{ds}, and the power loss due to discharging energy stored in $C_{\rm oss}$ of MOSFETs. The turn-OFF losses are ignorable since one of the switches turns OFF at zero current and the other at zero voltage. The LTH switching pattern has much larger turn-ON loss compared to HTL.

B. Optimal PWM Candidate for mosfet Devices

Fig. 6 illustrates the transformer primary voltage waveforms with different PWM schemes within 60° interval of sector I. Depending on where the reference vector is located and how the vector sequences are arranged, different switching patterns can be generated. As shown in Fig. 6, as the reference vector moving within 60° interval of sector I, the magnitudes of two line–line voltages, v_{AB} and v_{AC} are varying. If the reference vector is located at $-30^\circ \le \theta < 0^\circ$,$v_{AB}$ is greater than v_{AC} and if the reference vector is located at $0^\circ < \theta \le 30^\circ$, v_{AC} is greater than v_{AB}. Thus, for a given vector sequence, the switching pattern will be changed when the reference vector moves from regions of $\theta \in [-30^\circ, 0^\circ]$ to $\theta \in [0^\circ, 30^\circ]$. For example, "Type C" PWM in Fig. 6(c) exhibits the HTL switching pattern during the interval of $-30^\circ \le \theta < 0^\circ$, and the LTH switching pattern during the interval of $0^\circ < \theta \le 30^\circ$ with the same vector sequence of $\vec{I}_{x+}$, $\vec{I}_{y+}$,$\vec{I}_0$,$\vec{I}_{x-}$,$\vec{I}_{y-}$,$\vec{I}_0$. In order to maintain the same switching pattern during two intervals of $-30^\circ \le \theta < 0^\circ$ and $0^\circ < \theta \le 30^\circ$, the vector sequence of the two active vectors are swapped as shown in Fig. 6(a) and (b). As shown in Fig. 6(a), "Type A" PWM scheme always maintains the HTL switching pattern with the vector sequence of $\vec{I}_{x+}$,$\vec{I}_{y+}$,$\vec{I}_0$,$\vec{I}_{x-}$,$\vec{I}_{y-}$,$\vec{I}_0$ during the interval of $-30^\circ \le \theta < 0^\circ$ and $\vec{I}_{y+}$,$\vec{I}_{x+}$,$\vec{I}_0$,$\vec{I}_{y-}$,$\vec{I}_{x-}$,$\vec{I}_0$ during the interval of $0^\circ < \theta \le 30^\circ$. Whereas, "Type B" PWM, as shown in Fig. 6(b), always maintains the LTH switching pattern. "Type C" PWM pattern is the most popular PWM scheme [6], [7], [11] due to the simplicity of implementation, since no sequence swapping is required during each sector. "Type D" PWM pattern is rarely used due to the drawback of asymmetrical voltage pulses across the transformer primary winding. As discussed earlier in this paper, the HTL transition exhibits lower switching losses when comparing with the transition of LTH if MOSFETs are employed in the converter. Therefore, "Type A" PWM scheme is the optimal six-segment PWM to eliminate the turn-ON loss with ZVS implementation. "Type E" PWM scheme in Fig. 6(e) exhibits eight-segment switching pattern, which is initially introduced by Vlatković and Borojević [8]. The zero-voltage interval is equally distributed between the pulses in order to provide a necessary condition for ZVS, which is also attractive for MOSFETs employed in the converter. However, later in this paper, the comparisons between the two PWM schemes "Type A" and "Type E" reveal that the "Type A" is the optimal PWM scheme for the MOSFET devices used in three-phase isolated buck matrix-type rectifier.

C. Principle of Operation and Commutation of the Proposed PWM ("Type A")

1) Principle of Operation of "Type A" PWM: Within any 60° interval between two successive zero crossings of input phase voltage, there are two line voltages that do not change sign as shown in Fig. 2. For example, during the interval of $-30^\circ < \theta < 30^\circ$ (shaded area), the line voltages $v_{AB} = v_A - v_B$ and $v_{AC} = v_A - v_C$ are positive, and they both attain their maximum in this interval. Since the switching frequency of the converter is much higher than the line frequency, the two line voltages can be treated as slowly varying dc voltages. Therefore, the three-phase converter can be redrawn as an FB-PS converter, as shown in Fig. 7. In each 60° interval, one of the phase legs which has the highest or lowest voltage potential is shared by the "bridge *x*" and "bridge *y*". For example, in sector I, the phase leg *A* has the highest voltage potential and is the common leg of "bridge *x*" and "bridge *y*." In Fig. 6(a), the active vectors $\vec{I}_{x+}$ and $\vec{I}_{x-}$ are generated by "bridge *x*," likewise $\vec{I}_{y+}$ and $\vec{I}_{y-}$ are generated by "bridge *y*." The zero vector $\vec{I}_0$ is generated by turning ON all the switches in the common leg of "bridge *x*" and "bridge *y*." The circuit principle waveforms within 180° intervals with excessively increased switching period of PWM can be observed in Fig. 8. For example, in the sector I (a) of Fig. 8(b), the switches S_{11}, S_{21}, and S_{16}, S_{26} of "bridge *x*" are turned ON with ON-time $T_x/2$ creating a positive voltage pulse $v_P = v_{AB}$, and a current pulse flowing from phase *A* into phase

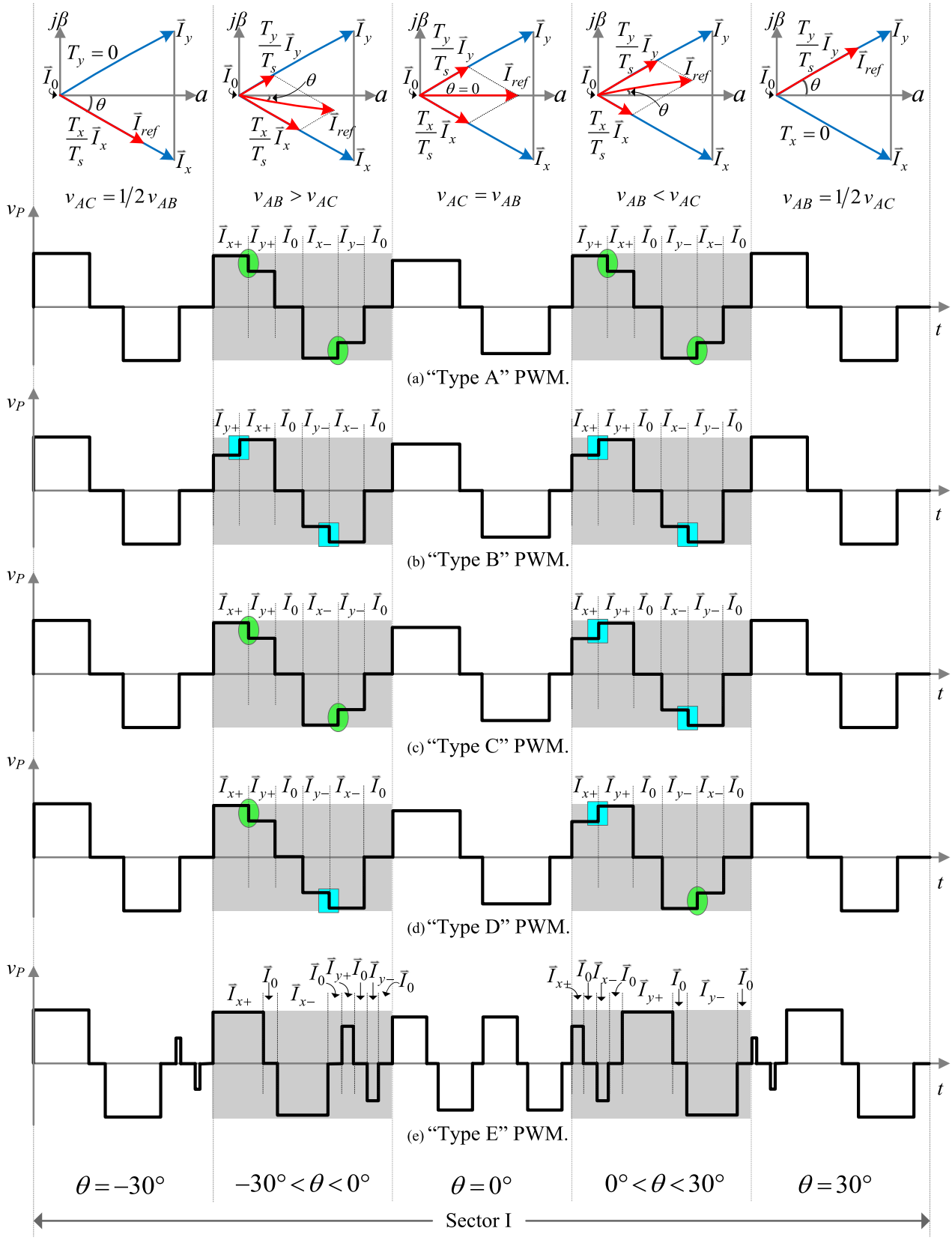

Fig. 6. Transformer primary voltage with different PWM schemes when $\vec{I}_{\mathrm{ref}}$ in Fig. 3 is moving within sector I.

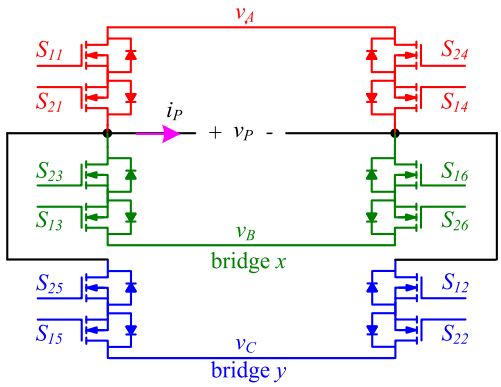

Fig. 7. Three-phase converter redrawn as ZVS full-bridge dc–dc converter with leg A as the common leg of "bridge x" and "bridge y" within sector I operation.

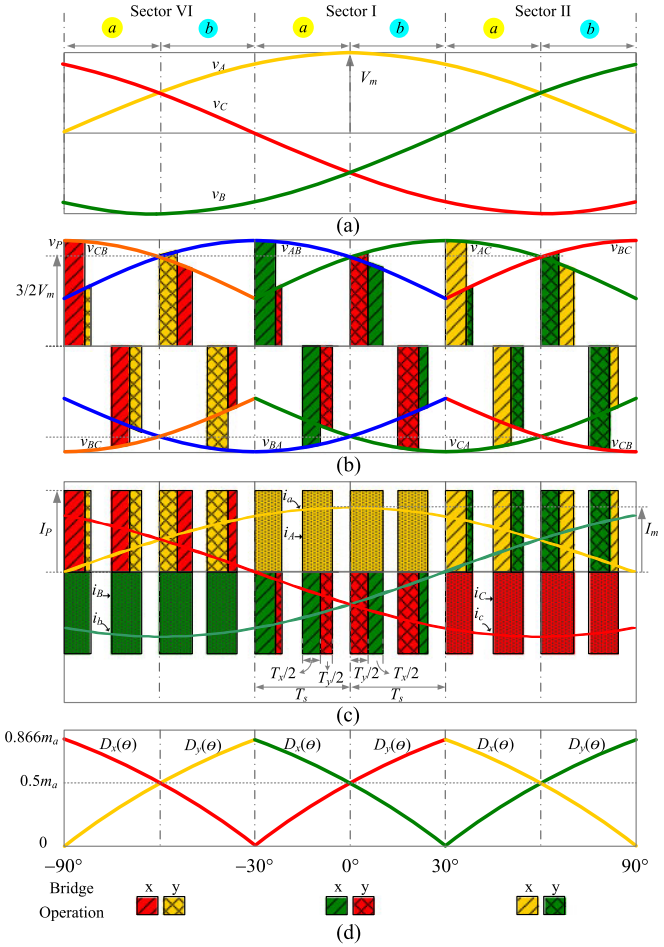

Fig. 8. Waveforms of "Type A" PWM with excessively increased switching period T_s: (a) phase voltages, (b) primary voltage, (c) phase currents i_A, i_B, and i_C, (d) $D_x(\theta)$ duty-cycle of "bridge x" and $D_y(\theta)$ duty-cycle of "bridge y."

B with the magnitude of I_P. Then, S_{11}, S_{21}, and S_{12}, S_{22} of "Bridge y" are turned ON with ON-time $T_y/2$, creating a positive voltage pulse $v_P = v_{AC}$ and a current pulse flowing from phase A into phase C with the magnitude of I_P. In order to keep the transformer flux balanced, a negative voltage pulse of the same duration is generated next by turning ON switches S_{14}, S_{24}, and S_{13}, S_{23} of "bridge x" and S_{14}, S_{24} and S_{15}, S_{25} of "bridge y." It should be noted that the grid-side currents shown in Fig. 8(c) remain the same regardless the alteration in the transformer current. As aforementioned in this paper, to realize "Type A" PWM, the sequence of the two attached active vectors need to be swapped in the middle of each sector. As shown in Fig. 8(b)–(d), the pulse with larger voltage magnitude and duty cycle always start first. The phase currents are synthesized by the current pulses with a constant magnitude of I_P. The duty cycles $D_x(\theta) = T_x/T_s$ and $D_y(\theta) = T_y/T_s$ of the input current pulses generated by "bridges x" and "bridge y," respectively, as shown in Fig. 8(c) and (d) within the chosen 60° interval (sector I) are given by (1), where I_m is the peak of the fundamental-frequency component in i_a and $m_a(\theta) = I_m/I_P$ is the modulation index which is in the range of $0 \le m_a \le 1$

$$\begin{bmatrix} T_x/T_s \\ T_y/T_s \\ (T_x+T_y)/T_s \end{bmatrix} = \begin{bmatrix} -i_b(\theta)/I_P \\ -i_c(\theta)/I_P \\ i_a(\theta)/I_P \end{bmatrix} = m_a \begin{bmatrix} -i_b(\theta)/I_m \\ -i_c(\theta)/I_m \\ i_a(\theta)/I_m \end{bmatrix}. \tag{1}$$

It can be observed that for a given m_a the duty cycle of current pulses for each phase is proportional to its fundamental current. Then, m_a can be used to adjust the three-phase current magnitude without affecting their sinusoidal shape.

2) Switching State and Commutation of "Type A" PWM: The corresponding switch gate signals in sectors I (a) and I (b) during one switching period T_s and the detail of ZVS switching transition analysis can be found in [14]. Since MOSFETs are employed in the main converter, some of the switches function as synchronous rectification to reduce the conduction loss. For example, during interval $-30° \le \theta < 0°$ [sector I (a)] in Fig. 8(a), voltage potential $v_A > v_C > v_B$, therefore, the switches S_{14}, S_{21}, S_{13}, and S_{26} of "bridge x" can be kept ON all the time since their body diodes are forward-biased, as shown in Fig. 9(a). Constraints need to be applied to S_{15} and S_{22} of "bridge y" in order to prevent short circuit between v_B and v_C. S_{15} of "bridge y" should be complimentary to S_{23} of "bridge x" to prevent short circuit between v_B and v_C, since S_{25} is forward-biased with the voltage potential of v_C higher than v_B. For the same reason, S_{22} of "bridge y" should be complimentary to S_{16} of "bridge x" since S_{12} is forward-biased. During interval $0° < \theta \le 30°$ [sector I (b)], voltage potential $v_A > v_B > v_C$ switches S_{14}, S_{21}, S_{15}, and S_{22} of "bridge y" can be kept ON all the time since body diodes of these switches are forward-biased, as shown in Fig. 9(b). The six switches (S_{21}, S_{14}, S_{13}, S_{26}, S_{15}, S_{22}) function as synchronous rectification and the active switches (S_{11}, S_{24}, S_{23}, S_{16}, S_{25}, S_{12}) operate in a similar manner as that of an FB-PS converter to achieve ZVS. The active switches and the synchronous rectification switches for "Type A" PWM scheme are summarized in Table I based on the SVM presented in [14]. In Table I, $\vec{I}_{x+}$ and $\vec{I}_{x-}$ represent switching states of vector $\vec{I}_x$ when $i_P > 0$ and $i_P < 0$, respectively, with equal dwell time of $T_x/2$. In addition, $\vec{I}_{y+}$ and $\vec{I}_{y-}$ represent switching states of vector $\vec{I}_y$

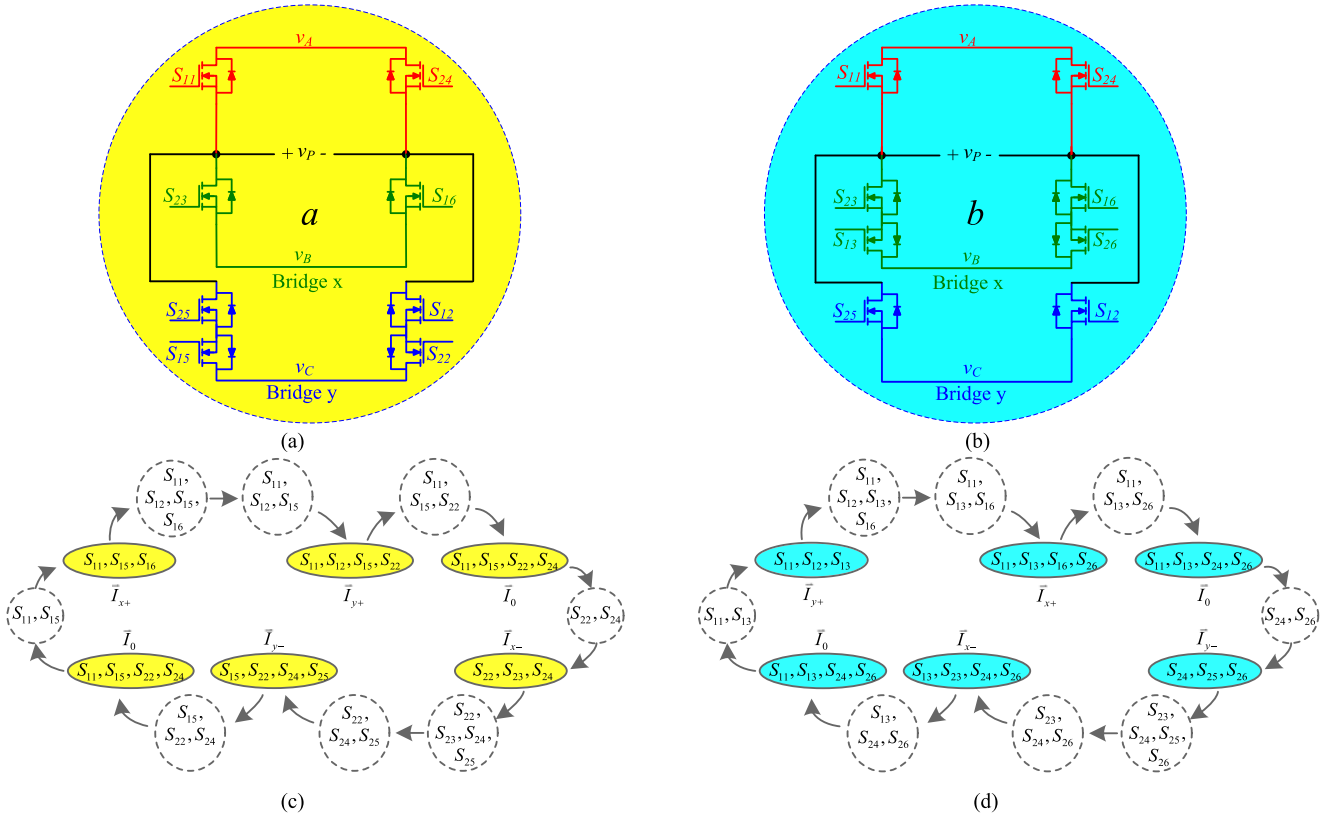

Fig. 9. Subtopology "bridge x" and "birdge y" and commutation method. (a) Subtopology "bridge x" and "bridge y" in sector I (a) (S_{13}, S_{14}, S_{21}, S_{26} are kept on all the time). (b) Subtopology "bridge x" and "bridge y" in sector I (b) (S_{14}, S_{15}, S_{21}, S_{22} are kept on all the time). (c) Finite commutation state machine in sector I (a). (d) Finite commutation state machine in sector I (b).

TABLE I
SWITCHING STATES AND SPACE VECTORS IN SECTOR I

Sector of $\bar{I}_{ref}$		I (a)						I (b)					
Angle (θ)		$-30^\circ < \theta < 0^\circ$						$0^\circ < \theta < 30^\circ$					
Primary Current		$i_P > 0$			$i_P < 0$			$i_P > 0$			$i_P < 0$		
Space Vector		$\bar{I}_{x+}$	$\bar{I}_{y+}$	$\bar{I}_0$	$\bar{I}_{x-}$	$\bar{I}_{y-}$	$\bar{I}_0$	$\bar{I}_{y+}$	$\bar{I}_{x+}$	$\bar{I}_0$	$\bar{I}_{y-}$	$\bar{I}_{x-}$	$\bar{I}_0$
Switching States	Active Switches	S_{11} S_{16}	S_{11} S_{12}	S_{11} S_{24}	S_{23} S_{24}	S_{24} S_{25}	S_{11} S_{24}	S_{11} S_{12}	S_{11} S_{16}	S_{11} S_{24}	S_{24} S_{25}	S_{23} S_{24}	S_{11} S_{24}
	Synchronous Rectification Switches	S_{13} S_{14} S_{21} S_{26} S_{15}	S_{13} S_{14} S_{21} S_{26} S_{15} S_{22}	S_{13} S_{14} S_{21} S_{26} S_{15} S_{22}	S_{13} S_{14} S_{21} S_{26} S_{22}	S_{13} S_{14} S_{21} S_{26} S_{15} S_{22}	S_{13} S_{14} S_{21} S_{26} S_{15} S_{22}	S_{14} S_{15} S_{21} S_{22} S_{13}	S_{14} S_{15} S_{21} S_{22} S_{13} S_{26}	S_{14} S_{15} S_{21} S_{22} S_{13} S_{26}	S_{14} S_{15} S_{21} S_{22} S_{26}	S_{14} S_{15} S_{21} S_{22} S_{13} S_{26}	S_{14} S_{15} S_{21} S_{22} S_{13} S_{26}

when $i_P > 0$ and $i_P < 0$, respectively, with equal dwell time of $T_y/2$. The finite commutation state machines of the proposed commutation method in sectors I (a) and (b) are shown in Fig. 9(c) and (d). The transition states (in dashed line) are added between main states (in shaded color) to achieve ZVS and synchronous rectification operation. Two-step commutation is applied for the transitions from the active vector to zero vector and from the zero vector to active vector, while three-step commutation is required for transitions from the active vector to another active vector.

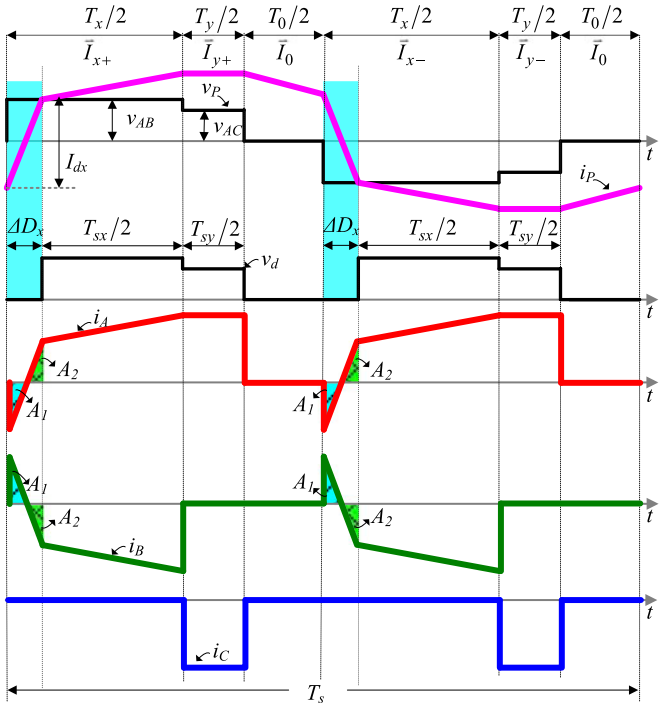

Fig. 10. Waveforms of the steady-state operation in sector I (a).

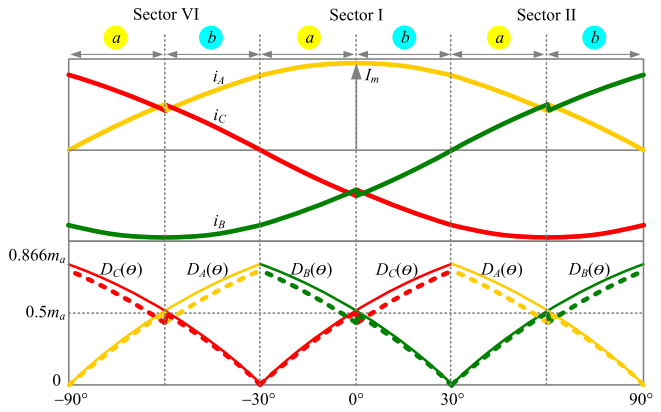

Fig. 11. Distorted input phase current waveforms without duty-cycle compensation (solid line: applied duty-cycle; dashed line: effective duty-cycle).

III. Steady-State Analysis and Comparison Between "Type A" and "Type E" PWM

In this section, duty-cycle loss, output inductor current ripple, and switching losses of the "Type A" and "Type E" PWM are compared. Also, the comparison indicates that the input current THDs of the converter are not significantly impacted by the two PWM patterns.

A. Analysis of Duty-Cycle Loss and THD

The duty-cycle loss is one of the major limitations of operating at higher switching frequency and it generates circulating current on the primary switches and transformer winding, which results in conduction loss and poor input current THD. Selection of the transformer turns ratio n and the modulation index m_a is related to the loss of duty cycle, which depends on the choice of the switching frequency, leakage inductance, and the ZVS range. This interdependence is evaluated in [17]. The duty-cycle loss ΔD_x happened at the transition from zero vectors to active vectors due to the finite transition time depending on the value of L_{lk} and the primary-side voltage v_P, as shown in Fig. 10 in the shaded area. During duty-cycle loss interval, the output inductor current is still freewheeling through the bridge rectifier and the transformer secondary voltage is clamped to zero. The primary current i_P swing from one direction to another direction and, as a result, the two input currents i_A and i_B [due to the bridge x duty-cycle loss in sector I (a)] contain two triangle A_1 and A_2, since the input phase current is synthesized by i_P. These two areas cancel each other and result in zero net current during the interval ΔD_x. Therefore, ΔD_x will not contribute to either the input phase-current or the output power, but generate losses due to the circulating current. The loss of duty cycle will also affect the input current THD and output voltage ripple if the applied duty cycle is not compensated well. In order to generate the phase current with sinusoidal shape, the duty cycle of each phase should also have a value in the sinusoidal shape that is proportional to the phase current as stated in (1). Due to the duty-cycle loss, however, the effective duty cycle (dashed line) is lower than the applied duty cycle (solid line). If the applied duty cycle is in the sinusoidal shape, the curve of the effective duty cycle will contain step changes which occurred every 60° interval as shown in Fig. 11. Since the phase current is determined by the effective duty cycle, the phase current is also distorted and contains low-frequency harmonics that affect the THDs. In addition, the output voltage will also contain low-frequency harmonics. In order to eliminate these affects, the effective duty cycle which is also the secondary duty cycle $D_{sx}(\theta) = T_{sx}/T_s$ and $D_{sy}(\theta) = T_{sy}/T_s$ needs to be calculated as

$$D_{sx}(\theta) = -m_a(I_b(\theta)/I_m)$$
$$D_{sy}(\theta) = -m_a(I_c(\theta)/I_m) \tag{2}$$

where m_a is effective modulation index as aforementioned, which is equal to the effective duty cycle at the peak of phase current. The range of m_a need to be selected based on the maximum available effective duty cycle. Then, the primary duty cycle with duty-cycle compensation is defined as

$$D_x(\theta) = D_{sx}(\theta) + 2\Delta D_x(\theta)$$
$$D_y(\theta) = D_{sy}(\theta). \tag{3}$$

The maximum loss of duty cycle is obtained when the magnitude of $v_P(\theta)$ is minimum at $\theta = 0°$ and $v_P(\theta) = 3/2V_m$. The maximum total loss of duty cycle in term of output load is given by

$$\Delta D_{\text{total\_max}} = \frac{4n^2 m_a L_{lk}}{R_o T_s} \tag{4}$$

where L_{lk} is the leakage inductance, n is the transformer turns ratio, and $R_o = V_o/I_o$ is the load resistance. After the duty-cycle compensation, given in (3), the maximum applied duty cycle happened at $\theta = 0°$ since both the effective duty-cycle and

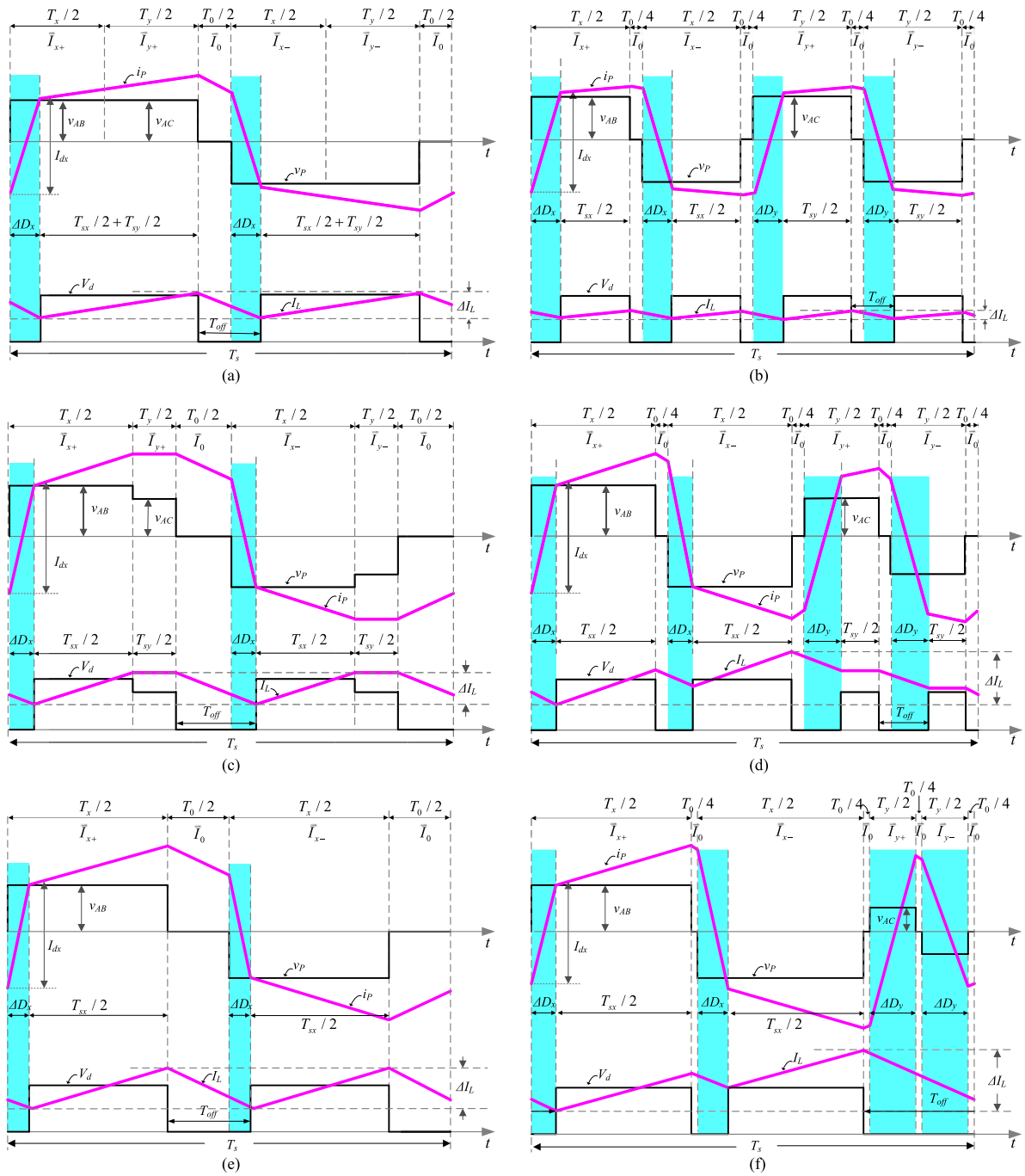

Fig. 12. Waveforms of the duty-cycle loss and the output inductor current ripple for "Type A" and "Type E" PWM. (a) "Type A" at $\theta = 0°$. (b) "Type E" at $\theta = 0°$. (c) "Type A" at $-30° < \theta < 0°$. (d) "Type E" at $-30° < \theta < 0°$. (e) "Type A" at $\theta = -30°$. (f) "Type E" at $\theta = -30°$.

the loss of duty cycle attain their maximum at $\theta = 0°$. Because the applied duty cycle cannot exceed one, the maximum available effective duty cycle is given by

$$D_{sx\_\max} = 1 - 2\Delta D_x(0). \tag{5}$$

Then, the effective m_a should be in the range of $[0, D_{sx\_\max}]$. Outwardly, large loss of duty cycle will reduce the range of the effective m_a and generate higher conduction loss. Compared with "Type A" PWM, the "Type E" has two additional duty-cycle losses, ΔD_y as shown in Fig. 12. The intervals of ΔD_y is longer than the intervals of ΔD_x, since ΔD_y is associated to the narrower pulse where the magnitude of $v_P(\theta)$ is lower. At the extreme case, when $\theta = \pm 30°$, the interval of ΔD_y is twice the interval of ΔD_x as shown in Fig. 12(e) and (f), where the magnitude of $v_P(\theta)$ is only half of that during intervals of ΔD_x. In spite of the two missing pulses $\bar{I}_{y+}$ and $\bar{I}_{y-}$ on the secondary side at $\theta = \pm 30°$, two pulses of $\bar{I}_{y+}$ and $\bar{I}_{y-}$ on primary side always exist in order to compensate for the duty-cycle losses as shown in Fig. 12(f). Therefore, these two pulses contribute no power to the output load, but create conduction and switching losses on the primary side. The total duty-cycle losses of "Type A" and "Type E" PWM schemes are compared

TABLE II
COMPARISON OF THE NORMALIZED TOTAL DUTY-CYCLE LOSSES

θ	ΔD_{total} of "Type A" PWM	ΔD_{total} of "Type E" PWM
$\theta = 0^\circ$	1	2
$-30^\circ < \theta < 0^\circ$, $0^\circ < \theta < 30^\circ$	$\sqrt{3}/2 < \Delta D_{total} < 1$	$2 < \Delta D_{total} < 3\sqrt{3}/2$
$\theta = \pm 30^\circ$	$\Delta D_{total} = \sqrt{3}/2$	$\Delta D_{total} = 3\sqrt{3}/2$

at different angle θ, as shown in Table II and Fig. 12. In order to make an easier comparison, all the total duty losses are normalized by using the total duty loss of "Type A" PWM at $\theta = 0^\circ$ as a base. It is interesting to note that the total duty-cycle loss of "Type E" PWM is two to three times higher than that of the "Type A" PWM if the same value of L_{lk} is used. In other words, if both designs have the same duty-cycle losses, the "Type A" PWM can achieve ZVS with wider load range by using larger value of L_{lk}. This significantly reduces the turn-ON switching losses at lighter load.

The reduction of duty-cycle losses also enables the operation of the converter at higher m_a and reduces the power losses caused by the circulating current in the primary-side switches.

B. Output Inductor Current Ripple Comparison of "Type A" and "Type E" PWM

For a given output voltage, the output inductor current ripple at steady state is determined by the OFF-time of the secondary voltage V_d. The OFF-time of V_d consists of the dwell time of zero vectors and the time intervals of duty-cycle loss. Fig. 12 shows the output inductor current ripple of "Type A" and "Type E" PWMs varying with phase angle θ due to the variable OFF-time of V_d. At $\theta = 0^\circ$, the total OFF-time of the secondary voltage V_d is minimum and is given by $(1 - m_a)T_s$, where m_a is the effective modulation index. Therefore, the current ripple for both "Type A" and "Type E" PWM schemes reaches a minimum value at $\theta = 0^\circ$. For the "Type E" PWM, the OFF-time of V_d is divided into four intervals while for "Type A" PWM, the off-time of V_d is divided into two intervals as shown in Fig. 12(a) and (b). Then, the current ripple for both "Type A" and "Type E" PWMs is given by

$$\Delta I_{\min} = \frac{V_o(1 - m_a)T_s}{2L_o} \tag{6}$$

$$\Delta I_{\min} = \frac{V_o(1 - m_a)T_s}{4L_o}. \tag{7}$$

As shown in (6) and (7), the minimum current ripple of "Type E" PWM is only half of that of the "Type A" PWM. At $\theta = \pm 30^\circ$, the total OFF-time of the secondary voltage V_d is maximum and can be derived as $(1 - \sqrt{3}/2m_a)T_s$. Therefore, the output current ripples of "Type A" and "Type E" PWMs reach maximum value as shown in Fig. 12(e) and (f). For "Type A" PWM, the OFF-time of V_d is still equally divided by two. The current ripple can be derived by

$$\Delta I_{\max} = \frac{V_o(1 - \sqrt{3}/2m_a)T_s}{2L_o}. \tag{8}$$

For the "Type E" PWM, three of the OFF-time intervals adjacent to the narrow pulses merge into one resulting in a larger current ripple. For example, at $\theta = -30^\circ$, the two pulses of $\bar{I}_{y+}$ and $\bar{I}_{y-}$ on the secondary side disappear so that three of the OFF-time intervals merge into one large interval, as shown in Fig. 12(f). Assuming that the difference between ΔD_x and ΔD_y is relatively small and can be ignored, the maximum current ripple of the "Type E" PWM can be derived by

$$\Delta I_{\max} = \frac{3V_o(1 - \sqrt{3}/2m_a)T_s}{4L_o}. \tag{9}$$

In summary, the minimum current ripple in the "Type A" PWM (at $\theta = 0^\circ$) is higher than the "Type E" PWM by two times. This is one of the drawbacks of "Type A" PWM. However, the maximum current ripple in the "Type A" PWM (at $\theta = \pm 30^\circ$) is smaller than that of "Type E" PWM. It is important to observe that, the frequency across the transformer with "Type E" is double of the "Type A" PWM, given that both PWM schemes have the same T_s. Then, the lower core loss and smaller core of the transformer can be expected with "Type E" PWM. However, "Type E" PWM will not offer a significant benefit in the transformer design if the transformer is designed based on the maximum flux density which is normally the most important constraints for the transformer design.

At the vicinity of $\theta = \pm 30^\circ$ as shown in Fig. 12(f), one of the two active vectors attained its maximum magnitude and the other vector reach to minimum. As a result, both PWM schemes attain the same maximum flux density on the transformer, although the transformer operating frequency of "Type A" is only half of "Type E."

C. Switching Loss Comparison Between "Type A" and "Type E" PWM

The analysis in this section is based on the switching operation in sector I (a), and this remains true for all the sectors due to the repetitive feature of the switching pattern. Switching losses can be analyzed for turn-ON and turn-OFF actions within a switching

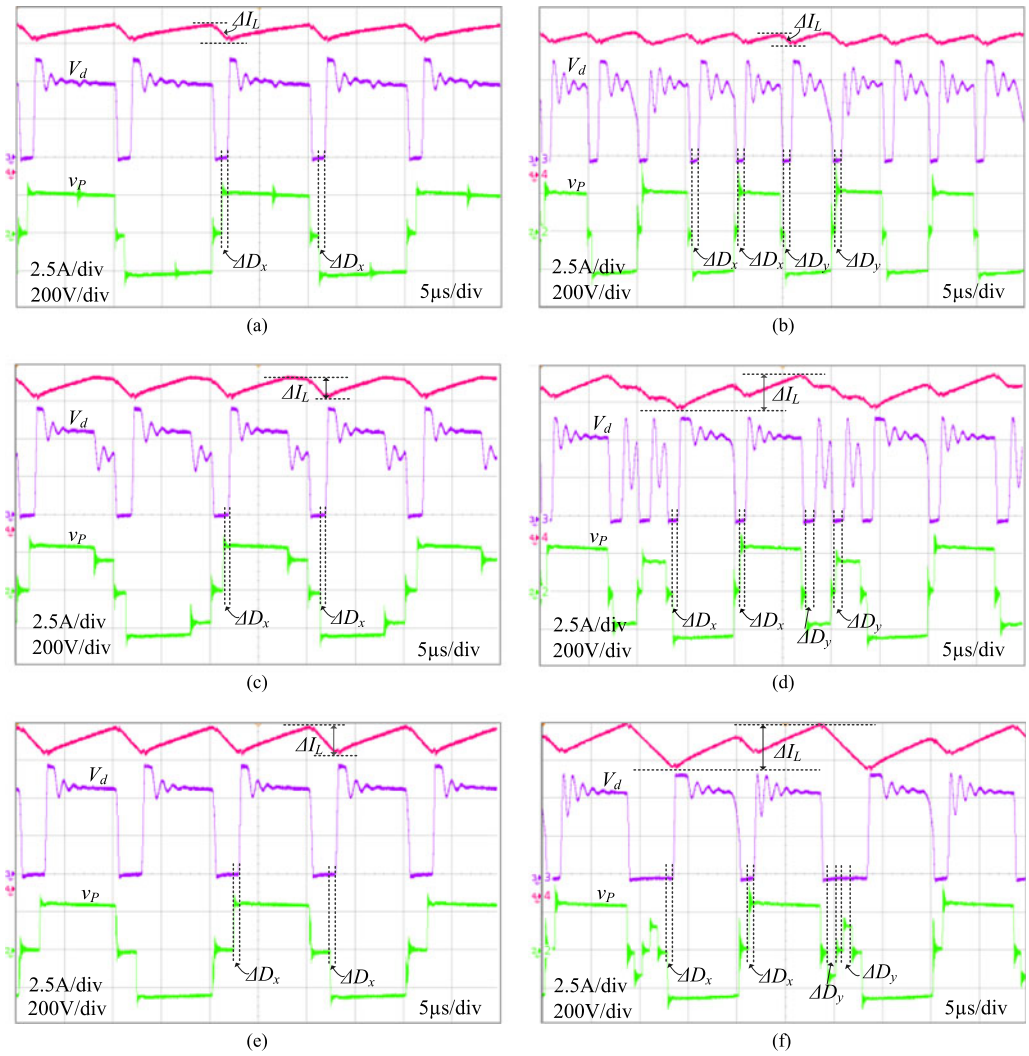

Fig. 13. Experimental waveforms of the transformer primary voltage v_P, rectifier voltage V_d, and inductor current ripple ΔI_L. (a) "Type A" at $\theta = 0°$. (b) "Type E" at $\theta = 0°$. (c) "Type A" at $-30° < \theta < 0°$. (d) "Type E" at $-30° < \theta < 0°$. (e) "Type A" at $\theta = -30°$. (f) "Type E" at $\theta = -30°$.

TABLE III
SWITCHING LOSSES COMPARISON OF "TYPE A" AND "TYPE E" PWM

PWM scheme	"Type A"	"Type E"
Number of turn-on actions with ZVS	6	6
Number of turn-on actions with non-ZVS $\left(1/2V_{ds}^{\ 2} \times C_{oss}\right)$	2	2
Number of turn-off actions with high voltage transition in the range of ($\sqrt{3}/2V_m \sim \sqrt{3}V_m$)	4	8
Number of turn-off actions with low voltage transition in the range of ($0 \sim \sqrt{3}/2V_m$)	2	0
Total turn-on losses	ignorable	ignorable
Total turn-off losses (normalize based on 6-segment)	1	1.6

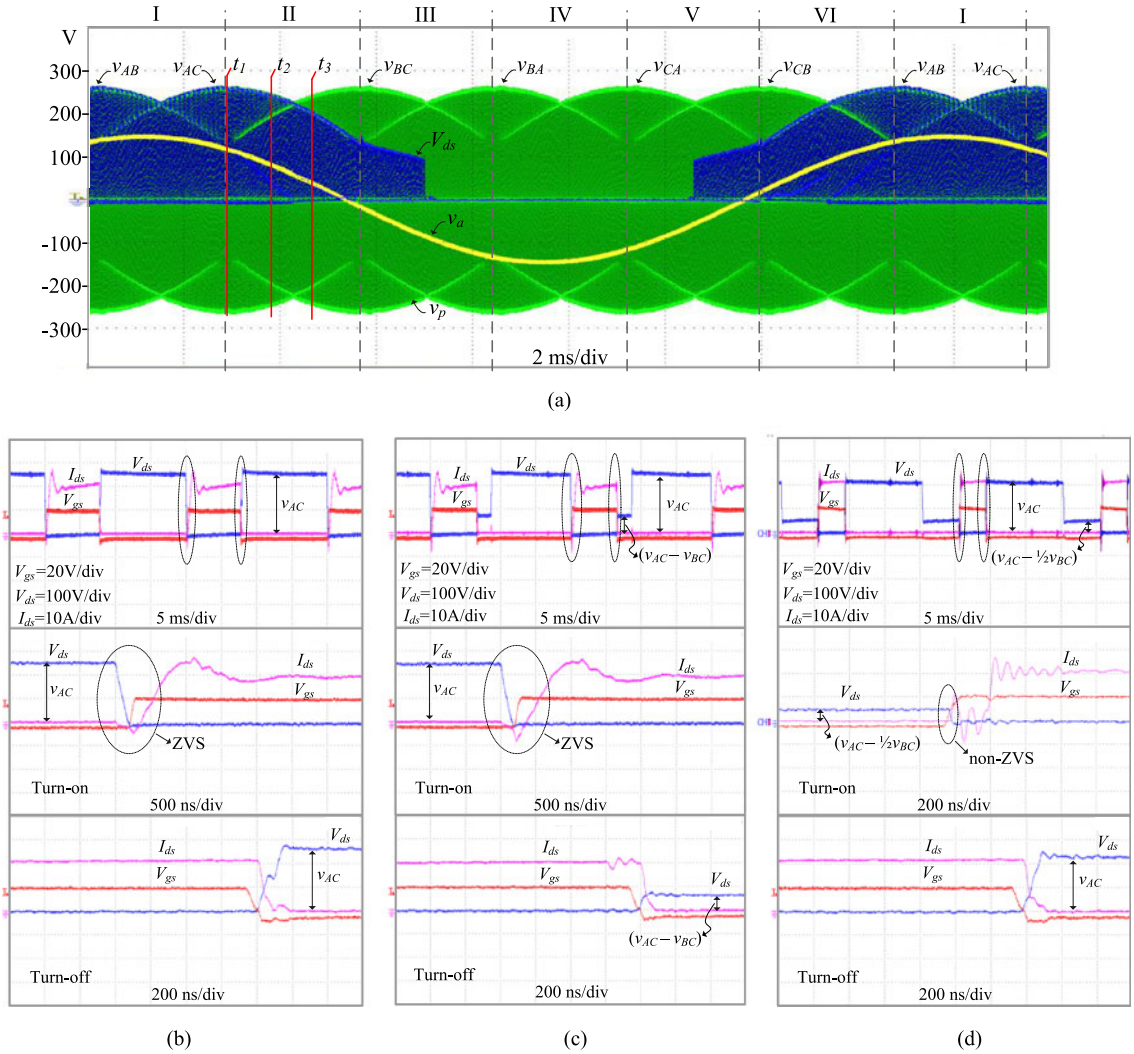

Fig. 14. Experimental waveforms for Converter MOSFETs switching behavior with "Type A" PWM implementation. (a) Voltage waveforms of v_a, v_p, and $V_{\rm ds}$ of S_{24}. (b) at t_1 the beginning of sector II. (c) at t_2 the beginning of sector II. (c) at t_3 the beginning of sector II.

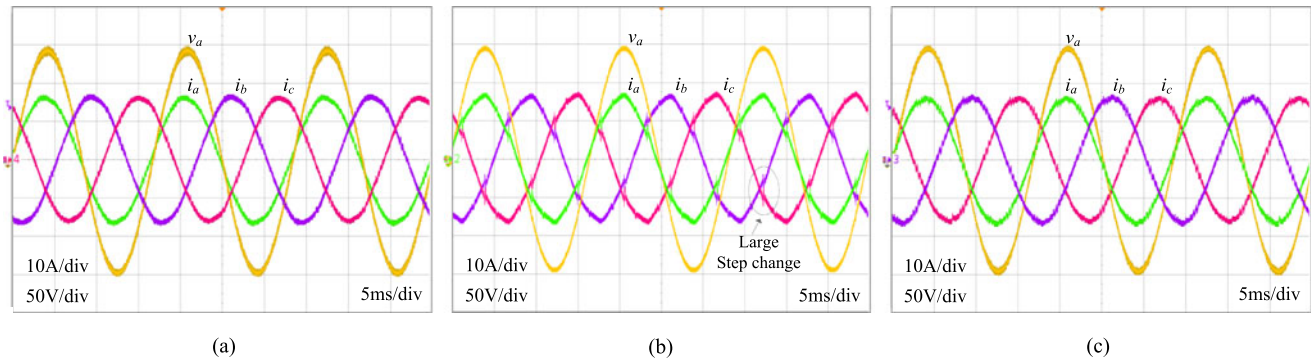

Fig. 15. Waveforms of grid voltage v_a and currents i_a, i_b, and i_c at the rated power. (a) "Type A" with duty-cycle compensation. (b) "Type A" without duty-cycle compensation. (c) "Type E" PWM.

cycle. As shown in Fig. 9(c) in the dashed line, there are eight turn-ON switching actions (four per half-cycle) and six turn-OFF switching actions (three per half-cycle). In the first half-cycle, S_{16}, S_{22}, and S_{24} are turned ON under ZVS, while S_{12} is not switched under ZVS [14, Section III-B]. Before the MOSFET S_{12} is turned ON the drain–source voltage $V_{\rm ds}$ is $(v_{AC}-1/2v_{AB})$, and it varies from 0 to $3/4V_m$ during one 30° interval, and the current i_{ds} through this switch is zero. Since S_{12} is turned ON at zero current to discharge the energy stored in output capacitance $C_{\rm oss}$ of MOSFET, the turn-ON loss $(1/2{V_{\rm ds}}^2 \times C_{\rm oss})$ should be

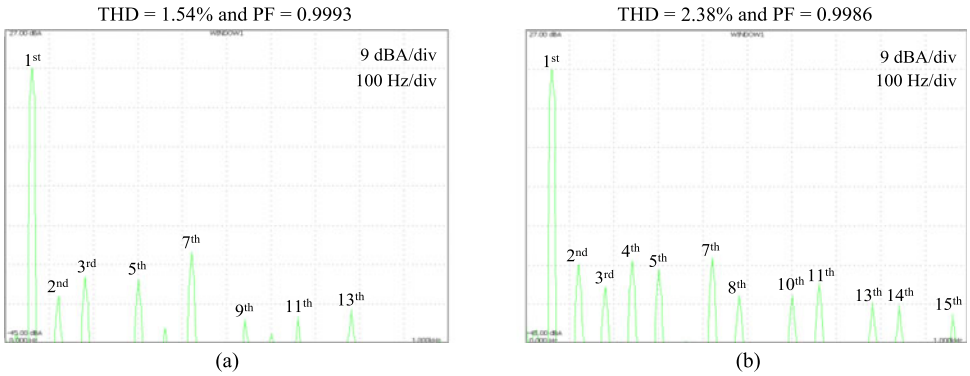

Fig. 16. Experimental spectrums of input phase current. (a) "Type A" PWM with compensation. (b) "Type E" PWM.

very small. All the three turn-OFF actions in the first half-cycle contribute to the switching losses since S_{11}, S_{16}, and S_{12} are turned OFF at full current. Switching loss is also a function of the voltage transition across the switching device. Because the voltage transition between two joint active vectors is only the difference of the two line–line voltages (as discussed for HTL transition in Section I-A), the turn-OFF loss of S_{16} corresponding to this transition is much smaller than the other two switches S_{11} and S_{12}. The number of switching actions and resulting switching losses in the second half-cycle are the same as the first half-cycle, but different switches are involved which will not be discussed here. In summary, six turn-OFF and two turn-ON actions contribute to switching losses within one switching cycle. However, these losses are very small as discussed before. For "Type E" PWM, there are eight turn-ON actions and eight turn-OFF actions within one switching cycle. As discussed in [9], among the eight turn-ON actions of "Type E" PWM, two turn-ON actions are not fully ZVS and the related switching losses are also very small. Compared with "Type A" PWM, "Type E" PWM has noticeable higher turn-OFF losses due to two reasons. First, the number of turn-OFF actions is higher. Second, all the turn-OFF actions are switched at high-voltage transition. The switching loss comparison between "Type A" and "Type E" is summarized in Table III.

IV. Experimental Results for "Type A" and "Type E" PWM

The simulation results are given in [14] and [17] to verify and validate the proposed PWM scheme ("Type A"). The experimental prototype is set up at the rated output power of 3.4 kW, $m_a = 0.8$ and regulated output voltage 345 V. Detail experimental system parameters are listed in Table IV.

1) Experimental Waveforms for Duty-Cycle Loss and Output Inductor Current Ripple

For the experimental results in Fig. 13, an RCD snubber is added to bridge rectifier in Fig. 1 to reduce the ringing and spike at the output of the bridge rectifier. The duty-cycle loss can be identified as the intervals ΔD_x and ΔD_y as shown in Fig. 13. In one cycle, the duty-cycle loss in "Type E" contains four intervals (two associated with wide pulses and two associated with narrow pulses), as shown in Fig. 13(b), (d), and (f). The duty-cycle loss of the proposed PWM only contains two intervals in one cycle as shown in Fig. 13(a), (c), and (e). In "Type E" PWM, the two intervals associated with the two wide pulses have the same duration as that of "Type A" PWM, while the other two intervals associated with the two narrower pulses have longer duration because the voltage across the transformer is lower and i_P has longer ramping time. Therefore, the total duty loss in "Type E" is more than twice of the total duty-cycle loss of the proposed "Type A" PWM. Although the operating frequency of the "Type A" PWM is only half of "Type E" PWM, the maximum output current ripple in "Type A" is lower than the "Type E" PWM by more than 20% as shown in Fig. 13(e) and (f). However, the minimum output current ripple in "Type A" is twice larger than "Type E" as shown in Fig. 13(a) and (b).

2) Converter MOSFET Switching Dynamics Behavior With "Type A" PWM Implementation

It is crucial to observe the ZVS operation of the MOSFET switches in the converter with "Type A" implementation, since the ZVS operation is an indicator of the switching loss reduction. To demonstrate the state of ZVS, one switch S_{24} on the leg "*A*" is selected, thereby showing the ZVS of all the active switches. Fig. 14(a) shows the voltage waveforms of phase "*A*" voltage v_a, the primary voltage of the transformer v_P, and the drain–source voltage $V_{\rm ds}$ of MOSFET S_{24} in six sectors operation. The MOSFET turn-ON and turn-OFF switching transitions are analyzed at three locations of t_1, t_2, and t_3 in sector II. At t_1 and t_2, S_{24} turn-ON represents the ZVS turn-ON action for the transition from zero vector to active vector, while S_{24} turn-OFF represents the turn-OFF action for the transition between the two joint active vectors. At t_3, S_{24} turn-ON represents the non-ZVS turn-ON action of the HTL transition, while S_{24} turn-OFF represents the turn-OFF action for the transition from the active vector to zero vector. As shown in Fig. 14(b) and (c), $V_{\rm ds}$ tends to zero before the gate-to-source voltage $V_{\rm gs}$ approaches high, which indicates that the body diode is ON before the turn-ON of the switch such that ZVS is realized. The non-ZVS transition is shown in Fig. 14(d). Prior to the turn-ON of this switch, the drain–source voltage $V_{\rm ds}$ of the MOSFET is very small and the current $i_{\rm ds}$ through this switch is zero. Therefore, the resulting switching loss is very low. Due to the ZVS operation, the primary-side voltage waveforms are free from high switching noise and no snubber is required. As

TABLE IV
EXPERIMENTAL PROTOTYPE PARAMETERS

Prototype Parameter	Value
C_f	10 μF
L_f	90 μH
$V_{LL,rms}$	180 V
f_{grid}	60 Hz
C_0	220 μF
L_0	450 μH
V_o	345 V
L_{lk}	5.7 μH
S_{11} - S_{26}	IPW60R041P6
D_1 - D_4	SCS215KG
n	2
T_r	Ferrite core (ZP47313TC)
f_{sw} of "Type A"	50 kHz
f_{sw} of "Type E"	100 kHz

shown in Fig. 14(b)–(d), all the turn-OFF actions contribute to the switching losses since the MOSFET is turning OFF at full current. Because the voltage transition between two joint active vectors is only the difference of the two line–line voltages $(v_{AC} - v_{AB})$ in Fig. 14(c), the turn-OFF loss at t_3 is much smaller than those at t_1 and t_2. However, the MOSFET turn-OFF produces negligible losses since the overlapping of voltage and current is very small during the turn-OFF transition.

3) Verification of the Input Current THD

Fig. 15 shows the input phase voltage and currents waveforms with "Type A" and "Type E" PWM schemes implementation. As shown in Fig. 15(b), without the duty-cycle compensation with the "Type A" PWM implementation, there are step changes in the input phase currents that are caused by swapping the duty cycle of "bridge *x*" and "bridge *y*" in the middle of each sector to achieve an HTL switching pattern. Fig. 16(a) and (b) shows the experimental spectrums of the input current obtained from the prototype with "Type A" and "Type E" implementation. The THD of the input phase current, calculated from the measurement, is 1.54% with "Type A" and 2.38% with "Type E" implementation.

V. CONCLUSION

The three-phase isolated Buck matrix-type rectifier using MOSFETS is considered as a promising topology in ac–dc applications, such as front-end power converters for HVDC and telecommunication. PWM schemes used for this topology are investigated and an optimal six-segment PWM scheme (Type A) is proposed. PWM modulation strategy and commutation for the "Type A" PWM is derived using the analysis synthesis method based on the ZVS FB-PS topology. The performance of "Type A" PWM is compared with that of the existing eight-segment PWM (Type E) based on the theoretical analysis and experimental results. "Type A" PWM features lower switching losses, a lower duty-cycle loss, and a lower maximum output inductor current ripple. Very low THD can be also achieved with duty-cycle compensation.

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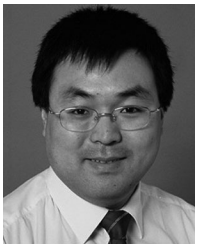

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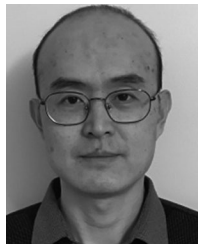

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