Investigation and Implementation of an Input-Series Auxiliary Power Supply Scheme for High-Input-Voltage Low-Power Applications

Tao Meng, *Member, IEEE*, Yilin Song, Zhongxian Wang, Hongqi Ben, and Chunyan Li

***Abstract*—Aiming at the high-input-voltage multiple-output low-power applications, an input-series two-transistor flyback auxiliary power supply scheme is proposed and investigated. In this converter, an integrated-transformer is adopted instead of the single-transformer in each series-module, all of the series-modules are operating synchronously, and the input voltage sharing (IVS) can be achieved automatically. The active IVS mechanism of this converter is analyzed, furthermore, through the influence analysis when the series-modules are operating asynchronously and the tolerance features of the key parameters are considered, the related design consideration of the input filter capacitor in each series-module is discussed. Finally, after the simulation verifications, a 60-W laboratory-made prototype of this auxiliary power supply composed of three series-modules is built, by which the feasibility of the presented scheme and the validity of the theoretical analysis are verified.**

***Index Terms*—Input-series, input voltage sharing (IVS), integrated-transformer, multiple-output auxiliary power supply, two-transistor flyback.**

I. Introduction

PRESENTLY, the applications of high dc input voltage are gradually increasing. It is well known that the large voltage stress of switches is one of the bottlenecks of the high-voltage dc/dc converters. One solution is to use series connection of power switches, but to achieve voltage balancing of each switch, some special passive or active balancing methods must be introduced, which causes the additional losses and restricts the switching frequency [1], [2]. Another solution is the adoption of multilevel dc/dc converters; however, as the number of "level" increases, the number of the clamping diodes or flying capacitors increases, and the associated control becomes more complex [3], [4]. Generally, the multilevel dc/dc converters cannot be suitable for the low-power applications. A third option is to use the input-series converters, and this option can solve the high-voltage problems efficiently [5]–[7].

For the input-series converters, the most important issues are to ensure their input voltage sharing (IVS) [8], [9]. To achieve IVS, many special control strategies have been investigated. The typical methods are as follows. In [10], a charge control technique with an input voltage feed forward is proposed. In [11] and [12], the three-loop control schemes are used, in which an additional IVS loop is involved. In [13], a sensor-less current mode controller is presented to guarantee the stable IVS. In [14], a decoupled master/slave control strategy is proposed to deal with the high-voltage auxiliary power supplies. In [15] and [16], the uniform voltage distribution control approach is employed. In [9], a wireless IVS control strategy is proposed. In [17], a decentralized inverse-droop control is presented. However, in these input-series converters, a dedicated IVS controller must be used, which results in the increasing complexity of the associated control and the decreasing reliability of the whole system. The auxiliary power supplies are designed for the low-power applications, so simplicity and high reliability of the whole system are very important.

To simplify the circuit system, some input-series converters without any special IVS controller have been investigated. In these converters, the simple common-duty-ratio control strategy is adopted, and IVS can be achieved automatically. For example, a forward converter is implemented in [18], a flyback converter is investigated in [19], and the full-bridge converters are presented in [3], [20], and [21]. However, due to the structure of their output sides, they are not suitable for the multiple-output power supplies, which is a typical low-power application.

Some input-series converters with a common integrated-transformer and a common set of output circuits have also been presented, which are suitable for multiple-output low-power applications. The typical investigations are as follows. In [22]–[24], some forward converters with two series-modules operating interleaved are investigated. In these converters, IVS can be achieved due to the volt–second balance between the two primary windings of the integrated-transformer without any additional controller. However, the number of the series-modules cannot be increased arbitrarily because of the interleaved oper-

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ating of each series-module. In [25]–[27], the converters composed of two full-bridge series-modules are presented. The two series-modules operate synchronously, and IVS can be achieved automatically. This configuration is suitable for the multiple-output low-power applications when forward or flyback topology is adopted in each series-module. However, these full-bridge converters are used in high-power applications, so their input filter capacitance is much larger, and the input voltage differences caused by the asynchronous operating of each series-module can be ignored, which cannot be ignored in the low-power applications. In [28], an auxiliary power supply composed of multiple single-transistor flyback series-modules is presented. The series-modules operate synchronously, and IVS can be achieved automatically. However, the active IVS can only be achieved in the stage when the switches are turning on, and the voltage difference of the switches may appear due to the tolerance features of the absorbing circuit in each series-module.

In this paper, based on [28], an input-series two-transistor flyback auxiliary power supply scheme is proposed, which is suitable for high-input voltage multiple-output low-power applications. In this converter, a common integrated-transformer is adopted, and IVS can be achieved automatically. Compared to the scheme in [28], the active IVS process can also be achieved in the stage after the switches are turned off, and the voltage balancing of the switches can also be achieved, therefore, it owns a higher reliability. The proposed scheme was first introduced by Meng *et al.* [29], and some more detailed analysis and experimental results are presented in this paper. The rest of this paper is organized as follows. In Section II, configuration of the auxiliary power supply is introduced, and its active IVS mechanism is analyzed. In Section III, the influence analysis is discussed when the series-modules are operating asynchronously and the tolerance features of the key parameters are considered, from which the design consideration of the input filter capacitors is analyzed. The proposed method and theoretical analysis are verified by the simulating and experimental results in Section IV. Finally, conclusions are given in Section V.

II. Proposed Converter and Its Active IVS Mechanism

The input-series two-transistor flyback auxiliary power supply scheme is shown in Fig. 1. In this configuration, all of the series-modules (the number of series-modules is *N*, $N \geq 1$) employ a common integrated-transformer T and a common set of output circuits (the number of output circuits is *n*, $n \geq 1$). V_i and I_i are the input voltage and current, $V_{i1}, V_{i2}, \ldots, V_{iN}$ are the input voltage of each series-module, $C_{i1}, C_{i2}, \ldots, C_{iN}$ ($C_{i1} = C_{i2} = \ldots = C_{iN} = C_i$) are the input filter capacitors of each series-module, $S_{11}, S_{12}, S_{21}, S_{22}, \ldots, S_{N1}, S_{N2}$ are the switches. $L_{i1}, L_{i2}, \ldots, L_{iN}$ ($L_{i1} = L_{i2} = \ldots = L_{iN} = L_i$) are the equivalent inductances in primary sides of T, $L_{o1}, L_{o2}, \ldots, L_{on}$ are the inductance in secondary sides of T, and $L_{lk1}, L_{lk2}, \ldots, L_{lkN}$ are the equivalent leakage inductance. $D_{o1}, D_{o2}, \ldots, D_{on}$ are the output rectifier diodes, $C_{o1}, C_{o2}, \ldots, C_{on}$ are the output filter capacitors, and $V_{o1}, V_{o2}, \ldots, V_{on}$ are the output voltage.

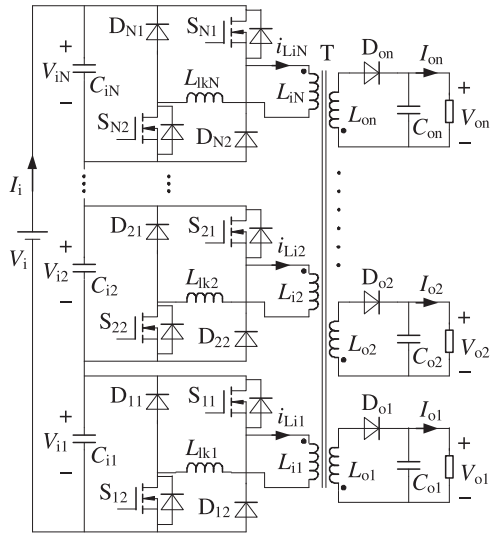

Fig. 1. Input-series two-transistor flyback power supply scheme.

The series-modules have the same parameters, and $S_{11}, S_{12}, S_{21}, S_{22}, \ldots, S_{N1}, S_{N2}$ are turned on and off synchronously. Therefore, the active IVS of each series-module can be achieved by the coupling of primary windings of the integrated-transformer T. According to the operational principle of the two-transistor flyback converter, the coupling of the primary windings will mainly appear in the following two stages during one switching period.

Stage 1 (t_0–t_1): All of the switches are turning on, and the primary inductors of T are charged by the input voltage of each series-module.

Stage 2 (t_1–t_2): All of the switches are turning off, and the energy of $L_{lk1}, L_{lk2}, \ldots, L_{lkN}$ is transferred to the input side of each series-module.

So the active IVS mechanism of each series-module should be analyzed in the above two stages. To simplify the analysis, it is assumed that: 1) the number of series-modules "N = 2" is considered; 2) the conduction resistance of each switch is ignored; and 3) the inductors in primary sides of T have a common magnetic circuit and the same number of turns, so the difference in their inductance is ignored.

A. Active IVS Mechanism in Stage 1

In stage 1, the secondary windings of T are not operating, so T is equal to a coupled-inductor. The equivalent circuit of this converter in stage 1 is shown in Fig. 2(a), where i_{Ci1-} and i_{Ci2-} are the discharging current of C_{i1} and C_{i2} ($i_{Ci1-} = i_{Li1} - I_i$, $i_{Ci2-} = i_{Li2} - I_i$), L_{i11}, L_{i22} are the self-inductances ($L_{i11} = L_{i22}$), and M_{12} is the mutual inductance. It can be obtained from the basic mathematical model of the coupled-inductor that

$$\begin{cases} V_{i1}(t) = L_{i11}\dfrac{di_{Li1}(t)}{dt} + M_{12}\dfrac{di_{Li2}(t)}{dt} \\ V_{i2}(t) = L_{i22}\dfrac{di_{Li2}(t)}{dt} + M_{12}\dfrac{di_{Li1}(t)}{dt} \end{cases} \quad (1)$$

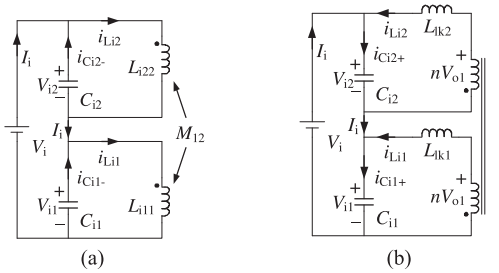

Fig. 2. Equivalent circuits. (a) Equivalent circuit in stage 1. (b) Equivalent circuit in stage 2.

where $M_{12} = kL_{\mathrm{i}11} = kL_{\mathrm{i}22}$, and k ($0 \le k \le 1$) is the coupling coefficient.

In stage 1, the primary inductors of T are charged, and it is well known that the charging process of the transformer in two-transistor flyback converter is the same as that in single-transistor flyback converter. So the IVS mechanism of this converter in stage 1 is also the same as that of the input-series single-transistor flyback converter in [28]. Generally, the flyback converter can be designed to operate in continuous conduction mode (CCM) or discontinuous conduction mode (DCM). In [28], the IVS mechanism is only analyzed for the input-series flyback converter operating in DCM in stage 1. Therefore, the common IVS mechanism of the input-series flyback converter operating in both CCM and DCM is analyzed as follows.

In stage 1, the time t_{m1} ($t_0 \le t_{m1} \le t_1$) is defined: before t_{m1}, $i_{\mathrm{Li}1} = i_{\mathrm{Li}2}$, $V_{\mathrm{i}1} = V_{\mathrm{i}2}$, and at t_{m1}, $i_{\mathrm{Li}1}(t_{m1}) = i_{\mathrm{Li}2}(t_{m1})$, $V_{\mathrm{i}1}(t_{m1}) = V_i/2 + \Delta V_i$, $V_{\mathrm{i}2}(t_{m1}) = V_i/2 - \Delta V_i$. After t_{m1}, it can be obtained from (1) that

$$\begin{cases} \dfrac{di_{Li1}(t-t_{\mathrm{m}1})}{dt} = \dfrac{V_i}{2(1+k)L_{i11}} + \dfrac{\Delta V_i(t-t_{m1})}{(1-k)L_{i11}} \\ \dfrac{di_{Li2}(t-t_{\mathrm{m}1})}{dt} = \dfrac{V_i}{2(1+k)L_{i11}} - \dfrac{\Delta V_i(t-t_{m1})}{(1-k)L_{i11}} \end{cases}. \quad (2)$$

From (2), the expressions of $i_{\mathrm{Li}1}$ and $i_{\mathrm{Li}2}$ after t_{m1} can be obtained

$$\begin{cases} i_{Li1}(t-t_{m1}) = i_{Li1}(t_{m1}) + \dfrac{V_i(t-t_{m1})}{2(1+k)L_{i11}} \\ \qquad\qquad + \int_{t_{m1}}^{t} \dfrac{\Delta V_i(t-t_{m1})}{(1-k)L_{i11}}dt \\ i_{Li2}(t-t_{m1}) = i_{Li2}(t_{m1}) + \dfrac{V_i(t-t_{m1})}{2(1+k)L_{i11}} \\ \qquad\qquad - \int_{t_{m1}}^{t} \dfrac{\Delta V_i(t-t_{m1})}{(1-k)L_{i11}}dt \end{cases}. \quad (3)$$

It can be seen from (3) that: 1) when $V_{\mathrm{i}1} > V_{\mathrm{i}2}$, $i_{\mathrm{Ci}1-} > i_{\mathrm{Ci}2-}$ ($i_{\mathrm{Ci}1-} = i_{\mathrm{Li}1} - I_i$, $i_{\mathrm{Ci}2-} = i_{\mathrm{Li}2} - I_i$) will occur, which can help accelerate the discharging of $C_{\mathrm{i}1}$ and decelerate the discharging of $C_{\mathrm{i}2}$, 2) as the coupling coefficient k increases, $i_{\mathrm{Ci}1-} - i_{\mathrm{Ci}2-}$ ($i_{\mathrm{Ci}1-} - i_{\mathrm{Ci}2-} = i_{\mathrm{Li}1} - i_{\mathrm{Li}2}$) will increase, and voltage balance between $C_{\mathrm{i}1}$ and $C_{\mathrm{i}2}$ will be achieved more easily, and 3) the sum of current in primary sides of T ($i_{\mathrm{Li}1} + i_{\mathrm{Li}2}$) is independent of ΔV_i.

For $C_{\mathrm{i}1}$, it can be obtained after t_{m1} that

$$\begin{aligned} C_i \frac{d\Delta V_i(t-t_{m1})}{dt} &= -i_{Ci1-}(t-t_{m1}) \\ &= I_i(t-t_{m1}) - i_{Li1}(t-t_{m1}) \end{aligned} \quad (4)$$

where $I_i(t-t_{m1}) = V_i(t-t_{m1})/L_{\mathrm{eq}2}$, and $L_{\mathrm{eq}2} = L_{i11} + L_{i22} + 2M_{12} = 2(1+k)L_{i11}$ is the series equivalent value of the coupled inductor.

From (3) and (4), the following differential equation can be obtained:

$$\frac{d^2\Delta V_i(t-t_{m1})}{dt^2} + \frac{1}{(1-k)L_{i11}C_i}\Delta V_i(t-t_{m1}) = 0. \quad (5)$$

Equation (5) has the initial data that: At t_{m1}, $\Delta V_{\mathrm{i}} = \Delta V_i(t_{m1})$, $i_{\mathrm{Ci}1-} = 0$. As a result, the expressions of $V_{\mathrm{i}1}$ and $V_{\mathrm{i}2}$ after t_{m1} can be obtained

$$\begin{cases} V_{\mathrm{i}1}(t-t_{m1}) = \dfrac{V_i}{2} + \Delta V_i(t_{m1})\cos\dfrac{t-t_{m1}}{\sqrt{(1-k)L_{i11}C_i}} \\ V_{\mathrm{i}2}(t-t_{m1}) = \dfrac{V_i}{2} - \Delta V_i(t_{m1})\cos\dfrac{t-t_{m1}}{\sqrt{(1-k)L_{i11}C_i}} \end{cases}. \quad (6)$$

From the aforesaid analysis, it can be seen that: whether the input-series flyback converter operates in CCM or DCM, the IVS mechanism in stage 1 is nearly identical.

B. Active IVS Mechanism in Stage 2

The equivalent circuit of this converter in stage 2 is shown in Fig. 2(b), where $i_{\mathrm{Ci}1+}$ and $i_{\mathrm{Ci}2+}$ are the charging current of $C_{\mathrm{i}1}$ and $C_{\mathrm{i}2}$ ($i_{\mathrm{Ci}1+} = i_{\mathrm{Li}1} + I_{\mathrm{i}}$, $i_{\mathrm{Ci}2+} = i_{\mathrm{Li}2} + I_i$). In this stage, the energy in primary side of T has been transferred to the secondary side, and the voltage of each primary winding is fixed at $nV_{\mathrm{o}1}$ (n is the turn ratio of T).

In stage 2, the time t_{m2} ($t_1 \le t_{m2} \le t_2$) is defined: before t_{m2}, $i_{\mathrm{Li}1} = i_{\mathrm{Li}2}$, $V_{\mathrm{i}1} = V_{\mathrm{i}2}$, and at t_{m2}, $i_{\mathrm{Li}1}(t_{m2}) = i_{\mathrm{Li}2}(t_{m2})$, $V_{\mathrm{i}1}(t_{m2}) = V_i/2 + \Delta V_i$, $V_{\mathrm{i}2}(t_{m2}) = V_i/2 - \Delta V_i$. After t_{m2}, the following relationships can be obtained:

$$\begin{cases} i_{\mathrm{Li}1}(t-t_{m2}) = i_{\mathrm{Li}1}(t_{m2}) - \int_{t_{m2}}^{t} \dfrac{V_{\mathrm{i}1}(t-t_{m2}) - nV_{\mathrm{o}1}}{L_{\mathrm{lk}}}dt \\ i_{\mathrm{Li}2}(t-t_{m2}) = i_{\mathrm{Li}2}(t_{m2}) - \int_{t_{m2}}^{t} \dfrac{V_{\mathrm{i}2}(t-t_{m2}) - nV_{\mathrm{o}1}}{L_{\mathrm{lk}}}dt \end{cases}. \quad (7)$$

The difference of inductance is ignored, so it is considered that: $L_{\mathrm{lk}1} = L_{\mathrm{lk}2} = L_{\mathrm{lk}}$.

From (7), it can be calculated that

$$\begin{cases} i_{\mathrm{Li}1}(t-t_{m2}) = i_{\mathrm{Li}1}(t_{m2}) \\ \qquad\qquad - \int_{t_{m2}}^{t} \dfrac{V_{\mathrm{i}} + 2\Delta V_{\mathrm{i}}(t-t_{m2}) - 2nV_{\mathrm{o}1}}{2L_{\mathrm{lk}}}dt \\ i_{\mathrm{Li}2}(t-t_{m2}) = i_{\mathrm{Li}2}(t_{m2}) \\ \qquad\qquad - \int_{t_{m2}}^{t} \dfrac{V_{\mathrm{i}} - 2\Delta V_{\mathrm{i}}(t-t_{m2}) - 2nV_{\mathrm{o}1}}{2L_{\mathrm{lk}}}dt \end{cases} \quad (8)$$

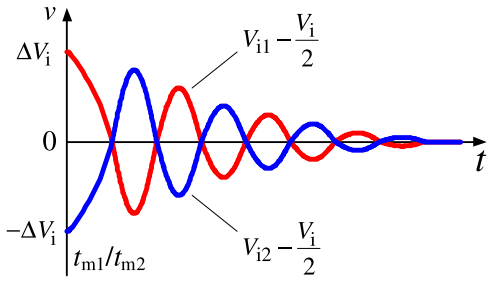

Fig. 3. IVS process in stage 1 or stage 2.

$$i_{\mathrm{Li1}}(t-t_{m2})+i_{\mathrm{Li2}}(t-t_{m2})=i_{\mathrm{Li1}}(t_{m2})+i_{\mathrm{Li2}}(t_{m2})-\frac{V_{\mathrm{i}}-2nV_{\mathrm{o1}}}{L_{\mathrm{lk}}}(t-t_{m2}) \tag{9}$$

$$i_{\mathrm{Ci1+}}(t-t_{m2})-i_{\mathrm{Ci2+}}(t-t_{m2})=-\int_{t_{m2}}^{t}\frac{2\Delta V_i(t-t_{m2})}{L_{\mathrm{lk}}}dt. \tag{10}$$

It can be seen from (9) that: the sum of current in primary sides of T after t_{m2} is independent of ΔV_i. From (10), it can be seen after t_{m2} that: 1) when $V_{\mathrm{i1}} > V_{\mathrm{i2}}$, $i_{\mathrm{Ci1+}} < i_{\mathrm{Ci2+}}$ will occur, which can help decelerate the charging of C_{i1} and accelerate the charging of C_{i2}, and 2) as the equivalent leakage inductance L_{lk} decreases, $i_{\mathrm{Ci2+}} - i_{\mathrm{Ci1+}}$ will increase, and voltage balance between C_{i1} and C_{i2} will be achieved more easily after t_{m2}.

For C_{i1}, it can be obtained after t_{m2} that

$$C_i\frac{d\Delta V_i(t-t_{m2})}{dt}=i_{\mathrm{Ci1+}}(t-t_{m2})=i_{\mathrm{Li1}}(t-t_{m2})+I_i(t-t_{m2}). \tag{11}$$

The expression of I_i after t_{m2} can be calculated

$$I_i(t-t_{m2})=-i_{\mathrm{Li1}}(t_{m2})+\frac{V_i-2nV_{o1}}{2L_{\mathrm{lk}}}(t-t_{m2}). \tag{12}$$

From (8), (11), and (12), the following differential equation is obtained:

$$\frac{d^2\Delta V_i(t-t_{m2})}{dt^2}+\frac{1}{L_{\mathrm{lk}}C_i}\Delta V_i(t-t_{m2})=0. \tag{13}$$

Equation (13) has the following initial data: at t_{m2}, $\Delta V_i = \Delta V_i(t_{\mathrm{m2}})$, $i_{\mathrm{Ci1+}} = 0$. As a result, the expressions of V_{i1} and V_{i2} after t_{m2} can be obtained

$$\begin{cases} V_{\mathrm{i1}}(t-t_{m2})=\dfrac{V_i}{2}+\Delta V_i(t_{m2})\cos\dfrac{t-t_{m2}}{\sqrt{L_{\mathrm{lk}}C_i}} \\ V_{\mathrm{i2}}(t-t_{m2})=\dfrac{V_i}{2}-\Delta V_i(t_{m2})\cos\dfrac{t-t_{m2}}{\sqrt{L_{\mathrm{lk}}C_i}} \end{cases}. \tag{14}$$

From (6) and (14), the IVS process of this converter in stage 1 and stage 2 can be obtained as shown in Fig. 3. It can be seen that if there is a difference between V_{i1} and V_{i2}, the high-frequency resonances will appear in the above two stages, and their resonant frequency expressions are shown in (15). However, their amplitudes decrease in each resonant period due to the resistance of each series-module

$$f_{r1}=\frac{1}{2\pi\sqrt{(1-k)L_{\mathrm{i11}}C_i}},\quad f_{r2}=\frac{1}{2\pi\sqrt{L_{\mathrm{lk}}C_i}}. \tag{15}$$

It can be seen that the voltage balance of the series-modules will be achieved more speedily as the coupling coefficient k increases or the equivalent leakage inductance L_{lk} decreases.

From the aforesaid analysis, it can be seen that: the active IVS of this converter can be achieved through the coupling of windings in primary sides of the integrated-transformer, and IVS can be realized more efficiently as the coupling coefficient k increases or the equivalent leakage inductance L_{lk} decreases. It can also be seen that the IVS process of this converter cannot be affected by its output circuits in secondary side of the integrated-transformer, and IVS of this converter can also be achieved when the power of its output circuits are unequal. Furthermore, for the two-transistor flyback converter, the maximum voltage of the switches is equal to its input voltage, so the voltage balancing of the switches in this converter can also be achieved.

III. Analysis and Design

From the aforesaid analysis, it can be seen that IVS of the series-modules can be realized automatically when the input voltage difference appears, however, the current difference of the primary inductors appears in the IVS process. For the converter with two series-modules, the instantaneous current difference can be calculated approximately

$$\Delta I_{\mathrm{Li12}}=\frac{2\Delta V_i}{R_1+R_2} \tag{16}$$

where R_1 and R_2 are the equivalent resistance of the two series-modules, in which conduction resistance of the switches and resistance of the primary inductors are included.

It can be seen from (16) that the current difference (ΔI_{Li12}) between the two primary inductors appears due to the input voltage difference (ΔV_i) of each series-module, and ΔI_{Li12} will increase as ΔV_i increases. If ΔI_{Li12} is large enough, the efficiency of this converter will decrease obviously because the series-module with a lower input voltage becomes a load for the other series-module. Therefore, the input voltage difference should be avoided or suppressed when the converter operating.

In Section II, the IVS is analyzed in ideal conditions, and it is assumed that the series-modules have the same parameters and the switches are operating synchronously. Generally, the input voltage difference will not appear in ideal conditions. In actual fact, due to the tolerance features of the devices in each series-module and the driving circuits of the switches, the parameters in each series-module cannot be identical absolutely and the switches cannot be achieved turning on or off at the same time. Therefore, the suppression of the input voltage difference should be analyzed in the real conditions.

A. Analysis When the Series-Modules are Operating Asynchronously

The switches are turned on at t_0 and turned off at t_1.

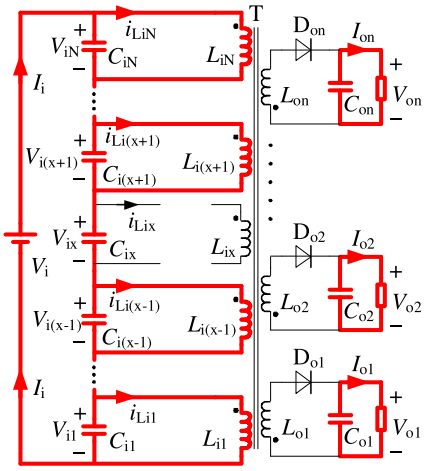

Fig. 4. Equivalent circuit when the series-modules are operating asynchronously.

First, it is assumed before t_0 that: $V_{\mathrm{i}1} = V_{\mathrm{i}2} = \ldots = V_{iN} = V_i/\mathrm{N}$. At t_0, the turning on signal is generated for each switch. After t_0, the input voltage of the series-modules with the switches turning on will decrease, the input voltage of the series-modules with the switches turning off will increase, and the maximum input voltage appears in the series-module with the two switches being turned on finally. It is defined that: the maximum difference of the turning on time among the switches in the series-modules is ΔT_{on}. The most serious input over voltage of the series-module with the last two turning on switches ($\mathrm{S}_{\mathrm{x}1}$ and S_{x2}, $\mathrm{x} = 1, 2, \ldots, \mathrm{N}$) will appear when all of the other switches are turned on synchronously at t_0, and $\mathrm{S}_{\mathrm{x}1}$, $\mathrm{S}_{\mathrm{x}2}$ are turned on at $t_0 + \Delta T_{\mathrm{on}}$.

Second, it is assumed before t_1 that: $V_{\mathrm{i}1} = V_{\mathrm{i}2} = \ldots = V_{iN} = V_i/\mathrm{N}$. At t_1, the turning off signal is generated for each switch. After t_1, the input voltage of the series-modules with the switches turning on will decrease, the input voltage of the series-modules with the switches turning off will increase, and the maximum input voltage appears in the series-module with the two switches being turned off first. It is defined that: the maximum difference of the turning off time among the switches in the series-modules is ΔT_{off}. The most serious input over voltage of the series-module with the first two turning off switches ($\mathrm{S}_{\mathrm{x}1}$ and $\mathrm{S}_{\mathrm{x}2}$, $\mathrm{x} = 1, 2, \ldots, \mathrm{N}$) will appear when all of the other switches are turned off synchronously at $t_1 + \Delta T_{\mathrm{off}}$, and $\mathrm{S}_{\mathrm{x}1}$, $\mathrm{S}_{\mathrm{x}2}$ are turned off at t_1.

The equivalent circuit of this converter when the series-modules are operating asynchronously is shown in Fig. 4, where $k = 1$ is considered, and the difference of turning on and off time between the two switches in the same series-module is ignored.

The influence in this converter when the series-modules are operating asynchronously is the same as that in the input-series single-transistor flyback converter in [28], so the analyzing process is not given here again.

According to the related analysis in [28], the input voltage of the series-module with the maximum input over voltage after t_0

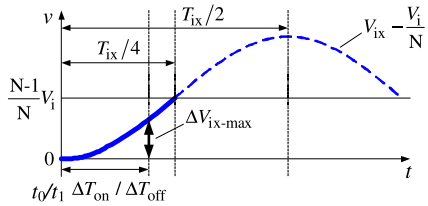

Fig. 5. Varying curve of V_{ix} after t_0 and t_1.

and t_1 can be calculated approximately

$$V_{\mathrm{ix}}(t-t_0) = \frac{V_i}{\mathrm{N}} + \frac{\mathrm{N}-1}{\mathrm{N}}V_i\left(1-\cos\frac{t-t_0}{\sqrt{(\mathrm{N}-1)L_iC_i}}\right) + I_i(t_0)\sqrt{\frac{(\mathrm{N}-1)L_i}{C_i}}\sin\frac{t-t_1}{\sqrt{(\mathrm{N}-1)L_iC_i}} \tag{17}$$

$$V_{\mathrm{ix}}(t-t_1) = \frac{V_i}{\mathrm{N}} + \frac{\mathrm{N}-1}{\mathrm{N}}V_i\left(1-\cos\frac{t-t_1}{\sqrt{(\mathrm{N}-1)L_iC_i}}\right) + I_i(t_1)\sqrt{\frac{(\mathrm{N}-1)L_{\mathrm{i}}}{C_i}}\sin\frac{t-t_1}{\sqrt{(\mathrm{N}-1)L_iC_i}}. \tag{18}$$

In (17), if this converter operates in DCM, $I_i(t_0) = 0$, and if this converter operates in CCM, $I_i(t_0) > 0$. This converter is mainly used in the high-input-voltage low-power applications, the latter items of (17) and (18) are much smaller than their former items, so the increasing of V_{ix} after t_0 and t_1 can be shown in Fig. 5 approximately.

Generally, the value of V_{ix} cannot be larger than that of V_i, therefore, the resonances in (17) and (18) can only occur in its first quarter period, and it must be achieved that

$$\Delta T_{\mathrm{on/off}} \le \frac{T_{\mathrm{ix}}}{4} = \frac{\pi}{2}\sqrt{(\mathrm{N}-1)L_iC_i}. \tag{19}$$

It can be seen from (17), (18) and Fig. 5 that the input voltage differences will appear when the switches are turned on or off asynchronously, and the maximum input over voltage ($\Delta V_{\mathrm{ix-max}}$) will increase as the turning on or off differences of the switches (ΔT_{on}, ΔT_{off}) increase.

B. Analysis When the Tolerance Features of the Key Parameters are Considered

In Section II, it is considered that the parameters in each series-module are identical, such as $C_{\mathrm{i}1} = C_{\mathrm{i}2} = \ldots = C_{iN} = C_i$, and $L_{\mathrm{i}1} = L_{\mathrm{i}2} = \ldots = L_{iN} = L_i$. However, due to the tolerance features, the capacitances and inductances cannot be exactly the same. If the mismatches of both the input filter capacitance and primary inductance are considered, the input voltage difference of each series-module will appear. The related influence is analyzed as follows.

During a very short time before t_0, it is assumed that there is no difference between $V_{\mathrm{i}1}$ and $V_{\mathrm{i}2}$ ("N = 2" is also considered here). As shown in Fig. 2(a), after t_0, I_i and $i_{\mathrm{Li}1}$, $i_{\mathrm{Li}2}$ can be

calculated as follows:

$$I_i(t-t_0) = I_i(t_0) + \frac{V_i}{L_{i1}+L_{i2}}(t-t_0) \tag{20}$$

$$\begin{cases} i_{Li1}(t-t_0) = i_{Li1}(t_0) + \int_{t_0}^{t} \dfrac{V_{i1}(t-t_0)}{L_{i1}}dt \\ i_{Li2}(t-t_0) = i_{Li2}(t_0) + \int_{t_0}^{t} \dfrac{V_{i2}(t-t_0)}{L_{i2}}dt \end{cases}. \tag{21}$$

In (20) and (21), it can be seen that: if this converter operates in DCM, $I_i(t_0) = i_{Li1}(t_0) = i_{Li2}(t_0) = 0$, and if this converter operates in CCM, $I_i(t_0) = i_{Li1}(t_0) = i_{Li2}(t_0) > 0$.

For the capacitors C_{i1} and C_{i2}, the following relationships can be obtained:

$$\begin{cases} C_{i1}\dfrac{dV_{i1}(t-t_0)}{dt} = -i_{Ci1-}(t-t_0) = I_i(t-t_0) \\ \qquad\qquad\qquad\qquad - i_{Li1}(t-t_0) \\ C_{i2}\dfrac{dV_{i2}(t-t_0)}{dt} = -i_{Ci2-}(t-t_0) = I_i(t-t_0) \\ \qquad\qquad\qquad\qquad - i_{Li2}(t-t_0) \end{cases}. \tag{22}$$

From (20)–(22), two differential equations can be obtained

$$\begin{cases} \frac{d^2V_{i1}(t-t_0)}{dt^2} + \dfrac{V_{i1}(t-t_0)}{L_{i1}C_{i1}} = \dfrac{V_i}{(L_{i1}+L_{i2})C_{i1}} \\ \dfrac{d^2V_{i2}(t-t_0)}{dt^2} + \dfrac{V_{i2}(t-t_0)}{L_{i2}C_{i2}} = \dfrac{V_i}{(L_{i1}+L_{i2})C_{i2}} \end{cases}. \tag{23}$$

Equation (23) has the following initial data: at t_0, $V_{i1} = V_{i1} = V_i/2$, $i_{Ci1-} = i_{Ci2-} = 0$. As a result, the solutions of (23) are:

$$\begin{cases} V_{i1}(t-t_0) = \dfrac{V_i}{2} + \dfrac{V_i}{2}\dfrac{L_{i1}-L_{i2}}{L_{i1}+L_{i2}}\left(1-\cos\dfrac{t-t_0}{\sqrt{L_{i1}C_{i1}}}\right) \\ V_{i2}(t-t_0) = \dfrac{V_i}{2} - \dfrac{V_i}{2}\dfrac{L_{i1}-L_{i2}}{L_{i1}+L_{i2}}\left(1-\cos\dfrac{t-t_0}{\sqrt{L_{i2}C_{i2}}}\right) \end{cases}. \tag{24}$$

From (24), it can be seen that if the tolerance features of C_{i1}, C_{i2} and L_{i1}, L_{i2} are considered, the input voltage difference will appear after t_0. If the active IVS process is not considered, the expression of input voltage difference after t_0 can be calculated

$$V_{i1}(t-t_0) - V_{i2}(t-t_0) = \frac{V_i}{2}\frac{L_{i1}-L_{i2}}{L_{i1}+L_{i2}}\left(2-\cos\frac{t-t_0}{\sqrt{L_{i1}C_{i1}}} - \cos\frac{t-t_0}{\sqrt{L_{i2}C_{i2}}}\right). \tag{25}$$

From (24) and (25), the varying curves of V_{i1}, V_{i2} can be obtained as shown in Fig. 6, where T_{i1} and T_{i2} are the resonance periods as shown in (26), it is believed that T_{i1} (or T_{i2}) is much larger than the turning on time of the switches. It can be seen that the difference between V_{i1} and V_{i2} is caused by the differences between C_{i1} and C_{i2}, L_{i1} and L_{i2}, and the difference between V_{i1} and V_{i2} will increase as the difference between C_{i1} and C_{i2} (or L_{i1} and L_{i2}) increases

$$T_{i1} = 2\pi\sqrt{L_{i1}C_{i1}}, \quad T_{i2} = 2\pi\sqrt{L_{i2}C_{i2}}. \tag{26}$$

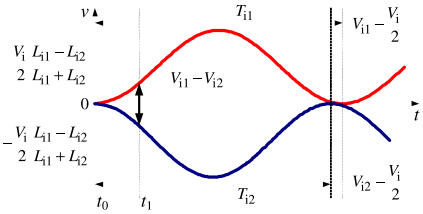

Fig. 6. Difference between V_{i1} and V_{i2} after t_0.

C. Design Considerations

In the series-modules, the switches cannot be achieved turning on or off at the same time, and the parameters cannot be identical absolutely, therefore, the input voltage difference of each series-module will appear which cannot be avoided.

From (17), (18) and Fig. 5, it can be seen that if ΔT_{on} and ΔT_{off} are constant, as the resonance period (T_{ix}) increases, the maximum input over voltage (ΔV_{ix-max}) will decrease. As shown in (19), T_{ix} is determined by the parameters N, L_i ,and C_i. However, N is designed according to the input voltage and voltage stress of the switches selected in each series-module, and L_i is also a key parameter for the flyback converter. Therefore, only the value of input filter capacitance C_i can be designed to suppress the input voltage difference when the series-modules are operating asynchronously.

Similarly, it can be seen from (24), (25) and Fig. 6 that for a constant duration from t_0 to t_1, the input voltage difference between V_{i1} and V_{i2} ($V_{i1} - V_{i2}$) will decrease as the resonance periods (T_{i1}, T_{i2}) increase. As shown in (26), the values of L_{i1}, L_{i2} are the key parameters in their series-module, therefore, only the value of input filter capacitance can be designed to suppress the input voltage difference between V_{i1} and V_{i2}.

Therefore, for a limitation of the input voltage differences, there must be a limitation of a minimum value (C_{imin}) for the input filter capacitors which can be determined according to (17), (18), (24), and (25). However, based on the limitation $C_i \geq C_{imin}$, C_i should also be designed according to the other requirements of the conventional flyback converter.

IV. Simulating and Experimental Verifications

To verify the proposed method and the theoretical analysis, the related input voltage simulation of this converter has been done in this section. Based on the simulation, the experimental verifications have also been done on a laboratory-made prototype of the proposed auxiliary power supply, which is operating in DCM. The main circuit parameters and the main utilized components' type in the prototype are follows:

1) input voltage V_i: 1000–2200 Vdc (aiming at the 1140-V frequency converter of a miner as an auxiliary power supply, the input voltage will be larger than 2000 V when the motor is operating in generating mode);
2) output voltage and current: $V_{o1} = V_{o2} = 24$ V, $I_{o1} = 1.5$ A, $I_{o2} = 1$ A, and $P_{omax} = 60$ W;
3) the series-modules number: $N = 3$ ("N = 2" is selected in the simulation);

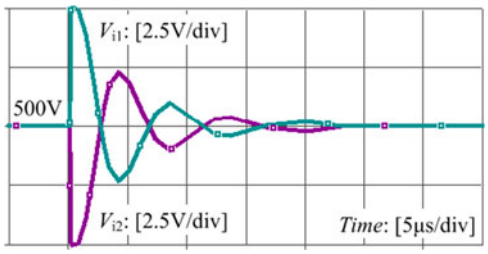

Fig. 7. Waveforms of V_{i1} and V_{i2} when $\Delta V_i = 5$ V appearing.

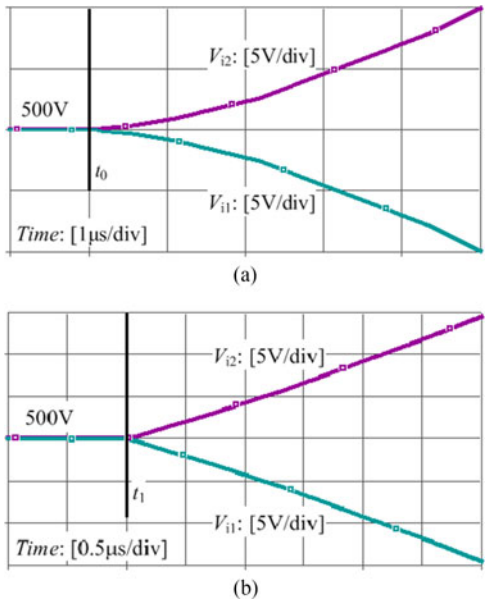

Fig. 8. Simulating results when the switches are turned on and off asynchronously. (a) Waveforms of V_{i1} and V_{i2} when $\Delta T_{on} = 5$ μs. (b) Waveforms of V_{i1} and V_{i2} when $\Delta T_{off} = 3$ μs.

4) input filter capacitors: $C_{i1} = C_{i2} = C_{i3} = 0.1$ μF (1200 V/104);
5) switches S_{11}, S_{12}, S_{21}, S_{22}, S_{31}, S_{32}: K1271 (NEC), switching frequency f: 50 kHz;
6) diodes D_{11}, D_{12}, D_{21}, D_{22}, D_{31}, D_{32}: BYV26G (Philips);
7) the flyback integrated-transformer T: Ferroxcube, EE35, $L_{i1} = L_{i2} = L_{i3} = 8712$ μH, the turns ratio $n = 11$, and $k \approx 0.99$;
8) the rectifier diodes D_{o1}, D_{o2}: MUR1520 (Onsemi);
9) the output filter capacitors $C_{o1} = C_{o2} = 1000$ μF.

A. Simulating Results

The series-modules number "$N = 2$" is considered in the simulation. Figs. 7–9 show the simulating results of this converter, where $V_i = 1000$ V.

Fig. 7 shows the varying of V_{i1} and V_{i2} when an input voltage difference ($\Delta V_i = 5$ V) occurs between C_{i1} and C_{i2}. It can be seen that the IVS of this converter can be achieved automatically when input voltage difference appearing.

Fig. 8 shows the varying of V_{i1} and V_{i2} when the two series-modules are operating asynchronously. It can be seen that the input voltage differences will appear when the switches are turned on or off asynchronously, which will increase as the turning on or off differences of the switches (ΔT_{on}, ΔT_{off}) increase.

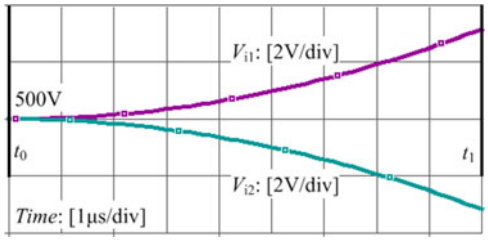

Fig. 9. Waveforms of V_{i1} and V_{i2} when $C_{i2} = 0.8C_{i1}$ and $L_{i2} = 0.8L_{i1}$.

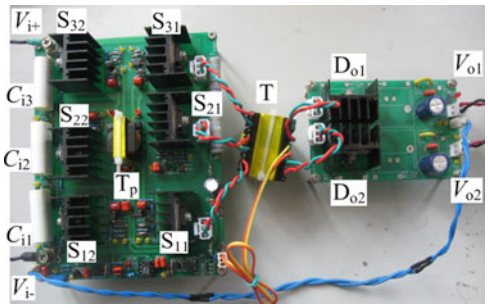

Fig. 10. Photo of the prototype.

Fig. 9 shows the varying of V_{i1} and V_{i2} when $C_{i2} = 0.8C_{i1}$, $L_{i2} = 0.8L_{i1}$ and the active IVS process is not considered. It can be seen that the difference between V_{i1} and V_{i2} appears when the key parameters of the two series-modules are not identical, and for a constant duration from t_0 to t_1, the input voltage difference will decrease as the vary periods of V_{i1} and V_{i2} (T_{i1}, T_{i2}) increase.

B. Experimental Results

The laboratory-made prototype of this converter is shown in Fig. 10, where the series-modules number "$N = 3$" is selected. In this prototype, a peak current mode controller is adopted, and V_{o1} (the output circuit with larger power) and i_{S12} (the current of S_{12}) are input to the controller, which generates a common PWM signal with a suitable duty ratio for the isolated driving circuits of S_{11}, S_{12}, S_{21}, S_{22}, S_{31}, and S_{32}. To minimize the turning on and off differences of the switches, a common pulse transformer (T_p) is adopted in driving circuits, of which a common primary winding and six secondary windings are used. The control strategy of this prototype is similar to that in [28], so the control block diagram is not given here again.

Table I shows the input voltage of three series-modules and the efficiency results of the prototype, where the input voltage results are measured by a dc voltmeter with the prototype operating under full load ($P_o = 60$ W). It can be seen that: the input voltage differences of the prototype are very small, IVS has been achieve efficiently, and it shows a good performance in conversion efficiency, which is similar to that of the conventional low-power two-transistor flyback converter.

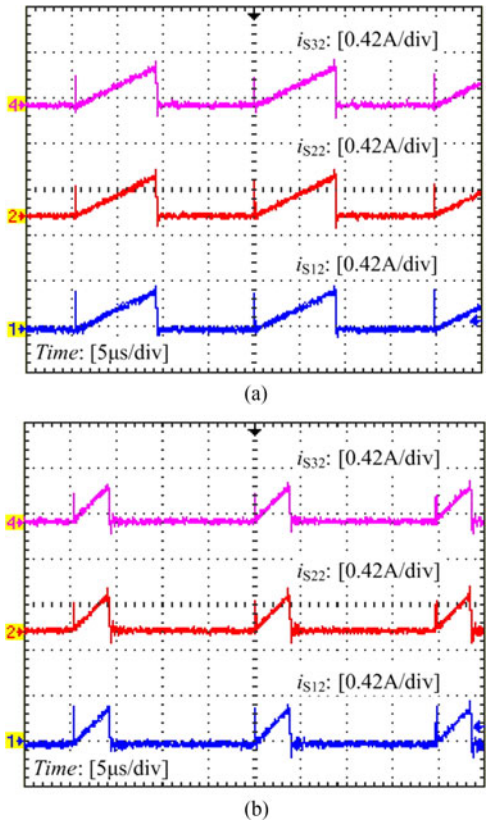

Fig. 11. Current waveforms of S_{12}, S_{22}, S_{32}. (a) When $V_i = 1000$ V. (b) When $V_i \approx 2200$ V.

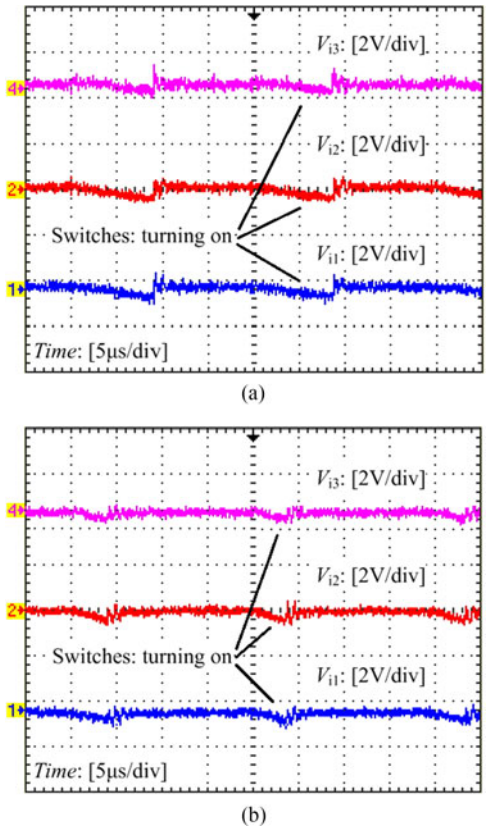

Fig. 12. Input voltage waveforms of the three series-modules (ac coupling). (a) When $V_i = 1000$ V. (b) When $V_i \approx 2200$ V.

TABLE I
EXPERIMENTAL DATA

V_i/kV	1.0	1.2	1.4	1.6	1.8	2.0	2.2
V_{i1}/V	334	400	467	533	600	666	733
V_{i2}/V	333	399	466	533	600	666	734
V_{i3}/V	333	400	466	534	600	667	733
η/% ($P_o = 16$ W)	64.59	64.71	63.24	61.98	62.07	62.01	61.54
η/% ($P_o = 38$ W)	85.57	85.86	85.42	85.50	85.78	85.08	84.78
η/% ($P_o = 60$ W)	88.50	89.73	89.22	89.01	88.86	88.49	88.22

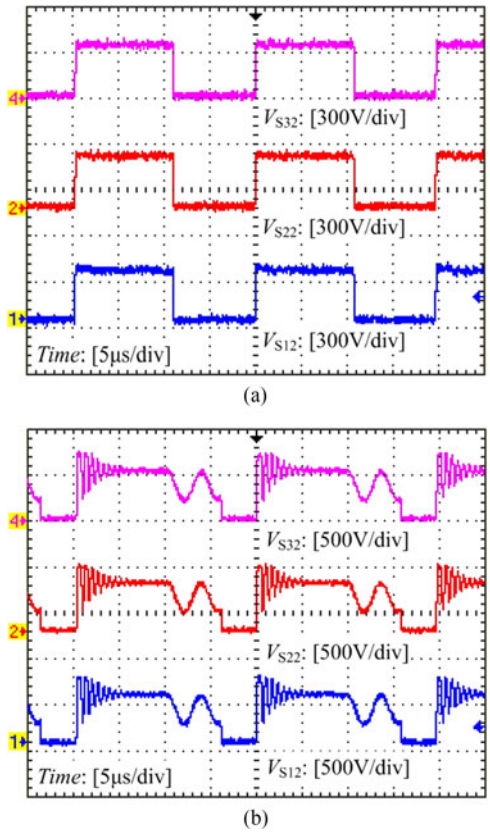

Fig. 13. Voltage waveforms of S_{12}, S_{22}, S_{32}. (a) When $V_i = 1000$ V. (b) When $V_i \approx 2200$ V.

Figs. 11–13 show the experimental results of the prototype operating under full load ($P_o = 60$ W).

Fig. 11 shows the current waveforms of S_{12}, S_{22}, S_{32} when $V_i = 1000$ V and $V_i \approx 2200$ V. It can be seen that there are no obvious differences among the current waveforms, which proves that the switches are turned on and off nearly synchronously. Fig. 12 shows input voltage waveforms (ac coupling) of the three series-modules when $V_i = 1000$ V and $V_i \approx 2200$ V. It can be seen that there are small differences among the three voltage waveforms, which is caused by the active IVS process of each series-module. However, the voltage differences are very small, which can be ignored when compared with the input voltage of each series-module. Moreover, it can be seen from Fig. 11 that there are no obvious current spike appearing during the IVS process, which proves that the prototype has a high reliability.

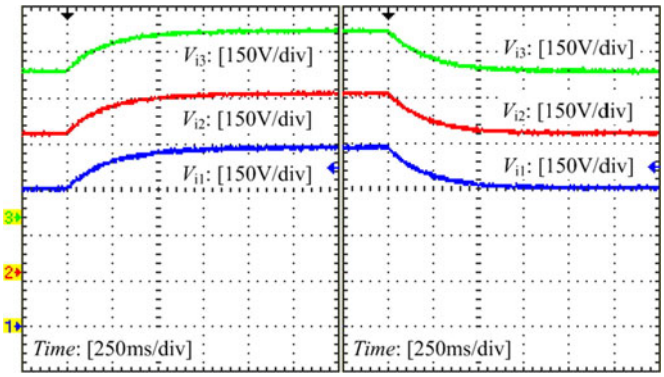

Fig. 14. Response of input voltage in the three series-modules when the input voltage $V_{\rm i}$ is changing.

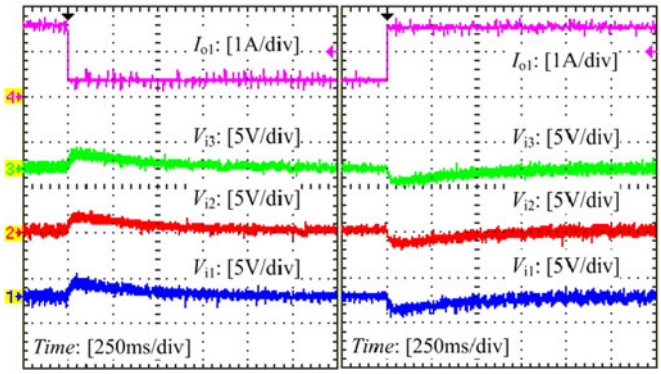

Fig. 15. Response of input voltage in the three series-modules (ac coupling) to a stepped load of the main output when $V_i \approx 1600$ V.

Fig. 13 shows the voltage waveforms of S_{12}, S_{22}, S_{32} when $V_i = 1000$ V and $V_i \approx 2200$ V. It can be seen that there are almost no differences among the three voltage waveforms and the voltage balancing of the switches in each series-module has be realized as well as the IVS of this prototype. It can be seen from Fig. 13(b) that there are two oscillations on each voltage waveform. The higher frequency one appears when the energy of leakage inductor is absorbed, which is due to the resonance between the leakage inductor and the parasitic capacitors in switches and diodes. The lower frequency one appears when the current in secondary side of T reduces to zero, which is due to the resonance between the primary inductor and the parasitic capacitors in switches and diodes. The two oscillations occur in each series-module, which are similar to those in the conventional two-transistor flyback converter.

Fig. 14 shows the input voltage waveforms of three series-modules when V_i is changing. Fig. 15 shows the input voltage waveforms (ac coupling) of the three series-modules corresponding to a load stepped in the output circuit 1 between the state $I_{o1} = 0.32$ A and the state $I_{o1} = 1.5$ A when $V_i \approx 1600$ V and $I_{o2} = 1$ A. Because there is a bulk capacitor connected in parallel with the dc bus of the former equipment, which is used to provide a high dc voltage (V_i) for this prototype, so V_i cannot be changed speedily, and it will also vary slightly with the load stepping. It can be seen that the changing processes of the three input voltage are identical, and IVS of the prototype has been achieved efficiently in the transient state.

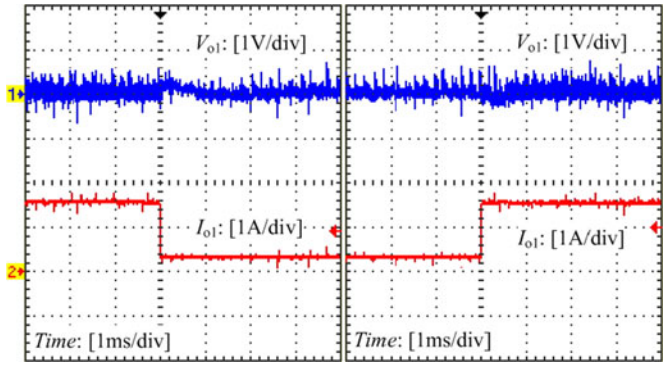

Fig. 16. Response of the main output voltage (ac coupling) to the stepped of its load current when $V_i \approx 1600$ V and $I_{o2} = 1$ A.

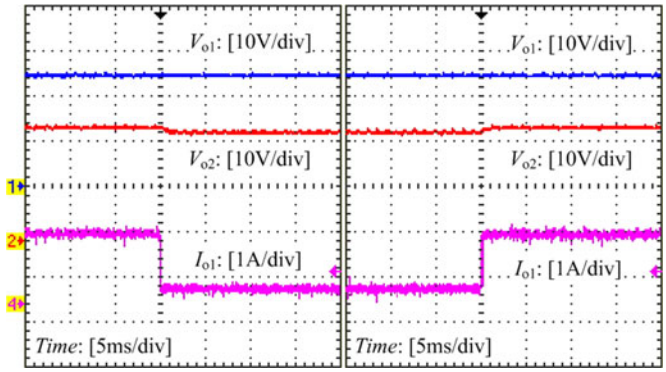

Fig. 17. Waveforms of V_{o1} and V_{o2} to the stepped change of I_{o1} when $V_i \approx 1600$ V and $I_{o2} = 1$ A.

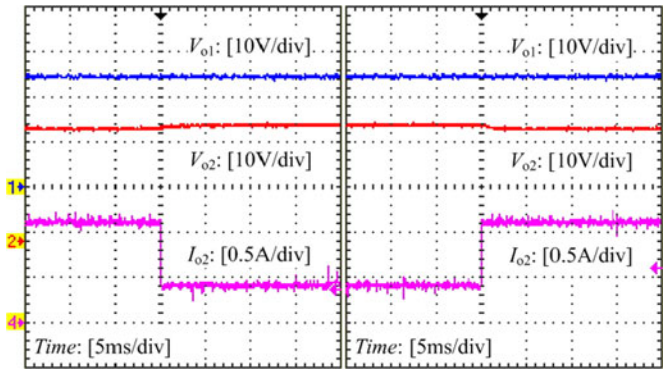

Fig. 18. Waveforms of V_{o1} and V_{o2} to the stepped change of I_{o2} when $V_i \approx 1600$ V and $I_{o1} = 1.5$ A.

Fig. 16 shows the waveforms of output voltage V_{o1} (ac coupling) to the stepped of its load current between the state $I_{o1} = 0.32$ A and the state $I_{o1} = 1.5$ A when $V_i \approx 1600$ V and $I_{o2} = 1$ A. It can be seen that the prototype shows a good performance of the output voltage regulation with the adoption of a peak current mode controller.

Fig. 17 shows the waveforms of output voltage V_{o1} and V_{o2} to a load stepped in the output circuit 1 between the state

$I_{o1} = 0.32$ A and the state $I_{o1} = 1.5$ A when $V_i \approx 1600$ V and $I_{o2} = 1$ A. Fig. 18 shows the waveforms of output voltage V_{o1} and V_{o2} to a load stepped in the output circuit 2 between the state $I_{o2} = 0.35$ A and the state $I_{o2} = 1$ A when $V_i \approx 1600$ V and $I_{o1} = 1.5$ A. It can be seen that the prototype shows a good performance of the multiple-output voltage cross-regulation feature, which is a well-known advantage of the conventional multiple-output flyback converter.

V. Conclusion

An input-series two-transistor flyback auxiliary power supply scheme is proposed and investigated, which is suitable for the high-input-voltage multiple-output low-power applications. This converter has an integrated-transformer, and all of the series-modules are operating synchronously. The active IVS process is analyzed in the two stages when the switches are turning on and off, which shows that active IVS of the series-modules can be achieved efficiently through the coupling of primary windings of the flyback integrated-transformer. Through the influence analysis on IVS effect when the series-modules are operating asynchronously and when the tolerance feature of the key parameters are considered, a minimum limitation of the input filter capacitance is obtained. Finally, the feasibility and validity of the proposed scheme and the theoretical analysis are verified by the simulating and experimental results.

References

[1] T. C. Lim, B. W. Williams, S. J. Finney, and P. R. Palmer, "Series-connected IGBTs using active voltage control technique," *IEEE Trans. Power Electron.*, vol. 28, no. 8, pp. 4083–4103, Aug. 2013.

[2] C. Abbate, G. Busatto, and F. Iannuzzo, "High-voltage, high-performance switch using series-connected IGBTs," *IEEE Trans. Power Electron.*, vol. 25, no. 9, pp. 2450–2459, Sep. 2010.

[3] J. J. Shi, J. Luo, and X. N. He, "Common-duty-ratio control of input-series output-parallel connected phase-shift full-bridge DC-DC converter modules," *IEEE Trans. Power Electron.*, vol. 26, no. 11, pp. 3318–3329, Nov. 2011.

[4] D. S. Sha, Z. Q. Guo, and X. Z. Liao, "Digital control strategy for input-series-output parallel modular DC/DC converters," *J. Power Electron.*, vol. 10, no. 3, pp. 245–250, May 2010.

[5] S. J. Chen, S. P. Yang, and M. F. Cho, "Analysis and implementation of an interleaved series input parallel output active clamp forward converter," *IET Power Electron*., vol. 6, no. 4, pp. 774–782, Apr. 2013.

[6] T. Z. Fang, X. B. Ruan, and C. K. Tse, "Control strategy to achieve input and output voltage sharing for input-series-output-series-connected inverter systems," *IEEE Trans. Power Electron.*, vol. 25, no. 6, pp. 1585–1596, Jun. 2010.

[7] X. B. Ruan *et al.*, "Control strategy for input-series-output-parallel converters," *IEEE Trans. Ind. Electron.*, vol. 56, no. 4, pp. 1174–1185, Apr. 2009.

[8] A. J. B. Bottion and I. Barbi, "Input-series and output-series connected modular output capacitor full-bridge PWM DC-DC converter," *IEEE Trans. Ind. Electron.*, vol. 62, no. 10, pp. 6213–6221, Oct. 2015.

[9] W. Chen, G. J. Wang, X. B. Ruan, W. Jiang, and W. Gu, "Wireless input-voltage-sharing control strategy for input-series output-parallel (ISOP) system based on positive output-voltage gradient method," *IEEE Trans. Ind. Electron.*, vol. 61, no. 11, pp. 6022–6030, Nov. 2014.

[10] J. W. Kim, J. S. You, and B. H. Cho, "Modeling, control, and design of input-series-output-parallel-connected converter for high-speed-train power system," *IEEE Trans. Ind. Electron.*, vol. 48, no. 3, pp. 536–544, Jun. 2001.

[11] R. Ayyanar, R. Giri, and N. Mohan, "Active input-voltage and load-current sharing in input-series and output-parallel connected modular DC-DC converters using dynamic input-voltage reference scheme," *IEEE Trans. Power Electron.*, vol. 19, no. 6, pp. 1462–1473, Nov. 2004.

[12] W. Chen, K. Zhuang, and X. B. Ruan, "A input-series- and output-parallel-connected inverter system for high-input-voltage applications," *IEEE Trans. Power Electron.*, vol. 24, no. 9, pp. 2127–2137, Sep. 2009.

[13] J. W. Kimball, J. T. Mossoba, and P. T. Krein, "A stabilizing, high-performance controller for input series-output parallel converters," *IEEE Trans. Power Electron.*, vol. 23, no. 3, pp. 1416–1427, May 2008.

[14] P. J. Grbovic, "Master/slave control of input-series- and output-parallel-connected converters: Concept for low-cost high-voltage auxiliary power supplies," *IEEE Trans. Power Electron.*, vol. 24, no. 2, pp. 316–328, Feb. 2009.

[15] K. Siri, M. Willhoff, and K. Conner, "Uniform voltage distribution control for series connected DC-DC converters," *IEEE Trans. Power Electron.*, vol. 22, no. 4, pp. 1269–1279, Jul. 2007.

[16] K. Siri, M. Willhoff, H. Hu, and I. Batarseh, "High-voltage-input, low-voltage-output, series-connected converters with uniform voltage distribution," in *Proc. IEEE Energy Convers. Congr. Expo.*, 2009, pp. 541–547

[17] G. Xu, D. S. Shang, and X. Z. Liao, "Decentralized inverse-droop control for input-series-output-parallel DC-DC converters," *IEEE Trans. Power Electron.*, vol. 30, no. 9, pp. 4621–4625, Sep. 2015.

[18] R. Giri, V. Choudhary, R. Ayyanar, and N. Mohan, "Common-duty-ration control of input-series connected modular DC-DC converters with active input voltage and load-current sharing," *IEEE Trans. Ind. Appl.*, vol. 42, no. 4, pp. 1101–1111, Jul./Aug. 2006.

[19] S. Zong, Q. L. Zhu, W. S. Yu, and A. Q. Huang, "Auxiliary power supply for solid state transformer with ultra high voltage capacitive driving," in *Proc. IEEE Appl. Power Electron. Conf. Expo.*, 2015, pp. 1008–1013.

[20] A. J. B. Bottion and I. Barbi, "Input-series and output-series connected modular full-bridge PWM DC-DC converter with capacitive output filter and common duty cycle," in *Proc. IEEE Ind. Appl. Soc. Annu. Meeting*, 2014, pp. 1–8.

[21] Q. W. Lu, Z. J. Yang, S. Lin, S. K. Wang, and C. Wang, "Research on voltage sharing for input-series-output-series phase-shift full-bridge converters with common-duty-ratio," in *Proc. IEEE Annu. Conf. Ind. Electon.*, 2009, pp. 1548–1553.

[22] R. T. Bascope and I. Barbi, "A double ZVS-PWM active-clamping forward converter: analysis, design, and experimentation," *IEEE Trans. Power Electron.*, vol. 16, no. 6, pp. 745–751, Nov. 2001.

[23] D. V. Ghodke and K. Muralikrishnan, "ZVZCS, dual, two-transistor forward DC-DC converter with peak voltage of Vin/2, high input and high power application," in *Proc. IEEE Power Electron. Spec. Conf.*, 2002, pp. 1853–1858.

[24] X. J. Ma, W. Wang, Y. Kang, and J. Chen, "Series of two transistors forward ZVZCS converter with phase-shift control for high input voltage," in *Proc. IEEE Annu. Conf. Ind. Electon.*, 2004, pp. 761–766.

[25] M. Miller, A. Buffin, and U. Carlsson, "High frequency ZVS for high power rectifiers," in *Proc. IEEE Int. Telecomm. Conf.*, 1993, pp. 424–430.

[26] D. S. Sha, Z. Q. Guo, and X. Z. Liao, "Input-series connected high frequency DC-DC converters with one transformer," in *Proc. IEEE Appl. Power Electron. Conf. Expo.*, 2010, pp. 662–665.

[27] X. Q. Song, D. S. Sha, and X. Z. Liao, "Input-series common transformer connected PS-FB DC-DC converters for pulsed MIG welding," in *Proc. IEEE Appl. Power Electron. Conf. Expo.*, 2012, pp. 2195–2199.

[28] T. Meng, C. Y. Li, H. Q. Ben, and, J. B. Zhao, "An input-series flyback auxiliary power supply scheme based on transformer-integration for high-input-voltage applications," *IEEE Trans. Power Electron.*, vol. 31, no. 9, pp. 6383–6393, Sep. 2016.

[29] T. Meng, C. Y. Li, H. Q. Ben, X. S. Wang, and, J. B. Zhao, "An input-series multiple-output auxiliary DC/DC converter," in *Proc. IEEE Int. Power Electron. Motion Control Conf.*, 2016, pp. 3056–3060.

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