Gate Driving Circuit With Active Pull-Down Function for a Solid-State Pulsed Power Modulator

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***Abstract*—This paper proposes a new gate driving circuit for the solid-state pulsed power modulator (SSPPM) based on semiconductor devices. The proposed circuit can be easily implemented by applying a short gate signal to the bypass insulated gate bipolar transistor (IGBT), i.e., switches connected in parallel with the load instead of a pull-down resistor. The IGBT_BPs are turned ON at the end-point of the pulse. It can quickly discharge the pulse voltage applied to the load. In addition, it can operate as bypass diode, which is used to protect the semiconductor switches when the gate signal malfunctions, by using the antiparallel diode of the IGBT. Moreover, power loss in the pull-down resistor used to achieve fast falling pulses can be eliminated by turning OFF the IGBT while applying the pulse state. Thus, the proposed circuit can be used for implementing SSPPM with small values of falling time and high efficiency. The circuit configuration, operational principle, relevant analysis results, and a PSpice modeling are presented and verified by the 10-kV SSPPM.**

***Index Terms*—Fast falling time, gate driving circuit, pulsed power applications, solid-state pulsed power modulator (SSPPM).**

I. Introduction

RECENTLY, research on a solid-state pulsed power modulator (SSPPM) has increased for highly repetitive and/or long pulse width pulsed-power applications such as in water or gas treatment, plasma-source ion implantation, linear particle accelerators, klystrons, magnetrons, and gyrotrons [1]–[6]. The SSPPM is clearly more suitable for pulsed power applications compared with a pulsed power modulator using mechanical switches because of its long lifespan, ease in controlling the pulse width/repetition, and rectangular pulse waveforms [7]–[12].

The basic configuration of the SSPPM is divided into three forms such as high-voltage direct switching (HVDS) method, using a step-up transformer for high-voltage pulse, and power cell-based solid-state pulse modulator. The HVDS method offers advantages such as a simple structure and compact design of the SSPPM. However, it is very difficult to design and requires complex circuit to protect the semiconductor devices from the frequent arcing condition of load, which occurs frequently during the pulsed-power application. The advantage of the SSPPM implemented using the step-up transformer is that it can apply a high-voltage pulse to the load with a relatively low primary voltage, even though the rising time of the pulse is limited because of the leakage inductance of the transformer and additional circuit is required to prevent transformer saturation. In addition, the size of the power supply increases because of the additional pulse transformer, and the pulse width variation is limited [11], [12]. At present, the power cell-based pulsed power modulator is widely used for SSPPM [13]. It has many advantages such as fast rising time of the pulse voltage and is capable of generating a high-voltage output pulse using a capacitor charger with a relatively low output voltage rating. In addition, it can protect the main semiconductor switches during the malfunctioning of the synchronization of switches. Inversely, serial stacking of the semiconductor switch is required, and the pull-down resistor is required in highly repetitive and/or long pulse width applications for small falling time [14]–[18].

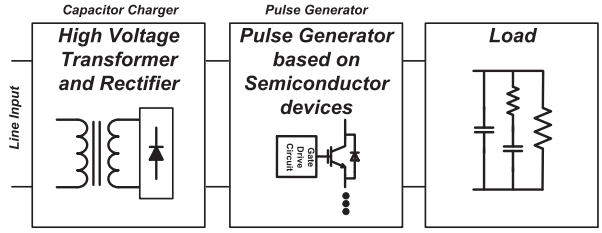

Fig. 1. Basic structure of the solid-state pulsed power modulator system.

The power cell-based pulsed power modulator is composed of the capacitor charger part and pulse generator part as shown in Fig. 1. Generally, the real load consists of resistors and capacitors in pulsed power applications. The main insulated gate bipolar transistor (IGBT) in the pulse generator part is used to apply pulse to the load, and the bypass diode is used to protect the main IGBT during malfunctioning of the gate signal. The gate driving circuit was developed to obtain a synchronized and isolated power supply for the main IGBT [19]. In [19], the gate driving circuit has good synchronization characteristics and the power supply to the main IGBT is isolated.

Meanwhile, the load in pulsed power applications is composed of a capacitor and resistor. It causes limitation of the repetitive rate and slow falling time of the pulse because the applied pulse voltage to the load is stored in the load capacitor.

Manuscript received July 12, 2016; revised December 22, 2016; accepted February 13, 2017. Date of publication February 23, 2017; date of current version October 6, 2017. This work was supported by the Korea Electrotechnology Research Institute Primary research program through the National Research Council of Science & Technology funded by the Ministry of Science, ICT and Future Planning under Grant 17-12-N0101-23. Recommended for publication by Associate Editor Jesus A. Oliver

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Digital Object Identifier 10.1109/TPEL.2017.2673000

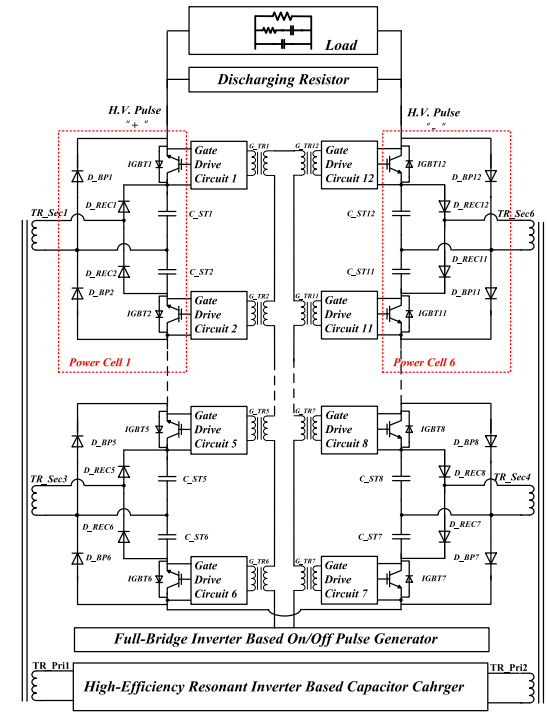
To solve this problem, connecting a pull-down resistor with load in parallel is a well-known method. The pull-down resistor can discharge the applied voltage to the load. Thus, it can achieve fast falling time of the pulse voltage. However, additional loss in the pull-down resistor occurs because the current continuously flows through the pull-down resistor during pulse ON state. It is sharply increased according to increase pulse width and repetitive rate. Therefore, the high power resistor, which has large size due to high power, is needed. Furthermore, the additional utility of high-voltage isolation is required for applying real applications because the pull-down resistor is installed in parallel with real load. It causes increased complexity of the system as well as additional loss. To overcome large losses, the push–pull circuit is considered to achieve fast falling time without additional loss [20]. In this method, the pull-down resistor is changed by simple stacked switches. It can achieve fast falling time without the pull-down resistor. Therefore, there is no additional loss from the pull-down resistor. However, the SSPPM with push pull circuit has complex structure due to following reasons. First, the external circuit for voltage balancing is required in this method. In case of simple stacked switches, there is a lot of voltage difference between each switch from manufacturing error which causes variety junction capacitance of switches. Accordingly, the simple stacked switches must have to use external balancing circuit for reliable operation. Second, the additional circuit is also needed to protect main switches. Without protection circuit, total output voltage applied to the asynchronous switch when gating signal synchronization fails. It makes main switch broken.

In this paper, a new gate driving circuit and power cell structure are proposed. In case of the SSPPM with proposed circuit, it can be easily implemented by replacing the bypass diode with the bypass IGBT (IGBT_BP). Also, the IGBT_BP can be simply operated by the proposed gate driver by using the ON/OFF signal that is used for operating the main IGBT. Therefore, IGBT_BP turn ON at the end of pulse to achieve fast falling time. Moreover, the additional loss generated by the pull-down resistor is eliminated by turning OFF the IGBT_BP during the applied pulse state. Furthermore, the voltage balancing problem does not occur due to power cell structure which clamps the voltage between switch at the voltage of one output capacitor as well as protecting their main IGBT.

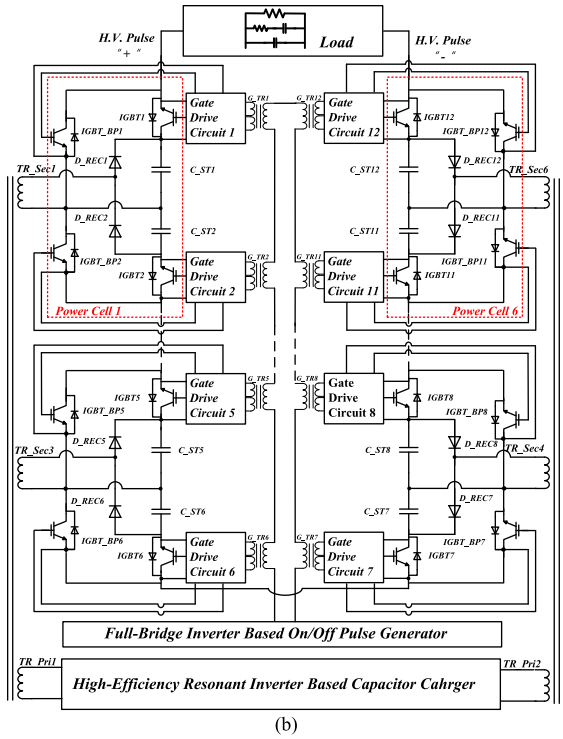
II. Proposed Circuit

A. Concept

Fig. 2 shows the overall structure of the 10-kV SSPPM. It mainly consists of the high-efficiency series resonant-type capacitor charger inverter with six power cells connected in series and charged through a power loop transformer. Each power cell consists of voltage-doubled rectifier, two main IGBT, and components for protecting the main IGBTs. The power cell can be charged in parallel through primary winding at 1600 V. Then, charged voltage in the power cell can be discharged in series to the load by turning ON the main IGBTs. When several switches are malfunctioning due to synchronization problems, voltage of the asynchronous main IGBT is clamped at one output capacitor



(a)



(b)

Fig. 2. Overall structure of the solid-state pulsed power. (a) Schematic of the conventional SSPPM-based 10-kV modulator. (b) Schematic of the SSPPM with the 10-kV modulator based on the proposed circuit.

voltage due to bypass path. The detailed operation of protecting main IGBT is mentioned in Section III-C. As shown in Fig. 2(a), in the conventional SSPPM, bypass diodes (D_BP1-D_BP12) are used to protect the main IGBT during the malfunctioning of the gate signal and the pull-down resistor is connected in

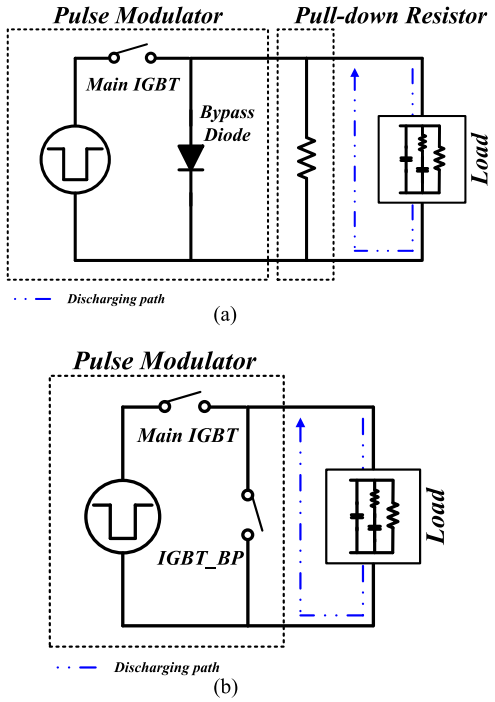


Fig. 3. Discharge path of the stored energy in the capacitive load after applying pulse. (a) Conventional circuit. (b) Proposed circuit.

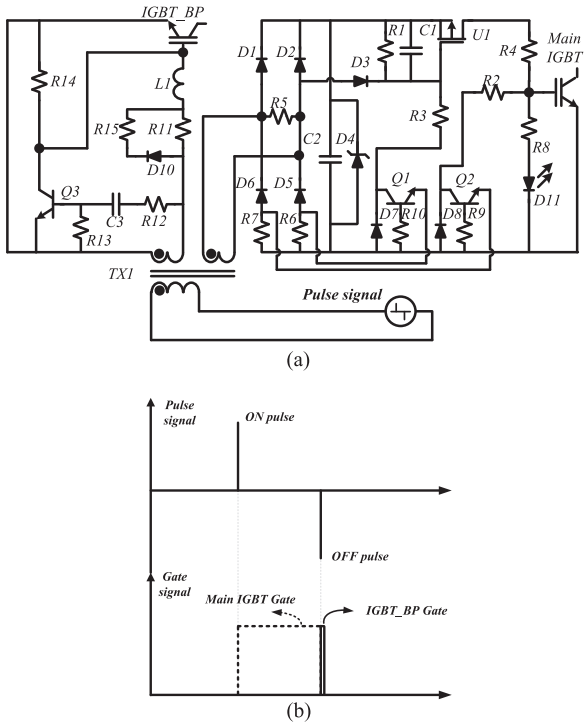


Fig. 4. Schematic of the proposed gate driver circuit. (a) Proposed gate driver circuit. (b) Waveforms of ON/OFF pulse signal, gate signal of the main IGBT, and gate signal of the IGBT_BP.

parallel with the load to achieve fast falling of the pulse. On the other hand, the SSPPM with the proposed circuit replaces the bypass diode with the IGBT_BPs as shown in Fig. 2(b). Thus, the SSPPM with proposed circuit is easily implemented by changing bypass diode to IGBT with proposed gate driver circuit in power cell. Therefore, it can help to achieve fast falling time without drawbacks caused by the discharging resistor.

The applied pulse voltage in the load capacitance has to discharge quickly for fast falling of the pulse. Fig. 3 shows the discharging path of the pulse voltage in the simplified conventional and proposed circuits. In the conventional circuit, the pull-down resistor is connected in parallel with the load for discharging the pulse voltage quickly. In this method, the current continuously flows thorough the pull-down resistor during pulse ON state as well as discharging voltage applied to the load. Therefore, a high power pull-down resistor is required and additional loss is generated. The proposed circuit uses the IGBT_BP for achieving fast-falling pulse without the pull-down resistor as shown in Fig. 3(b). In proposed method, the current only flows at the end point of the pulse to discharge voltage applied to the load. The IGBT_BP is turned ON at the end of the pulse voltage. It can discharge the pulse voltage quickly. Moreover, it can eliminate the additional loss from the pull-down resistor.

B. Operational Principle of Gate Driving Circuit

Fig. 4 shows the schematic of the proposed gate driver and the basic waveforms of the gate signal and ON–OFF pulse signal. The main concept of the proposed gate driving circuit is that the turn-ON pulse signal is transferred to charge the C2 designed for the turn-ON hold mode and the main IGBT input capacitance simultaneously via the transformer TX1. In this case, only one power source can be used for synchronizing the gate signals of a number of series-connected main IGBT stack and IGBT_BP stack. Hence, two problems concerning the isolated gate driver and synchronized gating signal are solved. Furthermore, the gate driver for the added IGBT_BPs is easily implemented using a simple circuit that uses the same pulse signal for driving the main IGBTs. Thus, it contributes toward decreasing the falling time as well as eliminating the additional loss from the pull-down resistor. The operational principle can be analyzed based on the operation modes, as shown in Fig. 5.

1) Turn-ON pulse mode—When a turn-ON pulse signal is applied to the TX1, C2 is charged with a clamped voltage by the zener diode. Simultaneously, C1 is also charged so that U1 can conduct at the same time, and Q2 conducts sequentially. Finally, the voltage across R8 is applied to the input capacitor of the main IGBT. Therefore, the main IGBT switch conducts. Meanwhile, the gate signal of the IGBT_BP is turned OFF.
2) Turn-ON hold mode—Once the U1 is made to conduct, the drain-to-source resistance of U1 is low enough to allow the main IGBT to conduct because of the energy stored in C2. Even though high instantaneous current is supplied during the turn-ON pulse mode, the total power consumption in the gate driver is low. Therefore, the capacitance of C2 can also be used to keep the main IGBT turned ON during the turn-ON hold mode. In this mode, the IGBT_BP is still turned OFF.
3) Turn-OFF pulse mode—During the turn-OFF pulse mode, C2 continues to charge through D2 and D6. On the other

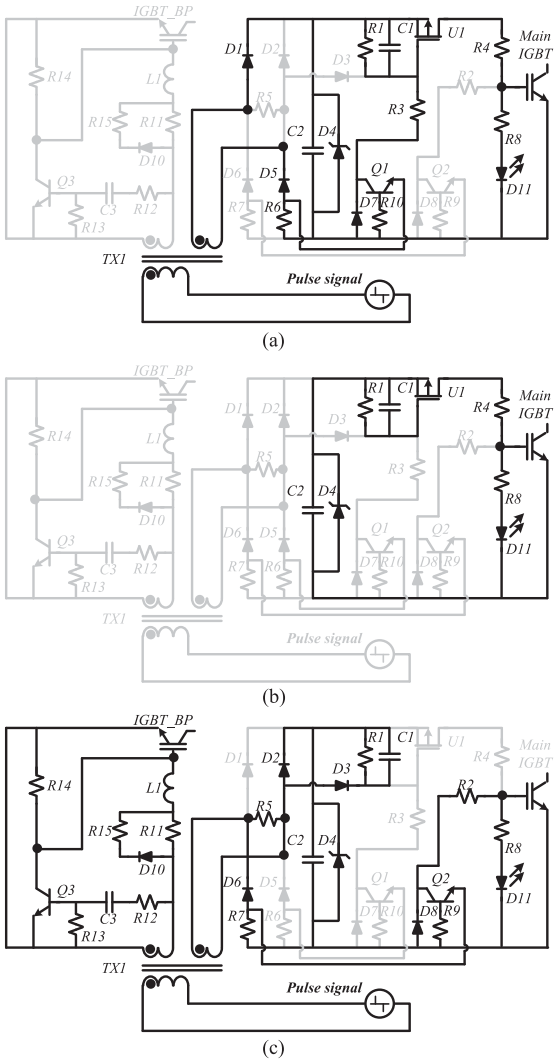


Fig. 5. Operation modes of the proposed gate driver circuit. (a) Turn-ON pulse mode. (b) Turn-ON hold mode. (c) Turn-OFF pulse mode.

hand, C1 is discharged through D3 so that U1 cannot conduct anymore. Thus, Q1 conducts to discharge the input capacitor of the main IGBT. Therefore, the main IGBT is turned OFF. Meanwhile, the turn-ON pulse signal is applied to the gate driver for IGBT_BP because the winding is in the opposite direction of the gate driver for the main IGBT. The pulse signal is applied to the gate of Q3 through the differentiator composed of R12 and C3. In an instant, Q3 conducts and L1 can build up energy for driving the IGBT_BP. Finally, the energy stored in L1 charges the input capacitor of the IGBT_BP. Therefore, the IGBT_BP switch conducts.

Thus, synchronized gate signal and an isolated power supply for the IGBT_BP as well as the main IGBT can be achieved by using the proposed circuit.

C. Design and Implementation

The design factors of proposed circuit are storage capacitor C2, zener diode D4, differentiator R12, and C3 in Fig. 4(a). The other parameters do not influence the overall operation of the proposed gate driving circuit much. The storage capacitor C2 can be adjusted according to the output pulse width. It has large value for long output pulse width because stored energy of C2 with ON/OFF pulse signal has to maintain gate voltage without external energy source. The developed SSPPM has long output pulse width of 300 μs. The capacitance of storage capacitor C2 is 1 μF to maintain gate voltage of main IGBT for 300 μs. On the other hand, the zener diode D4 can limit voltage of the storage capacitor C2 for driving IGBT. The developed SSPPM is adopted FGL40N120AND FAIRCHILD IGBT for their main switches, which has saturated at 15 V between gate and emitter of IGBT. Therefore, we select 15 V zener diode to drive main IGBT properly. It can adjust gate voltage according to switch model. Meanwhile, the differentiator of gate driver can determine gate delay of IGBT_BP. The single pulse signal is used for main switch and bypass switch with single toroidal core. Therefore, their switches can be shorted without delay circuit, which causes destruction of switches due to high current from output capacitor through shorted line. To prevent this problem, 150 ns delay is applied to the driver circuit with 3 nF, 50 Ω of C3 and R12.

On the other hand, the voltage rating of IGBT_BP is determined by charged voltage of one output capacitor from capacitor charger. The voltage of each IGBT_BP is clamped at charged voltage of one output capacitor when the IGBT_BP is turned OFF. Also, it is their maximum voltage. Therefore, the charging voltage of output capacitor can determine the voltage rating of the IGBT_BP.

The detailed implementation of the proposed gate driving circuit is described for operating the stacked switches as well as achieving fast falling pulse based on the analysis of the concept and operational principle of the proposed circuit.

As mentioned above, achieving an isolated power supply is important for driving the stacked switches. The proposed gate driver circuit was implemented by using the toroidal ferrite core (cross-section area: 18 mm^2) with a turn ratio of 1:2 for preventing core saturation and supplying isolated power to the stacked switches. The ON/OFF pulse signal generated by the full-bridge inverter-based ON/OFF pulse generator passed through this toroidal core with one turn and was transferred to each gate driver circuit. The switches (main IGBTs and IGBT_BPs) were attached directly to the gate driver Printed Circuit Board (PCB) for reducing the undesirable effect from the parasitic inductance between the gate driver circuit and the gate pin of the switch. The proposed circuit is implemented as depicted in Fig. 6. The main IGBTs and IGBT_BPs were located on the PCB and the heat sink was attached for radiating the high temperature of the switches.

III. Distinctive Feature of the Proposed Power Modulator

A. Effective Pull Down

The falling time is proportional to the resistance connected in parallel with the load. In the proposed circuit, IGBT_BPs

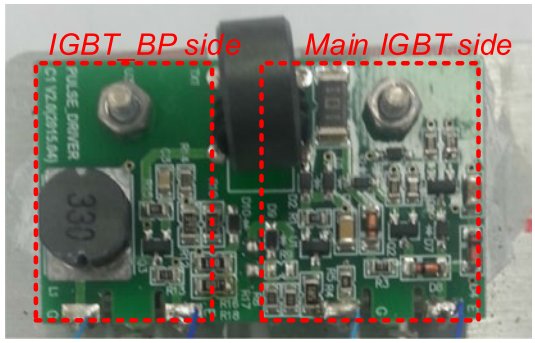


Fig. 6. Photograph of the implementation of the proposed gate driving circuit.

are turned ON at the end of the pulse. In this state, the parallel resistance is very small compared with the pull-down resistor. As a result, the proposed circuit has a small falling time compared with the conventional circuit because of the IGBT's small ON resistance. Indeed, a pull-down resistor with a small value can be used to achieve fast-falling pulses. However, the application of the pull-down resistor is limited because of the resistor power rating and additional loss, which increases with decrease in resistance. Therefore, the SSPPM with the proposed circuit provides fast-falling pulsed voltage applied to the load without the pull-down resistor.

B. Additional Loss Comparison at Load Side

When applying a pulsed voltage to the load, there are two additional losses at the load-side. First, a continuous loss occurs during the applied pulse state because of the high voltage applied to the pull-down resistor. Second, an instantaneous loss occurs because the energy stored in the load capacitance discharges through the pull-down resistor or the IGBT_BP. Two additional losses can be expressed in the following equation. In this equation, the additional loss from the gate driving circuit for operating the IGBT_BP in the proposed circuit is ignored because it is very small compared with the loss from the load-side:

$$\mathrm{Loss}_{\mathrm{Load-side}} = \left(\frac{V_{\mathrm{pulse}}^2 \times W_{\mathrm{pulse}}}{R_{\mathrm{pull-down}}} + \frac{C_{\mathrm{Load}} \times V_{\mathrm{pulse}}^2}{2} \right) \times F \tag{1}$$

where V_{pulse} is the pulse voltage, W_{pulse} is the pulse width, and F is the repetition rate of the pulse.

$R_{\mathrm{pull-down}}$ in case of the SSPPM with the proposed circuit has a value close to infinity because the IGBT_BP is turned OFF during the applied pulse state. In this case, the first additional loss is approximately zero. Fig. 7 shows the additional losses occurring at the load-side of the SSPPM with and without the proposed circuit. As shown in Fig. 7, the SSPPM without the proposed circuit has large loss from the pull-down resistor caused from the first additional loss. For these reason, the SSPPM has limitations of pulse width and repetition rate due to the large loss from the pull-down resistor. However, in case of SSPPM with proposed circuit, the load-side loss is independent of pulse width as shown in (1). Moreover, the generated loss in the second term of (1) is extremely smaller than first term of (1).

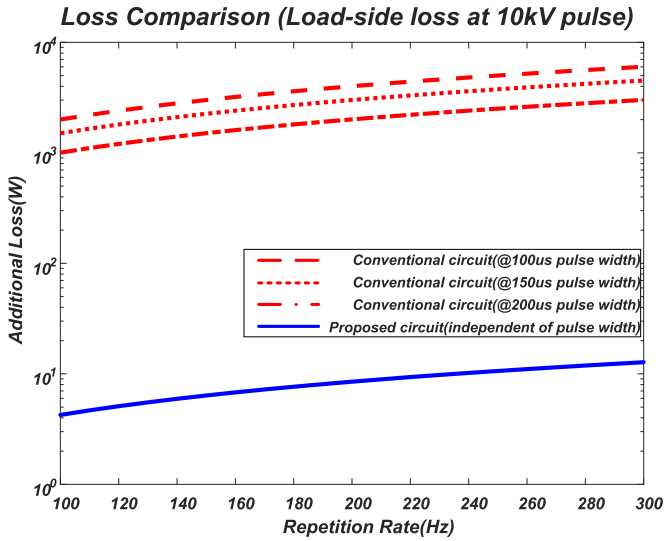


Fig. 7. Load-side loss comparison (@10 kV, parallel resistance = 1 kΩ).

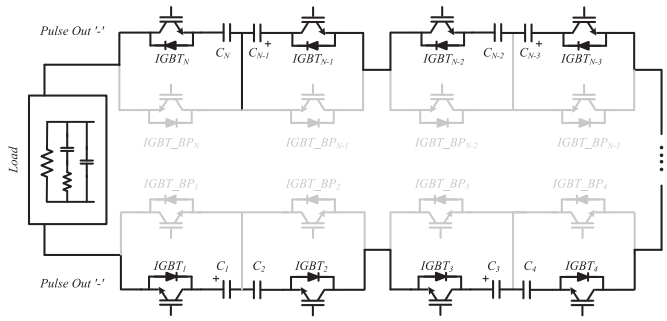


Fig. 8. Operation mode of a power cell-based stack (normal condition).

On the other hand, in case of conventional circuit, the voltage of load capacitor $v_c(t)$ is derived as

$$v_{C_{\mathrm{Load}}}(t) = V_{\mathrm{pulse}} \left(1 - e^{\frac{-t}{R_{\mathrm{pull-down}} \times C_{\mathrm{Load}}}} \right). \tag{2}$$

From the (2), the falling time T_{fall}, which is defined as the time to reach ten percent of initial voltage from ninety percent of initial voltage, can be calculated as

$$T_{\mathrm{fall}} = 2.2 \times R_{\mathrm{pull-down}} \times C_{\mathrm{Load}}. \tag{3}$$

To obtain similar falling time with proposed circuit, 100 Ω resistor can be used for the pull-down resistor. However, it causes exceeding loss in the pull-down resistor. Accordingly, it is difficult to apply in real system due to very big size and high cost.

C. Protection of Semiconductor Device

The SSPPM with the power cell based structure guarantees reliable operation even if the gating signal synchronization fails [13]. As shown in Fig. 8, in the normal operation mode, the voltage across each main IGBT ($\mathrm{IGBT}_1 - \mathrm{IGBT}_N$) is always clamped to the corresponding storage capacitor ($C_1 - C_N$) voltage. The sum of each capacitor voltage ($\mathrm{NV}_{\mathrm{ch}}$) can be applied to the load when all the switches are simultaneously turned ON.

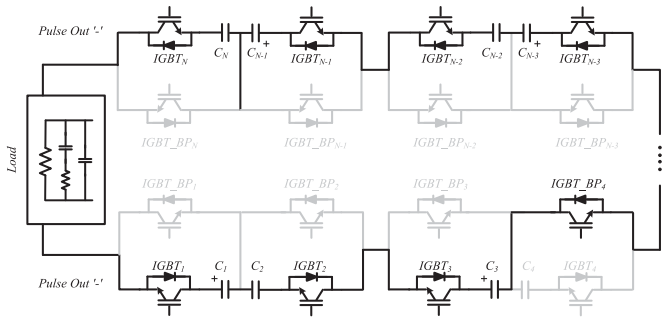


Fig. 9. Operation mode of a power cell-based stack (synchronization failure condition).

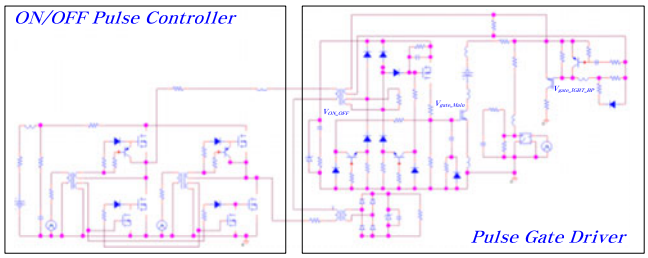


Fig. 10. Simulation model of the pulse gate driver circuit.

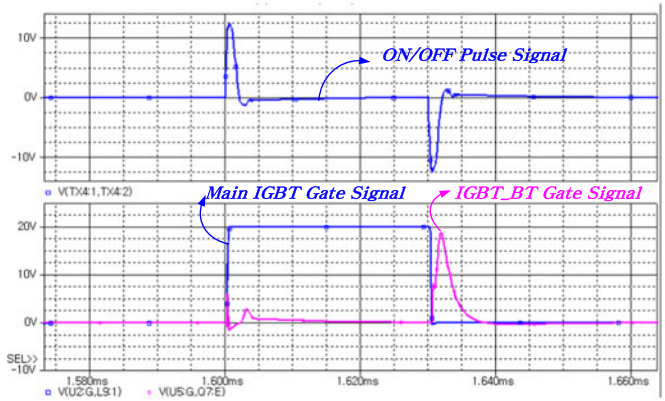
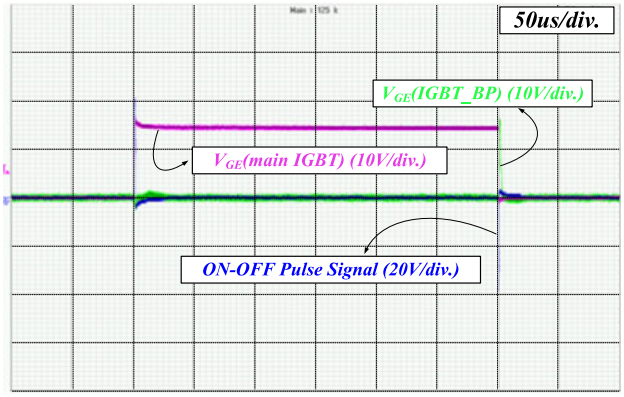


Fig. 11. Simulation results of the pulse gate driver circuit.

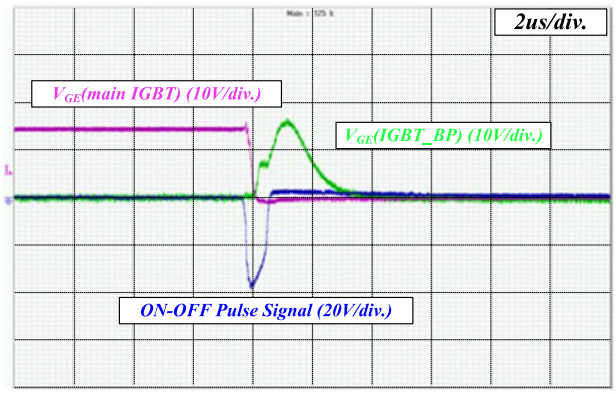
When one or several switches are malfunctioning because of the gate driver circuit or signal synchronization problems, the SSPPM with the power cell based structure operates without damaging the devices, as shown in Fig. 9. For example, even if IGBT4 turns OFF while the other switches are ON, the pulse current flows through the antiparallel diode D4 and the voltage across IGBT4 is clamped to the capacitor C4. That is, the SSPPM with the proposed circuit does not require an exactly synchronized gate signal.

IV. Simulation and Experimental Results

The simulation model of a pulse gate driver is presented in Fig. 10. It was designed for reliable operation. The value of all the parameters in a gate driver was determined from the simulation results. Fig. 11 shows the simulation results of the driver circuit. The IGBT_BP was turned ON with the OFF pulse signal as soon as the main IGBT was turned OFF.



(a)



(b)

Fig. 12. Experimental wavefroms of ON/OFF pulse and gate signals of the main IGBT and IGBT_BP. (a) At 50 μs per division. (b) At 2 μs per division.

The experiments were performed using the 10-kV SSPPM with 0.85-nF reactor load to verify the proposed work. The feasibility of the proposed circuit was confirmed by the fast-falling pulses observed in the experimental results. The main IGBT and IGBT_BP were staked for 10-kV pulse voltage. All the IGBTs used FGL40N120AND (1200 V/40 A). As shown in Fig. 12, the proposed gate driver shows reliable normal operation. The main IGBTs were turned ON with the ON pulse signal and were maintained for 300 μs by using the storage capacitor of gate driver. At that time, the output pulse was applied to the load through the main IGBTs. As applying OFF pulse signal, the main IGBTs were turned OFF and the gate signal was applied to the IGBT_BPs as shown in Fig. 12(b). Then, the stored energy in load capacitance can be discharged through the IGBT_BPs. Fig. 13 shows a comparison between the falling times of the conventional and proposed circuits. In the case of the conventional circuit, the pulse voltage applied to the load was discharged according to (3). As shown in Fig. 13(a), the pulse voltage of the conventional circuit has a slow falling time and exhibits an exponential waveform. In the case of the proposed circuit, the applied pulse voltage was discharged quickly through the IGBT_BPs. The output voltage in proposed circuit has ringing because of nonzero *dv/dt*. It is caused from resonance between load capacitance and parasitic inductance. However, the ringing does not influence the system much because of following reasons. First, the magnitude of ringing is not so much high because

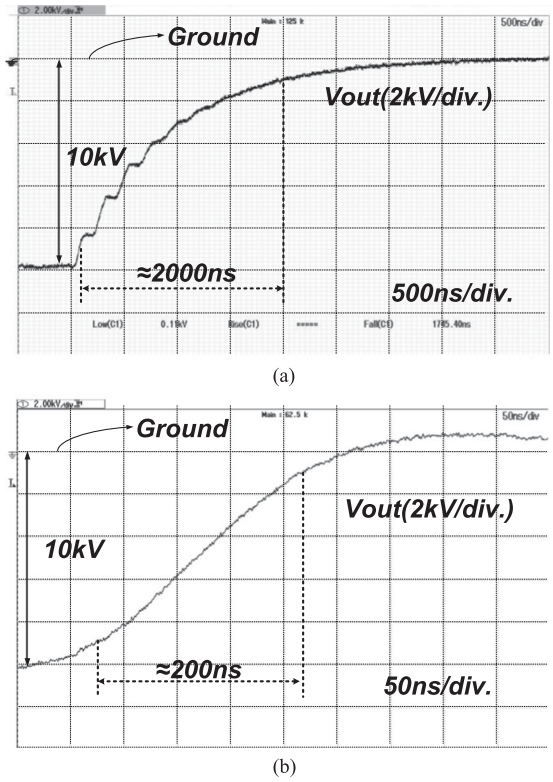


Fig. 13. Falling time of the pulse at 10-kV pulse voltage. (a) Conventional SSPPM (1 kΩ parallel resistor). (b) SSPPM with proposed circuit.

the parasitic inductance of the SSPPM has small value. Moreover, the ringing is attenuated quickly as shown in Fig. 13(b). For reducing the ringing, the parasitic inductance can be decreased by increasing the wire cross-sectional area and/or by reducing the wire length. Thus, the pulse voltage of proposed circuit had a falling time about ten times smaller than that of the conventional circuit.

V. Conclusion

This paper proposes a new gate driving circuit for the SSPPM. The SSPPM with the proposed circuit can be easily implemented by replacing the bypass diode of the conventional circuit with the IGBT_BP and adding a small number of components for driving the replaced IGBT_BP. The IGBT_BPs are turned ON with the OFF pulse signal as soon as the main IGBT is turned OFF. It can quickly discharge the pulse voltage applied to the load. In addition, it can operate as a bypass diode using the antiparallel diode. Moreover, the power loss in the pull-down resistor, which is used in the conventional SSPPM to achieve fast-falling pulses, can be eliminated. The experiment results confirm that the proposed circuit can widely be used by the SSPPM with fast-falling time in various applications such as in water or gas-treatment system.

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