Fixed-Switching Frequency Interleaved Sliding Mode Eight-Phase Synchronous Buck Converter

Víctor Repecho, Domingo Biel, Rafael Ramos-Lara, and Pilar Garcia Vega

***Abstract*—This paper describes the design of an interleaved sliding mode control for a multiphase synchronous buck converter, which inherits the properties of sliding mode control, operates with fixed switching frequency in the steady-state, and ensures current equalization among phases. Moreover, a power management algorithm is added in order to decide the number of active phases as function of the power load demand, thus optimizing the converter efficiency. The system uses a Master–Slave structure where each phase can actuate as the Master one in such a way that the overall system reliability is improved. Experimental results in a 1.5 kW eight-phase synchronous buck converter show that interleaving operation, robust output voltage regulation, phase current equalization, switching frequency regulation, and power management are achieved.**

***Index Terms*—Chattering reduction, current equalization, fixed switching frequency, interleaving, power management, sliding mode control (SMC).**

I. Introduction

DUE to their high efficiency, power density, fast transient response, and ability of interleaving operation [1], multiphase converters have gained interest within the industrial community for different applications. These structures were initially proposed as dc/dc voltage regulator modules for microprocessor supply [2]–[4]. Lately they were applied as automotive bidirectional converters [5], as battery chargers [6], as dc bus regulators [7], or in power line communications [8], among others. The literature also provides different studies as, interalia, the nonidealities effects [9], the possibility of dynamic variation of the output voltage [10], or the improvement of the interleaving with coupled inductor technique [11].

The interleaving operation allows us to cancel the current ripple through the output capacitor, which entails a reduction of the value, size, weight, and cost of this component. Since the current ripple is cancelled in the parallel connection, a reduction of the inductors values, size, and cost, is also possible. Another advantage of the multiphase structure is the reduction of the components' stress, due to the decrease of the power processed by each phase. Such reduction would allow us to increase the switching frequency, which in turn, would lead to an additional reduction of the value of the reactive components. Therefore, thanks to the interleaving operation, the designed multiphase converter can be smaller, lighter, cheaper, and more efficient than a single-phase converter managing the same power.

In ideal conditions, the different phases manage the same amount of power. However, structural differences among the phases, which can occur due to the component tolerances, tend to unbalance the power flowing by the phases. As the phases are designed maximizing the efficiency for a nominal power, the overall efficiency is lower when the power flow is not equalized. To overcome this drawback, modular systems usually employ current equalization algorithms that ensure power sharing among phases. In [12], a technique for current equalization based on measuring the input ripple voltage is proposed. The proposed structure modifies the current references for all the phases according to the input ripple measurement by a perturbation observation method, which becomes in a high complex procedure in multiphase systems with more than two phases. In the literature, one can also found systems that are able to balance the power flow using a single current measurement [13] or without additional current measurement [14]. In [13], the system requires N active switches in an N-phase converter, which increase the system complexity. Moreover, the ability to control each phase current separately is lost. In [14], the phase resistances are estimated using a perturbation technique, which implies a complex signal processing, especially high when the number of phases increases. Other approaches [15]–[17] propose to use N current sensors in N-phase converter for balance the phase currents. Using current sensor in all the phases the system achieves a perfect current equalization among them. The work presented here follows these approaches.

In addition, the connection or disconnection of phases allows us to optimize the converter performance. Depending on the desired feature to optimize, such as efficiency, reliability, or transient response, different connection-disconnection rules should be derived [18]–[20].

Using linear control tools simplifies the design of interleaving controllers, since the control signals are properly phase-shifted according to the number of converters by means of pulse width

Manuscript received September 23, 2016; revised December 16, 2016; accepted January 17, 2017. Date of publication February 1, 2017; date of current version October 6, 2017. This work was supported in part by the Government of Spain through the *Ministerio de Economia y Competitividad* Project DPI2013-41224-P and by the *Generalitat de Catalunya* through the Project 2014 SGR 267. Recommended for publication by Associate Editor S. Kapat.

V. Repecho is with the Institute of Industrial and Control Engineering, Universitat Politècnica de Catalunya, Barcelona 08028, Spain (e-mail: victor.repecho.del@upc.edu).

D. Biel is with the Department of Electronic Engineering, and the Institute of Industrial and Control Engineering,Universitat Politècnica de Catalunya, Barcelona 08028, Spain (e-mail: domingo.biel@upc.edu).

R. Ramos-Lara and P. Garcia Vega are with the Department of Electronic Engineering, Universitat Politècnica de Catalunya, Barcelona 08028, Spain (e-mail: rafa.ramos@upc.edu; pilar.garcia@repsol.com).

Color versions of one or more of the figures in this paper are available online at http://ieeexplore.ieee.org.

Digital Object Identifier 10.1109/TPEL.2017.2662327

modulation (PWM) [5], [9], [12]. The controller, which regulates the converter output voltage, is usually designed from a linear small signal averaged model of the converter. Due to the small signal model usage, the system responses are degraded with parametric variations, such as the equivalent output resistance or the number of active phases of the converter. In order to overcome this drawback and obtain a fast transient response, some authors have proposed the application of controllers with hysteresis for the multiphase converter [21], [22]. In [21], the interleaving operation is guaranteed by using fixed hysteresis band comparators and a digital circuitry, being the switching frequency variable. Fixed switching frequency and interleaving operation are achieved by synchronizing the duty cycle with an external fixed frequency clock reference in [22]. Nevertheless, this approach requires an external reference clock and a bandwidth changing loop for each converter phase. A very interesting control approach is found in [23], where a hybrid controller is proposed. The control ensures the system trajectories to converge to a boundary layer by a nonlinear controller and uses a PWM within such layer. The utilization of a PWM inside the boundary layer allows a simple implementation of the interleaving operation. However, due to the suppression of the nonlinear control action within the boundary layer the controller loses its inherent robustness.

Sliding mode control (SMC) stands out for its robustness with respect to parametric variations and external disturbances. It has been successfully applied in power electronics in [24] and [25], among others. In 2009, Lee *et al.* presented [26] a technique that minimizes the ripple in a sliding mode voltage controlled multiphase converter, with an interleaving sliding mode. This control technique represents an alternative to the aforementioned control methods. Specifically, SMC improves the converter performance when the load (or the number of active phases) suddenly changes due to its high robustness with respect to parameters variation. This technique was successfully implemented in a low power four-phase converter [17], where additionally an equalization algorithm was proposed in order to balance the power flowing through the phases. However, as the SMC was implemented by means of fixed hysteresis band comparators, the switching frequency became variable and, hence, sensitive to the power converter parameters and the input voltage. Such variations complicate the reactive components design, since they are generally designed for a constant switching frequency. Furthermore, as the switching frequency harmonic content is not fixed, the output voltage filtering capability is degraded.

The work presented here follows the SMC design procedure of [26] and [17]. The designed controller is applied to a 1.5 kW eight-phase synchronous buck converter, ensuring interleaving, current equalization among phases, and robust output voltage regulation. Moreover, the control architecture responds to a Master–Slave structure and three new functionalities are included: a power management algorithm (PMA), a rotatory master technique and, most importantly, a switching frequency regulator. The PMA deals with the connection or disconnection of phases depending on the delivered power to the load, and it is included to improve the efficiency of the converter. The rotatory master technique tends to equalize the working time among the phases, increasing the system reliability. Finally, in order to regulate the switching frequency of the phases, a switching frequency controller (SFC) is designed following the procedure proposed in [27] and [28]. This methodology does not require any synchronization clock signal and it is only applied to one of the converter phases.

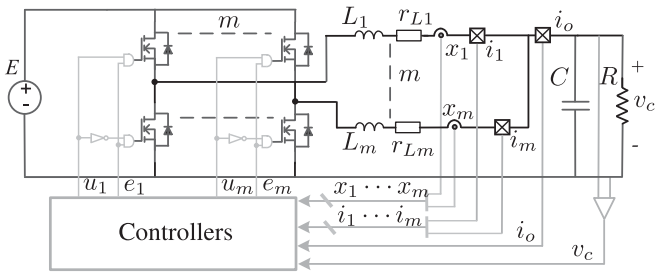

Fig. 1. Circuit scheme of the m-phase synchronous buck converter.

The remainder of the paper is organized as follows. In Section II, the dynamical model of the power converter is introduced. The description of the proposed controllers is presented in Section III. Section IV presents the developed prototype for experimental evaluation, followed by the experimental results obtained in the laboratory in Section V. Finally, the conclusions derived from this research are drawn in the last section.

II. Multiphase Synchronous Buck Converter Description

A multiphase step-down power converter is composed by several synchronous dc/dc buck converters with a common output capacitor. As shown in Fig. 1, an m-phase converter supplies a single load, which is assumed to be resistive and linear in this work, and can be modeled by the following set of differential equations:

$$L\frac{di_k}{dt} = -r_{Lk}\ i_k - v_c + E\ u_k; \quad k = 1, \ldots, m$$
$$C\frac{dv_c}{dt} = \sum_{k=1}^{m} i_k - \frac{v_c}{R}, \tag{1}$$

where i_k is the current flowing through the k-phase, v_c is the output voltage, and u_k is the k-phase control input which takes values in the set $\{0, 1\}$. The phase inductances, L_k, are assumed to be identical, and r_{Lk} denotes the unmatched resistive losses of the phases. The input voltage, E, is considered common to all phases.

Fig. 1 also depicts the equivalent scheme of the switches drivers and the sensing elements. Each phase includes a driver that generates the control signals for the power switches, and allows to inhibit the corresponding leg with the enabling signals $e_1 \ldots\ e_m$. The figure also shows the sensors used by the controllers. Both the load current, i_o, and the output voltage, v_c, are measured by the control system. Additionally, each phase uses two current sensors, a low cost current transformer ($x_1 \ldots\ x_m$ signals) and a Hall Effect one ($i_1 \ldots i_m$ signals). Using the current transformers and the Hall Effect sensors instead of shunt resistors preserves a good efficiency, keeping the capability of

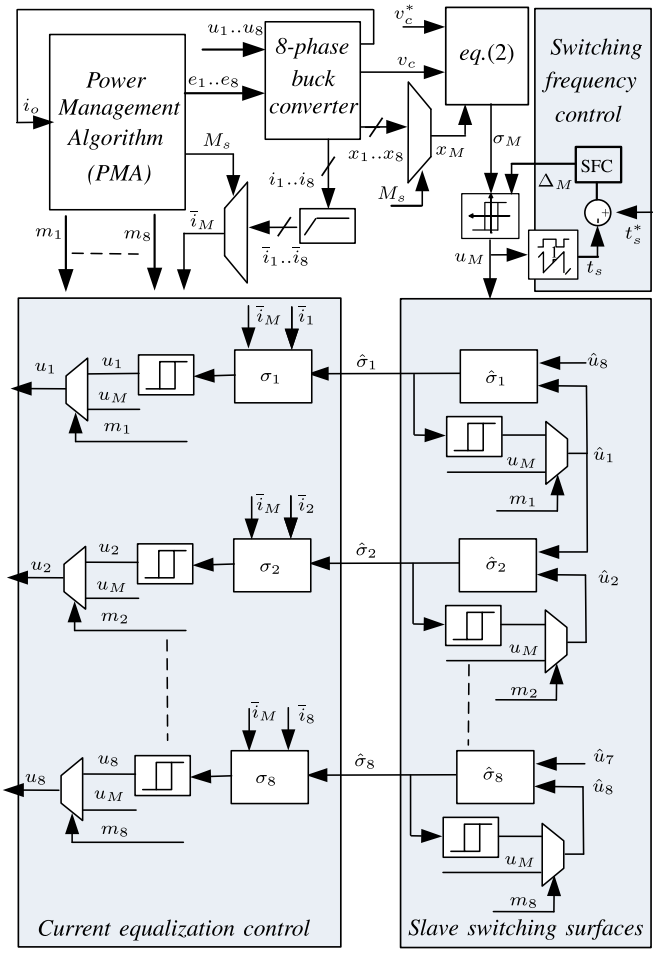

Fig. 2. Control scheme of eight-phase synchronous buck converter.

high frequency current measurement and improving the signal-to-noise ratio. In order to equalize the working time of the phases, the multiphase operates with a Master–Slave control architecture with a rotatory Master. This structure requires current transformers in all the phases. Furthermore, the current equalization algorithm needs the inclusion of Hall Effect current sensors in each phase in order to measure the values of the average currents. An additional Hall Effect current sensor is included for the output current measurement, enabling a fast overcurrent protection implemented by means of an analogue comparator (bypassing the acquisition time of the analogue-to-digital converter (ADC)), and allowing us to have an accessible current measurement in the laboratory. From a control point of view, this Hall sensor is not required, since the total output current is only used by the PMA to connect or disconnect phases, and this current can be computed by adding the currents of the active phases.

III. Control Structure

The control scheme is depicted in Fig. 2. As it has been already mentioned, the control uses a Master–Slave control strategy which can be divided in several parts that are described in the following subsections.

A. Master Switching Surface

The voltage regulation is performed by the Master phase with the following switching surface:

$$\sigma_M := \psi_1 \left(v_c - v_c^*\right) + \psi_2 x_M = 0 \tag{2}$$

where v_c^* is the desired output voltage, and $\psi_1, \psi_2 > 0$ are the switching surface parameters. As it can be seen in Fig. 2, the variable x_M corresponds to the current transformer output of the phase that the PMA selects as the Master one.

Taking into account the magnetic coupling equations and knowing that the secondary of the transformer is loaded with a resistor R_b, the equation that relates the output variable, x_M, which is the voltage through R_b, and the current flowing through the transformer's primary side is given by

$$L_x \frac{dx_M}{dt} = -R_b x_M + R_b M \frac{di_M}{dt} \tag{3}$$

where i_M is the Master phase current, and M and L_x are the mutual inductance and the secondary inductance, respectively.

Remark 1: The current ripple cancellation at the output capacitor caused by the interleaving operation prevents the possibility of using this current as the first time derivative of the output voltage in the Master switching surface (2). As a consequence, the inductors' currents are measured employing current transformers.

B. Sliding Dynamics

Assuming identical phases and applying the equivalent control method [24], which entails $\sigma_M = 0$ and $\dot{\sigma}_M = 0$, the ideal sliding dynamics is analyzed. The equivalent control for the Master phase is given by

$$u_{M_{\text{eq}}} = \frac{v_c}{E} + \frac{r_{L_M}}{E} i_M + \frac{L\psi_1}{EM\psi_2}(v_c^* - v_c) - \frac{\alpha L}{E}\dot{v}_c \tag{4}$$

where $\alpha = \frac{\psi_1 L_x}{\psi_2 R_b M}$. The sliding dynamics for the output voltage is

$$C\frac{d^2 v_c}{dt^2} + \left[m\alpha + \frac{1}{R}\right]\frac{dv_c}{dt} + \frac{m\psi_1}{M\psi_2} v_c = \frac{m\psi_1}{M\psi_2} v_c^* \tag{5}$$

while the sliding dynamics for the currents flowing through the phases is

$$\frac{di_k}{dt} = v_c\left(\frac{\alpha}{RC}\right) + \frac{\psi_1}{M\psi_2}\left(v_c^* - v_c\right) - i_k\frac{\alpha\, m}{C}; \quad k = 1, \ldots, m. \tag{6}$$

Since all the coefficients in (5) and (6) are positive, the differential equations are asymptotically stable and the output voltage converges to the reference one in steady state. In order to design the switching function parameters ψ_1 and ψ_2, the dynamics given by (5) for different working conditions of the converter must be evaluated. Specifically, the converter is to undergo variations of the number of active phases, m, the output load, R, and the desired output voltage v_c^*. In this case, according to the converter parameters shown in Table I, the switching parameters are set to: $\psi_1 = 0.078$ and $\psi_2 = 2.97$. These values ensure an overshoot in the transient response of the output voltage less that a 20% in the worst case (which happens when m=3 and

TABLE I
MULTIPHASE BUCK CONVERTER PARAMETERS

Parameter	Symbol	Value
Input Voltage Range	E	48– 36 V
Desired Output Voltage Range	v_c^*	12– 24 V
Output Capacitor	C	100 μF
Inductance	L	22 μH $\pm$ 10%
Resistance Inductance	r_L	2.6 mΩ $\pm$ 10%
Power Switches resistance losses	r_{dson}	10.8– 25 mΩ
Load Range	I_o	0– 65 A
Desired switching frequency	f_{sw}	100 kHz
Current transformer parameters	L_x, M	800 μH, 6.4 μH
Current transformer burden resistor	R_b	10 Ω
SMC parameters	ψ_1, ψ_2	0.078, 2.95
Switching frequency control parameter	k_i	$1.25e^8$

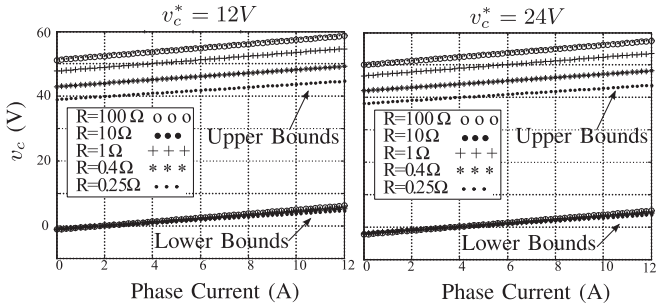

Fig. 3. Upper and lower bounds of the sliding domain for an output voltage of 12 V and 24 V.

the converter operates in no load condition). When m=8, the overshoot is of a 3.5%. It has to be remarked that these results are essentially the same for 12 V and for 24 V.

C. Control Law

Theorem 1: The control law $u_M = 0.5\,[1 - \text{sign}\,(\sigma_M)]$ enforces sliding motion on $\sigma_M = 0$ when the system trajectories are in the sliding domain given by $0 < u_{M_{\text{eq}}} < 1$.

Proof: The sliding motion is ensured when the inequality $\sigma_M \dot{\sigma}_M < 0$ is fulfilled. Therefore, applying the time derivative to (2) one gets

$$\sigma_M \dot{\sigma}_M = \sigma_M \left(\psi_1 \dot{v}_c + \psi_2 \dot{x}_m\right) \tag{7}$$

and, replacing (1) and (3), results in

$$\sigma_M \dot{\sigma}_M = \sigma_M \left(f(x_M, i_k, v_c) + \frac{\psi_2 R_b M}{L_x L} E\, u_M\right). \tag{8}$$

Adding and subtracting the equivalent control, yields to

$$\sigma_M \dot{\sigma}_M = \sigma_M \frac{\psi_2 R_b M}{L_x L} E \left(u_M - u_{M_{\text{eq}}}\right) \tag{9}$$

and, recalling the definition of the parameter α, can be expressed as

$$\sigma_M \dot{\sigma}_M = \sigma_M \frac{\psi_1}{\alpha L} E \left(u_M - u_{M_{\text{eq}}}\right). \tag{10}$$

Finally, replacing the control law $u_M = 0.5\,[1 - \text{sign}\,(\sigma_M)]$, one gets

$$\sigma_M \dot{\sigma}_M = -0.5 \frac{\psi_1}{\alpha L} E \left(|\sigma_M| + \sigma_M \left(2u_{M_{\text{eq}}} - 1\right)\right). \tag{11}$$

Since $\frac{\psi_1}{\alpha L} E > 0$, $\sigma_M \dot{\sigma}_M$ is negative when the inequality $0 < u_{M_{\text{eq}}} < 1$ is fulfilled. ■

D. Sliding Domain

Using the equivalent control method, the sliding domain is found as

$$0 < \left[1 + \alpha L \left(\frac{1}{RC} - \frac{R_b}{L_x}\right)\right] v_c + \left(r_{L_M} - \frac{\alpha L m}{C}\right) i_M + \frac{\alpha L R_b}{L_x} v_c^* < E. \tag{12}$$

If the inequality shown in (12) is fulfilled, the sliding motion is guaranteed. Fig. 3 shows the upper and lower bounds of (12) in the state plane for the desired output voltage v_c^* and the output resistance R as parameters. It has to be noted that the desired output voltage does not have much influence in the sliding domain. As it can be seen from the upper and lower bounds, there are space regions where the sliding motion is not guaranteed, as with a low output voltage (around 4 V) with phase currents higher than 8 A. Thanks to a good switching function parameters design, the output voltage does not take values inside these regions neither in the start-up nor in load transients. Furthermore, the start-up charges quickly the converter output capacitor and the output voltage reaches values high enough to fulfil the sliding domain inequalities.

E. Interleaved Sliding Mode

Assuming that the Master phase corresponds with the kth phase, the interleaved sliding mode operation is achieved by using the Master phase control signal, $u_k = u_M$, and the $(m-1)$ Slaves switching surfaces defined as follows:

$$\begin{aligned}
\hat{\sigma}_{k+1} &:= K \int (u_M - \hat{u}_{k+1})\, dt = 0 \\
\hat{\sigma}_{k+2} &:= K \int (\hat{u}_{k+1} - \hat{u}_{k+2})\, dt = 0 \\
&\vdots \\
\hat{\sigma}_m &:= K \int (\hat{u}_{m-1} - \hat{u}_m)\, dt = 0 \\
\hat{\sigma}_1 &:= K \int (\hat{u}_m - \hat{u}_1)\, dt = 0 \\
\hat{\sigma}_2 &:= K \int (\hat{u}_1 - \hat{u}_2)\, dt = 0 \\
&\vdots \\
\hat{\sigma}_{k-1} &:= K \int (\hat{u}_{k-2} - \hat{u}_{k-1})\, dt = 0
\end{aligned} \tag{13}$$

with $\hat{u}_i = 0.5\,[1 + \text{sign}\,(\hat{\sigma}_i)]$ being the control laws.

The proposed switching surfaces in (13) enforce the equalization of the average values of $u_{k_{\text{eq}}}$ and $u_{M_{\text{eq}}}$ under sliding motion. Additionally, the control law $\hat{u}_i = 0.5\,[1 + \text{sign}\,(\hat{\sigma}_i + \Delta\hat{u}_i)]$

generates a phase shift among the phases, Δ being the hysteresis width of the comparator. The works [17] and [26] show that this phase shift is $T_\phi = \Delta/K$. Obviously, the desired phase shift, $T_\phi = t_s/n$, depends on the switching period and the number of active phases. By equalling both expressions of T_ϕ, the value of K can be obtained as: $K = (\Delta n)/t_s$. Since the number of active phases, n, can vary according to the PMA algorithm decisions, the phase shift is adjusted on-line through K, measuring the Master phase switching period t_s.

F. Current Equalization Algorithm

From an implementation point of view, it is difficult to obtain a set of identical phases. It can be proven that, when phases have different losses, the quiescent working point of a multiphase converter is given by

$$v_c = v_c^*; \quad i_k = \frac{r_{L1}}{r_{Lk}} \left[1 + \sum_{i=2}^{m} \frac{r_{L1}}{r_{Li}}\right]^{-1} \frac{v_c^*}{R}; \quad k = 1, \ldots, m \tag{14}$$

where $r_{L1}, \ldots, r_{Lm}$ are the resistive losses of the phases which include the series resistance of the inductors and the conduction resistance of the MOSFETS. Therefore, the average currents through the phases are different. Notice that the equilibrium is very sensitive to resistive losses and the phase currents are affected by the same ratio than the resistive losses as

$$\frac{i_k}{i_1} = \frac{r_{L1}}{r_{Lk}}. \tag{15}$$

To overcome this drawback, a current equalization algorithm has been designed.

The equalization is achieved employing a new set of switching surfaces for the Slaves phases, defined as σ_k, which uses $\hat{\sigma}_k$ as an input. The surface σ_k copies the control signal generated by $\hat{\sigma}_k$, $\hat{u}_k$, increasing or decreasing the effective duty cycle of u_k such that the average current error $(\overline{i_M} - \overline{i_k})$ converges to zero, $\overline{i_M}$ and $\overline{i_k}$ being the average values of the respective currents. A deeper description of the applied equalization method can be found in [17].

G. Switching Frequency Regulation

The SMC implementation with fixed hysteresis band comparators instead of sign functions yields an inherently variable switching frequency. In order to regulate the switching frequency, this work follows the control scheme proposed in [27] and [28]. The technique adds a new loop which measures the Master phase switching period, updates the hysteresis band value using a SFC, and enforces the measured switching period t_s to converge to the reference one, t_s^*. For the multiphase configuration, the switching frequency regulation is just required for the Master phase, since the Slaves phases automatically replicate the Master one due to the interleaving operation. In this paper, an approach based on a continuous time integral action for the SFC is employed. The additional loop structure can be seen in the top right side of the system diagram shown in Fig. 2.

The analysis of the stability conditions for the switching frequency control loop and the design of the SFC are tackled at this stage. First at all, the expression which determines the value of Δ_M to be used for the hysteresis comparator of the Master switching surface is

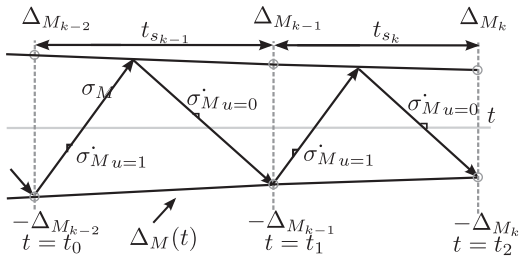

Fig. 4. Master Switching function behavior within a variable hysteresis band.

$$\Delta_M(t) = k_i \int e(\tau) d\tau \tag{16}$$

where k_i is the integral gain and $e = t_s^* - t_s$ is the switching period error. The expected behavior of the Master switching function within a time varying hysteresis band is shown in Fig. 4. Notice that $\Delta_{M_{k-2}}$, $\Delta_{M_{k-1}}$, and Δ_{M_k} are the values of $\Delta_M(t)$ at the corresponding time instants. Although the hysteresis value is a continuous time signal, the corresponding switching periods, t_{s_k}, and the switching period errors, $e_k = t_s^* - t_{s_k}$, are discrete values. From Fig. 4, the kth switching period is found as

$$t_{s_k} = \frac{2\,\Delta_{M_k}}{k_i e_{k-1} - \dot{\sigma}_{M_{u=0}}} + \frac{2\,\Delta_{M_{k-1}}}{\dot{\sigma}_{M_{u=1}} - k_i e_{k-1}}. \tag{17}$$

According to the equivalent control method, the values of $\dot{\sigma}_M$ can be written as follows:

$$\dot{\sigma}_M = \beta E \left(u_M - u_{M_{\text{eq}}}\right) \tag{18}$$

with $\beta = \frac{\psi_1}{\alpha L}$ and $u_{M_{\text{eq}}}$ was defined in (4). The expression providing the expected values of $\dot{\sigma}_M$ at the steady state sliding motion is

$$\begin{aligned} \dot{\sigma}_{M_{u=1}} &= \beta\left[E - v_c^* - r_{L_M} i_M\right] \\ \dot{\sigma}_{M_{u=0}} &= -\beta\left(v_c^* + r_{L_M} i_M\right). \end{aligned} \tag{19}$$

As detailed in [27], replacing (16) into (17) generates a nonlinear relation between t_s and Δ_M. In order to linearize this expression, the following hypothesis was proposed in [27]:

$$|k_i e_k| << \min\left\{|\dot{\sigma}_{M_{u=1}}|, |\dot{\sigma}_{M_{u=0}}|\right\} \quad \forall\ k \tag{20}$$

which entails that the time constant of the resulting Δ_M is much slower than the time constant of σ_M. Under this assumption, the redefined relation between t_s and Δ_M is found in (21) (see [27] for further explanations):

$$t_s = \lambda\,\Delta_M \tag{21}$$

where $\lambda = 2\left[\dot{\sigma}_{M_{u=1}}^{-1} - \dot{\sigma}_{M_{u=0}}^{-1}\right]$.

The control loop depicted in Fig. 5 corresponds to the linearized model of the proposed controller structure in the s domain. The transfer function shown in the feedback loop is the *Padé* approximation of the delay in the switching period measurement.

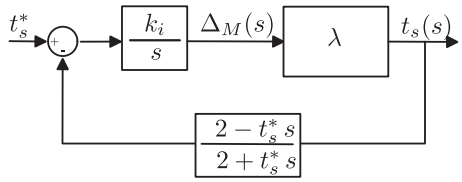

Fig. 5. Continuous time equivalent model of the switching frequency regulation control loop.

The stability conditions of the equivalent model can be easily derived using the characteristic polynomial of the closed loop system shown in Fig. 5, which is given by

$$p(s) = t_s^* s^2 + (2 - k_i t_s^* \lambda)\ s + 2 k_i \lambda. \tag{22}$$

Therefore, recalling that $t_s^* > 0$ and $\lambda > 0$, the system is asymptotically stable when

$$k_i < \frac{2}{\lambda t_s^*}. \tag{23}$$

It has to be highlighted that the previous model can be used only when (20) is fulfilled. The system poles move towards the unstable region when k_i increases, but higher the value of k_i is lower the compliance degree of (20). As a general design rule, it is recommended to choose a value of k_i such that (20) is ensured, and then check the stability condition deduced in (23).

Let us analyze the stability conditions for the frequency control loop of the multiphase converter with the parameters shown in Table I. Applying (19), the value of λ can be evaluated for $v_c^* = 12V$

$$\dot{\sigma}^{-1}_{M_{u=1}} = 2.6 \cdot 10^{-6};\ \dot{\sigma}^{-1}_{M_{u=0}} = -7.8 \cdot 10^{-6};\ \lambda = 2.1 \cdot 10^{-5} \tag{24}$$

and for $v_c^* = 24V$

$$\dot{\sigma}^{-1}_{M_{u=1}} = 3.9 \cdot 10^{-6};\ \dot{\sigma}^{-1}_{M_{u=0}} = -3.9 \cdot 10^{-6};\ \lambda = 1.6 \cdot 10^{-5}. \tag{25}$$

According to (24) and (25), for a desired switching period of $t_s^* = 10\,\mu s$, the stability condition found in (23) gives a limiting value of $k_{i_{\text{lmax}}} = 9.66 \cdot 10^9$ for 12 V, which is the worst case. Finally, the value of k_i is selected as $1.25 \cdot 10^8$, which yields real roots in the characteristic polynomial for the overall working voltage range.

Remark 2: The piecewise linear behavior of the switching surface, shown in Fig. 4, is required to derive (17). This assumption stands when the switching frequency of the control action is high enough with respect to the system dynamics. Specifically, considering the expression of the time derivative of the switching function given in (19), one can realize that the time derivatives depend on the dynamics of the output voltage and on the current flowing in the Master phase. The design of the converter parameters ensures that the output voltage can be considered constant in a switching period. On the other hand, the current of the Master phase appears multiplied out by the resistive losses, which are low for a converter with good efficiency.

H. Power Management Algorithm (PMA)

The control scheme includes a PMA in charge of selecting the enabled phases according to the output load. The PMA also decides the phase that will act as the Master one through the Master select signal, M_s, and properly configures the signals m_1 to m_8 (see Fig. 2). As stated in [26], there is a minimum number of active phases which guarantees interleaved sliding mode. Therefore, the number of active phases, n, at any time should fulfil the following inequalities:

$$\text{if } u_{k_{\text{eq}}} < 0.5,\ \text{then, } u_{k_{\text{eq}}} > \frac{1}{n};\ \text{otherwise } u_{k_{\text{eq}}} < 1 - \frac{1}{n} \tag{26}$$

where $u_{k_{\text{eq}}}$ is given by (4). Since the input voltage of the multiphase converter considered in this work is of 48 V, a minimum of three active phases are required to ensure the desired sliding mode interleaving operation with an output voltage of 24 V, whereas five phases are needed for a 12 V regulation.

The criteria for connecting or disconnecting phases can vary depending on the desired performance. This work uses a connection rule which maximizes the efficiency. Other connection rules minimizing the active phases or improving the transient response could be applied similarly.

Moreover, the PMA performs a Master rotation among phases in order to improve the converter reliability. When a phase has to be disconnected, the Master phase is turned off and the subsequent phase is chosen as the new Master one. This procedure has a ring structure and distributes the operation time among the different phases.

Remark 3: In applications where the load demand varies with a large value of di_o/dt, all the phases should remain activated, otherwise the connected phase currents could exceed the maximum level thus compromising the converter reliability.

IV. Implementation of the Multiphase Converter

Table I shows the main data of the power converter built for experimental evaluation. The output voltage range, the input voltage, and the desired switching frequency are defined, among other interesting system data.

The multiphase converter consists on eight synchronous buck converters, a motherboard, and an field programmable gate array (FPGA) control board. A brief explanation of each part is presented in the following sections.

A. Buck Converter Design

Each buck converter is built in a different board (see Fig. 6). The phases are connected in parallel in the motherboard, which accepts up to eight phases (see Fig. 7). Each phase incorporates a voltage regulator for the switches' drivers. The power switches (PSMN013100BS) are surface mount devices. This technology allows us a high automatization level in the manufacturing process, reducing costs, and increasing reliability. Furthermore, due to the power flow distribution related to the multiphase connection, the switches dissipate the power losses through the board copper path without any additional heatsink. Finally, each phase incorporates a power inductor (SER2918H-223),

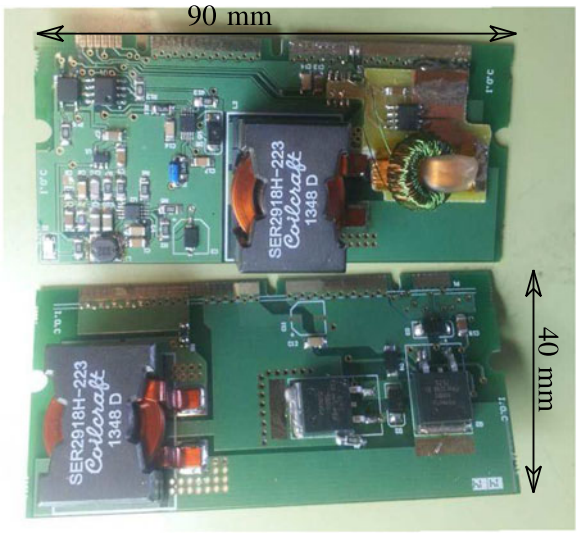

Fig. 6. Single phase picture.

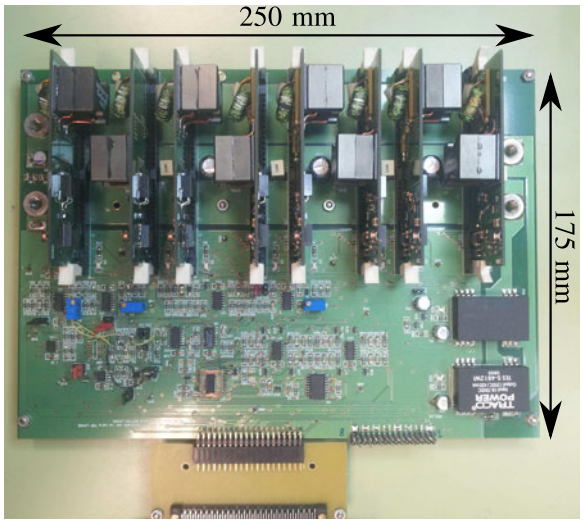

Fig. 7. Motherboard picture.

a current transformer, and a Hall Effect current sensor (ACS711T).

The current transformers are built in the laboratory using a gapped toroid which allows to hold dc current values without core saturation.

B. Motherboard Design

The motherboard has eight connectors (TMDSDIM100) where the buck converters are plugged in (see Fig. 7). In order to minimize the motherboard size, the converters have been designed making the inductor connection possible on both board sides. According to the maximum current value specified by the connector manufacturer (up to 0.5 A per pin), the 100 pins of each connector have been distributed as follows: 16 pins for control signals and current measurements, 18 pins for the input voltage, 34 pins for the output voltage, and 32 pins for the ground connection.

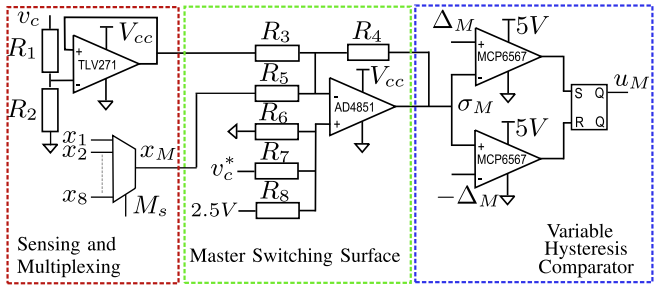

Fig. 8. Analogue electronic implementation of the Master switching surface and the variable hysteresis band comparator.

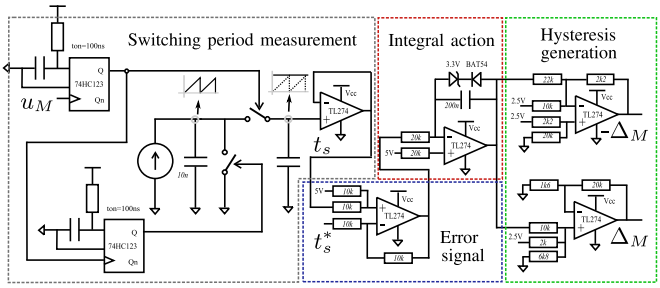

Fig. 9. Analogue electronic implementation of the SFC.

The motherboard contains the analogue circuit, shown in the Fig. 8, that implements the Master switching surface defined in (2) and the variable hysteresis comparator. Additionally, the motherboard has a connector where the FPGA is plugged in. On the one hand, the FPGA receives the Master switching surface control signal and the current measurements through an ADC MAX1228. As it was previously stated, each phase incorporates a Hall Effect current sensor providing the measurements $(i_1 \cdots i_m)$ through the connectors to the motherboard, where they are filtered by analogue circuitry to get also the average values $\bar{i}_1 \cdots \bar{i}_m$. The output current, i_o, is measured with a Hall Effect current sensor (ACS754-100) placed in the motherboard. All of these measurements, once converted by the ADC, are sent to the FPGA through the aforementioned connector. On the other hand, the FPGA uses this connector to deliver the enabling and control signals $(e_1 \cdots e_m, u_1 \cdots u_m)$ to the phases, and the Master's selection signal, M_s. The Master control signal received by the FPGA is routed to the phase selected as Master by the PMA, and the signal, M_s, configures the multiplexer MAX382 (located in the motherboard) in order to connect the signal x_m to the Master switching surface.

The motherboard also includes the circuit that regulates the switching period of the Master control signal. The circuit scheme is depicted in Fig. 9. The switching period of u_M is measured by charging a capacitor with a constant current source. The voltage across the charging capacitor results in a saw-tooth waveform, synchronized with u_M, since a monostable circuit resets this voltage at any rising edge of u_M. Just before resetting the voltage, the peak value of the signal is acquired, which provides a voltage proportional to t_s. The boxed areas in Fig. 9 *integral action* and *error signal* implement the controller defined in (16). Finally, the circuits on the right part of Fig. 9 generate

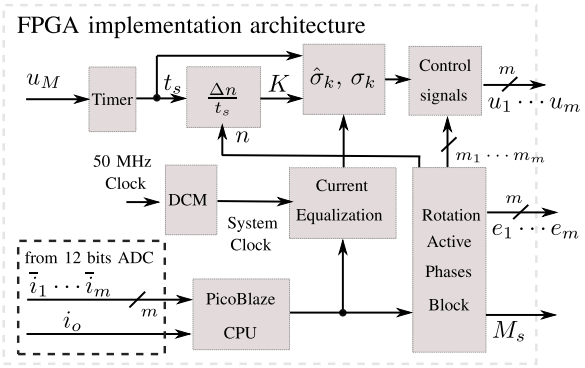

Fig. 10. FPGA block diagram implementation.

the two hysteresis values, Δ_M and $-\Delta_M$, for the Master phase hysteresis comparator shown in Fig. 8.

C. FPGA

For the implementation of the Slaves' switching surfaces, the PMA and the current equalization algorithm, an FPGA Spartan 3E-500 from Xilinx has been used. In this work, the evaluation board Nexys2 from Digilent has been selected. Fig. 10 shows the system architecture employed for the implementation of the aforementioned controllers.

The block diagram of Fig. 10 points out how the Slaves surfaces $\hat{\sigma}_k$ are implemented, and how the PMA selects the active phases, n. Notice that the value of K, which provides proper interleaving operation, is updated according to the Master switching period, t_s. With regard to the current equalization algorithm, the system takes the measured current through the ADC and, using an emulated μprocessor (PicoBlaze), computes the calculations required for the surfaces σ_k.

The PMA working principle can be separated in two main parts: the CPU Picoblaze block, and the rotation active phases block (RAPB).

1) The CPU Picoblaze block is in charge of selecting the number of active phases according to the total output current of the converter.
2) The RAPB block determines the enabled phases, and which of them acts as the Master phase. The desired rotatory Master phase procedure is implicit in the aforementioned selection, and it is performed at any disconnection phase event. The RAPB module generates the enabled signals, $e_1 \cdots e_m$, the master selection signal, M_s, and the auxiliary signals, $m_1 \cdots m_m$. Subsequently, the signal M_s is used as selector by a hardware multiplexer to route the signal x_m to the Master switching surface (see Fig. 8). The signals $m_1 \cdots m_m$ ensure that the signal generated by the Master switching surface, u_M, is properly routed to the converter acting as the Master one, and deliver the remaining control signals generated by the FPGA to the slaves. In the FPGA, the RAPB block is basically implemented using multiplexers.

TABLE II
MULTIPHASE BUCK CONVERTER EFFICIENCY (%)

$v_c^* \rightarrow$ / $n \rightarrow$ / $i_o \downarrow$	24	24	24	12	24	12	24	12	24	12
	n=3	n=4	n=5		n=6		n=7		n=8	
1	**69.4**	68.0	66.7	**53.6**	65.5	52.7	64.4	51.6	63.1	50.7
3	**87.3**	86.6	85.9	**78.3**	85.3	75.4	84.6	72.2	83.9	70.6
5	**91.8**	91.4	91.0	**85.2**	90.6	84.8	90.1	84.3	89.7	83.8
10	95.0	**95.8**	95.0	**91.3**	94.9	91.1	94.6	91.1	94.4	90.8
15	96.0	96.1	**96.2**	**93.0**	96.1	92.8	96.1	92.9	95.9	92.9
20	96.3	96.5	**96.6**	**93.9**	96.6	93.8	96.6	93.8	96.6	93.8
25	96.3	96.7	96.7	94.0	**96.8**	**94.4**	96.8	94.3	96.8	94.2
30		96.7	96.7	94.2	96.9	94.4	**97.0**	**94.5**	97.0	94.5
35			96.8	94.2	97.0	94.5	97.1	94.6	**97.1**	**94.8**
40			96.8	94.1	96.9	94.5	97.1	94.7	**97.1**	**94.8**
45				93.9	96.9	94.4	97.0	94.5	**97.1**	**94.8**

V. EXPERIMENTALS RESULTS

Different tests have been performed in order to check the operation of a multiphase converter with the control algorithms designed in this work. The tests results are detailed in the following sections.

A. Efficiency, Line Regulation and Load Regulation

Table II presents the measured efficiency for different load values depending on the number of active phases and the output voltage. It has to be remarked that the efficiency includes the power consumption of the control boards and the power stages. Notice also that, due to the theoretical restriction required to ensure interleaving operation [17], [26], (see Section III-H), the number of phases cannot be less than 3 for an output voltage of 24 V and must be greater than 4 in the case of 12 V. From the measured efficiency through exhaustive empiric measurements, the number of active phases are selected (bold values in the Table II for each case of output voltage and output current). Fig. 11 shows the optimum efficiency of the power converter, which achieves efficiencies of 95% and 97% for an output voltages of 12 V and 24 V, respectively. The second and third plots of Fig. 11 depict the measured load and line regulations with the number of phases that optimize the converter efficiency. Both measured indexes confirm the good performance of the designed multiphase converter. On the one hand, load regulation is less than 1% for both tested output voltages and, on the other hand, line regulation remains below 2% for all the power levels. It has to be noted that the system is constantly updating the number of active phases in order to maximize the overall efficiency. As a consequence, the load and line regulation responses present some unexpected variations when the output power increases.

B. Interleaving

Fig. 12 shows the behavior of the current transformer signals of the eight phases in the start-up, when the converter supplies a load of 21 A and the output voltage is regulated to 24 V. As it can be seen in the oscilloscope capture, the interleaving operation is started from the second switching period (see current waveforms on the left bottom window) and achieves

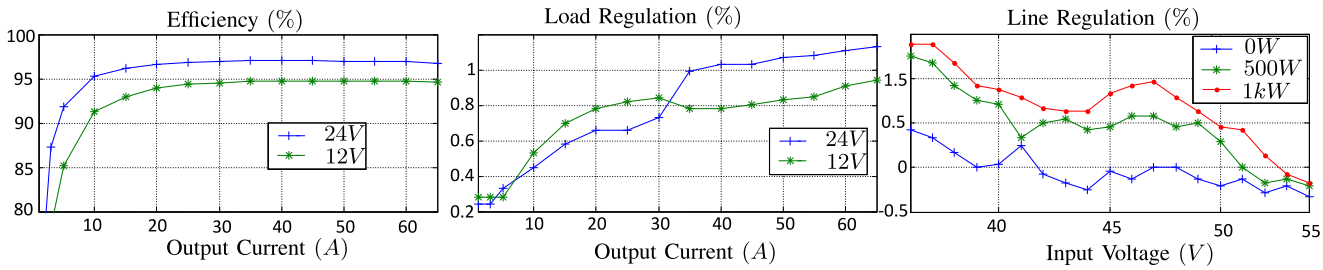

Fig. 11. Optimum efficiency and load regulation of the multiphase converter for 12 and 24 V. Line regulation for an output voltage of 24 V.

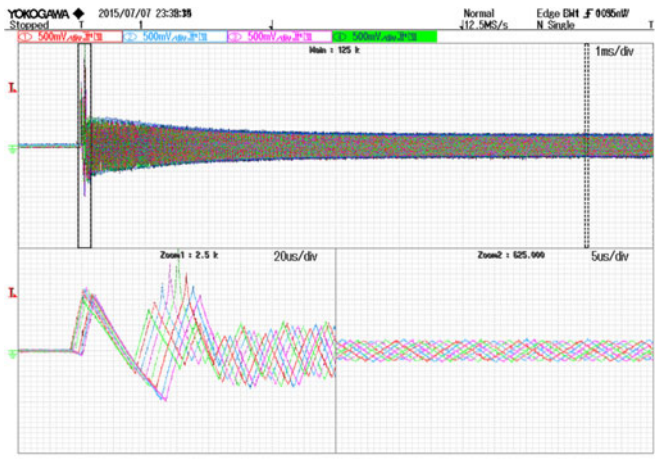

Fig. 12. Start-up of the current transformer signals of the eight phases with a load of 21 A for an output voltage of 24 V.

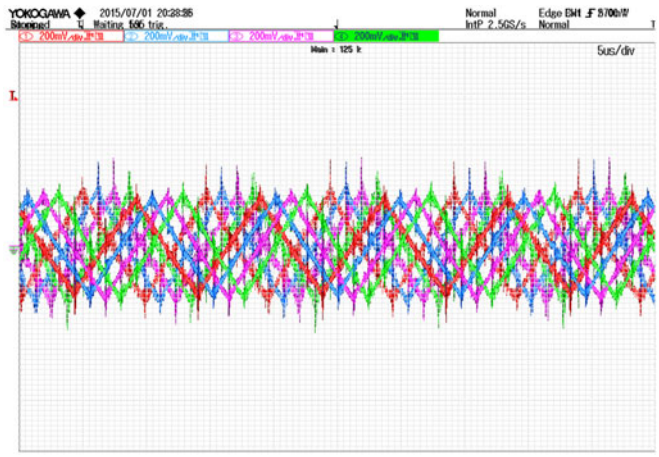

Fig. 13. Steady state of the current transformer signals of the eight phases with a load of 65 A for an output voltage of 24 V.

interleaving at the desired switching frequency of 100 kHz in the steady state (see right bottom window). Fig. 13 shows the steady state behavior of the current transformer signals of the eight phases for a load of 65 A with an output voltage of 24 V. The current ripple flowing through the inductances can be calculated from the current transformer signals measurements. The peak-to-peak measured voltage value shown in the figure is of 400 mV, approximately. Since the current transformer has a secondary winding of 125 turns, and this winding is loaded with

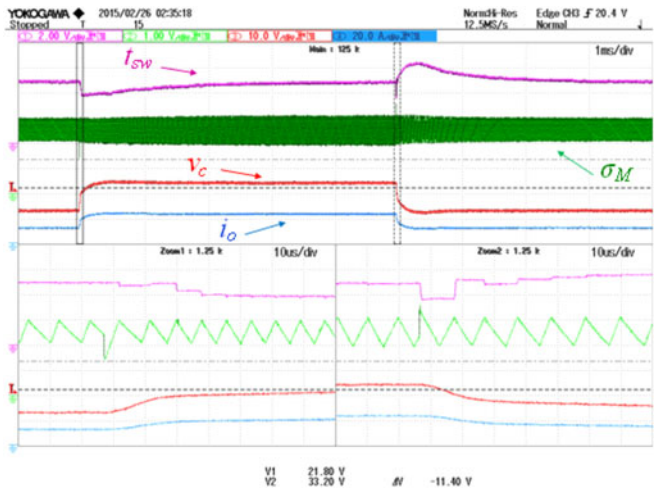

Fig. 14. Reference change 12-24-12 V for six phases and a load of 1 Ω.

a 10 Ω resistor, this voltage corresponds to a 5 A peak-to-peak current ripple, approximately.

C. Output Voltage Regulation Test

In this test, the reference voltage is changed from 12 to 24 V and reversely. The load is of 1 Ω and, according to Table II, the number of connected phases is 6. Fig. 14 portrays the responses of the output voltage, the load current, the switching surface, and the measured switching period (scaled by 0.5 V/μs). The bottom windows show a zoom view of the transient behavior when the output voltage reference changes from 12 to 24 V (left window) and when it decreases from 24 to 12 V (right window). Notice how the output voltage behaves with a smooth transient response, which corresponds to the ideal sliding motion, and the hysteresis values are adapted such that the switching frequency reaches the desired value at steady state.

D. Transient Response for a Load Change

The following figures depict the responses of the output voltage, the switching function, and the switching period (scaled by 0.5 V/μs) when the load changes from 21 to 65 A (see Fig. 15) and from 65 to 21 A (see Fig. 16). In both cases, the output voltage reference is set to 24 V. Since the load is suddenly changed, all the phases are connected during these tests. From these figures it can be inferred how the converter recovers the desired output voltage after a smooth transient response and the switching frequency is not affected by the load change.

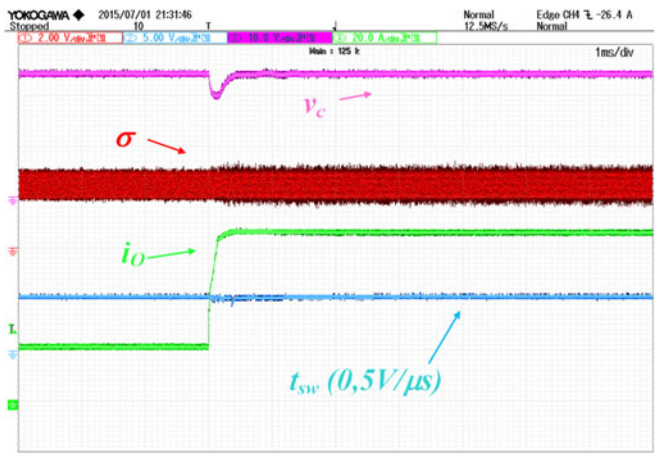

Fig. 15. Load change from 21 to 65 A for a regulated output voltage of 24 V.

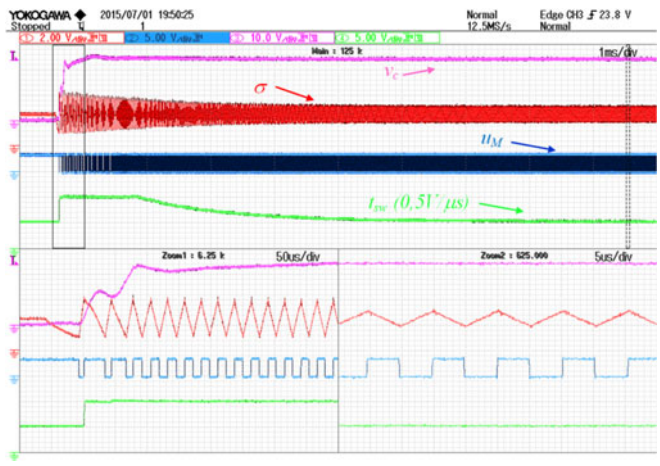

Fig. 17. Start-up with a load of 21 A for a desired output voltage of 24 V.

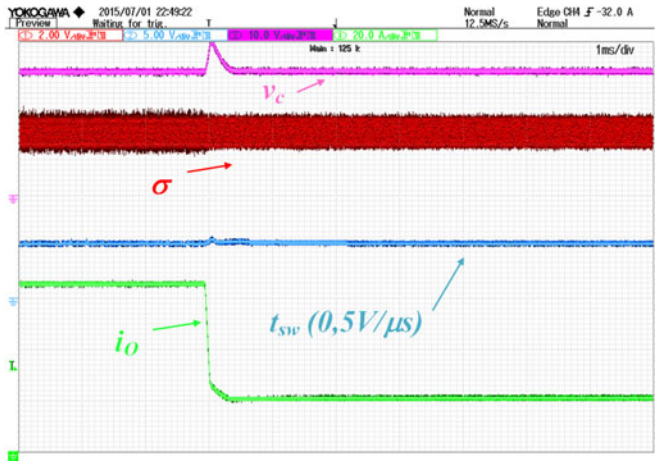

Fig. 16. Load change from 65 to 21 A for a regulated output voltage of 24 V.

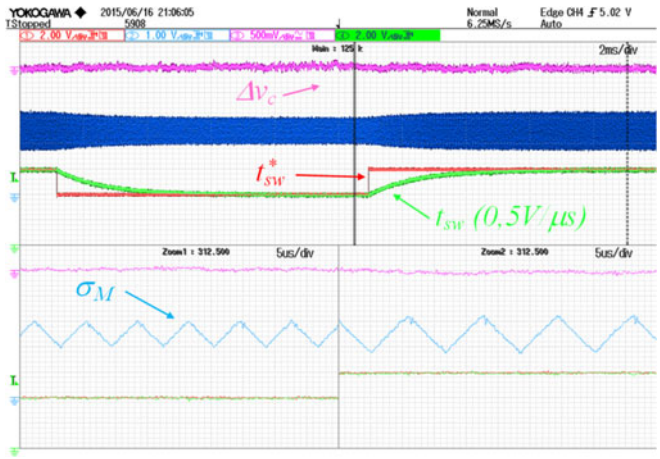

Fig. 18. Switching frequency variation from 8 to 12 μs with a desired output voltage of 24 V and no load.

E. Switching Frequency Regulation Test

Two different tests have been performed to show the proper switching frequency regulation. The first one consists in a start-up of the multiphase converter for an output voltage reference of 24 V delivering 21 A to the load. The results are presented in Fig. 17. The figure shows the behaviors of the output voltage, the switching function, the Master control signal, and the measured switching period. The bottom windows detail the waveforms in the transient state (left window) and in the steady state (right window). As it can be seen in the figure, the output voltage reaches the desired voltage with a smooth transient and with a small overshoot, the hysteresis bands are adapted such that the steady state switching frequency achieves the desired value of 100 kHz, and the theoretically predicted overdamped response is observed in the switching period transient motion.

The second test is devoted to highlight the switching frequency tracking of step type references. The switching period reference varies from 8 to 12 μs and vice-versa. The output voltage is regulated to 24 V and the load is in open circuit. Fig. 18 shows the behaviors of the output voltage ripple, the switching function, the switching period, and the switching period reference. The SFC adjusts the hysteresis band value in order to achieve the desired steady state switching period with the expected motion according to the model derived in Section III-G. Notice also that the switching function does not leave the bounds given by the hysteresis band, and therefore the multiphase converter remains in interleaving operation and the output voltage is not affected by the switching frequency reference variation. This effect can be inferred from the low output voltage ripple, Δv_c, observed during the entire test. The waveforms detailed in the bottom windows correspond to the steady state dynamics at 8 μs (left window) and at 12 μs (right window).

F. Current Equalization Test

Fig. 19 shows the effect over the phase currents when the equalization algorithm is enabled and disabled. Specifically, the figure details both transients for the eight average currents. The sensitivity of the Hall current sensors used to measure the average current is of 160 mV/A. The equalization test has been performed for the full load case and 24 V regulated at the output. When the algorithm is enabled the values of the currents flowing through each phase are around the expected value of 8.125 A with a maximum difference among them of 0.625 A. Within

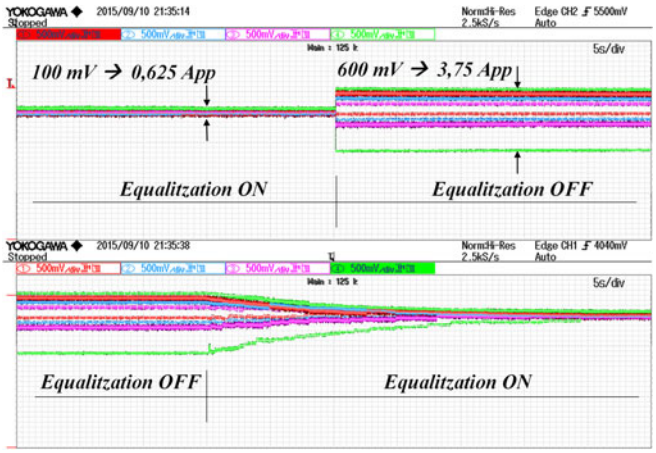

Fig. 19. Current equalization for 24 V/65 A.

TABLE III
ENABLING AND DISABLING CURRENT VALUES (A) FOR 24 V OUTPUT VOLTAGE

m (Number of Phases)	3	4	5	6	7	8
Optimum Value (A)	–	7.5	12.5	23	27.5	33
Connection Value (A)	–	8.7	13.7	24.2	28.7	34.2
Disconnection Value (A)	–	6.3	11.3	21.8	26.3	31.8

the time frame where the equalization algorithm is disabled, the unbalance among phases reaches a value of 3.75 A. The result confirms the good performance of the algorithm, and all the average current values converge to the same value in steady state. It has to be remarked that in the original configuration the phases present similar losses and the current unbalance becomes negligible. In order to show the good behavior of the equalization algorithm, the phases were deliberately unbalanced adding a 10 mΩ resistor in phases 4 and 7.

G. Power Management Test

The PMA selects the number of active phases at any time. Table III shows the connection and disconnection values of the output current according to the measured efficiency presented in Table II. In order to avoid undesirable connection-disconnection events, an hysteresis of 2.4 A has been added between the connection and the disconnection values.

Fig. 20 presents the currents waveforms of the eight phases when the reference voltage is set to 24 V and the multiphase converter supplies a specific load profile. As it has been stated in Section III-H, a minimum of three active phases is required to guarantee interleaving sliding mode. The figure shows how the different phases are sequentially connected (disconnected) as the load demand increases (decreases). The rotating assignment of the Master phase among the converter phases can also be checked in the figure. The figure also displays the number of active converters, one of which is the Master phase, and the values of the current supplied to the load at any time range.

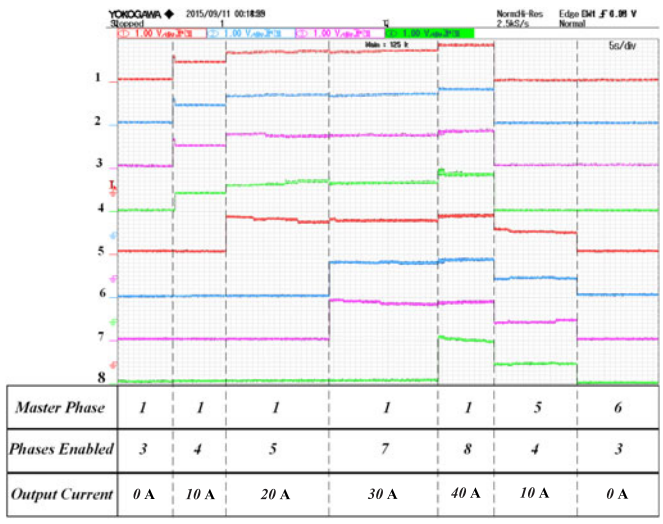

Fig. 20. Power management: average phase currents when the output voltage is regulated to 24 V.

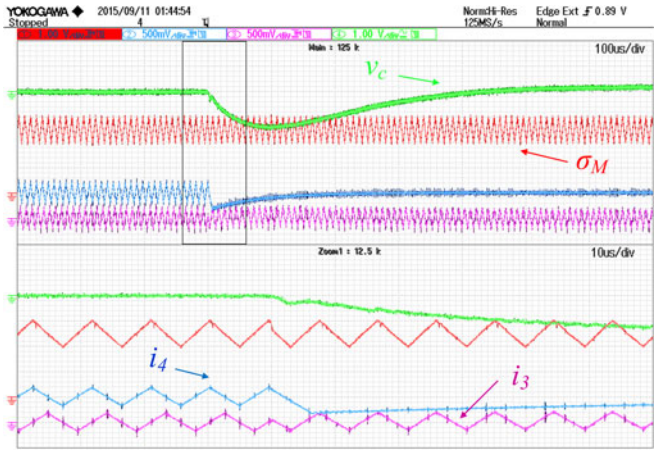

Fig. 21. Transient response of the output voltage when the system changes the number of active phases and the Master phase.

Fig. 21 presents the output voltage transient when a change of the number of the active phases happens. In the figure it can be seen how the system changes from 4 active phases to 3, delivering 18 A to the load. In this test, in order to decouple the transient effects of a phase disconnection and of a load reduction, the PMA is disabled, performing the disconnection event manually. Notice how being phase 4 the Master one, it is disabled (see the zoomed area in the bottom part of Fig. 21) and the system selects phase 3 as the new Master. The green signal of the figure corresponds to the output voltage. The output voltage transient has an undershoot lower than 1 V.

H. Thermal Test

Fig. 22 shows a thermal capture of the converter when supplies a load of 65 A with a regulated output voltage of 24 V. From the figure, it is confirmed that power losses are properly dissipated, since the temperature remains below 60° C in the hottest parts without any type of active cooling.

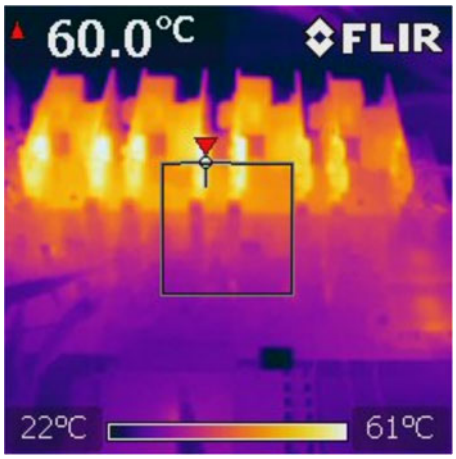

Fig. 22. Thermal image of the converter with 65 A delivered to the load with a regulated voltage of 24 V.

VI. Conclusion

In this paper, an interleaved SMC for a multiphase synchronous buck converter has been presented. Besides the interleaving operation, the sliding mode control includes an algorithm which enforces current equalization among the phases. Moreover, switching frequency regulation is performed using an additional control loop which acts over the hysteresis band value of the Master surface. Furthermore, a PMA and a rotatory master technique have also been added in order to select the number of active phases maximizing the overall efficiency and to equalize the working time among the phases, increasing the system reliability. A set of experimental tests has been carry out on an eight-phase converter built for this purpose. The controllers have been implemented using analogue circuitry together with an FPGA. The power stage of the prototype has been divided in eight phases (synchronous buck converters) and a motherboard where the phases can be easily plugged in. The measured overall efficiency is of 97% at 24 V when the multiphase converter supplies a load of 1.5 kW. The efficiency includes the energy consumption of the power stage, the analogue circuitry and the FPGA board. The experimental results confirm the robustness, interleaving operation, output voltage regulation, current equalization, power management, and fixed switching frequency in the steady state provided by the designed controllers.

References

[1] W. Chen, "High efficiency, high density, polyphase converters for high current applications," *Linear Technol. Appl. Note*, vol. 77, pp. 1–16, 1999.

[2] M. T. Zhang, M. M. Jovanović, and F. C. Lee, "Design considerations for low-voltage on-board DC/DC modules for next generations of data processing circuits," *IEEE Trans. Power Electron.*, vol. 11, no. 2, pp. 328–337, Mar. 1996.

[3] X. Zhou, P.-L. Wong, P. Xu, F. C. Lee, and A. Q. Huang, "Investigation of candidate VRM topologies for future microprocessors," *IEEE Trans. Power Electron.*, vol. 15, no. 6, pp. 1172–1182, Nov. 2000.

[4] A. V. Peterchev, J. Xiao, and S. R. Sanders, "Architecture and IC implementation of a digital VRM controller," *IEEE Trans. Power Electron.*, vol. 18, no. 1, pp. 356–364, Jan. 2003.

[5] O. Garcia, P. Zumel, A. De Castro , and J. Cobos, "Automotive DC-DC bidirectional converter made with many interleaved buck stages," *IEEE Trans. Power Electron.*, vol. 21, no. 3, pp. 578–586, May 2006.

[6] J.-B. Baek, W.-I. Choi, and B.-H. Cho, "Digital adaptive frequency modulation for bidirectional DC–DC converter," *IEEE Trans. Ind. Electron.*, vol. 60, no. 11, pp. 5167–5176, Nov. 2013.

[7] T. Dragicevic, J. C. Vasquez, J. M. Guerrero, and D. Skrlec, "Advanced LVDC electrical power architectures and microgrids: A step toward a new generation of power distribution networks," *IEEE Electrification Mag.*, vol. 2, no. 1, pp. 54–65, Mar. 2014.

[8] A. Kwasinski and P. T. Krein, "An integrated 42-V drive design for automobile loads with a low-distortion overmodulation strategy," *IEEE Trans. Power Electron.*, vol. 21, no. 3, pp. 648–658, May 2006.

[9] O. García, A. De Castro , P. Zumelis, and J. Cobos, "Digital-control-based solution to the effect of nonidealities of the inductors in multiphase converters," *IEEE Trans. Power Electron.*, vol. 22, no. 6, pp. 2155–2163, Nov. 2007.

[10] K. Zhang, S. Luo, T. X. Wu, and I. Batarseh, "New insights on dynamic voltage scaling of multiphase synchronous buck converter: A comprehensive design consideration," *IEEE Trans. Power Electron.*, vol. 29, no. 4, pp. 1927–1940, Apr. 2014.

[11] P.-L. Wong, P. Xu, B. Yang, and F. C. Lee, "Performance improvements of interleaving VRMs with coupling inductors," *IEEE Trans. Power Electron.*, vol. 16, no. 4, pp. 499–507, Jul. 2001.

[12] S. Chae, Y. Song, S. Park, and H. Jeong, "Digital current sharing method for parallel interleaved DC–DC converters using input ripple voltage," *IEEE Trans. Ind. Inform.*, vol. 8, no. 3, pp. 536–544, Aug. 2012.

[13] R. P. Singh and A. M. Khambadkone, "Current sharing and sensing in N-paralleled converters using single current sensor," *IEEE Trans. Ind. Appl.*, vol. 46, no. 3, pp. 1212–1219, May 2010.

[14] R. Foley, R. Kavanagh, and M. Egan, "Sensorless current estimation and sharing in multiphase buck converters," *IEEE Trans. Power Electron.*, vol. 27, no. 6, pp. 2936–2946, Jun. 2012.

[15] J. A. Abu-Qahouq , "Analysis and design of N-phase current-sharing autotuning controller," *IEEE Trans. Power Electron.*, vol. 25, no. 6, pp. 1641–1651, Jul. 2010.

[16] J. Sun, Y. Qiu, M. Xu, and F. C. Lee, "High-frequency dynamic current sharing analyses for multiphase buck VRs," *IEEE Trans. Power Electron.*, vol. 22, no. 6, pp. 2424–2431, Nov. 2007.

[17] R. Ramos, D. Biel, E. Fossas, and R. Griño, "Sliding mode controlled multiphase buck converter with interleaving and current equalization," *Control Eng. Pract.*, vol. 21, no. 5, pp. 737–746, 2013.

[18] A. Costabeber, P. Mattavelli, and S. Saggini, "Digital time-optimal phase shedding in multiphase buck converters," *IEEE Trans. Power Electron.*, vol. 25, no. 9, pp. 2242–2247, Sep. 2010.

[19] Y. Ahn, I. Jeon, and J. Roh, "A multiphase buck converter with a rotating phase-shedding scheme for efficient light-load control," *IEEE J. Solid-State Circuits*, vol. 49, no. 11, pp. 2673–2683, Nov. 2014.

[20] J.-T. Su and C.-W. Liu, "A novel phase-shedding control scheme for improved light load efficiency of multiphase interleaved DC–DC converters," *IEEE Trans. Power Electron.*, vol. 28, no. 10, pp. 4742–4752, Oct. 2013.

[21] J. Abu-Qahouq , H. Mao, and I. Batarseh, "Multiphase voltage-mode hysteretic controlled dc-dc converter with novel current sharing," *IEEE Trans. Power Electron.*, vol. 19, no. 6, pp. 1397–1407, Nov. 2004.

[22] K. Lee, F. C. Lee, and M. Xu, "A hysteretic control method for multiphase voltage regulator," *IEEE Trans. Power Electron.*, vol. 24, no. 12, pp. 2726–2734, Dec. 2009.

[23] S. Mazumder and S. Kamisetty, "Design and experimental validation of a multiphase VRM controller," *IEE Proc.-Electric Power Appl.*, vol. 152, no. 5, pp. 1076–1084, Oct. 2005.

[24] V. Utkin, J. Guldner, and J. Shi, *Sliding Mode Control in Electro-Mechanical Systems*. Boca Raton, FL, USA: CRC Press, 2009, vol. 34.

[25] F. Bilalovic, O. Music, and A. Sabanovic, "Buck converter regulator operating in the sliding mode," in *Proc. VII Int. PCI*, 1983, vol. 10, pp. 333–340.

[26] H. Lee, V. I. Utkin, and A. Malinin, "Chattering reduction using multiphase sliding mode control," *Int. J. Control*, vol. 82, no. 9, pp. 1720–1737, 2009.

[27] V. Repecho, D. Biel, and E. Fossas, "Fixed switching frequency sliding mode control using an hysteresis band controller," in *Proc. 13th IEEE Int. Workshop Variable Struct. Syst.*, 2014, pp. 1–6.

[28] V. Repecho, D. Biel, J. M. Olm, and E. F. Colet, "Switching frequency regulation in sliding mode control by a hysteresis band controller," *IEEE Trans. Power Electron.*, vol. 32, no. 2, pp. 1557–1569, Feb. 2017.

Víctor Repecho received the B.S and M.S. degrees in electronic engineering from the Universitat Politècnica de Catalunya (UPC), Barcelona, Spain, in 2006 and 2012, respectively.

Since 2010, he has been a development Engineer with the Institute of Industrial and Control Engineering, UPC. His research interests include digital control, nonlinear control, and control of power electronic converters.

Domingo Biel received the B.S, M.S., and Ph.D. degrees in telecommunications engineering from the Universitat Politècnica de Catalunya (UPC), Barcelona, Spain, in 1990, 1994, and 1999, respectively.

Since 1998, he has been an Associate Professor in the Department of Electronic Engineering, UPC, where he teaches power electronics and control theory. He is the coauthor of around 20 papers in international journals and more than 50 communications in international conferences. His research interests include nonlinear control and its application to renewable energy systems and power electronics.

Rafael Ramos-Lara received the B.S., M.S., and Ph.D. degrees in telecommunications engineering from the Universitat Politècnica de Catalunya (UPC), Barcelona, Spain, in 1990, 1996, and 2006, respectively.

Since 1999, he has been an Associate Professor in the Department of Electronic Engineering, UPC. His research interests include nonlinear controller, sliding mode control, power electronics, adaptive signal processing and digital implementation of signal processing systems, and biometrics algorithms.

Pilar García Vega received the B.S and M.S. degrees in electronic engineering from the Universitat Politècnica de Catalunya, Barcelona, Spain, in 2006 and 2016, respectively.

Her research interest includes power electronic converters.