Design and Implementation of a Two-Channel Interleaved Vienna-Type Rectifier With >99% Efficiency

Qiong Wang, *Student Member, IEEE*, Xuning Zhang, Rolando Burgos, *Member, IEEE*, Dushan Boroyevich, *Fellow, IEEE*, Adam M. White, and Mustansir Kheraluwala

***Abstract*—In this paper, the design and implementation of a 3 kW, three-phase, two-channel interleaved Vienna-type rectifier with greater than 99% efficiency is presented. The operating principle of the interleaved Vienna-type rectifier is introduced, with particular attention paid to the switching-frequency circulating current generated by the interleaved operation, as well as effective mitigation methods. An optimized design procedure for the converter is then presented to achieve maximum efficiency, for which detailed loss calculation models and hardware design guidelines are developed and introduced. Finally, experimental results obtained with a 3 kW experimental prototype are presented for validation purposes, demonstrating the 99.28% extreme efficiency attained by the converter at nominal load, in close agreement with the 99.32% predicted by the design procedure developed.**

***Index Terms*—AC–DC power converters, coupled inductor, efficiency, interleaved.**

I. Introduction

THREE-PHASE active pulse width modulation (PWM) rectifiers are commonly used as a means of increasing efficiency and improving the source current power quality, as they feature a superior performance compared to their diode-based counterparts. In effect, conventional two-level three-phase boost rectifiers have become dominant in industry, a choice further supported by their inherent simplicity. However, if higher efficiency is sought, three-level converters represent a better solution thanks to their lower switching voltage [1]. This type of topology is increasingly being adopted for these applications, a trend that has been made easier by the recent availability of integrated power semiconductor modules in various three-level configurations.

Three-level rectifiers can be classified in bidirectional and unidirectional power flow topologies. Among bidirectional topologies, one of the most recognized is the three-level neutral-point-clamped (NPC) boost rectifier [2]. An alternative realization of the latter is the T-type topology, which uses a hybrid phase-leg implementation with two devices blocking the dc bus voltage and two devices in ac-switch configuration blocking half the dc bus voltage [3]. Unidirectional topologies feature a reduced number of switching devices. These topologies are usually referred as Vienna-type [4] or force commutated rectifiers [5]. The term "Vienna-type rectifier" is used to refer to the unidirectional three-level boost rectifier in this paper. Several phase-leg implementations for Vienna-type rectifiers have been proposed and discussed attaining different key features [4]–[6]. Fig. 1 shows the most used phase leg for this converter. The main features of these phase legs and the topologies mentioned above are summarized in Table II in Appendix A.

To illustrate the potential efficiency gain brought forth by three-level converters, Fig. 2 shows the loss breakdown for several three-level topologies including Vienna-type rectifiers with alternative phase-leg realizations. A two-level boost rectifier is included as benchmark. The losses were calculated using the design procedure developed in this paper (see Section IV) in accordance with the specifications under consideration; namely 3 kW output power, 230 V ac input voltage, and 650 V dc output voltage. As shown, the Vienna-type rectifier with phase-leg implementation (d) features the lowest loss among these converters. This is due to the minimum losses that result from the main commutation loop (MOSFET and diode), which takes advantage of the use of silicon–carbide (SiC) Schottky devices, and due to the fact that only one diode conducts when clamping the positive or negative dc bus. Although these are rated at 1200 V, the forward and characteristics and junction capacitance of SiC Schottky diodes differ little between 600 and 1200 V devices [7], [8]; hence the advantage attained. In addition, this phase-leg implementation only requires one isolated gate driver per phase leg.

Manuscript received July 18, 2016; revised December 11, 2016; accepted February 2, 2017. Date of publication February 20, 2017; date of current version October 6, 2017. This work was supported by UTC Aerospace Systems. Recommended for publication by Associate Editor Prof. Toshihisa Shimizu.

Q. Wang, R. Burgos, and D. Boroyevich are with the Center for Power Electronics Systems, Bradley Department of Electrical and Computer Engineering,Virginia Tech, Blacksburg, VA 24061 USA (e-mail: wangq@vt.edu; rolando@vt.edu; dushan@vt.edu).

X. Zhang was with the Center for Power Electronics Systems, Bradley Department of Electrical and Computer Engineering,Virginia Tech, Blacksburg, VA 24061 USA. He is now with Monolith Semiconductor, Inc., Ithaca, NY 14850 USA (e-mail: xuning45@vt.edu).

A. M. White was with United Technology Aerospace Systems, Rockford, IL 61108 USA. He is now with Kaney Aerospace, Rockford, IL 61109 USA (e-mail: white.adam.m@gmail.com).

M. Kheraluwala is with United Technology Aerospace Systems, Rockford, IL 61108 USA (e-mail: mustansir.kheraluwala@hs.utc.com).

Color versions of one or more of the figures in this paper are available online at http://ieeexplore.ieee.org.

Digital Object Identifier 10.1109/TPEL.2017.2671844

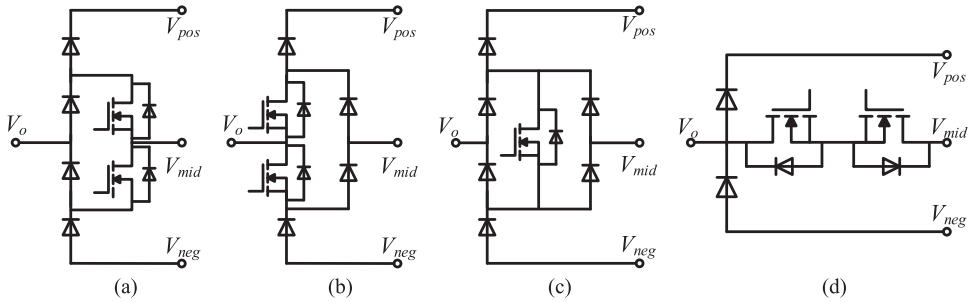


Fig. 1. Alternative phase-leg implementations of the Vienna-type rectifier.

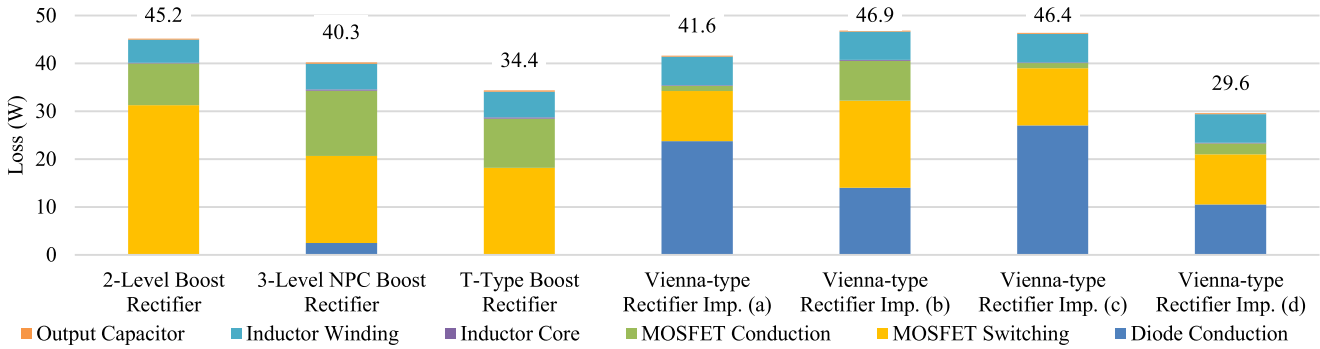


Fig. 2. Loss distribution and comparison between three-phase active rectifier topologies.

A method to further increase efficiency and improve the thermal management of a power converter is to use parallel switches or parallel phase legs. In the latter case, if additionally the gate signals of the corresponding switches of each phase leg are interleaved, both the converter efficiency and power density can be increased [9]–[16]. Specifically, the harmonic cancellation effect among the interleaved phase legs allows for the use of lower switching frequencies, while simultaneously reducing the size of input power quality and electromagnetic interference (EMI) filters [17]. It is expected then that an interleaved *n*-channel Vienna-type rectifier [16], [18], [19] would feature even higher efficiency and power density than its single-channel embodiment. In search of a topology with an efficiency exceeding 99% that could eliminate the need for active cooling, this work adopted a two-channel interleaved Vienna-type rectifier.

Specifically, this paper presents the design and optimization of a 3 kW, three-phase, two-channel interleaved Vienna-type rectifier with an efficiency greater than 99%. The converter operation is optimized for: three-phase 230 V ac, 360–800 Hz line frequency, 650 V dc output, and 3 kW output power. The paper is organized as follows: Section II presents the operation principles of the interleaved Vienna-type rectifier; Section III presents the analysis of the resultant circulating current between converter channels; Section IV presents the comprehensive design procedure developed for the converter in question, including the design flow chart, detailed loss estimation, and semiconductor selection; Section V presents and discusses the experimental results; and finally, Section VI presents the conclusions drawn from this work.

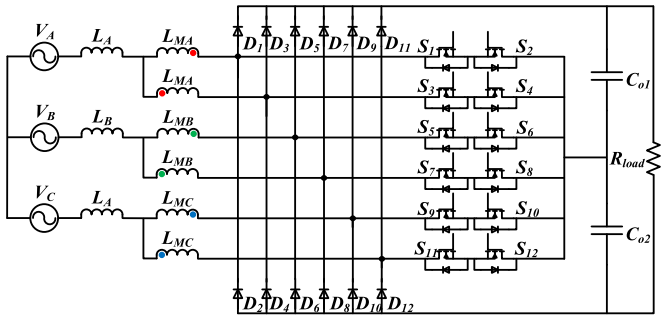


Fig. 3. Topology of a dual-channel interleaved Vienna-type rectifier.

II. Interleaved Vienna-Type Rectifier Operation

A. Topology Introduction

Fig. 3 shows the topology of the interleaved Vienna-type rectifier considered in this paper. In this circuit, $S_1 - S_2$, $S_5 - S_6$, and $S_9 - S_{10}$ and the diodes directly connected to these MOSFET switch pairs $D_1 - D_2$, $D_5 - D_6$, and $D_9 - D_{10}$ form a three-phase subconverter that can operate independently as a rectifier. The remaining switch pairs $S_3 - S_4$, $S_7 - S_8$, and $S_{11} - S_{12}$ and their corresponding diodes $D_3 - D_4$, $D_7 - D_8$, and $D_{11} - D_{12}$ form a second subconverter. The corresponding phase legs in these two subconverters are connected using interphase inductors L_{MA}, L_{MB}, and L_{MC}, as seen in Fig. 3. L_A, L_B, and L_C correspond to the input boost inductors of the converter, which are shared by the phase legs of both subconverters as energy storage inductors. As example, the phase leg

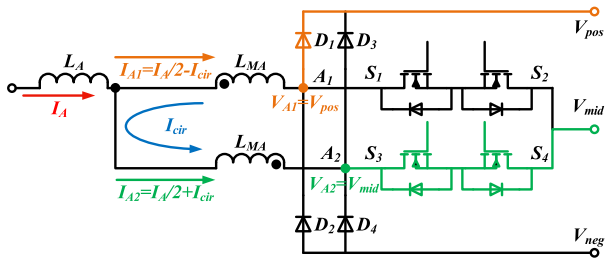


Fig. 4. Circulating current generation mechanism.

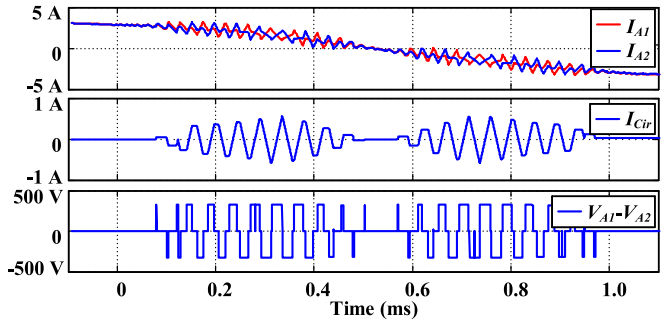


Fig. 5. From top to bottom: simulated current of each subconverter, circulating current, and the corresponding voltage difference.

constituted by D_1, D_2, S_1, and S_2 and the phase leg constituted by D_3, D_4, S_3, and S_4 are connected by the interphase inductor L_{MA} sharing the input boost inductor L_A.

B. Operating Principle

The Vienna-type rectifier is a current-commutated converter [5], [20], that is, the devices that commutate at any given switching instant are determined by the instantaneous current direction. For example, if current $I_{\mathrm{A}1}$ in Fig. 4 is positive, the commutation will take place between D_1 and the combined switch $S_1 - S_2$. As a result, the voltage potential at point A_1 with reference to the middle point of the dc bus will be either half of the dc bus voltage, when $S_1 - S_2$ is OFF, or zero, when $S_1 - S_2$ is ON.

To operate the converter in an interleaved manner, a phase shift is introduced between the PWM carriers of the two subconverters that compound it [11], [16], [21]. This operating mode forces specific current harmonic components to circulate between the corresponding phase legs of the subconverters, which renders smoother the current drawn from the source. In many applications, this is known as the harmonic cancellation effect, where the cancellation frequency depends on the number of interleaved phases and interleaving angle used [11], [16]. As a result, the switching frequency of each subconverter in the interleaved system can be lower while keeping the same input current quality (or total harmonic distortion (THD)), which helps reduce the converter switching loss.

III. Circulating Current Generation and Mitigation in Interleaved Converters

A. Generation Mechanism of Circulating Current in Interleaved Converters and Its Influence

An unwanted effect of interleaving two subconverters is the generation of circulating current [11]. This phenomenon is the side effect of the harmonic cancellation that occurs as a result of interleaving. As described in the previous section, harmonic components of the two interleaved phase legs that are out of phase are cancelled on the source side, but are left to circulate freely between the two subconverter phase legs. The circulating current is produced by the voltage difference between the interleaved phase legs. This is illustrated in Fig. 4, where currents in the two interleaved phase legs are labeled I_{A1} and I_{A2} and the circulating current I_{cir} is defined as the averaged difference between the currents in two interleaved phase legs ($I_{\mathrm{cir}} = (I_{A1} - I_{A2})/2$). In addition, the current flowing through the input boost inductor is labeled I_A, which splits evenly in the two interleaved phase legs. With all these definitions, I_{A1} and I_{A2} equal to $(I_A/2 + I_{\mathrm{cir}})$ and $(I_A/2 - I_{\mathrm{cir}})$, respectively.

Assuming now, without loss of generality, I_{A} is greater than zero. If point A_1 is clamped to the positive rail by diode D_1 and A_2 is connected to the middle point of the dc bus by S_3 and S_4, the voltage difference between A_1 and A_2 will generate current (I_{cir}) circulating between these two phase legs. Fig. 5 shows the simulated waveforms of the current in phase A of each subconverter (I_{A1} and I_{A2}), the circulating current (I_{cir}), and the voltage difference between A_1 and A_2; namely $V_{A1} - V_{A2}$. This clearly shows that the voltage difference determines the circulating current, such that when the voltage difference is positive, the circulating current increases, and when negative, it decreases.

If the amplitude of the circulating current is too large, it will not only create additional conduction losses, but it will also impede the proper operation of the converter. For instance, when I_A is positive, point A_1 should be clamped to either the positive rail by D_1 or the middle point of dc bus by $S_1 - S_2$; however, if I_{cir} is high enough that I_{A1} becomes negative $(I_{A1} = I_A/2 - I_{\mathrm{cir}} < 0)$, it will be impossible to connect point A_1 to the positive rail when $S_1 - S_2$ are OFF. Instead, this phase leg would clamp to the negative dc bus rail, resulting in a modulation error. This illustrates why the circulating current in interleaved current-commutated converters, as the Vienna-type rectifier, should be well controlled.

B. Circulating Current Attenuation Method

The voltage difference between the two interleaved phases, which causes the circulating current, is inevitable in interleaved converters. In each switching cycle, the voltage difference is predetermined by the modulation scheme and working conditions; thus, a known approach to attenuate the circulating current is to increase the impedance between the two interleaved phases. Adding coupling inductors between the interleaved phases, also known as interphase inductors, can effectively increase the impedance of the circulating loop while maintaining only a minor influence on the common current $(I_A/2)$ [11], [14], [16], [22]. In Fig. 4, such inductor is depicted as L_{MA} for phase legs A_1 and A_2. A physical implementation example of the coupling

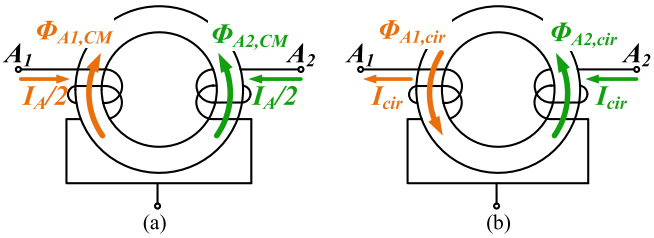


Fig. 6. (a) Interphase inductor and flux generated by common current $(I_A/2)$. They cancel each other. (b) Interphase inductor and flux generated by circulating current $(I_{\rm cir})$. They couple to the other windings.

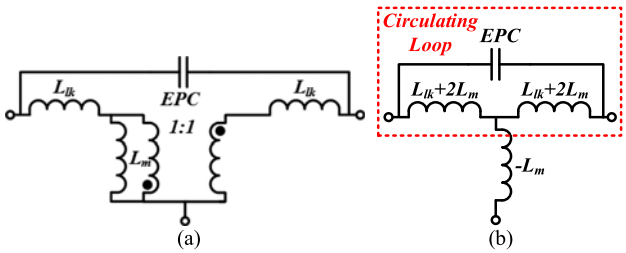


Fig. 7. (a) Transformer-based equivalent circuit of the interphase inductor; and (b) T-equivalent circuit based model of the interphase inductor.

inductors is shown in Fig. 6. The orange and green arrows represent the flux generated by the orange and green currents (in Fig. 4) of phase leg A_1 and A_2, respectively.

Fig. 6(a) shows the flux components generated by the source current components $I_A/2$. It illustrates how the coupled inductor has no effect over the source current components as the flux cancels out in the magnetic core. Whereas Fig. 6(b) shows the flux components generated by the circulating currents. These flux components add up, effectively embodying an inductor and consequently adding a high impedance to the circulating current path.

C. Design and Implementation Considerations of Interphase Inductors

The interphase inductors in the dual channel interleaved Vienna-type rectifier should be designed to avoid the modulation errors described above. Its impedance should be high enough to ensure that for any fundamental period half-cycle, the respective phase currents should be either positive or negative.

Equivalent circuits of coupled inductors have been used to facilitate the design. Fig. 7(a) shows the transformer-based equivalent circuit of a coupled inductor, and Fig. 7(b) shows its T-shape equivalent representation. From the latter, the inserted impedance of the interphase inductor can be determined. As seen in Fig. 7, the equivalent circuit also includes an equivalent-parallel-capacitance (EPC), which represents the parasitic capacitance between the different winding layers, and the parasitic capacitance between the windings and the magnetic core of the inductor. These parasitic capacitances are all lumped as a single EPC component. In general, for frequencies close to the converter switching frequency (20–100 kHz), the effect of the EPC can be neglected as its value is typically in the order of tens of pico-farads.

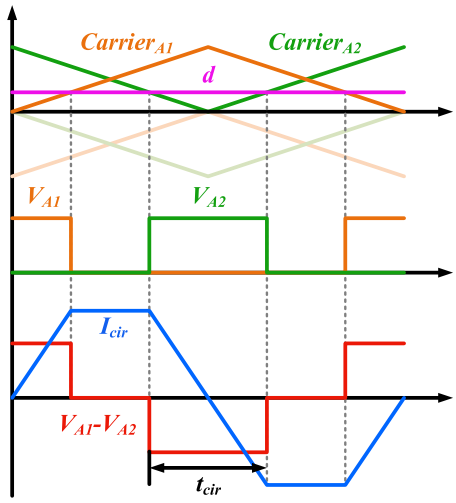


Fig. 8. Relationship between modulation, phase leg output voltage, and circulating current.

To illustrate the detailed operation of the interleaved converter phase legs and the resultant circulating current, Fig. 8 presents a zoomed view of the modulator and the resultant voltage and current waveforms in one switching cycle. The top axis shows the two double-carrier signals—proper of three-level converters, namely Carrier_{A1} and Carrier_{A2}, phase shifted by 180° in accordance with the interleaving scheme used. The duty cycle in this switching cycle is labeled as d in the top axis. The resultant output voltages of the interleaved phase legs V_{A1} and V_{A2} are shown in the second axis. The difference between these two voltages $V_{A1} - V_{A2}$, which corresponds to the voltage source of the circulating current, is shown in the bottom axis together with the resultant circulating current $I_{\rm cir}$. From this figure, as well as the equivalent circuit of coupled inductor (shown in Fig. 7), the relationship between the peak value of $I_{\rm cir}$ and the voltage applied across A_1 and A_2 can be determined as follows:

$$|I_{\rm cir,peak}| = \frac{|V_{A1} - V_{A2}|\frac{t_{\rm cir}}{2}}{4L_m + 2L_{\rm lk}} \tag{1}$$

where $I_{\rm cir,peak}$ is the peak circulating current value, V_{A1}, V_{A2} are the voltage outputs of the interleaved phase legs (referred to the dc bus middle point), $t_{\rm cir}$ is the duration of the voltage pulse (positive or negative) at the given switching cycle, and L_m and $L_{\rm lk}$ the magnetizing and leakage inductances of the interphase inductor. The voltage difference $V_{A1} - V_{A2}$ is always equal to half of the dc-link voltage. However, the width of the applied pulse $t_{\rm cir}$, determined by modulation scheme and operating condition, varies significantly throughout the line cycle. Consequently, and taking into consideration that the only control over $I_{\rm cir,peak}$ is given by the interphase inductor impedance, the inductance of the latter should fulfill the following condition to avoid modulation errors:

$$|I_{\rm cir,peak}| = \frac{|V_{A1} - V_{A2}|\frac{t_{\rm cir}}{2}}{4L_m + 2L_{\rm lk}} < |\frac{I_A}{2}| \tag{2}$$

where I_A is the total input phase current of phase A during the switching cycle in question (see Fig. 4). This condition should be naturally met throughout the entire line cycle, requiring that

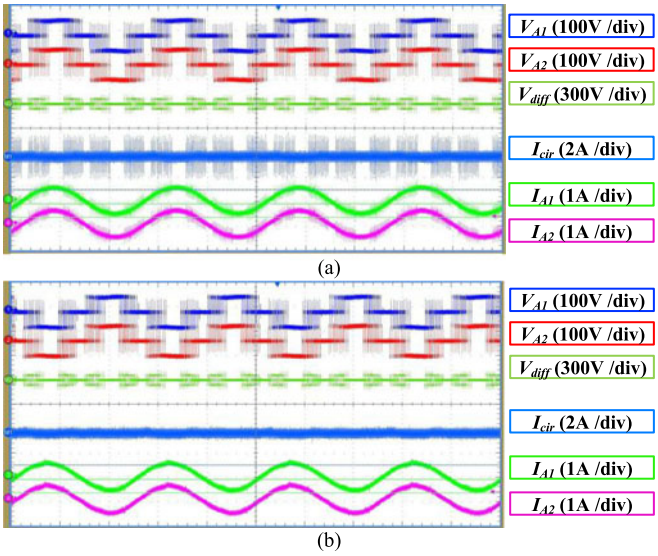


Fig. 9. (a) Waveforms without enough impedance in the circulating loop at high frequency. High-frequency ringing can be observed on $I_{\rm cir}$ (the averaged difference between I_{A1} and I_{A2}), I_{A1}, and I_{A2}. (b) Waveforms with high impedance inserted at high frequency. $I_{\rm cir}$, I_{A1}, and I_{A2} are less distorted.

a switching cycle-by-cycle analysis be carried out. Given that different modulation schemes will result in significantly different volt-second quantities applied to the interphase inductor, a MATLAB Simulink model based analysis was carried out to determine the required inductance in this case.

The complete design of the interphase inductor will finally require that other constraints be considered. In order to avoid magnetic material saturation, as well as excessive core and winding losses of the inductor, higher inductance values might be required in its final construction.

Another important problem in the construction of the interphase inductor is that its winding EPC is not negligible at high frequencies (>1 MHz). While the inductance of the interphase inductor increases the impedance of the circulating loop, the EPC has a significant but reverse effect on the total impedance in this frequency range. This is important since the voltage applied to the circulating loop contains high-frequency components that result from the drain-to-source voltage ringing. This effect is exacerbated when using wide-bandgap power semiconductor with *dv/dt* slew rates in the 20–100 V/ns range. This phenomenon is shown in Fig. 9, which illustrates the interleaved phase voltages V_{A1N}, V_{A2N} and the resultant circulating current $I_{\rm cir}$. The waveforms are obtained with the Vienna-type rectifier prototype presented in this paper.

To highlight the above-mentioned phenomenon, Fig. 9(a) shows the measured high-frequency current spikes in the converter prototype; namely, $I_{\rm cir}$, I_{A1}, and I_{A2}. As observed, the magnitude of the high-frequency spikes in I_{A1} and I_{A2} is high enough that it may well impede the proper operation of the converter. A dedicated effort is hence required to minimize the EPC of the interphase inductors in order to limit this current, for which the inductor physical structure should be taken into consideration. For instance, nonbifilar winding should be preferred over bifilar windings since the latter result in higher EPC. Similarly, single layer windings, not tightly wound, should be preferred in order to reduce the EPC. Alternatively, the use of an additional series-connected interphase inductor may be sought, implementing it with a magnetic core and winding structure featuring superior high-frequency characteristics. Fig. 9(b) shows for comparison purposes the measured current when an 18 μH interphase inductor is added in series using a Ferroxcube TX36/23/10-3C90 magnetic core. This additional interphase inductor was constructed with nonbifilar, single layer windings, which ensured that a high impedance could be attained at and beyond the switching frequency of the converter. As a result, the high-frequency spikes in $I_{\rm cir}$, I_{A1}, and I_{A2} were effectively mitigated in this prototype as the corresponding waveforms depict.

The EPC of the interphase inductor also induces additional switching losses on MOSFET devices. Specifically, as one phase leg is switching, the EPC will be either charged or discharged through the MOSFET channel during turn-ON transients. The energy loss will equal the energy stored in the EPC, which can be calculated in the case of the interleaved Vienna-type rectifier as follows:

$$P_{\rm EPC} = 3 \times 2 \times f_{\rm sw} \times \left[\frac{1}{2} C_{\rm EPC} \left(\frac{V_o}{2}\right)^2\right] \tag{3}$$

where $P_{\rm EPC}$ is the EPC-dependent power loss in all three phases, $f_{\rm sw}$ is the switching frequency of a single channel, $C_{\rm EPC}$ the equivalent capacitance, and V_o is the output voltage. This loss component is quite small and accordingly not considered in the loss prediction of the design procedure mentioned below. In effect, this loss is estimated to account for 340 mW in the experimental prototype in question.

IV. Converter Design Procedure, Loss Estimation, and Converter Implementation

To achieve an optimum efficiency while meeting power quality and power density constraints, an efficiency-oriented design procedure was developed in this paper for the interleaved Vienna-type rectifier in question. Its specifications are three-phase 230 V ac, 360–800 Hz line frequency, 650 V dc output, and 3 kW output power. The details of this procedure are presented hereinafter.

A. Converter Design

The efficiency-oriented design procedure developed for a dual-channel interleaved Vienna-type rectifier is described in the flow chart diagram in Fig. 10.

This procedure starts with the specifications and standards to be met by the converter. The specific power quality requirements used for current harmonics are detailed in Table I. This should be ensured over the whole input frequency range (360–800 Hz), e.g., with 800 Hz input frequency, the current harmonic limits should be met up to 32 kHz (40 × 800 Hz). Additionally, an input current THD lower than 10% is required. The second step in the process developed is to select the proper modulation scheme of the converter, which will be discussed in depth in Section IV-B.

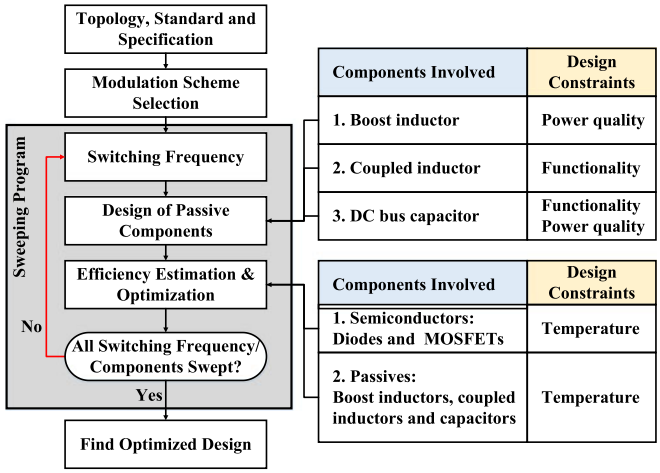


Fig. 10. Efficiency-oriented design procedure for a dual-channel interleaved Vienna-type rectifier.

TABLE I
CURRENT HARMONIC LIMITS

Harmonic Order	Limits
Odd Non-Triplen Harmonics ($h = 5, 7, \ldots, 37$)	$I_h = 0.3\, I_1/h$
Odd Triplen Harmonics ($h = 3, 9, 15, 21, \ldots, 39$)	$I_h = 0.15\, I_1/h$
Even Harmonics 2 and 4	$I_h = 0.01\, I_1/h$
Even Harmonics > 4 ($h = 6, 8, 10, \ldots, 40$)	$I_h = 0.0025\, I_1/h$

To find the optimum design point for the converter, a numerical iterative process was developed in what is referred to as the "sweeping program" in the diagram shown in Fig. 10. This loop starts with the switching frequency selection, after which all passive components in the converter, including the input boost inductor, interphase inductors, and the dc bus capacitors, are designed. The sizing of these components is primarily constrained by the power quality standards and thermally by their estimated power loss. Si and silicon SiC devices are then considered in the efficiency estimation and optimization step, seeking the best performer among the candidates considered based on a preliminary datasheet selection. A full list of component candidates is provided in Section IV-D. Specifically, at each switching frequency point, the conduction and switching losses from all combinations of semiconductor device candidates are calculated (the loss model used is discussed in Section IV-C). The design that achieves the lowest total loss is accordingly chosen for the optimized design point for this specific switching frequency. Continuing with the iteration process, the relationship among total power loss, design of passive components, and switching frequency is finally attained. From the resultant set of alternative design options, the optimized converter design with the lowest power loss—and highest efficiency, which meets the power quality and power density constraints, is finally selected. It should be mentioned that there was no EMI specification in the case under consideration, hence EMI filters were considered to be out of the scope of this work and are not included in the design procedure of the converter. A detailed description of each of these steps and analytical models involved are presented below.

B. PWM Scheme Selection

All modulation schemes applicable to Vienna-type rectifiers can be used in the interleaved system because interleaved subconverters generate their outputs independently. In order to achieve high efficiency, nonetheless, discontinuous PWM (DPWM), which clamps one phase in every switching period, is preferable in this case. Reference [23] has proposed and compared two DPWM schemes for Vienna-type rectifiers; one of these schemes, whose vector selection is depicted in Fig. 19 in Appendix B, is adopted in this paper. This PWM scheme not only avoids switching the phase leg with the highest current magnitude, but also avoids switching the phase leg going through zero crossing thus avoiding commutation failures. A comparison between DPWM and other modulation schemes, such as sinusoidal PWM and space vector modulation for two-level converter, was documented in [21]. Reference [21] claimed that DPWM not only reduces switching loss but also input current THD for two-channel interleaved Vienna-type rectifiers.

Furthermore, since according to (2) the interphase inductance must be large enough to limit the circulating current throughout the entire line cycle, the use of this DPWM scheme brings yet another benefit. Specifically, when a pair of phase legs is clamped to one of the dc bus terminals, no effective voltage difference exists between them, and hence no volt-seconds are applied across the interphase inductors. As a result, no circulating current can be generated during this time. This can be clearly observed in Figs. 5 and 9, where the circulating current is zero during the clamping period. The interphase inductance is accordingly not determined by the converter operation when the input current is close to zero, reducing in this way the inductance requirements in accordance to (2).

C. Loss Estimation

The losses in the converter result mainly from its power semiconductor devices and inductors. Accordingly, the conduction and switching losses of semiconductor devices, as well as the magnetic core and winding losses of inductors have been carefully modeled in this work. Specifically, the conduction loss of a MOSFET is function of its drain–source resistance during the on-stage (R_{dson}), and the rms current flowing through its channel. The rms current through each device can be accurately calculated using closed-form expressions or obtained numerically from simulations. This can be ensured by adopting the right measures to attain an even current distribution between interleaved phase legs, and by effectively limiting, if not canceling, the circulating current between them. The MOSFET conduction loss $P_{\mathrm{MOS,con}}$ is given by

$$P_{\mathrm{MOS,con}} = {I_{\mathrm{MOS,rms}}}^2 R_{\mathrm{dson}} \tag{4}$$

where $I_{\mathrm{MOS,rms}}$ is the rms value of the current flowing through the device, which is obtained through simulation in this paper. Furthermore, since R_{dson} is temperature dependent, several iterations are needed to estimate the MOSFET junction temperature

and the corresponding on-state resistance. The diode conduction loss $P_{\mathrm{Diode,con}}$ on the other hand is a function of its conduction characteristics and the current flowing through it. It is expressed as

$$P_{\mathrm{Diode,con}} = I_{\mathrm{Diode,Ave}} V_{\mathrm{FD}} + {I_{\mathrm{Diode,rms}}}^2 R_{\mathrm{Diode}} \tag{5}$$

where $I_{\mathrm{Diode,Ave}}$ is the average value of current flowing through it, V_{FD} is its forward voltage drop, $I_{\mathrm{Diode,rms}}$ is the rms value of the current, and R_{Diode} is the equivalent series resistance, which is usually found be curve fitting. It should be noted that both V_{FD} and R_{Diode} are function of the junction temperature as well.

Similarly, the winding conduction losses of the boost and interphase inductors can be calculated using current information obtained from simulation. The winding conduction loss $P_{\mathrm{WD,con}}$ can be calculated as

$$P_{\mathrm{WD,con}} = {I_{\mathrm{WD,rms}}}^2 R_{\mathrm{WD}} \tag{6}$$

where $I_{\mathrm{WD,rms}}$ is the rms value of the current flowing through the boost or interphase inductor and R_{WD} is its dc winding resistance. In (6), skin and proximity effect losses are assumed to be negligible with the use of Litz wire and carefully wound windings. As discussed in [24], bundle-level skin and proximity effect are controlled by Litz wire. Strand-level skin effect is controlled by using strands that are smaller than the skin depth in the frequency range of interest. Strand-level proximity effect is on the other hand determined by the magnetic field in the inductor. In a typical gapped-core (E-cores were used), the magnetic field concentrates around the core gaps [25]. Accordingly, in this work all windings were kept away from the gap in order to minimize the strand-level proximity effect, which was neglected in the calculations. For interphase inductors, thanks to their bifilar structure, the magnetic field that penetrates the winding is largely reduced, which also allowed the strand-level proximity effect to be neglected.

The core loss of the boost inductors was calculated based on the volt-second information obtained from simulation and existing analytical models. Reference [26] showed that in ac applications the core loss from the fundamental and switching frequency components could be calculated separately. For fundamental frequency components, since the excitation on the inductor is sinusoidal, core loss could be calculated using Steimetz equation as

$$P_{\mathrm{core},f} = V_e k {f_{\mathrm{in}}}^{\alpha} {B_{f,\mathrm{peak}}}^{\beta} \tag{7}$$

where $P_{\mathrm{core},f}$ is the time-averaged fundamental frequency component related core loss, V_e is the effective volume of the magnetic core, f_{in} is the fundamental frequency, $B_{f,\mathrm{peak}}$ is the peak value of fundamental frequency flux density, and α, β, and k are the Steimetz parameters.

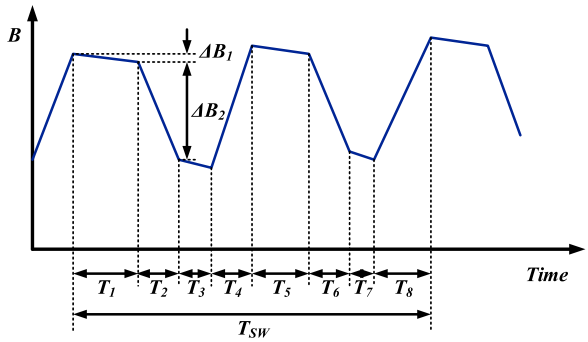


Fig. 11. Example of boost inductor flux density change in one switching cycle. Eight segments are observed in one switching cycle from the interleaved Vienna rectifier with DPWM.

For the switching-frequency related loss, the improved generalized Steinmetz equation proposed in [27] can be used:

$$\begin{aligned} P_{\mathrm{core,sw}} &= V_e f_{\mathrm{in}} \sum_{i=1}^{N} \left(\int_0^{T_i} k_i \left| \frac{dB}{dt} \right|^{\alpha} {\Delta B_i}^{\beta-\alpha} dt \right) \\ &= V_e f_{\mathrm{in}} \sum_{i=1}^{N} \left(k_i \left| \frac{\Delta B_i}{T_i} \right|^{\alpha} {\Delta B_i}^{\beta-\alpha} \right) \end{aligned} \tag{8}$$

where $P_{\mathrm{core,sw}}$ is the switching frequency loss component, k_{i} is defined as follows:

$$k_i = \frac{k}{(2\pi)^{\alpha-1} \int_0^{2\pi} |\cos\theta|^{\alpha} 2^{\beta-\alpha} d\theta}. \tag{9}$$

V_e, f_{in}, α, and β are the same parameters defined in (7), N is the total number of flux segments in one fundamental cycle, and it is equal to $8 f_{\mathrm{sw}}/f_{\mathrm{in}}$, and where ΔB_i and T_i are the flux density change and the duration of the ith segment. The segmentation of (8) is necessary given that in a three-phase converter the magnetic flux in line inductors changes multiple times in one switching cycle. An example is shown in Fig. 11 illustrating how in the Vienna-type rectifier the flux changes eight times per cycle. Accordingly, (8) was used to calculate the core-loss of the interphase inductors, where there is no dc or low-frequency bias in magnetic flux thanks to the symmetry of their volt-second product (see Fig. 8). Boost inductors on the other hand feature a negligible loss due to the interleaving action and PWM scheme used. Equation (8) was used in this case for simplicity without taking into consideration the change in the dc bias point. This was deemed reasonable given the very low loss in these inductors, which is verified by both predicted and measured losses in Section V. In addition, the loss of magnetics components represents a small fraction of the total converter loss, reducing the relative impact that this simplification could have when predicting the conversion efficiency. This will be illustrated in Fig. 15.

Loss in output capacitors P_{Co} is calculated as

$$P_{\mathrm{Co}} = {I_{\mathrm{Co,rms}}}^2 R_{\mathrm{Co,ESR}} \tag{10}$$

where $I_{\mathrm{Co,rms}}$ is the rms value of the current flowing through the output capacitors and $R_{\mathrm{Co,ESR}}$ is the equivalent series resistor of the output capacitors.

The switching loss modeling and estimation of power MOSFETs is a harder task given the nonlinear nature of their commutation process. Accordingly, the most accurate way to calculate the switching loss of a MOSFET is by measuring them in a double-pulse test experimental set up. If, however, many alternative devices are under consideration, as in the case under consideration, this approach is too time consuming and not desirable. The use of an analytical loss estimation method is more suitable for this work, as it can provide a fast and accurate loss estimation based solely on the information provided in datasheets. The caveat is to ensure that the model employed is of sufficient fidelity for the design task.

Several analytical models have been developed in the past years to predict the switching loss of power MOSFETs. One of the most accurate models so far analyzing the switching behavior of this device in great detail is derived in [28]. It takes into consideration the nonlinear capacitances of the MOSFET as well as the parasitic inductance of the device package and circuit layout. The price paid for this detailed model was however a fairly intricate set of equations and solutions that rendered the model hard to implement and adopt. A piecewise linear model predicting MOSFET switching loss based on gate charge was proposed in [29] and [30]. Though easy to use, the description of loss generated by diode capacitive charging and MOSFET turn-OFF procedure is incomplete. To circumvent the above-mentioned shortcoming, this paper has developed a set of equations to predict the switching loss of this device based on the piecewise linear model proposed in [29]. Both turn-ON and turn-OFF times are determined in this model using the gate charge of the MOSFET, as opposed to its capacitances, which eliminates the need to deal with the nonlinear voltage dependence of the latter. The parasitic inductance of the package, namely the common-source inductance, as well as the loss caused by charging the diode junction capacitance during turn-ON, is taken into consideration. The complete model as well as the equations derived to calculate losses is described in detail in Appendix C.

D. Semiconductor Devices Selection

The selection of semiconductors is critical in order to achieve a high power conversion efficiency given that they determine both the conduction and switching losses in the converter. For diodes, 1.2 kV SiC Schottky diodes (candidates included: CREE C4D10120A, C4D15120A, and C4D20120A) were selected in order to eliminate the reverse recovery loss in the commutation process. It is worth noting that diodes not only generate conduction loss but also produce switching loss due to charging of the junction capacitance. Diodes with larger current capability have higher junction capacitance that produces more switching loss. To achieve maximum efficiency, SiC diodes should be carefully selected considering their influence on both conduction loss and switching loss.

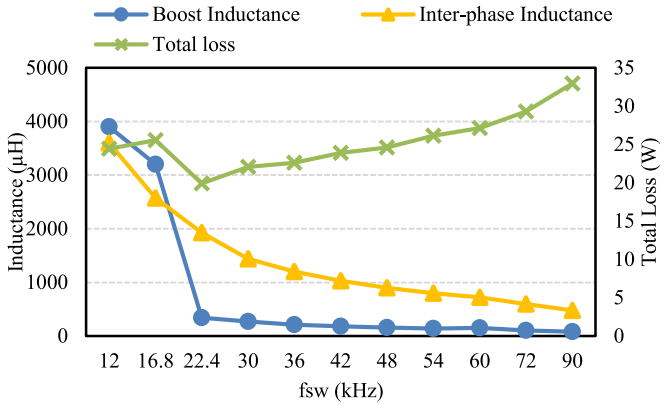


Fig. 12. Relationship among switching frequency and boost inductance, interphase inductance, and minimized loss.

Regarding active semiconductors, Vienna-type rectifiers require four-quadrant switches to block voltage and conduct current in both directions. Two MOSFETs are used and connected in a common-source configuration to attain this functionality, in which case they can be driven by the same circuit and a single isolated power supply. Several 600 V (or 650 V) Si MOSFETs (Infineon IPP60R199CP, IPW65R110CFD, IPW60R045CP) and 1.2 kV SiC MOSFETs (CREE C2M0160120D, C2M0080120D) were examined in the optimization process.

E. Converter Loss Estimation

Continuing with the design procedure, Fig. 12 shows the resultant relationship found between the boost and interphase inductance values, and the total loss of the converter as a function of the switching frequency of each subconverter. It should be noticed that the first group of switching harmonics is located at twice the switching frequency as a result of PWM interleaving. The boost inductance required below 22.4 kHz switching frequency is determined by the current harmonic limits (detailed in Table I); hence the jump observed for lower switching frequency values. Beyond 22.4 kHz switching frequency, boost inductance is designed to ensure THD to be below 10% at nominal load. The final design point chosen for switching frequency to ensure minimum loss, while avoiding a large inductor size, was accordingly 22.4 kHz. In this case the estimated loss was 19.9 W, which translated to an efficiency of 99.32%.

F. Converter Implementation

To achieve the optimized design, boost inductors were built using E55/28/21-3C90 cores with 40 turns, achieving the required 360 μH inductance value. The interphase inductor was implemented using TX51/32/19-3C90 cores with 42 turns, while the additional high-frequency interphase inductor was implemented using a 3-turn TX36/23/10-3C90 core. The windings of both types of inductors were implemented using 120/36 Litz wire. Based on the loss model presented previously, at a switching frequency of 22.4 kHz, CREE C4D15120A SiC Schottky

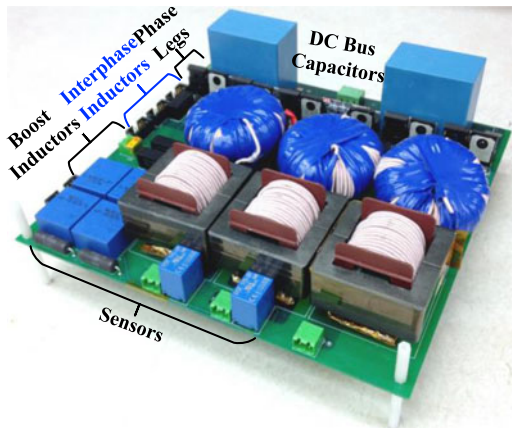


Fig. 13. Converter prototype of a dual-channel interleaved Vienna-type rectifier.

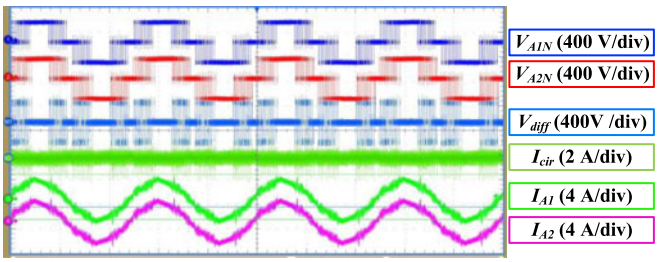


Fig. 14. Experimental waveforms of converter prototype under nominal load.

diodes and CREE C2M0080120D SiC MOSFETs attained the lowest semiconductor loss, and were, therefore, selected.

V. Experimental Results and Performance Evaluation

This section presents the results of the experimental evaluation conducted with the converter prototype constructed, including efficiency, THD, and thermal behavior. The converter prototype is shown in Fig. 13. The dimensions of the prototype are $8.7'' \times 8.8'' \times 2''$. Experimental waveforms obtained at nominal output power are shown in Fig. 14, where V_{A1n} and V_{A2n} correspond to the voltages of phases A_1 and A_2 with respect to the dc bus midpoint, V_{diff} to the voltage difference between these voltages, I_{A1} and I_{A2} to the input currents of phase A_1 and phase A_2, and I_{cir} to the circulating current. As observed, the latter was effectively attenuated by the interphase inductor arrangements, while the converter phase currents are perfectly sinusoidal and the converter phase voltages are shown to effectively clamp their operation to the positive and negative dc bus rails during the times when the respective phase currents are close to zero or at their maximum value.

The efficiency of the converter at its nominal output power condition was measured with a Yokogawa PZ4000 power analyzer, which indicated a 99.26% efficiency. The accuracy of this instrument is $\pm 0.2\%$ for dc power measurement and $\pm 0.125\%$ for ac power measurement, which corresponds to a $\pm 0.33\%$ accuracy in said measurement. To verify the efficiency measurement, an offline temperature characterization was done, where a controlled dc current was injected into each device under test producing the same temperature rise as in their normal operation. This dc condition renders the consumed power measurable by using higher precision dc voltage and current meters. In these measurements, it was assumed that the temperature of the interphase and boost inductors is not dependent on neighboring components. Diodes and MOSFETs on the other hand do have mutual heat transfer due to the short distance between them, and thus two current sources were used simultaneously in the test. The estimated total loss from offline thermal characterization was 21.4 W, which is in close agreement with the 19.9 W total loss predicted by the optimized design procedure.

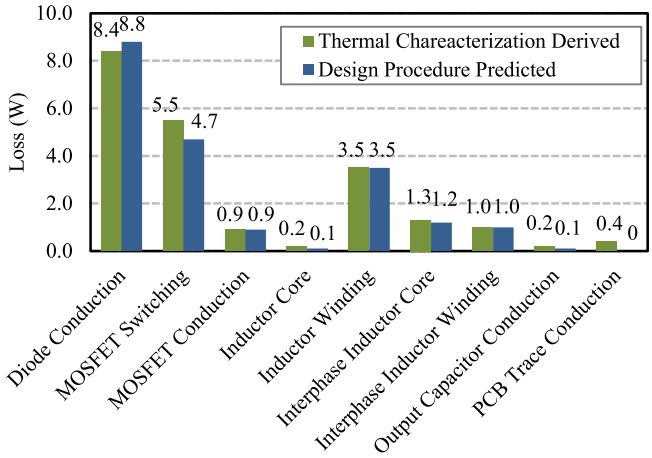


Fig. 15. Loss distribution of an interleaved Vienna-type rectifier at nominal load.

The predicted and thermal-characterization-derived loss breakdown at nominal load is shown in Fig. 15, where a good match is observed between them. For data derived from thermal characterization, the loss distribution of each device (e.g., MOSFET) is estimated based on device characteristics (e.g., conduction loss of MOSFET could be calculated and the rest is switching loss). The predicted and thermal-characterization efficiency measurement as well as the efficiency measured with the power analyzer are shown for different load values in Fig. 16. The good match of all three plots, but especially of the two experimental ones, validates this result.

The measured current THD at full load is 9.5% (full frequency range). The measured low-frequency current harmonics and harmonic standard limits are depicted in Fig. 17, where the compliance of the latter is shown.

The temperatures of the semiconductor devices were measured during nominal operating conditions with both thermocouples and a thermal camera. Under 25°C ambient conditions, and without any active cooling, the thermal image of the converter prototype is shown in Fig. 18. In this figure spot 1 and spot 2 correspond to the MOSFET and diode in one of the converter phase legs, indicating 61°C and 73°C in steady state after 30 min of operation. The measurements obtained with the thermocouple on the other hand indicated respective temperatures

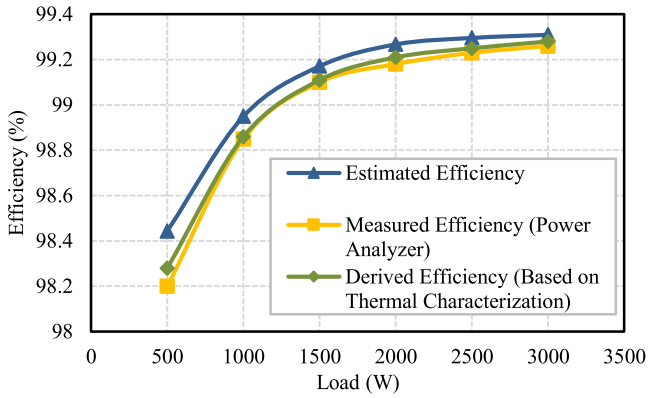


Fig. 16. Estimated and measured converter efficiency under different loads.

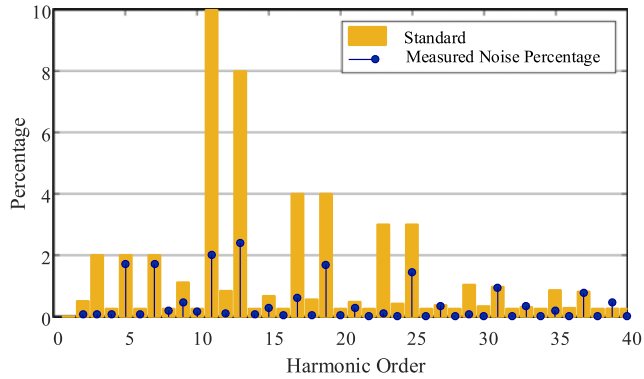


Fig. 17. Measured low-frequency harmonics and harmonic standard.

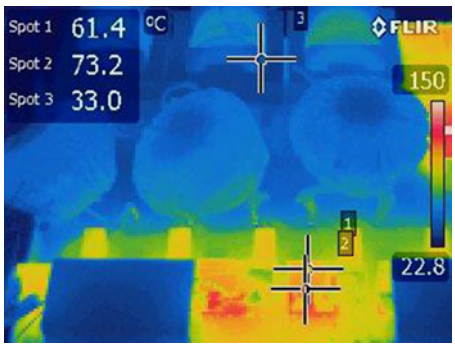


Fig. 18. Temperature distribution of the converter prototype.

of 53°C and 74°C, also after 30 min of operation. This slight discrepancy is attributed to the fact that the converter prototype was not coated in black prior to conduct the imaging process; hence, the dual measurement conducted. These results also verified the design conducted that pursued an operation without active cooling for the converter prototype.

Comparing to the single-channel Vienna-type rectifier with phase-leg implementation (d) (shown in Fig. 1), a 27% loss reduction is achieved by the interleaved prototype. The loss reduction is attributed to the following aspects:

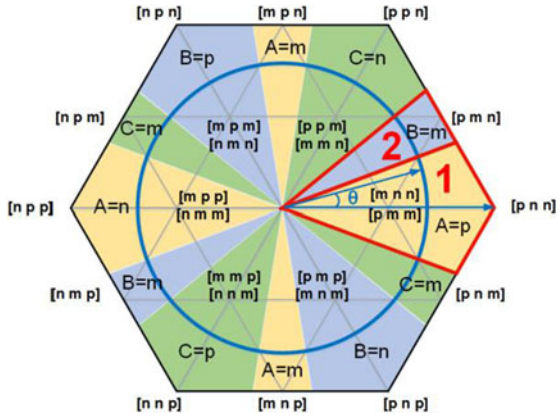


Fig. 19. Space vectors of DPWM and clamping options.

1) the switching loss of MOSFETs is reduced from 10.4 to 5.5 W, though the equivalent switching frequency is the same;
2) the conduction loss of both MOSFET and diode devices is reduced, from 2.3 to 0.9 W and from 10.6 to 8.4 W in the MOSFET and diode cases, respectively; and
3) the conduction losses of the boost inductor are reduced from 5.8 to 3.5 W.

The latter point is illustrated in Figs. 5 and 14 that show how the current ripple is nearly zero at the peak and trough of the phase currents thanks to the use of interleaving and DPWM. Accordingly, these inductors can be implemented with fewer turns for the same peak-flux density and inductance, if the same magnetic core is used. Interphase inductors, however, are required when using interleaving, whose 2.3 W loss was small enough in this case to not affect the overall loss reduction attained by the method.

The above-mentioned loss reduction translates into an improved thermal design for the interleaved converter, which in this case eliminated the need for active cooling. In effect, it is estimated that a case temperature of 138°C and 152 °C would be the operating condition of the MOSFET and diodes of a single-channel Vienna-type rectifier built to the same set of specifications assuming an ambient temperature of 25°C. The interleaved Vienna-type rectifier on the other hand featured temperatures of 53°C and 74°C for its MOSFET and diode devices for the same conditions, making possible the operation without active cooling up to 60°C ambient conditions.

VI. Conclusion

This paper presented the design and hardware implementation of a three-phase interleaved Vienna-type rectifier with 99.28% nominal load efficiency operating without active cooling. The operating principle of the interleaved Vienna-type rectifier was presented in detail, analyzing in depth the generation of the switching-frequency circulating current as well as effective methods for its attenuation. A design and optimization procedure to attain maximum efficiency was then proposed, based on detailed loss models developed for the power converter semiconductors and its boost and interphase inductors. From

these, hardware design guidelines were presented to ensure the correct operation and functionality of the converter, while demonstrating the feasibility of the efficiency-optimized design procedure. Finally, experimental results obtained with a 3 kW experimental prototype were presented to validate the design procedure and converter operation.

APPENDIX A

TABLE II
KEY FEATURES OF TWO-LEVEL BOOST RECTIFIER, THREE-LEVEL NPC BOOST RECTIFIER, T-TYPE BOOST RECTIFIER, AND DIFFERENT PHASE-LEG IMPLEMENTATIONS OF THE VIENNA-TYPE RECTIFIER

Topology	Device blocking voltage	Pos. /Neg. clamping path	Middle point clamping path	Devices in commutation
Two-level	Whole dc bus	MOSFET	N/A	MOSFET⇔MOSFET Body Diode
Three-level NPC	Half-dc bus	MOSFET ∗ 2	MOSFET+Diode	MOSFET⇔MOSFET Body Diode
T-type	Hybrid:two blocks whole dc bus, two blocks half-dc bus	MOSFET	MOSFET ∗ 2	MOSFET⇔MOSFET Body Diode
Vienna-type (a)	Half-dc bus	Diode ∗ 2	Diode+MOSFET	External Diode⇔MOSFET
Vienna-type (b)	Half-dc bus	Diode+MOSFET	Diode+MOSFET	MOSFET⇔MOSFET body Diode
Vienna-type (c)	Half-dc bus	Diode ∗ 2	Diode ∗ 2+MOSFET	External Diode⇔MOSFET
Vienna-type (d)	Diodes:half dc busMOSFETs:whole dc bus	Diode	MOSFET ∗ 2	External Diode⇔MOSFET

Additionally, the isolated gate drivers per phase leg in each topology are 2, 4, 3, 2, 2, 1, and 1.

APPENDIX B

Under this DPWM scheme, to achieve phase clamping in sector 1, vectors [p n n], [p n m], and [p m m] would be selected in the lower half of the region, and vectors [p n m], [p m n], and [p m m] in the upper half, where the vector elements "p," "m," and "n" refer, respectively, to the positive, midpoint, and negative dc bus terminals. This choice of vectors ensures that phase A remains connected to the positive dc bus rail when the desired output voltage vector lies in sector 1, effectively clamping phase A during this period of time. Conversely, in sector 2, vectors [p m m], [p m n], and [m m n] are selected to ensure that phase B is clamped to the dc bus mid-point instead, corresponding to the instant of time when the current in phase B crosses zero.

APPENDIX C

The voltage and current transitions during commutation are assumed to be linear as illustrated in Figs. 21 and 22. These figures also show the four time intervals that take place during the turn-ON and turn-OFF process. The duration of these intervals is determined by the driving circuit, the parasitic inductance and, most importantly, the gate charge. In this part, Fig. 20 depicts the circuit for MOSFET switching loss prediction with all considered parasitics. Figs. 21 and 22 depict the voltage and current waveforms during the turn-ON and turn-OFF commutation process, respectively.

For turn-ON loss prediction, four different intervals are described and modeled separately.

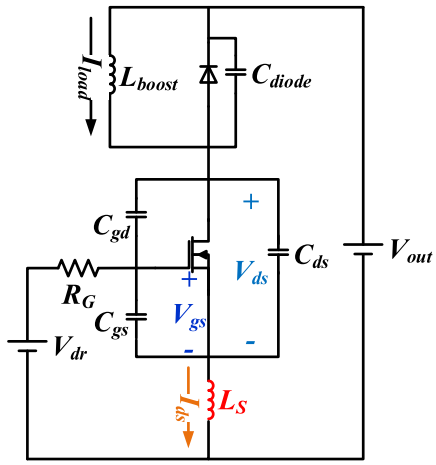


Fig. 20. Circuit for MOSFET switching loss prediction.

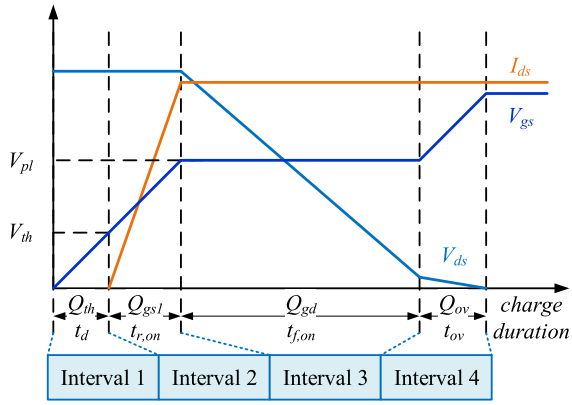


Fig. 21. Waveforms during the turn-ON procedure.

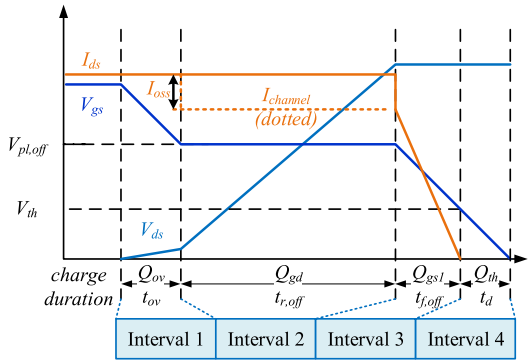


Fig. 22. Waveforms during the turn-OFF procedure.

Interval 1: The gate-to-source voltage $V_{\rm gs}$ increases from zero to the threshold voltage level $V_{\rm th}$. The gate charge provided by the driver during this time is $Q_{\rm th}$. There is no switching loss resulting from this interval.

Interval 2: $V_{\rm gs}$ increases from $V_{\rm th}$ to the plateau voltage level the MOSFET, $V_{\rm pl}$. In [30], it was assumed that $V_{\rm pl}$ was constant under different load current value $I_{\rm load}$, so that $V_{\rm gs}$ remained at $V_{\rm pl}$ during this interval, while in this revised model, $V_{\rm pl}$ changes as $I_{\rm ds}$ changes and $V_{\rm gs}$ increases linearly to $V_{\rm pl}$, making it more accurate. Since the MOSFET works in saturation regime

during this interval, the relationship between $V_{\rm pl}$ and $I_{\rm load}$ can be expressed as

$$I_{\rm load} = k(V_{\rm pl} - V_{\rm th})^2 \tag{11}$$

where k is a constant and is determined by the device intrinsic parameters (gate oxide capacitance, channel dimensions, and carrier mobility). Based on (11), $V_{\rm pl}$ can be found using

$$V_{\rm pl} = \sqrt{\frac{I_{\rm load}}{k}} + V_{\rm th}. \tag{12}$$

In this interval, as $V_{\rm gs}$ increases, the drain-to-source current $I_{\rm ds}$ rises to $I_{\rm load}$. The gate charge provided by the gate driver during this interval is $Q_{\rm gs1}$, from where the following set of equations can be derived

$$\begin{cases} V_{\rm gs}(t) = \dfrac{V_{\rm pl} - V_{\rm th}}{t_{r,\rm on}} t + V_{\rm th} \\ V_{\rm Ls} = L_s \dfrac{dI_{\rm ds}}{dt} = L_s \dfrac{I_{\rm load}}{t_{r,\rm on}} \\ I_{{\rm gate},P2}(t) = \dfrac{V_{\rm dr} - V_g(t) - V_{\rm Ls}}{R_g} \\ Q_{\rm gs1} = \int_0^{t_{r,\rm on}} I_{{\rm gate},P2}(t)dt \end{cases} \tag{13}$$

where $V_{\rm Ls}$ is the voltage across the common-source inductance L_s, $t_{r,\rm on}$ is the duration of the interval, R_g is the gate resistor, $I_{{\rm gate},P2}$ is the output current of the gate driver, and $V_{\rm dr}$ is the gate-driver output voltage.

Solving these equations yields $t_{r,\rm on}$, which is given by

$$t_{r.\rm on} = \frac{2R_g\left(Q_{\rm gs1} + \frac{L_s I_{\rm load}}{R_g}\right)}{2V_{\rm dr} - V_{\rm th} - V_{\rm pl}}. \tag{14}$$

Interval 3: $V_{\rm gs}$ stays at $V_{\rm pl}$ due to the Miller effect, and the drain-to-source voltage $V_{\rm ds}$ begins to fall. The total charge required by the Miller capacitor is $Q_{\rm gd}$, which can be found in the datasheet. Based on this analysis, the output current of the gate-driver during this interval $I_{{\rm gate},P3}$ is given by

$$I_{{\rm gate},P3} = \frac{V_{\rm dr} - V_{\rm pl}}{R_g}. \tag{15}$$

The duration of this interval $t_{f,\rm on}$ is given by

$$t_{f,\rm on} = \frac{Q_{\rm gd} R_g}{V_{\rm dr} - V_{\rm pl}}. \tag{16}$$

The junction capacitor of the freewheeling diode is also charged during this interval, where the charging current also flows through the MOSFET channel causing additional loss. The total energy $E_{\rm diode,total}$ provided by the dc voltage source to charge this junction is given by

$$E_{\rm diode,total} = V_{\rm out} \int_0^{V_{\rm out}} C_{\rm diode}(V)dV \tag{17}$$

where $V_{\rm out}$ is the dc bus voltage and $C_{\rm diode}$ is the (nonlinear) diode junction capacitance. In this process, part of the energy stored in the capacitor is returned to the source during the diode turn-ON transient (MOSFET turn-OFF); thus the total energy dissipated $E_{\rm diode}$ can be calculated as follows:

$$\begin{aligned} E_{\rm diode} &= E_{\rm diode,total} - E_{c,\rm diode} \\ &= V_{\rm out} \int_0^{V_{\rm out}} C_{\rm diode}(V)dV - \int_0^{V_{\rm out}} C_{\rm diode}(V)VdV \end{aligned} \tag{18}$$

where $E_{c,\rm diode}$ is the total energy stored in the diode junction capacitor. Given the nonlinear nature of this relationship, it is highly recommended that this expression be used—together with the *C–V* datasheet curves—to estimate the capacitive charging loss, as opposed to a simplified one, for the sake of the estimation accuracy.

Additionally, the diode reverse recovery may take place during this interval during the turn-OFF of the diode. This energy loss $E_{\rm RR}$ can be calculated as follows:

$$E_{\rm RR} = Q_{\rm RR} V_{\rm out} \tag{19}$$

where $Q_{\rm RR}$ is the total reverse recovery charge of the diode. If Schottky diodes are used this term is zero.

Finally, the energy stored in the MOSFET output capacitor $E_{\rm oss,MOS}$ will be dissipated in the MOSFET channel during this interval. This energy is expressed as

$$E_{\rm oss,MOS} = \int_0^{V_{\rm out}} C_{\rm oss,MOS}(V)VdV \tag{20}$$

where $C_{\rm oss,MOS}$ is the nonlinear output capacitance of the MOSFET. The relationship between $C_{\rm oss,MOS}$ and the drain-to-source voltage is always provided in datasheets.

Interval 4: $V_{\rm gs}$ continues to rise, resulting in a further reduction of the ON-state resistance of the MOSFET. There is no switching loss in this interval.

Accordingly, the turn-ON loss energy in the total switching period is given by

$$\begin{aligned} E_{\rm on} = \ & \frac{1}{2} V_{\rm out} I_{\rm load}(t_{r,\rm on} + t_{f,\rm on}) + E_{\rm diode} \\ & + E_{\rm oss,MOS} + Q_{\rm rr} V_{\rm out}. \end{aligned} \tag{21}$$

The turn-OFF of the MOSFET follows a similar but inverse process than the turn-ON transient and the corresponding waveforms are illustrated in Fig. 22. Four time intervals are used to describe the turn-OFF procedure.

Interval 1: $V_{\rm gs}$ falls to the turn-OFF plateau voltage $V_{\rm pl,off}$. $I_{\rm ds}$ and $V_{\rm ds}$ stay at $I_{\rm load}$ and zero, respectively. No switching loss is associated with this interval.

Interval 2: $V_{\rm gs}$ stays at $V_{\rm pl,off}$ while $V_{\rm ds}$ rises from zero to the blocking voltage. It is worth noting that $V_{\rm pl,off}$ could be different from $V_{\rm pl}$ described previously. $I_{\rm ds}$ stays at the same level during this interval. Part of the drain-to-source current flows through MOSFET channel (depicted as $I_{\rm channel}$ in Fig. 22) while the other part flows through $C_{\rm ds}$ of the MOSFET (evinced as $I_{\rm oss}$ in Fig. 22) to charge the MOSFET output capacitor. The energy provided by $I_{\rm oss}$ is stored in the output capacitor during turn-OFF and is not dissipated until the MOSFET turns ON, which was accounted for in the turn-ON loss calculation. Only the overlap of $I_{\rm channel}$ and $V_{\rm ds}$ yields switching losses during the turn-OFF procedure. It is further assumed that $I_{\rm channel}$ and $I_{\rm oss}$ are constant during this interval. Finally, the Miller charge $Q_{\rm gd}$ is removed by the gate current during the same time interval. Accordingly, the duration

$t_{r,\mathrm{off}}$ should satisfy

$$\begin{cases} t_{r,\mathrm{off}} = \dfrac{Q_{\mathrm{oss}} - Q_{\mathrm{gd}}}{I_{\mathrm{oss}}} \\ t_{r,\mathrm{off}} = \dfrac{Q_{\mathrm{gd}}}{I_{\mathrm{gate,off}}} = \dfrac{Q_{\mathrm{gd}}}{\frac{V_{\mathrm{pl,off}} - V_{\mathrm{dr,off}}}{R_g}} = \dfrac{Q_{\mathrm{gd}}}{\frac{\left(\sqrt{\frac{I_{\mathrm{channel}}}{k}} + V_{\mathrm{th}}\right) - V_{\mathrm{dr,off}}}{R_g}} \\ I_{\mathrm{gate}} + I_{\mathrm{oss}} + I_{\mathrm{channel}} = I_{\mathrm{load}} \end{cases} \tag{22}$$

where Q_{oss} is the MOSFET output charge and $V_{\mathrm{dr,off}}$ is the turn-OFF voltage present at the gate driver. Though an analytical solution exists, it is easier to use numerical methods, e.g., Newton–Raphson, to find the approximate solution for I_{channel}, I_{oss}, and $t_{r,\mathrm{off}}$ in practical implementations.-

Interval 3: V_{gs} falls to the threshold voltage V_{th} while I_{channel} falls to zero. This interval follows a similar but inverse process than interval 2 during the turn-ON process. For the sake of brevity, the derivation is omitted here and only the equation for the duration of this interval is provided as

$$t_{f,\mathrm{off}} = \frac{-2R_g\left(Q_{\mathrm{gs1}} + \frac{L_s I_{\mathrm{channel}}}{R_g}\right)}{2V_{\mathrm{dr,off}} - V_{\mathrm{th}} - V_{\mathrm{pl,off}}}. \tag{23}$$

Interval 4: V_{gs} further decreases to zero. No switching loss is generated.

The total turn-OFF loss E_{off} is finally given by

$$E_{\mathrm{off}} = \frac{1}{2}V_{\mathrm{out}}I_{\mathrm{channel}}(t_{r,\mathrm{off}} + t_{r,\mathrm{off}}). \tag{24}$$

REFERENCES

[1] J. Rodriguez, L. Jih-Sheng, and P. F. Zheng, "Multilevel inverters: A survey of topologies, controls, and applications," *IEEE Trans. Ind. Electron.*, vol. 49, no. 4, pp. 724–738, Aug. 2002.

[2] A. Nabae, I. Takahashi, and H. Akagi, "A new neutral-point-clamped PWM inverter," *IEEE Trans. Ind. Appl.*, vol. IA-17, no. 5, pp. 518–523, Sep. 1981.

[3] M. Schweizer and J. W. Kolar, "Design and Implementation of a highly efficient three-level T-type converter for low-voltage applications," *IEEE Trans. Power Electron.*, vol. 28, no. 2, pp. 899–907, Feb. 2013.

[4] J. W. Kolar and F. C. Zach, "A novel three-phase utility interface minimizing line current harmonics of high-power telecommunications rectifier modules," *IEEE Trans. Ind. Electron.*, vol. 44, no. 4, pp. 456–467, Aug. 1997.

[5] Z. Yifan, L. Yue, and T. A. Lipo, "Force commutated three level boost type rectifier," *IEEE Trans. Ind. Appl.*, vol. 31, no. 1, pp. 155–161, Jan./Feb. 1995.

[6] J. W. Kolar and T. Friedli, "The essence of three-phase PFC rectifier systems—Part I," *IEEE Trans. Power Electron.*, vol. 28, no. 1, pp. 176–198, Jan. 2013.

[7] CREE. Inc., CREE C4D20120A silicon carbide Schottky diode datasheet (C ed.), 2016. [Online]. Available: http://www.wolfspeed.com/downloads/dl/file/id/82/product/56/c4d10120a.pdf.

[8] CREE. Inc., CREE C3D10060A silicon carbide Schottky diode datasheet (E ed.), 2005. [Online]. Available: http://www.wolfspeed.com/media/downloads/842/C3D10060A.pdf.

[9] L. Asimmoaei *et al.*, "An interleaved active power filter with reduced size of passive components," in *Proc. 21st Annu. IEEE Appl. Power Electron. Conf. Expo.*, 2006, p. 8.

[10] X. Kun, F. C. Lee, D. Borojevic, Y. Zhihong, and S. Mazumder, "Interleaved PWM with discontinuous space-vector modulation," *IEEE Trans. Power Electron.*, vol. 14, no. 5, pp. 906–917, Sep. 1999.

[11] Z. Di, F. Wang, R. Burgos, L. Rixin, and D. Boroyevich, "Impact of interleaving on ac passive components of paralleled three-phase voltage-source converters," *IEEE Trans. Ind. Appl.*, vol. 46, no. 3, pp. 1042–1054, May/Jun. 2010.

[12] S. K. T. Miller, T. Beechner, and S. Jian, "A comprehensive study of harmonic cancellation effects in interleaved three-phase VSCs," in *Proc. IEEE Power Electron. Spec. Conf.*, 2007, pp. 29–35.

[13] B. Cougo, T. Meynard, and G. Gateau, "Parallel three-phase inverters: Optimal PWM method for flux reduction in intercell transformers," *IEEE Trans. Power Electron.*, vol. 26, no. 8, pp. 2184–2191, Aug. 2011.

[14] F. Ueda, K. Matsui, M. Asao, and K. Tsuboi, "Parallel-connections of pulsewidth modulated inverters using current sharing reactors," *IEEE Trans. Power Electron.*, vol. 10, no. 6, pp. 673–679, Nov. 1995.

[15] I. Barbi and R. Hausmann, "Three-phase multi-level dc-ac converter using three-phase, coupled inductors," in *Proc. Power Electron. Conf.*, 2009, pp. 332–339.

[16] M. S. Ortmann, S. A. Mussa, and M. L. Heldwein, "Three-phase multilevel PFC rectifier based on multistate switching cells," *IEEE Trans. Power Electron.*, vol. 30, no. 4, pp. 1843–1854, Apr. 2015.

[17] X. Zhang, P. Mattavelli, D. Boroyevich, and F. Wang, "Impact of interleaving on EMI noise reduction of paralleled three phase voltage source converters," in *Proc. 29th Annu. IEEE Appl. Power Electron. Conf. Expo.*, 2013, pp. 2487–2492.

[18] M. L. Heldwein and I. Barbi, "Conversores multinìveis unidirecionais do tipo elevador baseados na conexão de múltiplos conversores através de células de comutação de múltiplos estados," *Brazil Patent BRPI0805177*, Nov. 21, 2008.

[19] G. V. Torrico-Bascope, "Method and device of electrical power," *Worldwide Patent WO2011147117*, Jul. 29, 2010.

[20] J. W. Kolar, H. Ertl, and F. C. Zach, "Spacevector-based analytical analysis of the input current distortion of a three-phase discontinuous-mode boost rectifier system," *IEEE Trans. Power Electron.*, vol. 10, no. 6, pp. 733–745, Nov. 1995.

[21] M. S. Ortmann, S. A. Mussa, and M. L. Heldwein, "Evaluation of carrier-based PWM strategies for multi-state switching cells-based multilevel three-phase rectifiers," in *Proc. 9th Brazilian Power Electron. Conf.*, 2011, pp. 903–910.

[22] P. In Gyu and K. Seon Ik, "Modeling and analysis of multi-interphase transformers for connecting power converters in parallel," in *Record 28th Annu. IEEE Power Electron. Spec. Conf. Formerly Power Conditioning Spec. Conf. 1970-71. Power Process. Electron. Spec. Conf.*, vol. 2, 1972, pp. 1164–1170.

[23] L. Dalessandro, S. D. Round, U. Drofenik, and J. W. Kolar, "Discontinuous space-vector modulation for three-level PWM rectifiers," *IEEE Trans. Power Electron.*, vol. 23, no. 2, pp. 530–542, Mar. 2008.

[24] C. R. Sullivan, "Optimal choice for number of strands in a litz-wire transformer winding," *IEEE Trans. Power Electron.*, vol. 14, no. 2, pp. 283–291, Mar. 1999.

[25] M. Mu and F. C. Lee, "Comparison and optimization of high frequency inductors for critical model GaN converter operating at 1MHz," in *Proc. Int. Power Electron. Appl. Conf. Expo.*, 2014, pp. 1363–1368.

[26] T. Shimizu and S. Iyasu, "A practical iron loss calculation for ac filter inductors used in PWM inverters," *IEEE Trans. Ind. Electron.*, vol. 56, no. 7, pp. 2600–2609, Jul. 2009.

[27] K. Venkatachalam, C. R. Sullivan, T. Abdallah, and H. Tacca, "Accurate prediction of ferrite core loss with nonsinusoidal waveforms using only Steinmetz parameters," in *Proc. IEEE Workshop Comput. Power Electron.*, 2002, pp. 36–41.

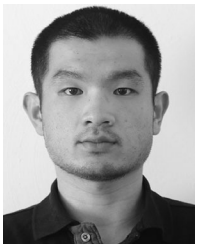
[28] T. Abdallah and H. Tacca, "Accurate prediction of ferrite core loss with nonsinusoidal waveforms using only Steinmetz parameters," in *Proc. IEEE Workshop Comput. Power Electron.*, 2002, pp. 36–41.

[29] R. Yuancheng, X. Ming, J. Zhou, and F. C. Lee, "Analytical loss model of power MOSFET," *IEEE Trans. Power Electron.*, vol. 21, no. 2, pp. 310–319, Mar. 2006.

[30] W. Bo, C. Rengang, and D. Jauregui, "Common source inductance (CSI) of power devices and the impacts on synchronous buck converters," in *Proc. 29th Annu. IEEE Appl. Power Electron. Conf. Expo.*, 2014, pp. 157–162.

[31] D. Jauregui, B. Wang, and R. Chen, "Power loss calculation with common source inductance consideration for synchronous buck converters," Texas Instruments Application Reports, 2011. [Online]. Available: www.ti.com.

[32] *CREE. Inc., CREE C2M0080120D silicon carbide power MOSFET datasheet (C ed.)*, 2015. [Online]. Available: http://www.wolfspeed.com/media/downloads/167/C2M0080120D.pdf.



Qiong Wang (S'13) received the B.S. degree in electrical engineering from Tsinghua University, Beijing, China, in 2012, and the M.S. degree in electrical engineering from the Center for Power Electronics Systems (CPES), Virginia Tech, Blacksburg, VA, USA, in 2015, where he is currently working toward the Ph.D. degree.

His research interests include multiphase multilevel power conversion, high power density, and efficiency power electronics and applications.

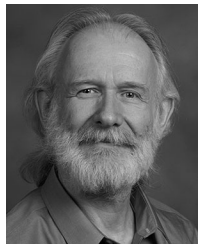
Xuning Zhang received the Bachelor's and Master's degrees in electrical engineering from Tsinghua University, Beijing, China, in 2007 and 2009, respectively, and the Ph.D. degree in electrical engineering from the Center for Power Electronics Systems (CPES), Virginia Tech, Blacksburg, VA, USA, in 2014.

From 2014 to 2016, he joined CPES as a Research Scientist. From 2016, he joined Monolith Semiconductor, Inc., Ithaca, NY, USA, as an Application Engineer. His research interests include high efficiency, high power density converter design, system EMI modeling and filter optimization, interleaving and multilevel converters, GaN-based high-frequency system integration, and passive component design and optimization, SiC device design, and driving optimization.

Rolando Burgos (S'96–M'03) received the B.S. degree in electronics engineering, the Electronics Engineering Professional Degree, and the M.S. and Ph.D. degrees in electrical engineering from the University of Concepción, Concepción, Chile, in 1995, 1997, 1999, and 2002, respectively.

In 2002 he joined, as a Postdoctoral Fellow, the Center for Power Electronics Systems (CPES), Virginia Tech, Blacksburg, VA, becoming a Research Scientist in 2003, and a Research Assistant Professor in 2005. In 2009, he joined ABB Corporate Research in Raleigh, NC, as a Scientist, becoming a Principal Scientist in 2010. In 2010, he was also appointed an Adjunct Associate Professor in the Electrical and Computer Engineering Department, North Carolina State University, working at the Future Renewable Electric Energy Delivery and Management Systems Center. In 2012, he returned to Virginia Tech, where he is currently an Associate Professor in the Bradley Department of Electrical and Computer Engineering and CPES faculty. His research interests include multiphase multilevel power conversion, grid power electronics systems, stability of ac and dc power systems, high power density power electronics, modeling, and control theory and applications.

Dr. Burgos is a member of the IEEE Power Electronics Society where he currently serves as an Associate Editor for the IEEE TRANSACTIONS ON POWER ELECTRONICS, the IEEE POWER ELECTRONICS LETTERS, and the IEEE JOURNAL OF EMERGING AND SELECTED TOPICS IN POWER ELECTRONICS. He is also the Vice-Chair of the Power and Control Core Technologies Committee of the Power Electronics Society. He is a member as well of the IEEE Industry Applications Society, the IEEE Industrial Electronics Society, and the IEEE Power and Energy Society.



Dushan Boroyevich (S'81–M'86–SM'03–F'06) received the Dipl.Ing. degree in electrical engineering from the University of Belgrade, Beograd, Serbia, in 1976, the M.S. degree in electrical engineering from the University of Novi Sad, Novi Sad, Serbia, in 1982, and the Ph.D. degree in electrical engineering from the Virginia Polytechnic Institute and State University (Virginia Tech), Blacksburg, VA, USA, in 1986.

From 1986 to 1990, he was an Assistant Professor and the Director of the Power and Industrial Electronics Research Program in the Institute for Power and Electronic Engineering, University of Novi Sad. He then joined the Bradley Department of Electrical and Computer Engineering, Virginia Tech, as an Associate Professor. He is currently an American Electric Power Professor in the Department and a Co-Director of the Center for Power Electronics Systems. His research interests include multiphase power conversion, electronic power distribution systems, power electronics systems modeling and control, and multidisciplinary design optimization.

Dr. Boroyevich was the President of the IEEE Power Electronics Society for 2011–2012. He received the IEEE William E. Newell Power Electronics Technical Field Award. He is a member of the US National Academy of Engineering.

Adam M. White is a native of Tipton, IA, USA. He received the B.Sc. degree from the Iowa State University, Ames, IA, USA, in 2005, and the M.Sc. degree from the Union Graduate College (now Clarkson University), Schenectady, NY, USA, in 2009, both in electrical engineering.

He is currently a Senior Research Engineer for Kaney Aerospace, Rockford, IL, USA. Previously, he performed power electronics research and development at United Technologies Aerospace Systems, Rockford, IL, and the Knolls Atomic Power Laboratory, Niskayuna, NY. He is a listed inventor on ten US patents. His current research interests include magnetic design, high density power conversion, and design optimization for thermal performance.

Mustansir Kheraluwala received the B.Tech. degree from the Indian Institute of Technology, Kharagpur, India, and the M.S. and Ph.D. degrees from the University of Wisconsin, Madison, WI, USA, in 1984, 1987, and 1991, respectively, all in electrical engineering.

He is currently with the United Technologies Aerospace Systems, Rockford, IL, USA, and is a UTC Fellow in Power Electronics. He has more than 27 years of experience in the field of power electronics having worked across several industries including aerospace, medical, lighting, and transportation. Prior to joining UTC, he was with Siemens-Osram for 7 years, and GE-Global Research Center for 11 years. He holds 28 granted patents, and has authored/co-authored more than 25 technical publications.