Current-Mode Hysteretic Buck Converter With Spur-Free Control for Variable Switching Noise Mitigation

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***Abstract*—This paper proposes a current-mode hysteretic buck converter with a spur-free constant-cycle frequency-hopping controller that fully eliminates spurs from the switching noise spectrum irrespective of variations in the switching frequency and operating conditions. As a result, the need for frequency regulation loops to ensure nonvarying switching frequency (i.e., fixed spurs location) in hysteretic controllers is eliminated. Moreover, compared to frequency regulation loops, the proposed converter offers the advantage of eliminating mixing and interference altogether due to its spur-free operation, and thus, it can be used to power, or to be integrated within noise-sensitive systems while benefiting from the superior dynamic performance of its hysteretic operation. The proposed converter uses dual-sided hysteretic band modulation to eliminate the inductor current imbalance that results from frequency hopping along with the output voltage transients and low-frequency noise floor peaking associated with it. Moreover, a feedforward adaptive hysteretic band controller is proposed to reduce variations in the switching frequency with the input voltage, and an all-digital soft-startup circuit is proposed to control the in-rush current without requiring any off-chip components. The converter is implemented in a 0.35-μm standard CMOS technology and it achieves 92% peak efficiency.**

***Index Terms*—DC–DC power conversion, frequency hopping, hysteretic control, power integrated circuits, spur-free buck converters, switched-mode power supplies, switching noise mitigation.**

I. Introduction

With the growing demand for integrating digital, analog, and radio frequency (RF) subsystems together in a single system-on-chip (SoC), power delivery to these diverse functions within an SoC has become more complex than ever [1]. In fact, power conversion circuits are now required to feature even faster dynamic operation, better power efficiency, smaller footprint, and reduced cost. Although, linear regulators are more likely to achieve smaller footprint and reduced cost, buck converters continue to be preferred due to their much better power efficiency over a wide range of operating conditions [2]. Since the power train and passive components in buck converters are determined mainly by the load demand, the differentiating factor between one design and another lies in the choice of the control topology that meets the demand for faster dynamic operation and reduced cost. Thus, hysteretic control topologies are attractive as they offer superior transient performance with a simple and cost-effective implementation due to their nonlinear, inherently stable nature [3]. Nevertheless, hysteretic controllers have some drawbacks that must be carefully considered, most notably, they are self-oscillating with the switching frequency varying widely with operating conditions [3]. Thus, the tones (i.e., spurs) produced by the converter due to periodic switching will have highly variable locations. Spurs are a serious concern for noise-sensitive loads, such as RF and data converter circuits due to mixing and interference [4]–[6]. Moreover, integrating the converter in SoCs, where the substrate, power/ground rails, and I/O rings are shared with many other circuits, compromises the system performance due to coupling of the spurs from the converter to these circuits. This problem is exacerbated when the location of the spurs is highly variable or cannot be precisely predicted.

Although various flavors of frequency regulation loops were proposed in the literature [7]–[15] and employed in some industrial implementations [16], [17] to mitigate the issue of switching frequency variability in hysteretic controllers, these techniques introduce major design complexity and significant additional power consumption and silicon area. The basic structure of a frequency regulation loop in a hysteretic converter is shown in Fig. 1 [11], where similar to a phase locked loop (PLL), the switching frequency is sensed, then synchronized to a reference clock by adjusting one of the design parameters of the controller (i.e., hysteretic band, bias current, etc.). However, the stability of such loop is nontrivial, and frequency compensation is needed such that its operation does not interfere with the operation of the main power regulation loop [12], [18]. Moreover, although frequency regulation loops may result in nonvarying spurs location, spurious noise is still problematic in systems sensitive to mixing and interference [4]–[6].

This paper proposes incorporating a switching technique within current-mode hysteretic buck converters that fully eliminates the spurious components of the switching noise at all

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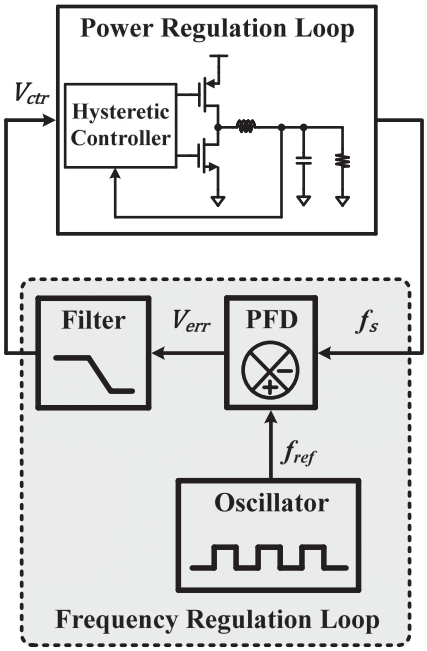


Fig. 1. Block diagram showing a frequency regulation loop used to maintain a constant switching frequency in hysteretic converters. The phase frequency detector (PFD) is used to detect frequency errors and the filter is used to ensure stability.

nodes within the converter, thereby producing spur-free noise spectrum irrespective of the actual switching frequency of the converter or any variability in its operating conditions [19]. As a result, the need for frequency regulation loops for ensuring nonvarying spurious noise is eliminated, and the simple and cost-effective implementation of hysteretic control can be preserved. The digital-friendly realization of the spur-free switching technique constitutes minimal power and footprint overhead, while enabling integrating hysteric buck converters within noise-sensitive systems. Moreover, a feedforward adaptive hysteretic band controller is proposed to reduce variations in the switching frequency, and an all-digital soft-startup circuit is proposed to limit in-rush current with no off-chip components. The paper is organized as follows: Sections II discusses the operation of current-mode hysteretic buck converters; Section III presents spread-spectrum and spur-free switching techniques; Sections IV and V present the system- and circuit-level aspects of the proposed design; while Section VI presents the measurement results. Conclusion is presented in Section VII.

II. Current-Mode Hysteretic Buck Converters

The basic structure of a current-mode hysteretic buck converter is shown in Fig. 2(a), where the low-pass, current sensing RC filter integrates the voltage across the inductor to emulate the inductor current [3]. This method causes less loss and consumes less power than other passive and active current sensing techniques [20]. The feedback signal (V_{fb}) is a triangular voltage waveform that is in phase with the inductor current, and has a dc component equal to the output voltage (V_{out}) with an offset equal to the voltage drop across the parasitic dc resistance (DCR) of the inductor. Although such offset degrades the dc load

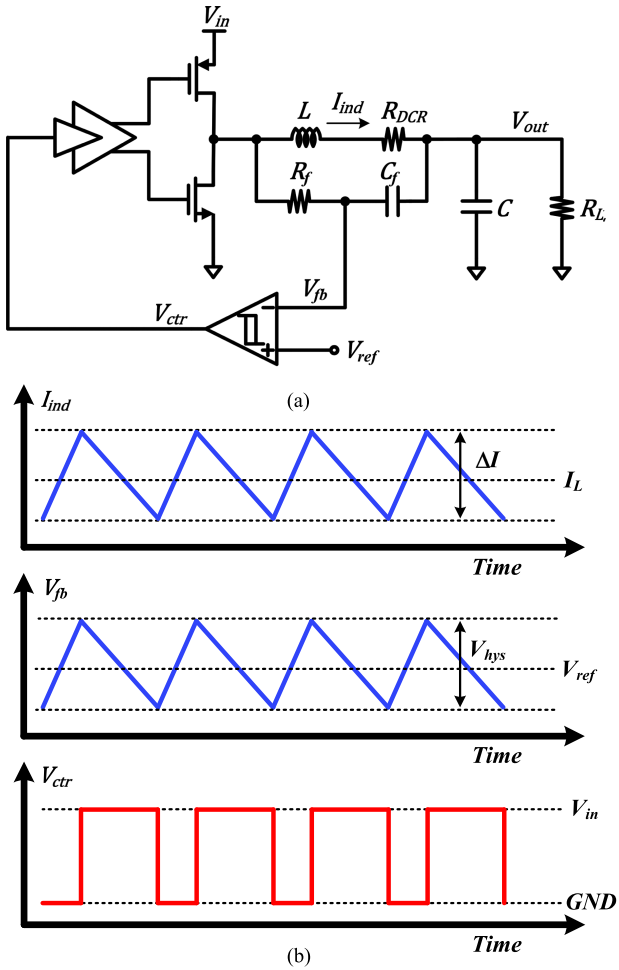


Fig. 2. Current-mode hysteretic buck converter: (a) Block diagram and (b) key waveforms.

regulation of the converter, it can be mitigated by an additional high-gain voltage regulation loop as discussed in later sections. The hysteretic comparator confines the feedback signal within the hysteretic band (V_{hys}) by turning OFF the high-side power switch once the feedback signal exceeds the upper bound of the hysteretic band (V_{hys_H}), and back ON once it drops below the lower bound (V_{hys_L}) as illustrated in Fig. 2(b). Unlike voltage-mode hysteretic topologies, current-mode hysteretic topologies are stable regardless of the estimated series resistance (ESR) of the output capacitor [15]. Therefore, ceramic capacitors with low ESR can be used to achieve small output voltage ripple. Moreover, since the swing of the feedback signal is not coupled to the output voltage ripple, the resolution and speed requirements of the hysteretic comparator can be relaxed.

Since the operation of the hysteretic controller relies on the cycle-to-cycle swing in the feedback signal rather than its average, fast line and load transient response can be achieved. This, however, comes at the expense of a variable switching frequency. In fact, the switching frequency (f_s) of the buck converter in Fig. 2(a) can be expressed as [9]

$$f_s = \frac{D\ (1-D)}{\tau_{RC}\ (V_{hys}/V_{in}) + \tau_D} \tag{1}$$

where D is the duty cycle of the control signal (V_{ctr}), V_{in} is the input voltage, V_{hys} is the comparator's hysteretic band, τ_{RC} is the time constant of the current sensing filter, and τ_D is the total loop delay (i.e., due to the comparator, the gate-drive circuit, and the power switches). Since the input and output voltages typically vary within a specified range, while the loop delay, the filter's time constant, and the comparator's hysteretic band vary with process and temperature, the switching frequency becomes dependent on the operating conditions.

III. Spread-Spectrum and Spur-Free Techniques in Switching Power Converters

Several spread-spectrum schemes have been proposed to reduce or eliminate spurious noise in switching power supplies. Some techniques rely on sigma-delta ($\Sigma\Delta$) modulators to inject random quantization noise in the control loop to reduce spurs, then use noise shaping to push the quantization noise to higher frequencies [21], [22]. However, these techniques result in excessively high random noise floor due to the additional quantization noise [21]. Moreover, they are only suitable for average-based rather than ripple-based controllers such as hysteretic topologies. Other techniques rely on random frequency hopping or stepping between a finite set of frequencies using a constant hopping rate to reduce the magnitude of the spurs without injecting additional random noise [23], [24]. However, in addition to producing new, though smaller, spurs at multiple switching frequencies, these techniques periodically disturb the switching duty cycle and produce additional spurs corresponding to the hopping rate. Thus, incorporating such techniques in hysteretic controllers, where the switching frequencies are operating condition dependent, will lead to varying spurs location unless a frequency regulation loop is used. Other techniques also rely on random frequency hopping, but use a continuum of frequencies within a given range [25]. This is equivalent to hopping between an infinite set of switching frequencies, and thus results in full elimination of spurs. However, such technique requires an analog white noise source and a sample-and-hold network to modulate the switching frequency, which makes it unattractive due to design complexity and high variability with process and temperature.

An alternative technique to achieve spur elimination was recently proposed in [26]–[28] and is referred to as spur-free switching. It relies on random constant cycle frequency hopping (CCFH) to chop the phases of the switching frequencies to produce a spur-free spectrum. The technique has the advantage of requiring only a finite set of switching frequencies (as few as two) to fully eliminate spurs, versus [25] where a continuum of frequencies is necessary. As a result, it can be realized using simple digital implementations as demonstrated in [27] for pulse width modulation (PWM)-controlled converters, and in [28] for pulse frequency modulation (PFM)-controlled converters. Moreover, since the spur-free CCFH switching technique relies only on phase chopping rather than filtering, it produces spur-free spectrum at all nodes within the converter not just the output. To achieve spur-free operation, the switching frequencies used must conform to the following sufficient condition [27]:

$$\frac{f_{s(M)}}{f_{s(i)}} = \left(1 + \frac{m_{(i)}}{n_{(i)}}\right) \neq \text{Integer for } i = 1 \text{ to } (M-1) \quad (2)$$

where M is the number of switching frequencies used, $f_{s(i)}$ is the i^{th} switching frequency, $m_{(i)}$ and $n_{(i)}$ are arbitrary integers selected to ensure that (2) is met for all frequencies.

IV. Proposed Spur-Free Current-Mode Hysteretic Buck Converter

Adopting the spur-free CCFH switching described in the previous section in PWM controllers is straightforward because of the direct control over the switching frequencies [i.e., the condition in (2) can be easily ensured]. However, in a self-oscillating hysteretic controller, incorporating such technique is challenging due to the dependency of the switching frequency on the operating conditions. In this paper, an implementation of a spur-free CCFH hysteretic buck converter is proposed to address these challenges. The remainder of this section will discuss the system-level aspects of the proposed design, while Section V will discuss circuit-level realization.

A. Top-Level Implementation

The top-level block diagram of the proposed current-mode hysteretic buck converter incorporating spur-free CCFH is shown in Fig. 3, where the startup module is used to pass the hysteretic controller output or the digital soft-startup output to the power switches in normal or startup conditions, respectively. The details of the startup module will be discussed in Section V. The high-gain error amplifier (EA) is added to the control loop in order to improve the dc load regulation of the converter by adjusting the average of the feedback voltage (V_{fb}) such that the offset due to the DCR resistance of the inductor is eliminated. In normal operation, the hysteretic band of the comparator is modulated randomly in order to hop the switching frequency of the converter between a set of M frequencies. Although hopping could have been achieved by modulating other parameters, such as the control loop delay, the proposed method is chosen since the hysteretic band can be more accurately controlled. The hysteretic band is modulated every switching cycle by using the rising edge of the control signal (V_{ctr_hys}) to trigger at 20-stage, digital pseudo-random number (PRN) generator, which in turn selects a different hysteretic band. This configuration ensures that modulation takes place only at the end of a full cycle, which eliminates switching duty-cycle disturbances. It also ensures the hysteretic band is modulated every cycle, which results in better spectral spreading due to rapid hopping [27].

B. Spur-Free Operation

Although the design in Fig. 3 implements the random CCFH component, spur elimination also requires meeting the condition in (2), and therefore, the sizes of the hysteretic band cannot be arbitrary. By inspecting the condition in (2), an important observation that can be made is the fact that it is relative in nature, i.e., a condition on ratios rather than on absolute values

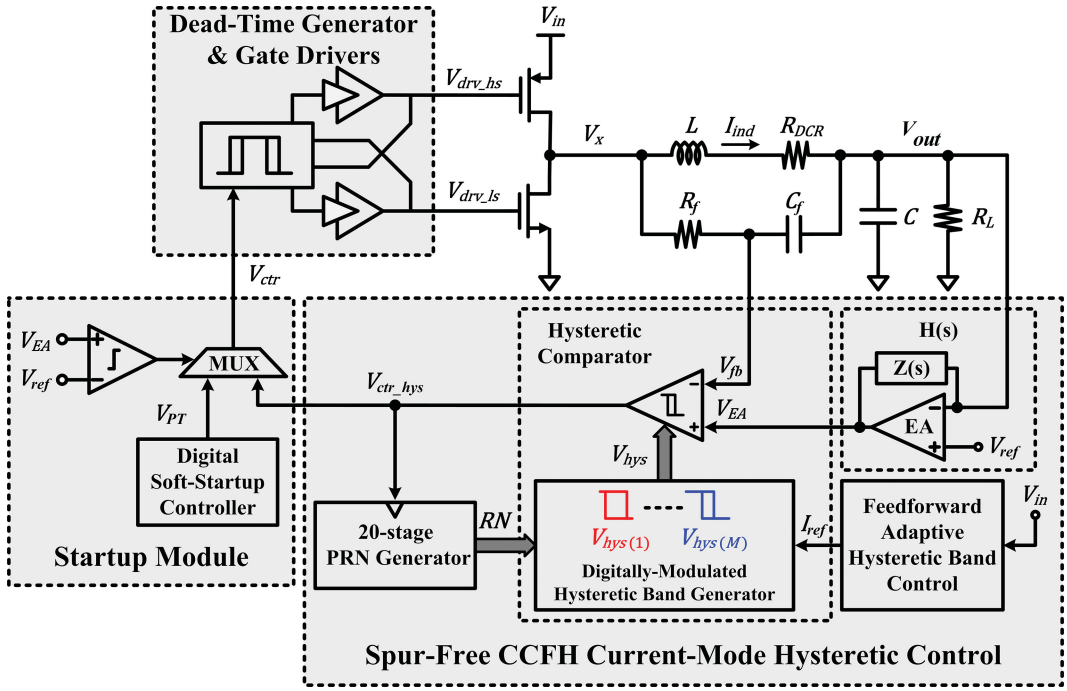


Fig. 3. Top-level block diagram of the proposed current-mode hysteretic buck converter incorporating spur-free CCFH control.

of frequencies. This essentially implies that variations in the absolute values of the switching frequencies are irrelevant and only the mutual relationship is what matters. This observation can be leveraged in hysteretic controllers where the absolute values of switching frequencies are always operating conditions dependent. Using (1), the condition in (2) can be rewritten as

$$\frac{f_{s(M)}}{f_{s(i)}} = \frac{\tau_{RC}\left(V_{hys(i)}/V_{in}\right)+\tau_D}{\tau_{RC}\left(V_{hys(M)}/V_{in}\right)+\tau_D} = \left(1+\frac{m_{(i)}}{n_{(i)}}\right) \neq \text{Integer} \tag{3}$$

for $i = 1$ to $M-1$. By minimizing the loop delay (τ_D) through careful design of the comparator and the dead-time generator and gate drivers, and maximizing both the current sensing filter's time constant (τ_{RC}) and hysteretic band sizes, the loop delay can be made substantially smaller than $\tau_{RC}(V_{hys(M)}/V_{in})$. In which case, (3) can be simplified as

$$\frac{f_{s(M)}}{f_{s(i)}} = \frac{V_{hys(i)}}{V_{hys(M)}} = \left(1+\frac{m_{(i)}}{n_{(i)}}\right) \neq \text{Integer}. \tag{4}$$

Thus, the condition of spur elimination can be met, irrespective of the absolute band sizes or switching frequencies, by setting the ratios between the hysteretic bands according to (4). Moreover, this enables better prediction and control of the ratio between the frequencies (through well-controlled ratios of the hysteretic bands), and consequently, better prediction and control of the frequency range around the average switching frequency and the resulting noise floor peaking [27]. It is worth noting that if the loop delay τ_D is sufficiently large compared to $\tau_{RC}(V_{hys(M)}/V_{in})$ that it cannot be neglected, spur-free performance will still be preserved as long as τ_D is designed to prevent (3) from yielding an integer, but the ratio between the frequencies will deviate from the well-controlled ratios between the hysteretic bands.

C. Eliminating Inductor Current Imbalance

One of the common side effects of employing any form of frequency hopping in switching power converters is inductor current imbalance, i.e., the average inductor current is disturbed due to changing the switching frequency even if the load current is staying constant [29]. In the time domain, this effect manifests itself as additional transients in the output voltage every time the frequency is hopped, which makes meeting the voltage ripple requirements quite difficult. In the frequency domain, it manifests itself as peaking in the low-frequency noise floor and/or additional low-frequency spurs shaped by the *LC* output filter [27]. One method to eliminate this problem in PWM-controlled converters is to use equal rising and falling slopes in the ramp signal, i.e., a triangular ramp [24], [30]. Another method relies on injecting an additional pulse into the control signal to ensure that frequency hopping takes place exactly at the point where the inductor current is equal to the load current such that the average of the inductor current is preserved as the frequency is hopped [29]. However, since there is no ramp signal in hysteretic controllers, and injecting an additional pulse at the correct time to preserve constant average inductor current requires complex and precise timing control (difficult to achieve reliably in self-oscillating topologies), alternative methods must be developed for hysteretic controllers.

One method that can be employed for modulating the hysteretic band in a hysteretic controller is referred to as single-sided band modulation, where only one of the bounds of the band is modulated while the other is maintained at a constant level.

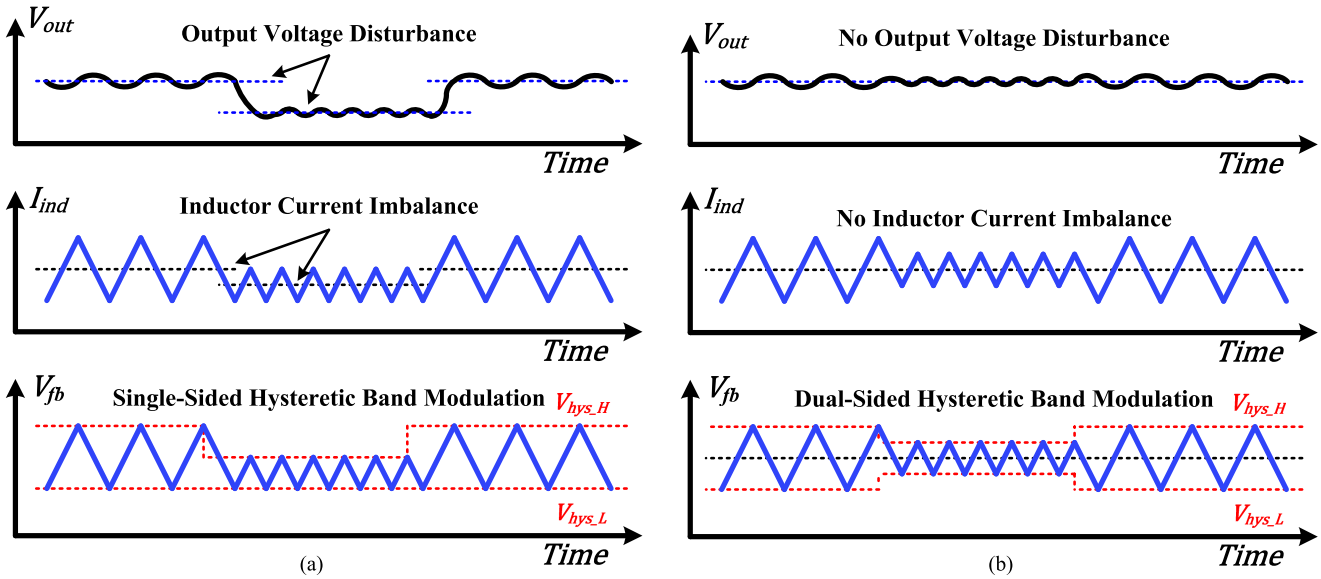


Fig. 4. Key waveforms for: (a) single-sided hysteretic band modulation and (b) dual-sided hysteretic band modulation.

This is illustrated in Fig. 4(a) where the hysteretic band is modulated between only two different values for simplicity by keeping the lower hysteretic bound (V_{hys_L}) constant and modulating the upper bound (V_{hys_H}). As shown in the figure, this method results in inductor current imbalance since the peak current is changing while the valley is not, and thus the average inductor current is changing, which causes output voltage disturbances. In order to eliminate this imbalance, this paper proposes a dual-sided band modulation approach, where both the upper and lower bounds of the hysteretic band are modulated simultaneously and symmetrically as illustrated in Fig. 4(b), where V_{hys_H} and V_{hys_L} are modulated such that their average is always constant. As shown in the figure, this approach ensures the average inductor current stays constant regardless of the hysteretic band size or the switching frequency. Thus, output voltage disturbances due to hopping are eliminated and the worst-case output voltage ripple will simply correspond to the lowest switching frequency.

D. Reducing Switching Frequency Variations

Although incorporating spur-free CCFH switching in the hysteretic controller eliminates the spurious noise irrespective of variations in the average switching frequency of the converter, excessive variations are still undesired as they can potentially degrade efficiency and result in highly varying output voltage ripple. Using (2), and assuming negligible loop delay and equal probability of occurrence for each of the hysteretic bands used for frequency hopping, the average switching frequency $f_{s(\text{avg})}$ can be derived as

$$f_{s(\text{avg})} = \frac{M}{\sum_{i=1}^{i=M}\left(\frac{1}{f_{s(i)}}\right)} = \frac{M\,V_{in}\,D\,(1-D)}{\tau_{RC}\sum_{i=1}^{i=M}V_{hys(i)}} \quad (5)$$

which shows that $f_{s(\text{avg})}$ is a strong function of the input voltage V_{in}. To reduce variability in $f_{s(\text{avg})}$, this paper proposes employing feedforward adaptive hysteretic band control as shown in Fig. 3, to adapt the digitally modulated hysteretic bands such that $(V_{hys(i)}/V_{in})$ for $i = 1$ to M is kept constant. With such design, although the average switching frequency continues to vary with the duty cycle and the sensing filter time constant, but the overall variations are greatly reduced.

E. Loop Stability and Compensation

The proposed top-level implementation contains a ripple-based, fast current regulation loop, and an average-based, high-gain voltage regulation loop. To ensure the stability of the voltage regulation loop, its transfer function must be obtained to determine the needed compensation, i.e., $H(s)$. The control-to-output transfer function of the voltage regulation loop is $V_{out}(s)/V_{EA}(s)$, and it can be derived by observing that the current regulation loop sets the average of $V_{EA}(s)$ and the feedback signal ($V_{fb}(s)$) to be equal [31]. Considering that $V_{fb}(s)$ can be expressed in terms of inductor current ($I_{ind}(s)$) and output voltage ($V_{out}(s)$), $V_{EA}(s)$ can be written as

$$V_{EA}(s) = \left(\frac{1+s\frac{L}{R_{DCR}}}{1+sR_fC_f}\right)R_{DCR}\,I_{ind}(s) + V_{out}(s) \quad (6)$$

where L is the inductor and R_{DCR} is its series resistance. By expressing the inductor current in terms of the load resistance (R_L) and output capacitor (C), $V_{out}(s)/V_{EA}(s)$ can be expressed as

$$\frac{V_{out}(s)}{V_{EA}(s)} = \frac{\left(\frac{R_L}{R_L+R_{DCR}}\right)(1+sR_fC_f)}{1+s\frac{R_LR_fC_f+L+R_LR_{DCR}C}{R_{DCR}+R_L}+s^2\frac{R_LLC}{R_{DCR}+R_L}}. \quad (7)$$

Since R_{DCR} and C_f are typically small, this transfer function contains two complex poles at approximately $(1/\sqrt{LC})$. Thus, the compensation network $H(s)$ in Fig. 3 can be type-I, type-II, or type-III to ensure the stability of the loop. However, considering that (7) contains a zero at $(1/R_fC_f)$, which facilitates compensation, a fully integrated type-II network is chosen

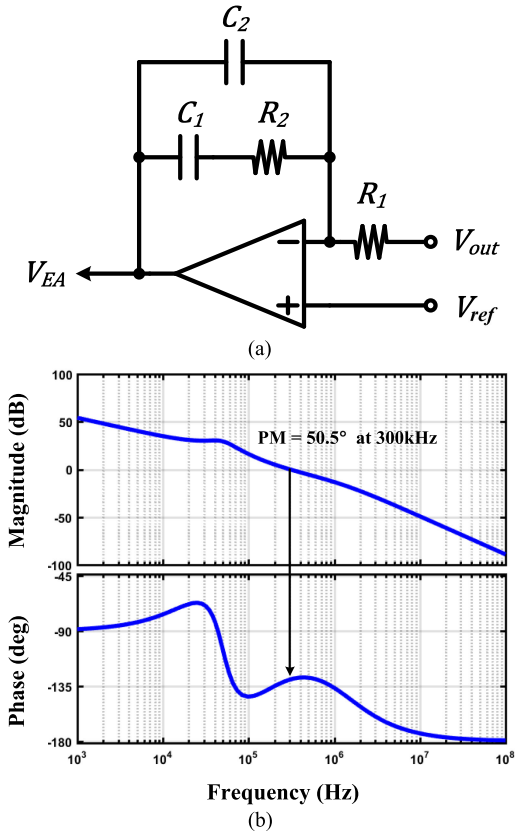


Fig. 5. Type-II compensation network: (a) circuit realization and (b) loop gain and phase responses.

to avoid the excessively slow response and large off-chip capacitor of a type-I network, and the large number of passives of a type-III network [2]. In this case, $H(s)$ can be represented as

$$H(s) = \frac{(1 + sR_2C_1)}{sR_1(C_1 + C_2)\left(1 + s\left(\frac{C_1C_2}{C_1+C_2}\right)R_2\right)} \quad (8)$$

which can be implemented as shown in Fig. 5(a), and results in the overall voltage loop gain and phase responses shown in Fig. 5(b). It is worth noting that although current-mode controllers are generally expected to have a loop transfer function without the two *LC* complex poles [2], the loop transfer function in (7) turned out to have these poles because the feedback signal $V_{fb}(s)$ is derived from the switching node rather than the inductor current. Thus, it bears only the inductor current profile and not actual current values. As a result, the current is not regulated by the current control loop and the inductor continues to behave as an inductor within the voltage regulation loop rather than a current source, thus the emergence of the two complex poles [31].

V. Proposed Circuit-Level Realization

In this section, the circuit-level realization of the critical blocks in the proposed spur-free CCFH current-mode hysteretic buck converter will be presented. This includes the hysteretic controller, the digital soft-startup, and the dead-time generator and gate-driver circuits.

A. Spur-Free CCFH Hysteretic Controller

The dual-sided hysteretic function needed for the proposed spur-free CCFH controller is realized using two independent comparators with the hysteretic bounds generated separately using a band generator as shown in Fig. 6(a). This method is chosen over using a single hysteretic comparator or two offset comparators (similar to [37]) since modulating the hysteretic band through modulating voltage references is easier than modulating transistor sizes within the comparator itself. Since the feedback signal (V_{fb}) used by the comparators is derived from the switching node, and although it is filtered through the current sensing filter, remnants of the sharp transitions of the switching node may still make it through the filter and falsely trigger the comparators. Thus, a glitch-free latching circuit is implemented using an XNOR gate and delay cells to provide a blanking period for latching the comparators' outputs [32]. This method is more effective and more area efficient than the alternative approach of increasing the size of the current sensing filter. The circuit realization of the digitally modulated hysteretic band generator is shown in Fig. 6(b). A unity-gain voltage buffer is used to set the middle point between the identical resistors (R_{hys}) to the same level as the error signal (V_{EA}) of the EA, such that the upper and lower hysteretic bounds (V_{hys_H} and V_{hys_L}) are generated symmetrically around V_{EA} by forcing the modulation current (I_{mod}) into the two resistors. This configuration implements the feedback path of the voltage regulation loop shown in Fig. 3. To modulate the hysteretic band, I_{mod} is generated through an M-branches of current mirrors from the shared reference current (I_{ref}), where I_{mod} is modulated by enabling/disabling branches using a 20-stage $(\log_2 M)$-bit PRN generator followed by a binary-to-thermometer decoder. Thermometer coding is selected to guarantee the monotonicity of the generated bands and to eliminate glitches that occur with standard binary coding. The finger ratios between the current mirror branches are designed to meet the spur-elimination condition in (4). The adaptation of the hysteretic band with the input voltage is implemented using the feedforward adaptive hysteretic band controller shown in Fig. 6(b), where a potential divider from the input voltage and a voltage-to-current converter are used together to modulate the reference current (I_{ref}) as a function of the input voltage. This way, adaptation with the input voltage can be achieved while preserving the spur-elimination condition in (4) since I_{ref} is common to all values of I_{mod}.

The 20-stage $(\log_2 M)$-bit PRN generator is implemented using the linear feedback shift register shown in Fig. 7, where 20 D flip-flops are used with an XNOR gate to generate a 20-bit pseudo-random digital code. Therefore, if the desired number of hysteretic bands is M, only $\log_2 M$ bits are needed out of the 20 bits generated. Although any bits can be selected, it is important to note that selecting consecutive bits should be avoided since in that case, and for any given code, the number of possible outcomes for the next code would be less than the theoretical number (i.e., M). This introduces a memory effect that degrades

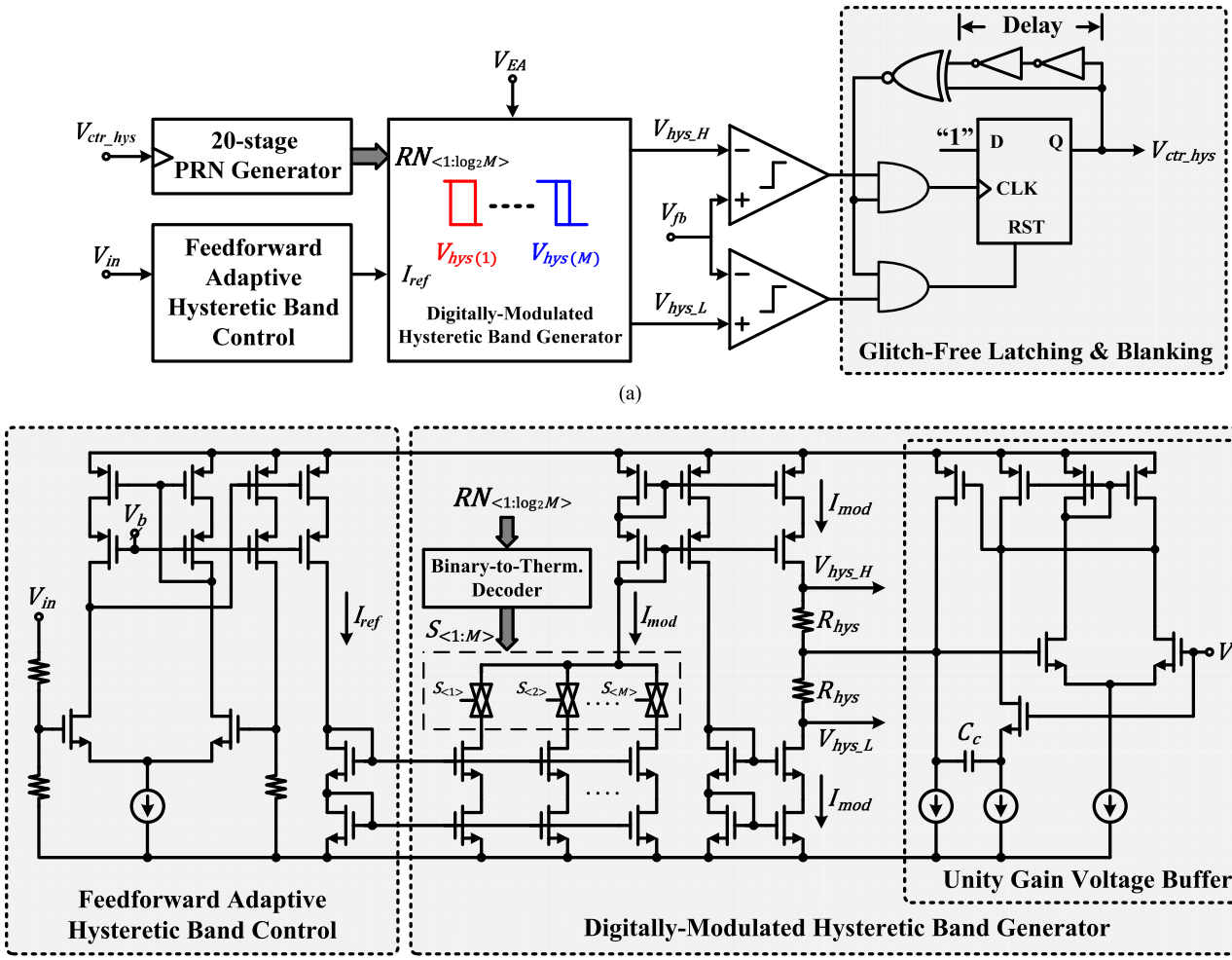


Fig. 6. Proposed spur-free CCFH hysteretic controller: (a) simplified schematic showing the glitch-free latching circuit and (b) transistor-level details of the hysteretic band generator with feedforward adaptive control.

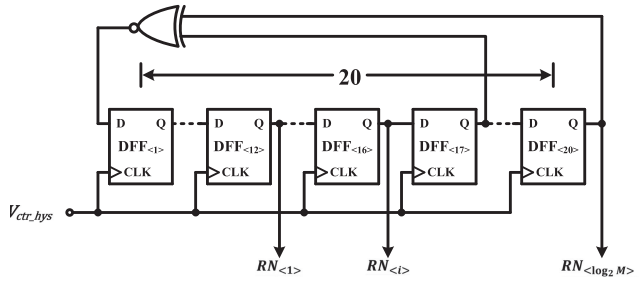


Fig. 7. Pseudo-random number (PRN) generator using a 20-stage linear feedback shift register (LFSR).

the randomness of the generated codes. Instead, the $\log_2 M$ bits should be tapped from nonconsecutive flip-flops such that for any code, there is an equal likelihood for the next code to be any of the M possibilities independent of the current code.

B. All-Digital Soft Startup

During startup conditions, the main control loop detects that the output voltage is far off from the target value, and generates a large error signal. If no additional precautions are taken, this large error signal produces excessively long ON-time intervals, which leads to dangerously high in-rush current [33]. To mitigate this issue, the main controller is commonly bypassed during startup conditions, and a separate soft-startup controller is employed instead to control the in-rush current. Once the output reaches its target value, control is handed off from the soft startup to the main control loop for normal operation. A conventional soft-startup circuit is shown in Fig. 8(a), where the sawtooth signal (V_{saw}) is compared to a slow ramp voltage (V_{ramp}) to generate a train of pulses with small, yet gradually increasing duty cycle to control the power switches and the inrush current [33]. However, the generation of the slow ramp requires either an off-chip capacitor and a dedicated pin, or a relatively large on-chip capacitor. Although alternative soft-startup circuits have been proposed to reduce the size of the on-chip capacitor, their operation remains analog in nature and requires custom circuit design [34].

In this work, the all-digital soft-startup circuit shown in Fig. 8(b) with its timing diagrams is proposed. The fundamental idea lies in generating a train of pulses with incremental,

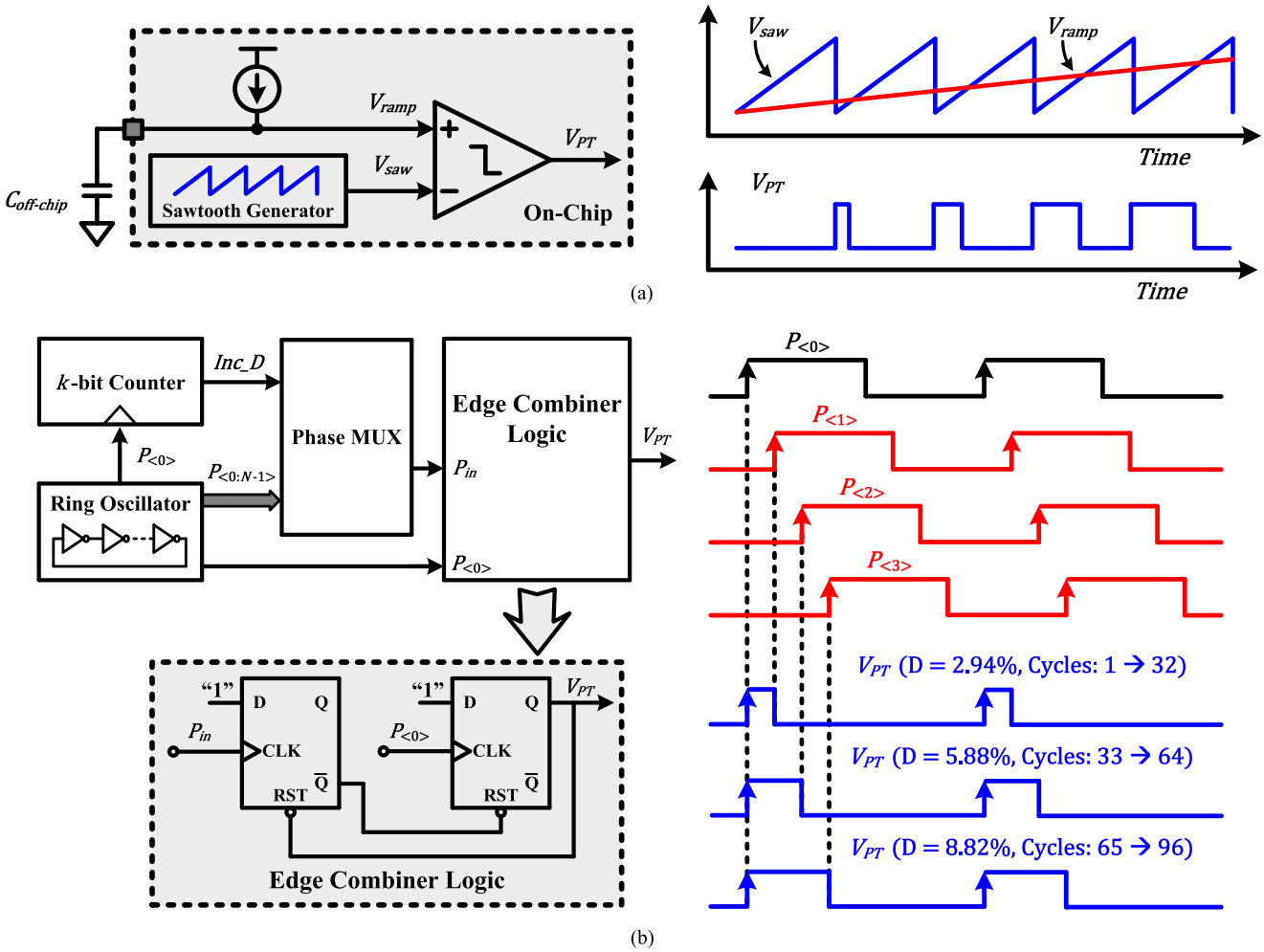


Fig. 8. Soft-startup circuits: (a) conventional analog realization and its timing diagrams and (b) proposed all-digital circuit and its timing diagrams.

digitally controlled duty cycle. First, a simple N-stage ring oscillator is implemented to generate N equally spaced clock phases ($P_{\langle 0\rangle}$ to $P_{\langle N-1\rangle}$). By combining the rising and falling edges of the various phases using a phase combiner logic circuit, pulses with duty cycle that is an integer multiple of $(1/2N)\%$ can be generated up to $(2N-1)/2N\%$. The duty cycle of the pulses is swept from the minimum to the maximum, with the number of pulses at each duty-cycle controlled using a k-bit counter as shown in Fig. 8(b). In this particular design, a 17-stage ring oscillator is used to generate pulses with duty cycle that is an integer multiple of 2.94% with maximum duty cycle of 97.05%. Each duty cycle is applied for 32 pulses. Once the output of the EA (V_{EA}) exceeds the reference voltage (V_{ref}), the control is handed over to the hysteretic controller of the converter as shown in Fig. 3. The proposed all-digital soft startup can be synthesized using standard digital cells (including the ring oscillator) and requires no analog components, while the soft-startup time can be fine tuned by changing the k-bit counter size.

C. Dead-Time Generator and Gate Drivers

In buck converters, a dead time must be inserted between the gate control signals of the high-side and low-side power switches to avoid shoot-through current. A standard technique to accomplish that is shown in Fig. 9(a), where a nonoverlapping clock generator circuit [35] is used to create two versions of the control signal (i.e., V_{pre_hs} and V_{pre_ls}) with a dead time equal to the total delay of the circuit. However, in order to ensure that the actual dead time at the gates of the power switches (i.e., V_{drv_hs} and V_{drv_ls}) is always nonzero, the delay mismatches between the level shifters and the gate drivers must be accounted for by making the dead time, and consequently the loop delay, excessively long. Moreover, the loop delay is further increased due to the additional delay of the level shifters and the gate drivers. Since the loop delay in the proposed spur-free CCFH hysteretic controller must be minimized to make the condition in (4) valid, a different approach is needed. Thus, the dead time generator circuit in [36] is adopted as shown in Fig. 9(b), where the control signal (V_{ctr_hys}) is first level-shifted, and then the gate drivers are incorporated within the dead-time generation process. The first advantage of such circuit is that the dead time is inserted right in the gate-drive signals, and thus can be ensured to be nonzero regardless of delay mismatches and without designing the dead time to be excessively long. The second advantage is that the delay of the gate drivers becomes part of the dead-time generation, and thus, the number of delay stages

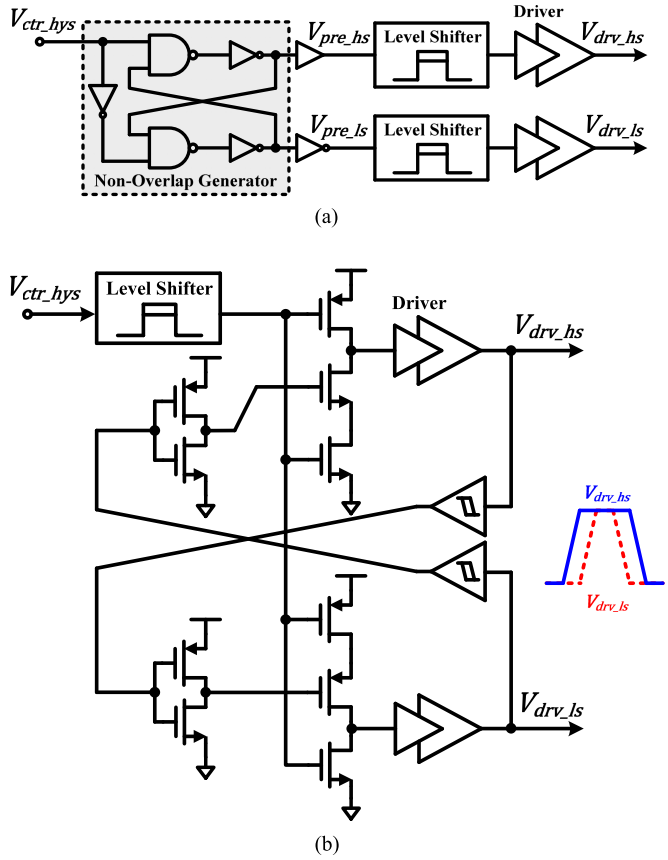
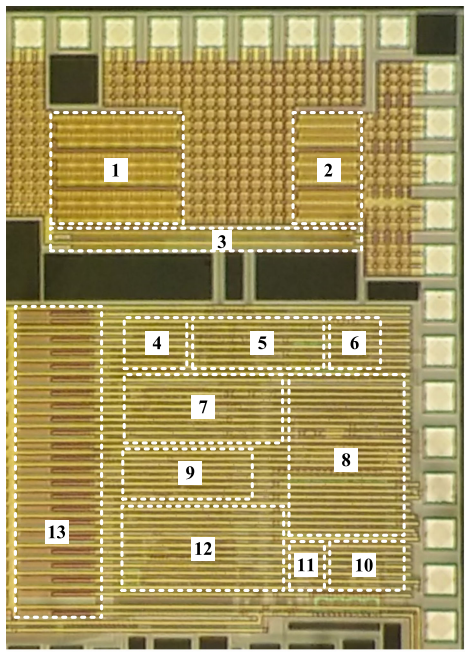


Fig. 9. (a) Standard dead-time generator and gate drivers and (b) adopted architecture from [36] modified by adding Schmitt triggers to prevent glitches and false triggering.



(1) High-side switch (PMOS)
(2) Low-side switch (NMOS)
(3) Dead-Time Gen. + Gate Drivers
(4) PRN Generator
(5) Comparators + Logic
(6) RC Filter
(7) Hysteretic Band Generator
(8) Error Amp. + Type-II Network
(9) All-Digital Soft-Startup
(10) Adaptive Feedforward Control
(11) Biasing
(12) Analog-Soft Start-up (for testing)
(13) Decoupling Capacitors

Fig. 10. Die photo of the proposed spur-free CCFH current-mode hysteretic buck converter with the main building blocks highlighted.

needed for generating the dead time is reduced. These two advantages ultimately result in a much shorter overall loop delay. However, a proposed modification to the circuit in [36] is the additional Schmitt triggers shown in Fig. 9(b). Since the feedback signals of the dead-time generator circuit are now driven by the gate-driver signals, which are noisy, nonmonotonic, and have a relatively slow rise and fall times. The Schmitt triggers ensure proper buffering of these signals to prevent glitches and false triggering.

VI. Measurement Results

The proposed spur-free CCFH current-mode hysteretic buck converter is implemented in a 0.35-μm standard CMOS technology. The converter is designed to operate from Li-ion battery input levels (i.e., 2.7–4.2 V) and to generate a programmable output in the range of 1.2–1.8 V with a maximum load current of 600 mA. The die photo of the converter is shown in Fig. 10 with the main design components highlighted. The total active silicon area of the converter is 0.9 mm^2, 37% of which is taken by the power switches and their drivers, while the rest is taken by the controller, including the proposed all-digital soft-startup circuit and type-II compensation. The test setup used to characterize the converter is shown in Fig. 11(a) and (b), while the evaluation printed circuit board is shown in Fig. 11(c) with its main components highlighted. The hysteretic band is hopped between eight different sizes within the following set:

$$V_{hys(i)} = \left(\frac{i+5}{13}\right) \times V_{hys(8)} \qquad \text{for } i = 1 \text{ to } 8 \qquad (9)$$

where $V_{hys(8)}$ is the largest band size. This ensures meeting the spur-elimination condition in (4) with a target ratio of the maximum and minimum frequencies that is always 13/6 to minimize the noise floor peaking due to spreading the spurs. Detailed analysis of the relationship between the ratio of the maximum and minimum frequencies and noise floor peaking in spur-free control can be found in [27].

The measured output voltage spectrum up to 20 MHz under two different operating conditions is shown in Fig. 12 with and without the proposed spur-free CCFH switching technique and with the actual switching frequencies noted. As shown, spurs are fully eliminated as predicted by the theory irrespective of the operating conditions or the actual switching frequencies. The full spreading of the fundamental spur is manifested as a peaking in the noise floor around the average of the switching frequencies used for hopping, while the high-frequency noise floor is barely changed since the energy contained in the higher frequency spurs is much smaller than the fundamental. To demonstrate the importance of meeting the spur-elimination condition in (4), the converter is designed to have the option to apply CCFH with two different hysteretic band sizes that violate the condition in (4) and the resulting output spectrum is shown in Fig. 13, along with

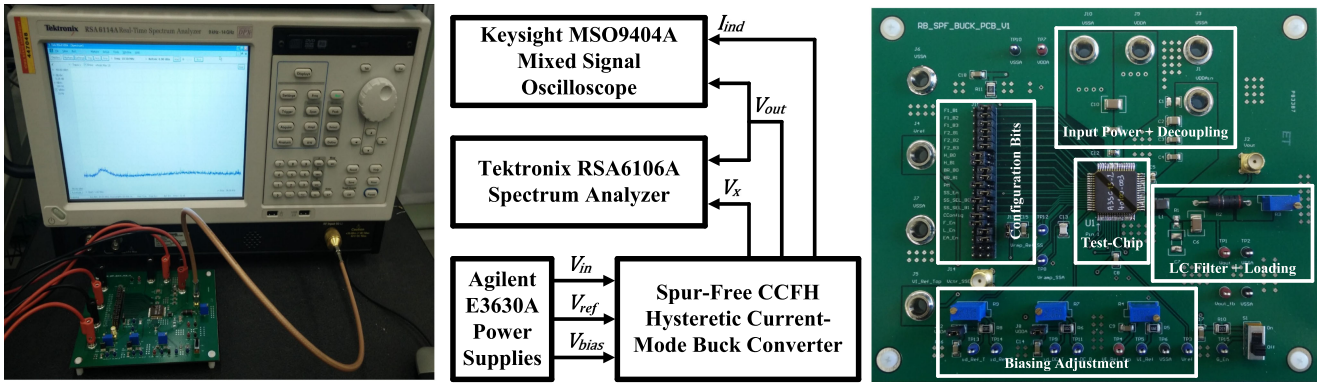


Fig. 11. (a-b) Test setup used to characterize the proposed converter and (c) evaluation printed circuit board (PCB) with its main components highlighted.

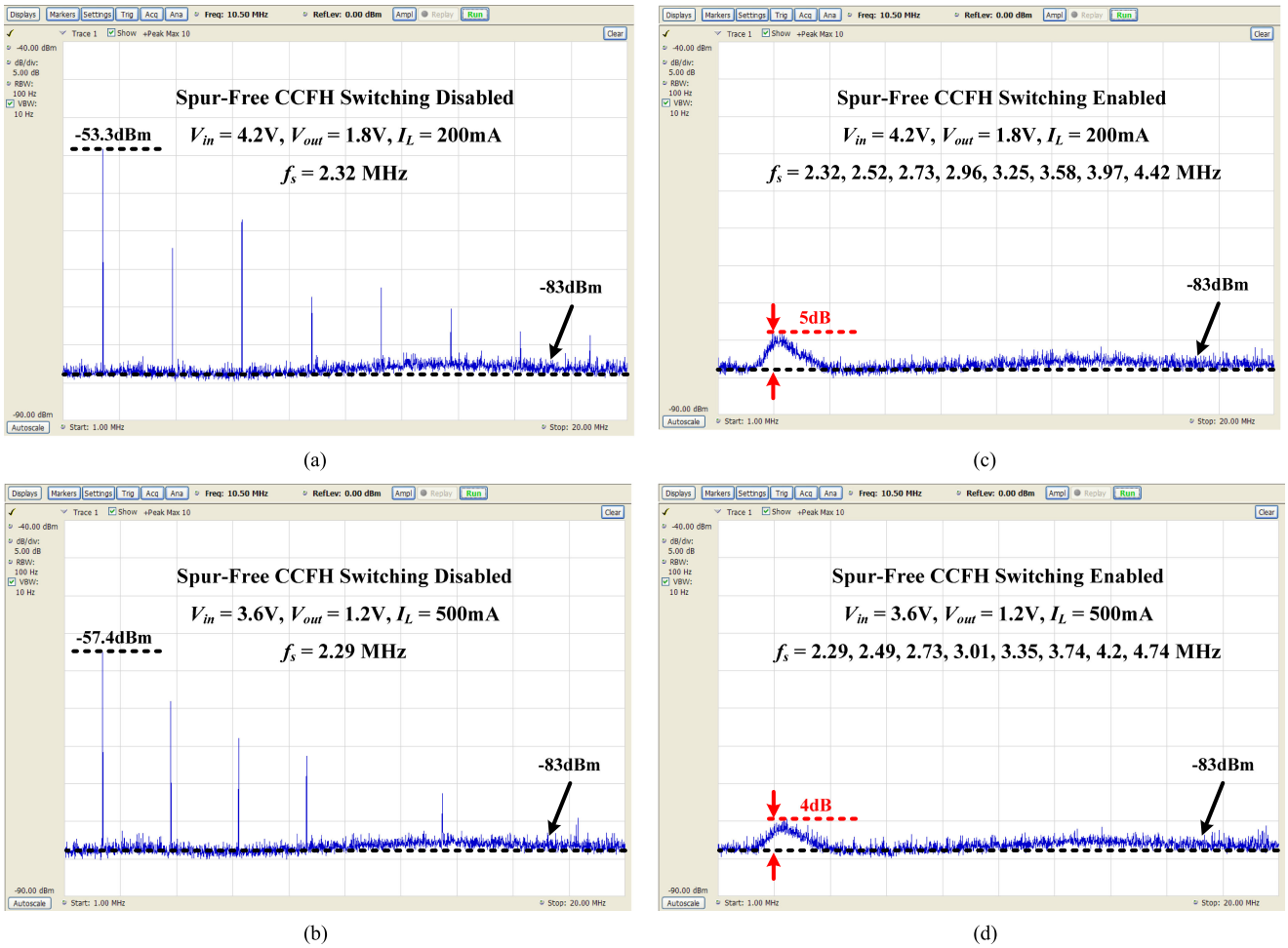
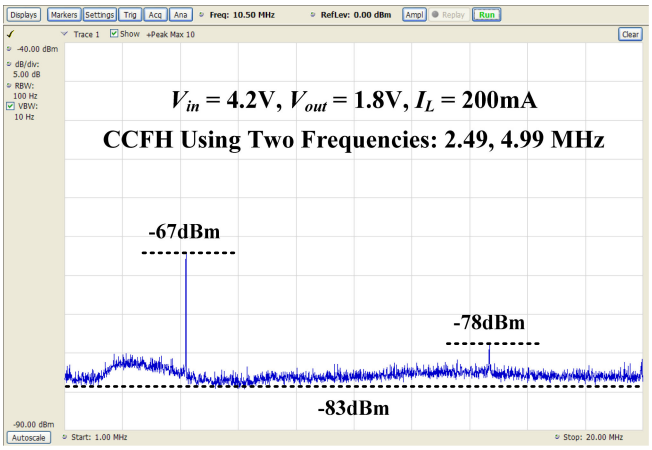
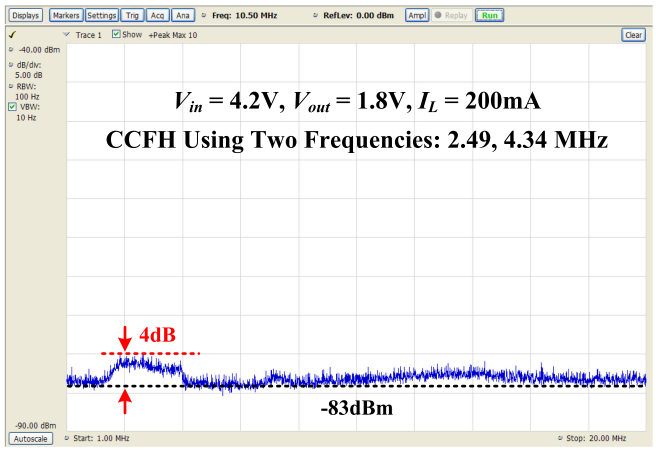


Fig. 12. Output voltage spectrum under two different operating conditions with spur-free CCFH disabled (i.e., single switching frequency) in (a) and (b), and with the proposed spur-free CCFH switching enabled in (c) and (d).

the case where the two band sizes are meeting the condition. As shown, when the condition is violated, spurs persist in the output spectrum. Therefore, CCFH by itself is insufficient for eliminating the spurs (will only reduce the spurs as in [23] and [24]), and meeting the condition in (4) is necessary for eliminating the spurs [27], [28]. To demonstrate that full spur elimination is achieved at various nodes within the converter and not just at the heavily filtered output node, the spectrum is measured at the switching node (the worst in terms of noise). The results are shown in Fig. 14 with and without the proposed spur-free CCFH switching, where spurs are fully eliminated. It is worth noting that the ~30 dB elevation in the noise floor is due to the

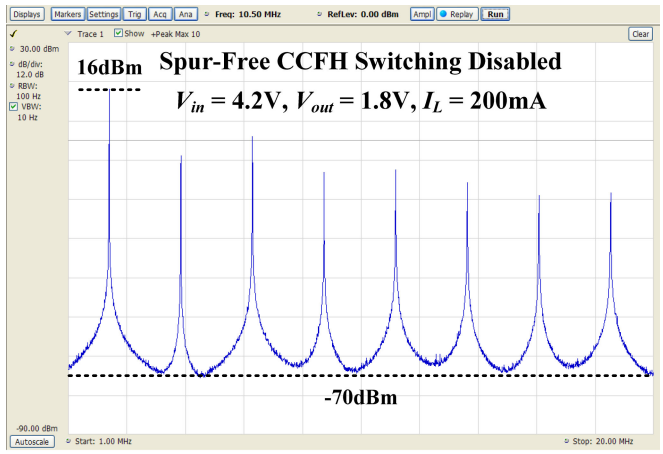


(a)

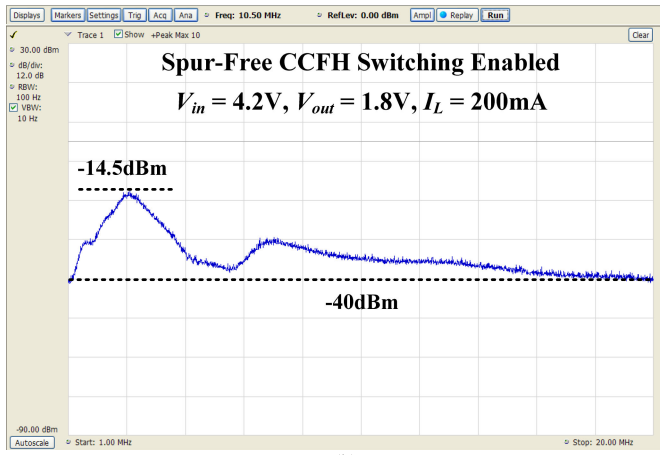


(b)

Fig. 13. Output voltage spectrum with: (a) CCFH between two frequencies that do not meet the spur-elimination condition in (4), and (b) spur-free CCFH between two frequencies that meet the spur-elimination condition in (4). Operating conditions are noted on each figure.



(a)



(b)

Fig. 14. Switching node spectrum with: (a) spur-free CCFH switching disabled (i.e., single switching frequency) and (b) spur-free CCFH switching enabled.

large magnitude of the unfiltered spurs at the switching node. The results of Figs. 12 and 14 show that the proposed spur-free hysteretic converter can be used to power noise-sensitive loads, or be integrated within noise-sensitive systems while accommodating widely varying operating conditions with no need for frequency regulation loops to set the location of the spurs accurately.

To validate the effectiveness of the proposed dual-sided hysteretic band modulation in terms of eliminating inductor current imbalance due to hopping, the converter is designed with the option to apply single-sided modulation for comparison purposes. The output voltage is examined without any modulation, and with single- and dual-sided modulation, and the results are shown in Fig. 15 in both the time and frequency domains. As shown, dual-sided modulation is quite effective in minimizing inductor current imbalance, which is evident by observing the reduction in the output transients and their corresponding low-frequency spectrum compared to single-sided modulation. In fact, by comparing Fig. 15(a) and (c), dual-sided modulation produces very similar results to the case without any modulation at all in terms of voltage ripple and low-frequency spectral content, while single-sided modulation increases the ripple by over a factor of two and causes about 12 dB peaking in the low-frequency noise floor. The transient response of the converter is also measured using a 500-mA load step with and without the proposed spur-free CCFH. As shown in Fig. 16, the response of the converter is almost identical in both cases, which indicates that incorporating spur-free CCFH has minimal impact on the transient response, whether in steady state as in Fig. 15(c), or in load transient conditions as in Fig. 16(b).

To demonstrate the effectiveness of the proposed feedforward adaptive hysteretic band control in reducing switching frequency variability with the input voltage, the switching frequency of the converter is measured versus the input voltage with and without the feedforward controller. The switching frequency versus the input voltage is shown for both cases in Fig. 17, where the normalized frequency deviation $2(f_{s(\max)} - f_{s(\min)})/(f_{s(\max)} + f_{s(\min)})$ is reduced from 64% to 21% at 1.8-V output, and from 26% to 14% at 1.2-V output. The hysteretic bands are designed such that with feedforward adaptive hysteretic band control, the average switching frequency ranges from 2.5 to 3.1 MHz across an input voltage range from 2.7 to 4.2 V in order to meet a peak efficiency target of around 90%.

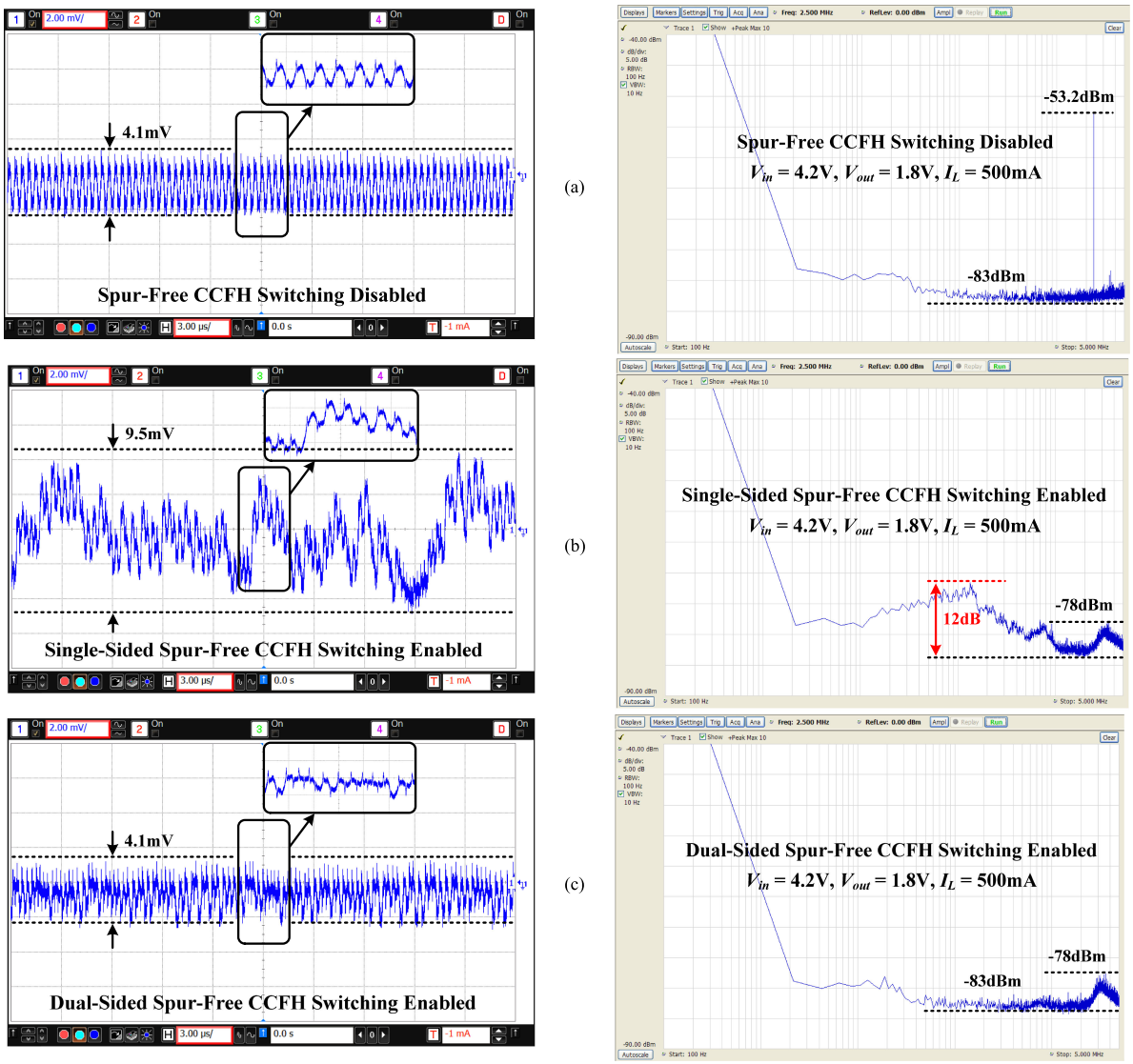


Fig. 15. Output voltage ripple and low-frequency spectrum up to 5 MHz with: (a) spur-free CFFH switching disabled (i.e., single switching frequency), (b) spur-free CCFH switching with single-sided band modulation, and (c) spur-free CCFH switching with dual-sided band modulation.

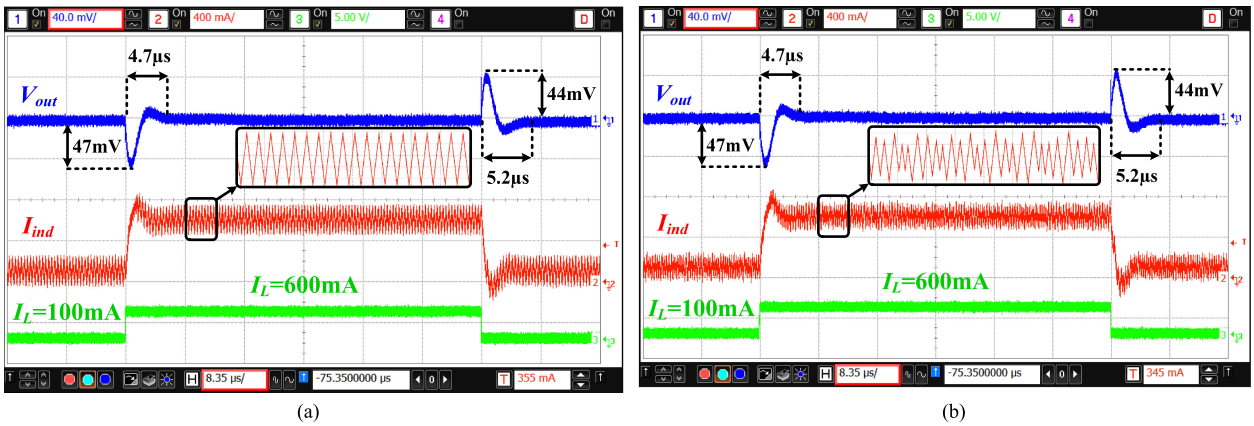


Fig. 16. Output transient response to a 500-mA load step with: (a) spur-free CCFH switching disabled (i.e., single switching frequency) and (b) spur-free CCFH switching enabled. Input voltage 4.2 V, output voltage 1.8 V.

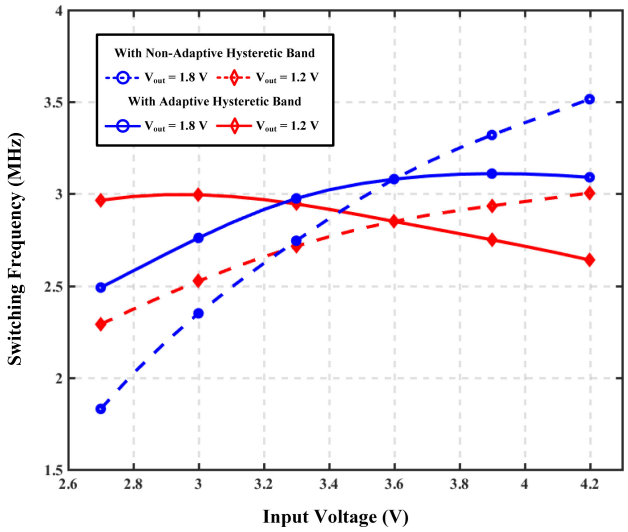
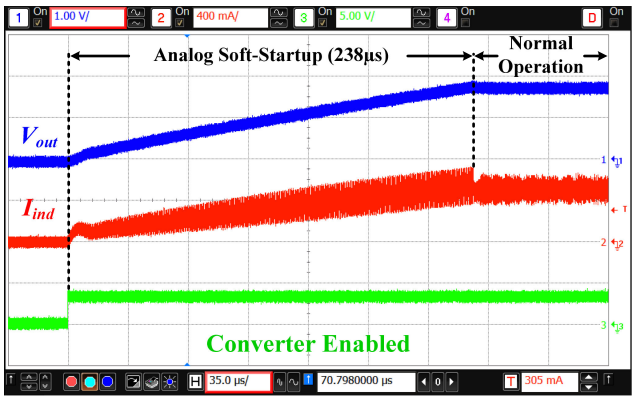
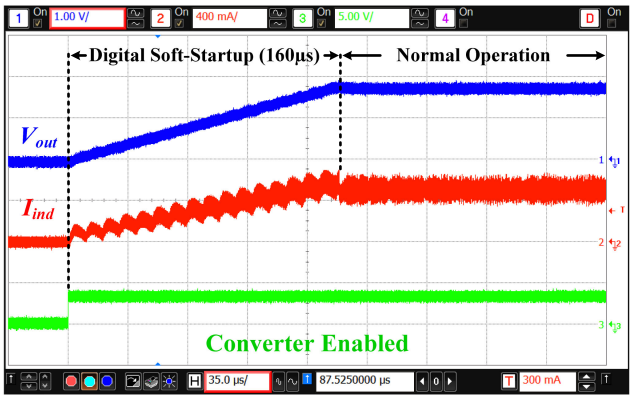


Fig. 17. Switching frequency versus input voltage at different output voltages with and without the proposed feedforward adaptive hysteretic band controller.



(a)



(b)

Fig. 18. Startup operation of the converter with: (a) a conventional analog soft-startup circuit and (b) the proposed all-digital soft-startup. Input voltage 4.2 V, output voltage 1.8 V, load current 500 mA.

To demonstrate the operation of the proposed all-digital soft-startup circuit, a conventional analog soft-startup circuit with an off-chip capacitor (discussed in Section V-B) is also implemented in the same chip for performance comparison purposes. The operation of the soft-startup circuit is tested by periodically

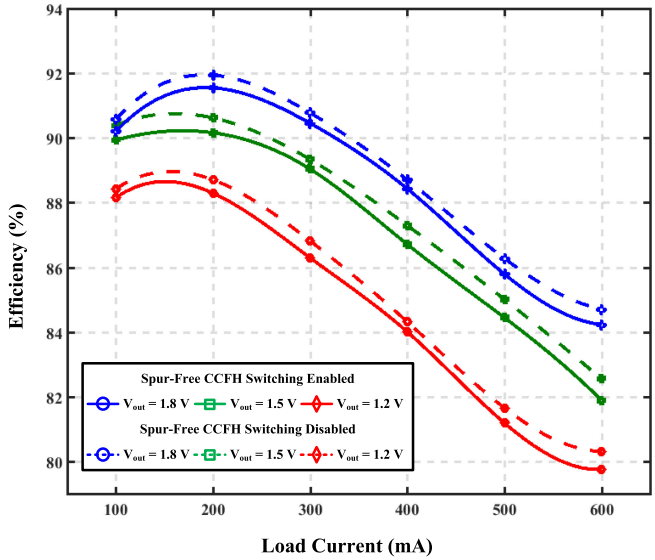


Fig. 19. Power conversion efficiency versus load current at different output voltages with and without the proposed spur-free CCFH switching. Input voltage 4.2 V.

enabling and disabling the converter and measuring the output voltage and inductor current as shown in Fig. 18. As seen, both circuits yield similar performance. However, the proposed circuit is faster and has the advantage of being purely digital with no large on-chip or off-chip capacitances as discussed in Section V-B. Therefore, it can be easily tweaked to meet the required performance without extensive design modifications. The converter's power conversion efficiency is measured versus load current at various output voltages with and without spur-free CCFH as shown in Fig. 19, where the peak efficiency is 92% and the degradation in efficiency due to spur-free CCFH switching is less than 0.7%. The reason for this slight drop is that when CCFH is disabled, the largest hysteretic band is used, and thus, the converter switches at the lowest switching frequency of the eight frequencies used when CCFH is enabled. As a result, the average switching frequency when CCFH is enabled is higher than when it is disabled, which leads to slightly higher switching losses, and thus the 0.7% efficiency drop. This drop can be minimized by choosing the eight hysteretic bands so that the average switching frequency when CCFH is enabled is the same as the switching frequency when CCFH is disabled [26]–[28]. It is also worth noting that for lighter load conditions (less than 100 mA), a PFM type of controller would be more appropriate in order to scale the losses with the load to maintain high efficiency. In fact, combining the proposed spur-free hysteretic controller with the spur-free PFM controller proposed in [28] would provide a complete solution for achieving a low-noise operation with high efficiency across all load conditions.

Table I summarizes the key performance and design aspects of the proposed converter versus existing literature. Compared to spur-free CCFH converters with PWM control [27], the proposed spur-free CCFH hysteretic converter offers much better transient load regulation with significantly smaller overshoot/undershoot and faster recovery time without

TABLE I
PERFORMANCE SUMMARY AND COMPARISON WITH OTHER PUBLISHED WORK

		This Work	TPEL 2013 [11]	TVLSI 2013 [27]	TVLSI 2012 [12]	SOVC 2012 [13]	SOVC 2011 [14]	ISSCC 2009 [15]
Control Scheme		Current-Mode Hysteretic with Feedforward Adaptive Band Control and Spur-Free CCFH	Current-Mode Hysteretic	Voltage-Mode PWM with Spur-Free CCFH	Pseudo-PWM Voltage-Mode Hysteretic	Hybrid Voltage/Current-Mode Hysteretic	ΔI_L-Emulated Hysteretic	Quasi-V^2 (Current-Mode) Hysteretic
Technology		0.35-μm CMOS	130-nm CMOS	0.35-μm CMOS	0.35-μm CMOS	130-nm CMOS	0.35-μm CMOS	0.35-μm CMOS
Active Silicon Area		0.9 mm^2	0.732 mm^2	0.36 mm^2 *	4.18 mm^2 **	0.7 mm^2	1.3 mm^2	1.8 mm^2 **
Input Voltage		2.7–4.2 V	2.4–4.8 V	3.3–5.5 V	2.4–4.2 V	2.5 V	3 V	2.7–3.3 V
Output Voltage		1.2–1.8 V	1.8 V	1.3–3.8 V	1.8 V	0.7–1.8 V	0.9–2.1 V	0.9–2.1 V
Maximum Load		600 mA	2 A	600 mA	500 mA	900 mA	800 mA	500 mA
Inductor		2.2 μH	330 nH	2.2 μH	4.7 μH	1–5 μH	4.7 μH	2.2 μH
Output Capacitor		4.7 μF	10 μF	10 μF	4.7 μF	10 μF	9.1 μF	4.4 μF
Frequency Regulation Scheme		Eliminated	Analog PLL	None (PWM control)	Analog PLL	Digital Frequency Regulation Loop	Digital Adaptive Frequency Control	Digital Frequency Locked Loop (FLL)
Switching Frequency		Hopped: 2.5 MHz $\leq f_{s(avg)} \leq$ 3.1 MHz	Regulated at 3.2 MHz	Hopped: $f_{s(avg)}$ = 4.75 MHz	Regulated at 1 MHz	Regulated at 1 MHz	Regulated at 1.7 MHz	Regulated at 3 MHz
Spur-Free Spectrum		Yes	No	Yes	No	No	No	No
Peak Efficiency		92%	89%	90%	95%	93%	92.7%	93%
Load Step Response	**Load Step (ΔI_L)**	500 mA (@ V_{in} = 4.2 V, V_{out} = 1.8 V)	1 A (@ V_{in} = 3.6 V)	200 mA (@ V_{in} = 4.2 V, V_{out} = 1.8 V)	200 mA (@ V_{in} = 3.3 V)	600 mA (@ V_{out} = 1.2 V, L = 1.8 µH)	400 mA (@ V_{out} = 0.9 V)	450 mA (@ V_{in} = 3 V)
	Undershoot/ Overshoot	47 mV / 44 mV	40 mV / 60 mV	70 mV / 120 mV	40 mV / 40 mV	61 mV / 72 mV	35 mV / 52 mV	38 mV / 45 mV (@ V_{out} = 0.9 V) 72 mV / 40 mV (@ V_{out} = 2.1 V)
	Recovery Time	4.7 μs / 5.2 μs	12 μs / 12 μs	58 μs / 54 μs	5 μs / 5 μs	< 10 μs	7.6 μs / 14.4 μs	2.4 μs / 2.8 μs (@ V_{out} = 0.9 V) 10 μs / 7.2 μs (@ V_{out} = 2.1 V)

*** Requires off-chip compensation.**
**** Total chip area with pads.**

compromising spur-free operation. Compared to other hysteretic controllers [11]–[15], it offers superior noise performance by eliminating spurs at every node within the converter without compromising the efficiency or dynamic performance expected from hysteretic controllers.

VII. CONCLUSION

A spur-free current-mode hysteretic buck converter with spur-free CCFH switching was presented. The converter fully eliminates spurious noise irrespective of variability in operating conditions and switching frequency. Thus, it enables hysteretic topologies to be used to power noise-sensitive loads, or to be integrated within noise-sensitive systems without requiring frequency regulation loops or compromising the superior dynamic response of hysteretic converters. The proposed realization of the spur-free CCFH switching scheme using dual-sided band modulation eliminates inductor current imbalance due to hopping, and thus eliminates the output glitches and the low-frequency noise floor peaking typically associated with frequency hopping. Furthermore, the feedforward adaptive hysteretic band control reduces the variations in the converter's average switching frequency with the input voltage, while the all-digital soft-startup circuit limits in-rush current without requiring off-chip components. The converter was fabricated in a 0.35-μm standard CMOS technology, and it achieves 92% peak efficiency.

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