Analysis and Design of a Novel High-Step-Up DC/DC Converter With Coupled Inductors

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***Abstract*—A new high step-up interleaved converter is proposed in this paper. This new high step-up converter utilizes the interleaved boost converter to be in series connection with the voltage-double module. The secondary sides of the coupled inductors are in interleaved series connection and shared by two voltage-double modules to accomplish the interleaved energy storage. Then, the input voltage, coupled-inductors, and multiplier capacitors are in series connection with the output to achieve the purpose of high voltage gain. The proposed circuit can be operated at a lower duty cycle to achieve high voltage gain by adjusting the turn ratio of the coupled inductors. The proposed circuit has less elements and the voltage stress of the switches and diodes can be decreased to reduce the cost. The conduction loss can be reduced and the efficiency can be increased when the switch with lower conduction resistance is applied. Finally, a prototype circuit of a 400 W high step-up converter with input voltage of 24 V and output voltage of 400 V is realized. Through simulation and experiments, the validity and property of the proposed converter can be verified.**

***Index Terms*—Coupled inductor, high step-up converter, interleaved boost converter, voltage-double module.**

I. Introduction

RECENTLY, accompanying with the rapid exhaust of the earth energy and affection of the global warming, many countries devote themselves to the research of the green energy, including the solar energy, wind energy, fuel energy, etc, [1]–[5]. However, the green energy (such as fuel cell, solar panel etc.) generally belongs to the kind of source with the low voltage and large current. Therefore, their outputs need a high efficiency and high step-up converter to convert the low-voltage source to the application with the necessary high output voltage (such as the dc bus of the microgrid, the high-voltage dc load, the dc input of the inverter, etc.) effectively to improve the utilization of the green energy. To achieve the requirement of high power density and possible application of high-voltage load environment, if the conventional boost converter is used, the high voltage gain may not be obtained or the converter may be operated at the extreme duty cycle to make the components sustain the high voltage stress and to increase the conversion loss of the circuit.

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To improve the operation of high duty cycle and to achieve the high voltage gain, many single-switch high step-up converters uniting the switching capacitor topology [6]–[8], switching inductor topology [9]–[11], voltage lift technique [12], [13], coupled inductor [14]–[17], and hybrid methods [18]–[22] have been proposed. Although they can achieve the high voltage gain, their input ripples are larger when they are operated in the high wattage load to increase the conduction loss. The performance is sacrificed. The conventional interleaved boost converter can be operated in the high output power; however, its voltage gain is limited. To solve this problem, many interleaved step-up converters combine the voltage-double module topology to increase the voltage gain. The topology is simple, but it needs more components when the circuit is needed to be extended to increase the circuit cost [23]–[26]. Other circuits utilize the coupled inductor to achieve the high voltage gain by adjusting the turn ratio of the coupled inductor even when the circuit is not operated at the high duty cycle [27]–[30]. Some present researches mix the voltage lift, switching capacitor, switching inductor, series connection, cascade connection methods with the interleaved converter to step up the voltage gain. The common hybrid topologies use the voltage-double module to accompany the coupled inductor. They own the high voltage gain and have the lower voltage stress [31]–[35].

This paper proposes a new interleaved high step-up converter. This new high step-up converter utilizes the interleaved converter to combine the voltage-double module with the coupled inductor. The secondary sides of the coupled inductors charge the two voltage-double modules interleavedly and then are in series connection with the input voltage and primary sides of the coupled inductors to charge the output side to achieve the effect of high voltage gain. In this proposed topology, the turn ratio can also be adjusted to further reduce the operating duty cycle and decrease the voltage stress of the switch.

II. New Interleaved Series High Step-Up Converter

The proposed new high step-up converter is shown in Fig. 1. It consists of two switches, four diodes, four capacitors, and two coupled inductors. The circuit can be divided into two blocks. The blue block is the conventional interleaved converter and the red block is the interleaved voltage-double modules. The secondary sides of the coupled inductors belong to the interleaved series type and the two voltage-double modules share the secondary-side inductors together. After having the interleavedly stored energy of the voltage-double modules, the

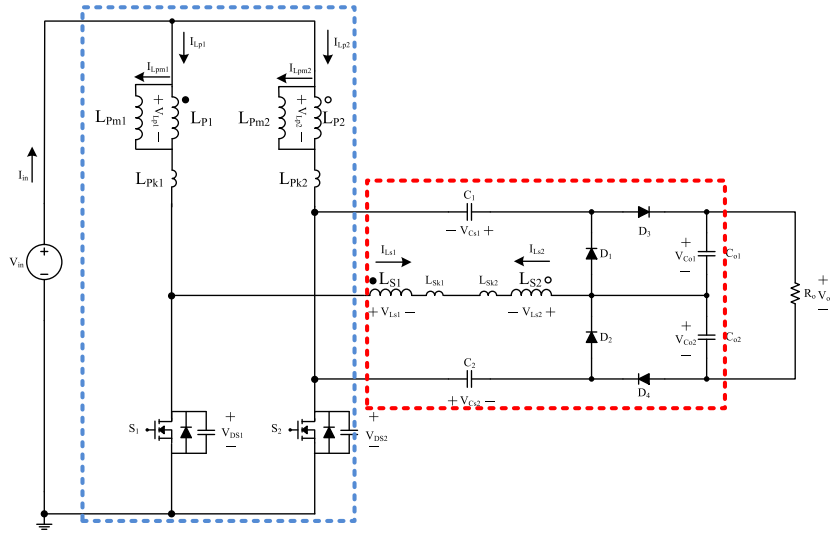

Fig. 1. Proposed new interleaved series-type high step-up converter.

capacitor modules are in series with the input voltage, the primary-side inductors, and the secondary-side inductors to charge the output capacitor and the load.

A. Analysis of the Operating Modes

The operating principles of the proposed high step-up converter will be described in this section. There are eight operating modes in one complete switching period. Fig. 2 shows the important operating waveforms. When this circuit is operated in DCM or when the operating duty cycle is smaller than 0.5, the inductor does not have enough energy to be transferred to the output side. The voltage gain then cannot reach the high value as that operating in CCM or operating at duty cycle being greater than 0.5. The proposed circuit is therefore operated in CCM and its duty cycle is greater than 0.5. To simplify the circuit analysis, some assumptions are first made here as follows.

1) All switching components are ideal; that is, the ESRs of the capacitor and the inductor, the conduction drops of the diodes, and the conduction resistance of the switches are neglected.
2) N_1 and N_2 are the turn ratios of the coupled inductors. Where $N_1 = \frac{n_{s1}}{n_{p1}}$ and $N_2 = \frac{n_{s2}}{n_{p2}}$.
3) The magnetizing and leakage inductances are the same for the two coupled inductors L_1 and L_2. That is, $L_{Pm1} = L_{Pm2} = L_{Pm}$ and $L_{Pk1} = L_{Pk2} = L_{Pk}$. The leakage inductances are smaller than the magnetizing inductances.
4) The mutual inductances of the coupled inductors L_1 and L_2 are $M_1 = k_1 \cdot \sqrt{L_{Pm1} \cdot L_{S1}}$ and $M_2 = k_2 \cdot \sqrt{L_{Pm2} \cdot L_{S2}}$, respectively. Where k_1 and k_2 are the coupling coefficients and are equal to $\frac{L_{pm1}}{L_{pm1}+L_{pk1}}$ and $\frac{L_{pm2}}{L_{pm2}+L_{pk2}}$, respectively.
5) The voltage-double capacitors and output capacitors are large enough so that the voltages across them can be considered to be constant.

Mode 1 $[t_0 - t_1]$: At $t = t_0$, S_1 is turned ON. This mode belongs to the transient interval. The leakage inductance energy of

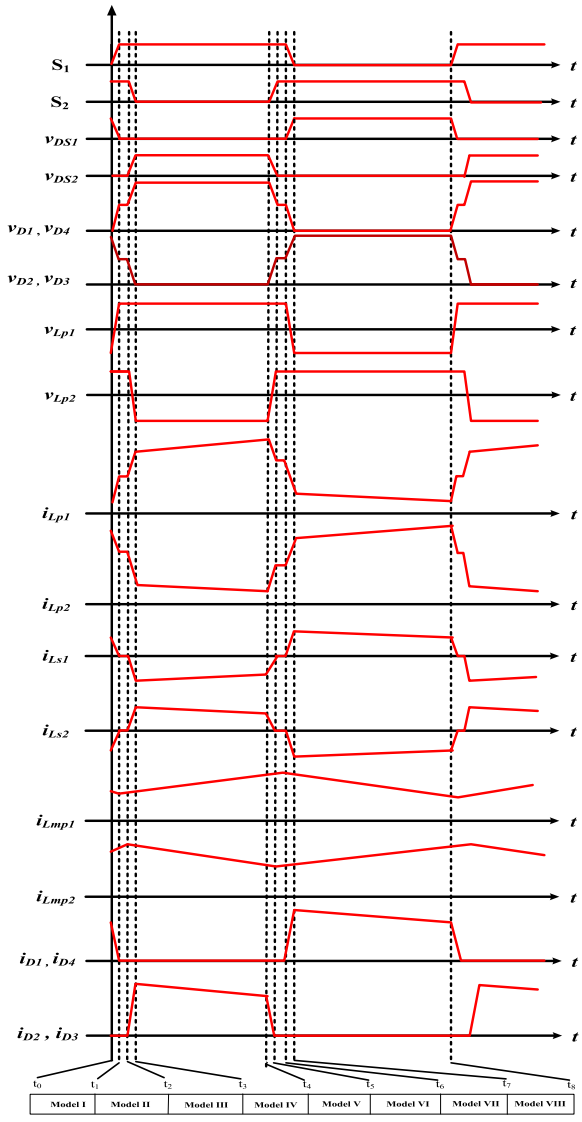

Fig. 2. Related operating waveforms of the proposed interleaved series-type high step-up converter.

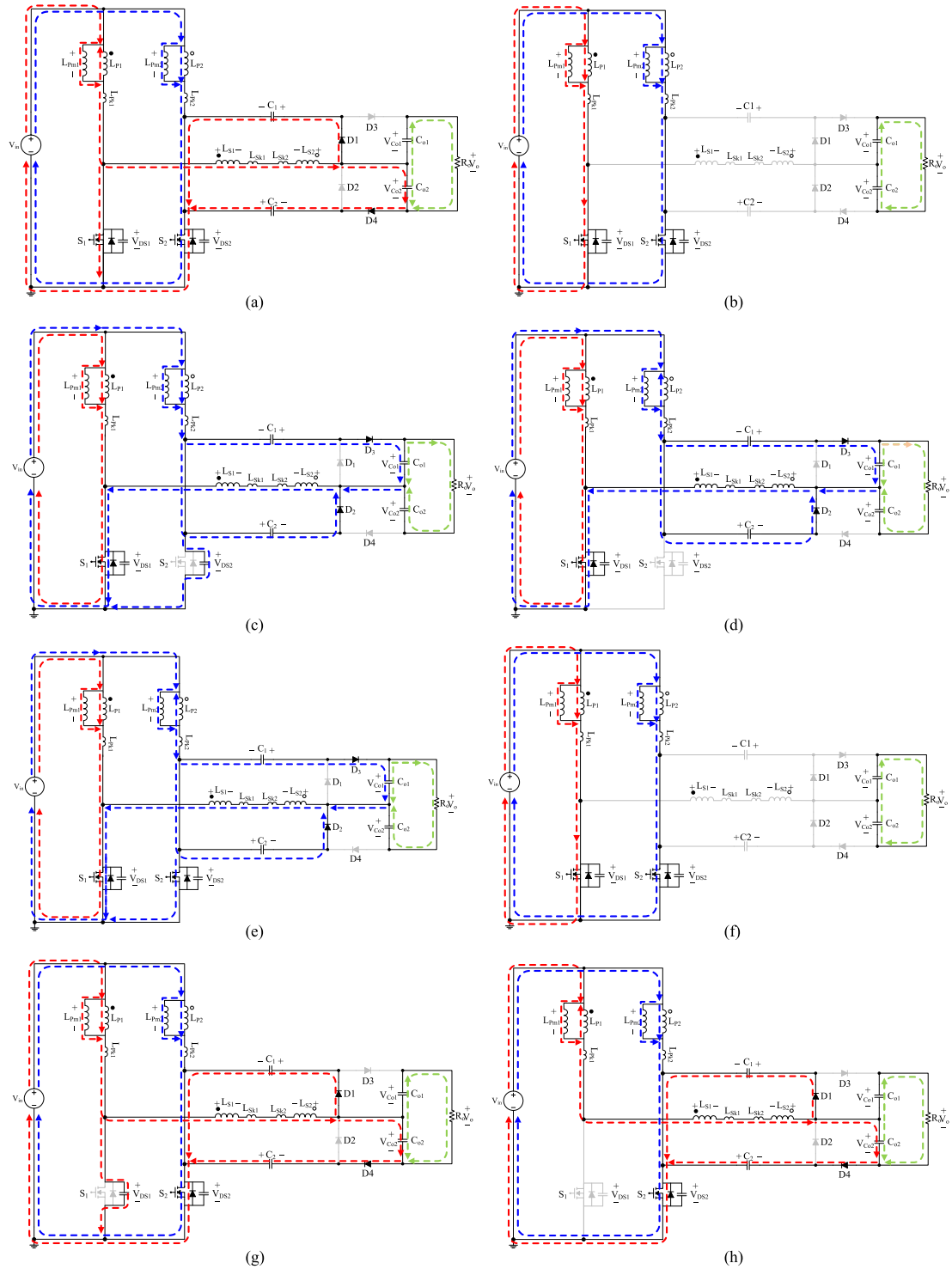

Fig. 3. Various operating modes of the proposed circuit during one switching cycle.

the secondary-side of the coupled inductor is not released completely; therefore, the diodes D_1 and D_4 are still in conduction. The current in the leakage inductance maintain the direction of the above mode as shown in the red line of Fig. 3(a). The switch S_2 is still in conduction like that shown in blue line. This mode ends when the leakage inductance energy of the secondary side is released completely at $t = t_1$.

Mode 2 $[t_1 - t_2]$: At this mode, the inductor L_{pm1} begins to store the energy (red line) and the inductor L_{Pm2} continues to store the energy (blue line). Both currents are increased linearly

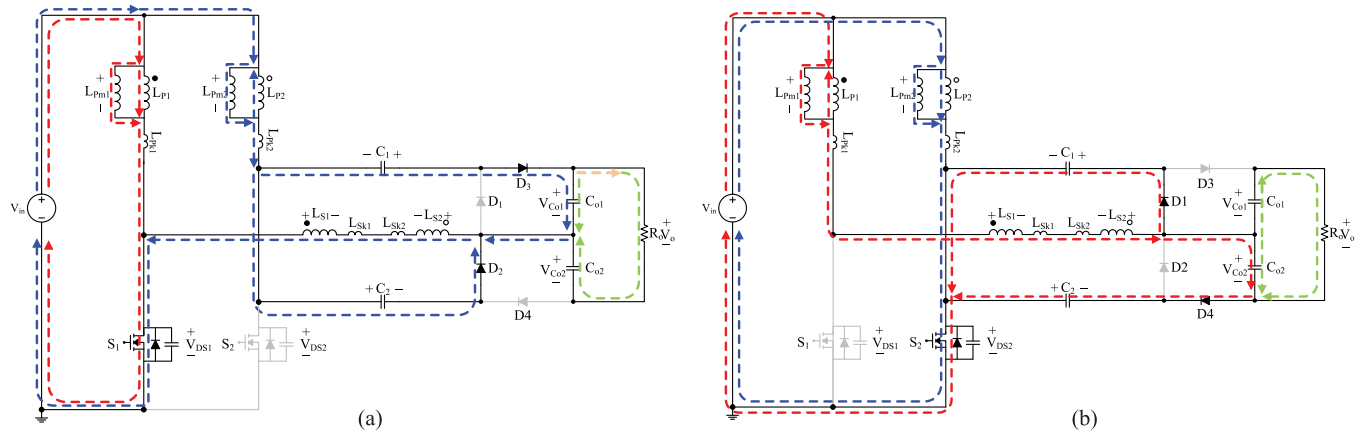

Fig. 4. Simplified modes of the proposed circuit for steady-state analysis.

and their across voltages are both equal to V_{in}. At the same time, the output capacitors release the energy to the load as shown in Fig. 3(b). This mode ends when the switch S_2 is turned OFF at $t = t_2$.

Mode 3 $[t_2 - t_3]$: When $t = t_2$, the switch S_2 is turned OFF. The coupled inductor L_{Pm2} begins to release the energy and the diodes D_2 and D_3 begin to conduct as shown in the blue line of Fig. 3(c). The inductor L_{Pm1} continues to store the energy (red line). This mode is also a transient interval. When the switch current i_{S2} is down to zero at $t = t_3$, this mode ends.

Mode 4 $[t_3 - t_4]$: When $t = t_3$, the switch S_2 is in the OFF state. The diodes D_2 and D_3 are still in the conduction state. The coupled inductor L_{Pm2} has two energy-released paths as shown in the blue line of Fig. 3(d). One path is through the diode D_2 with the input voltage V_{in} and the secondary-side of the coupled inductor to charge the voltage-double capacitor C_2. The other path is through the diode D_3 with the input voltage, voltage-double capacitor C_1, and secondary-side of the coupled inductor to charge the output capacitor C_{o1}. The coupled inductor L_{Pm1} still stores the energy (red line). This mode ends when the switch S_2 is turned ON at $t = t_4$.

Because the topology and driving signals of the proposed circuit are all in the symmetrical type, the analyses of mode 5 to mode 8 are similar to those of mode 1 to mode 4. Therefore, the related analyses about mode 5 to mode 8 are omitted here.

III. Derivation of the Related Formula

The results of the above mode analyses are used to derive the related formula. Because the topology and driving signals of the proposed circuit have the symmetrical characteristics and the time of the transient intervals is much shorter than the switching period, the formula derivation of the steady-state analysis when the proposed circuit is operated in the CCM can be simplified to only consider the two modes as shown in Figs. 4(a) and (b).

From Fig. 4(a), the coupled inductor L_{Pm1} stores the energy and the coupled inductor L_{Pm2} releases the energy. Then, (1)–(4) can be derived

$$V^{\text{I}}_{Lpm1} = k_a \cdot V_{\text{in}} \tag{1}$$

$$V_{\text{in}} - \frac{V^{\text{II}}_{Lpm2}}{k_b} - V_{c2} - N_2 \cdot V^{\text{II}}_{Lpm2} + N_1 \cdot V^{\text{I}}_{Lpm1} = 0 \tag{2}$$

$$V_{co1} = V_{\text{in}} - \left(\frac{1 + N_2 \cdot k_b}{k_b}\right) \cdot V^{\text{II}}_{Lpm2} + V_{c1} + N_1 \cdot V^{\text{I}}_{Lpm1} \tag{3}$$

$$V_o = V_{co1} + V_{co2} \tag{4}$$

where $k_a \cong \frac{2k_1}{k_1+1}$ and $k_b \cong \frac{2k_2}{k_2+1}$.

Substituting (1) into (2), the voltage across the L_{pm2} can be derived as

$$V^{\text{II}}_{Lpm2} = \frac{k_b \cdot (V_{\text{in}} + N_1 \cdot k_a \cdot V_{\text{in}} - V_{c2})}{1 + N_2 \cdot k_b}. \tag{5}$$

From Fig. 4(b), the coupled inductor L_{Pm2} stores the energy and the coupled inductor L_{Pm1} releases the energy. Then, (6) can be obtained

$$V^{\text{I}}_{Lpm2} = k_b \cdot V_{\text{in}}. \tag{6}$$

According to the principle of flux balance for L_{pm2}, the following equation can be obtained:

$$\int_0^{DT} V^{\text{I}}_{Lpm2}\, dt + \int_{DT}^{T} V^{\text{II}}_{Lpm2} dt = 0. \tag{7}$$

Substituting (5) and (6) into (7), the voltage across the capacitor C_2 can be achieved as (8). Due to the symmetrical structure of the circuit, the values of V_{C1} and V_{C2} are the same

$$V_{C1} = V_{C2} = V_{\text{in}} \left[\frac{(1 + N_2 \cdot k_b) \cdot D}{1 - D} + (1 + N_1 \cdot k_a)\right]. \tag{8}$$

If the turn ratios N_1 and N_2 are equal and the values are both equal to N, the coupling coefficients k_1 and k_2 are also the same

and equal to k, then (8) can be rewritten as

$$V_{C1} = V_{C2} = \frac{V_{\text{in}} \cdot (1 + N \cdot k_a)}{1 - D}. \tag{9}$$

Substituting (1), (5), and (8) into (3), the voltage of the output capacitor V_{Co1} can be derived as (10). Because of the symmetrical topology, the voltages across the output capacitors C_{o1} and C_{o2} are the same

$$V_{co1} = V_{co2} = 2 \cdot V_{\text{in}} \left[\frac{(1 + N_2 \cdot k_b) \cdot D}{1 - D} + (1 + N_1 \cdot k_a) \right]. \tag{10}$$

If $N_1 = N_2 = N$ and $k_1 = k_2 = k$, then (10) can be rewritten as

$$V_{co1} = V_{co2} = \frac{2 \cdot V_{\text{in}} \cdot (1 + N \cdot k_a)}{1 - D}. \tag{11}$$

Substituting (10) into (4), then the voltage gain equation can be obtained

$$\frac{V_o}{V_{\text{in}}} = 4 \cdot \left[\frac{(1 + N_2 \cdot k_b) \cdot D}{1 - D} + (1 + N_1 \cdot k_a) \right]. \tag{12}$$

Therefore, (13) can be achieved if $N_1 = N_2 = N$ and $k_1 = k_2 = k$

$$\frac{V_o}{V_{\text{in}}} = \frac{4 \cdot (1 + N \cdot k_a)}{1 - D}. \tag{13}$$

When k=1, (13) can be changed to

$$\frac{V_o}{V_{\text{in}}} = \frac{4 \cdot (1 + N)}{1 - D}. \tag{14}$$

According to the above results, the voltage stresses of S_1, S_2, D_1, D_2, D_3, and D_4 can be derived as the following equations:

$$V_{S1} = V_{S2} = \frac{V_{\text{in}}}{1 - D} = \frac{V_o}{4 \cdot (1 + N)} \tag{15}$$

$$V_{D1} = V_{D2} = V_{D3} = V_{D4} = \frac{V_o}{2}. \tag{16}$$

From (15) and (16), the voltage stresses of the switches S_1 and S_2 can be reduced by adjusting the turn ratio N. As for the voltage stresses of the diodes D_1, D_2, D_3, and D_4, they are all equal to one-half of the output voltage.

Fig. 5 shows the voltage gain curves of the proposed circuit under different coupling coefficients. From the results of this figure, one can see the affection on the voltage gains of different coupling coefficients is not obvious.

Fig. 6 shows the voltage gain comparisons of the proposed circuit with [31], [32], [35], and [20] under the situation of k=1 and N=2. According to the results, the voltage gain of the proposed circuit is higher than those of the other topologies.

Comparisons of the proposed topology with the other topologies are shown in Table I. The related characteristics can be understood. From Table I, one can see the proposed circuit owns the performances of the highest voltage gain, the lowest voltage stress of the switches, the voltage stresses of the diodes being one-half of the output voltage, and the lowest number of the components (interleaved topology).

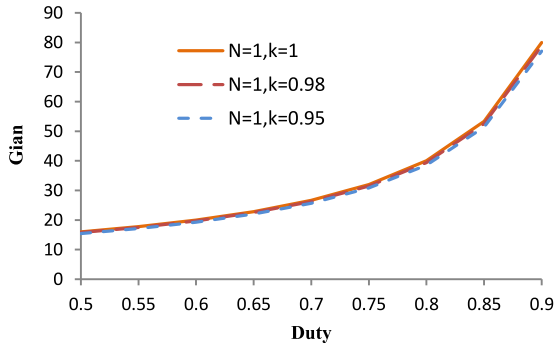

Fig. 5. Relationship between voltage gain (V_o/V_{in}) and duty cycle of the proposed circuit under different coupling coefficient k.

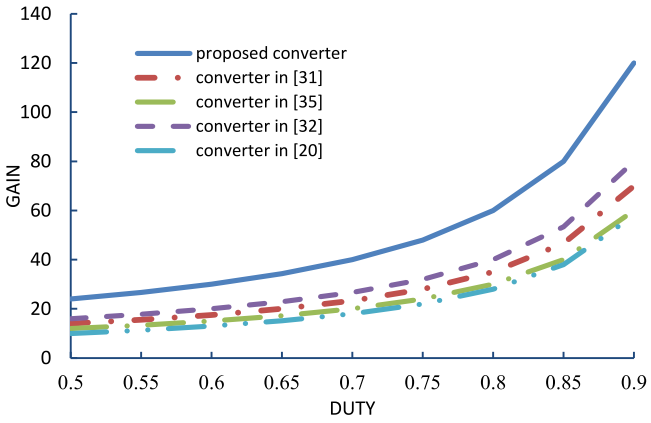

Fig. 6. Voltage gain comparisons of the proposed circuit with [31], [32], [35], and [20].

IV. Component Design and Efficiency Estimation

To realize the new interleaved series-type high step-up converter, the designs of the related components are discussed here. The related design specification is listed in Table II.

A. Component Design

1) Design of Inductors L_1 and L_2: To design the needed inductor values, the efficiency η of the converter is assumed to be 0.9. By using (17) and (18), the average values of the input current and the inductor current can be obtained

$$I_{\text{in(avg)}} = \frac{P_o}{V_{\text{in}} \cdot \eta} = \frac{400}{24 \cdot 0.9} = 18.52 \text{ A} \tag{17}$$

$$I_{Lp1(\text{avg})} = I_{Lp2(\text{avg})} = \frac{I_{\text{in(avg)}}}{2} = \frac{18.52}{2} = 9.26 \text{ A}. \tag{18}$$

To make the characteristic of the circuit meet the above analyses, the proposed circuit needs to be operated in CCM. Then, the current variation of the inductor can be designed to satisfy

TABLE I
PERFORMANCE COMPARISON OF THE PROPOSED CIRCUIT WITH [31], [32], [35], AND [20]

	[31]	[32]	[35]	[20]	The proposed topology
Voltage gain	$\frac{3N+1}{1-D}$	$\frac{4N}{1-D}$	$\frac{2N+2}{1-D}$	$\frac{2+N+ND}{1-D}$	$\frac{4N+4}{1-D}$
Voltage stress	$\frac{V_o}{3N+1}$	$\frac{V_o}{4N}$	$\frac{V_o}{2N+1}$	$\frac{V_o+NV_i}{2N+2}$	$\frac{V_o}{4N+4}$
Highest voltage stress of diode	$\frac{2NV_o}{3N+1}$	$\frac{V_o}{2}$	$\frac{NV_o}{N+1}$	$\frac{V_o+NV_i}{2}$	$\frac{V_o}{2}$
Number of switch	2	4	2	1	2
Number of diode	8	4	6	4	4
Number of capacitor	7	6	5	4	4

TABLE II
SPECIFICATIONS OF THE PROPOSED CIRCUIT

Parameters	Symbol	Type/Value
Input voltage	V_{in}	24 V
Output voltage	V_o	400 V
Maximum output current	I_o	1 A
Maximum output power	P_o	400 W
Switching frequency	f_S	60 kHz
Duty cycle of the switch	D	0.52
Main switches	S_1, S_2	IRFP4668PBE
Diodes	D_1, D_2, D_3, D_4	MBR40250TG
Core of the coupled inductor	*MPP Core*	CM400125
Magnetizing inductors of the coupled inductors	L_{P1}, L_{P2}	99.1 μH, 100.5 μH
Leakage inductances of the coupled inductors	L_{k1}, L_{k2}	1.486 μH, 1.4 μH
Turn ratios of the coupled inductors	N_1, N_2	1
Coupling coefficients	k_1, k_2	0.98
Voltage-double capacitors	C_1, C_2	5 μF
Output capacitors	C_{o1}, C_{o2}	220 μF

this condition

$$V_L = L \cdot \frac{di_L}{dt} \tag{19}$$

$$\Delta i_L = \frac{D \cdot V_L}{L_m \cdot f_s} \tag{20}$$

$$L_m \geq \frac{D \cdot V_L}{\Delta i_L \cdot f_s}. \tag{21}$$

Here, the current ripple of the inductor γ is assumed to be 30%, then

$$\Delta i_L = I_{Lp(\text{avg})} \cdot r = 2.778 \text{ A} \tag{22}$$

$$L_{Pm1} = L_{Pm2} \geq \frac{0.52 \cdot 24}{2.778 \cdot 60 \cdot 10^3} = 74.87 \ \mu\text{H}. \tag{23}$$

In the prototype circuit, to make the circuit operated in CCM, the real value used in the experiment is about 1.2–1.5 times of the calculated value. Therefore, the real primary-side inductances of the coupled inductors are 99.1 and 100.5 μH.

2) Design of the Switches S_1 and S_2: According to the parameters listed in Table II and (14), the duty cycle of the switch can be calculated to be 0.52. Then, the voltage stresses of the switches can be derived as

$$V_{S1} = V_{S2} = \frac{V_{\text{in}}}{1 - D} = \frac{24}{1 - 0.52} = 50 \text{ V}. \tag{24}$$

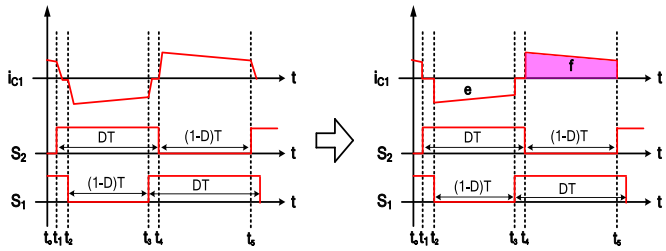

Fig. 7. Simplified current chart for the current estimation of the voltage-double capacitor.

To consider the voltage spike induced from the switching, the rating of the switch can be chosen to be larger than the designed value.

3) Design of the Diodes D_1, D_2, D_3, and D_4: The voltage across each diode is one-half of the output voltage. So

$$V_{D1} = V_{D2} = V_{D3} = V_{D4} = \frac{V_o}{2} = \frac{400}{2} = 200 \text{ V}. \tag{25}$$

Having the same reason with that of the switches, the rating of the diode is also chosen to be 1.2-1.5 times larger than the calculated value.

4) Design of the Capacitors C_1, C_2, C_{o1}, and C_{o2}: The values of voltage-double capacitors C_1, C_2 and output capacitors C_{o1}, C_{o2} can be estimated from (26)–(30). However, in the realization, the larger capacitor will make the circuit volume increased. To make the circuit volume decreased and not to increase the ripple of the capacitor too much, the ripple of the voltage-double capacitor is designed to be below 4%. As for the output capacitors, their ripples are assumed to be below 1%.

According to the capacitor equation during the discharging interval, the needed capacitor value can be obtained

$$C \cdot \frac{dv}{dt} = i_c. \tag{26}$$

a) Voltage-double capacitors C_1 and C_2: From section f of Fig. 7, one can know that the maximum current value flowing through the voltage-double capacitor is like that shown in (27). The minimum current value flowing through the voltage-double capacitor is like that shown in (28). The time interval of section f is (1-*D*)*T*. So, (26) can become (29) and (30) can be used to

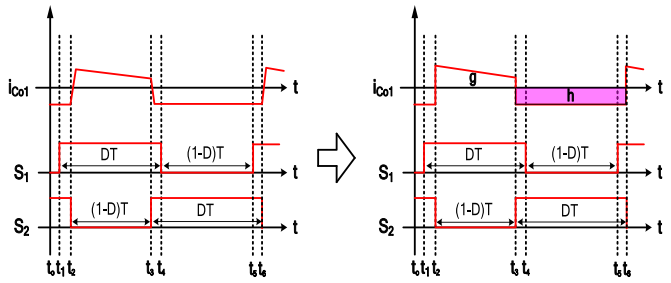

Fig. 8. Simplified current chart for the current estimation of the output capacitor.

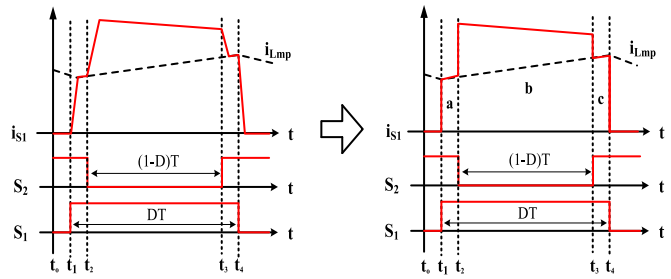

Fig. 9. Simplified current chart for the conduction-loss estimation of the switch.

obtain the values of the voltage-double capacitors

$$I_{f,\text{high}} = \frac{1}{4}\cdot\left(i_{L(\text{avg})} + \frac{\Delta i_L}{2}\right) = 2.663\ \text{A} \tag{27}$$

$$I_{f,\text{low}} = \frac{1}{4}\cdot\left(i_{L(\text{avg})} - \frac{\Delta i_L}{2}\right) = 1.968\ \text{A} \tag{28}$$

$$\Delta V_c = \frac{(I_{f,\text{high}} + I_{f,\text{low}})\cdot(1\ -\ D)\cdot T}{2\cdot C} \tag{29}$$

$$\begin{aligned} C_1 = C_2 &\geqq \frac{(2.663+1.968)\cdot(1-0.52)\cdot 16.67\cdot 10^{-6}}{2\cdot 100\cdot 0.04} \\ &= 4.632\ \mu\text{F}. \end{aligned} \tag{30}$$

In the real implementation, the voltage-double capacitors are chosen to be 5 uF/250 V.

b) Output capacitors C_{o1} and C_{o2}: During the section h of Fig. 8, the current flowing through the output capacitor can be known to be I_o. The time duration of section h is *DT*, so (26) can become (31). Then the values of the output capacitors can be derived from (32)

$$\Delta V_c = \frac{I_o\cdot D\cdot T}{C} \tag{31}$$

$$\begin{aligned} C_{o1} = C_{o2} &\geqq \frac{1\cdot 0.52\cdot 16.67\cdot 10^{-6}}{200\cdot 0.01} \\ &= 4.334\ \mu\text{F}. \end{aligned} \tag{32}$$

In the real implementation, when the ESR effects of the output capacitors are considered, their values are chosen to be 220 μF/250 V to reduce the possible output ripple due to the ESR.

B. Efficiency Estimation

1) Switch Loss:

a) Conduction loss: To simplify the calculation process, the real waveform of the switch current is divided and simplified to be three parts— a, b, and c as shown in Fig. 9. From Fig. 9, the time interval of each section can be known as: $[t_1 - t_2]$ of section $a = [t_3 - t_4]$ of section c $=(D-\frac{1}{2})\cdot T$, $[t_2 - t_3]$ of section b $= (1\ -\ D)\cdot T$.

Section a: From Fig. 9, one can know the lowest current in section a is the average inductor current minus one-half of the current ripple and the highest current is the lowest current plus the current variation amount during this interval. Then, the rms value during this interval can be derived as

$$I_{a,\text{low}} = i_{L(\text{avg})} - \frac{\Delta i_L}{2} = 7.871\ \text{A} \tag{33}$$

$$I_{a,\text{high}} = I_{a,\text{low}} + \frac{V_{\text{in}}}{L}\cdot\left(D-\frac{1}{2}\right)\cdot T = 7.952\ \text{A} \tag{34}$$

$$\begin{aligned} I_{a,\text{rms}} &= \sqrt{\frac{0.02\cdot\left(7.871^2 + 7.871\cdot 7.952 + 7.952^2\right)}{3}} \\ &= 1.119\ \text{A}. \end{aligned} \tag{35}$$

Section c: The highest current in setion c can be known to be the average inductor current plus one-half of the ripple current from Fig. 9. As for the lowest current in this section, it is the highest current value minus the current variation amount during this interval

$$I_{c,\text{high}} = i_{L(\text{avg})} + \frac{\Delta i_L}{2} = 10.649\ \text{A} \tag{36}$$

$$\begin{aligned} I_{c,\text{low}} &= I_{c,\text{high}} - \frac{V_{\text{in}}}{L}\cdot\left(D-\frac{1}{2}\right)\cdot T \\ &= 10.568\ \text{A} \end{aligned} \tag{37}$$

$$\begin{aligned} I_{c,\text{rms}} &= \sqrt{\frac{0.02\cdot\left(10.649^2 + 10.649\cdot 10.568 + 10.568^2\right)}{3}} \\ &= 1.5\ \text{A}. \end{aligned} \tag{38}$$

Section b: From Fig. 9, the highest point of section b can be known to be the interleaved current plus the circulating current. Because the decreased amount of the circulating current of one coupled inductor is equal to the increased amount of the other one, the highest value can be approximated as the highest value in section a plus the highest value in section c. The lowest value is the lowest value in section c plus the lowest value in section

a. Then, the rms value in this section can be achieved as

$$I_{b,\text{high}} = I_{a,\text{high}} + I_{c,\text{high}} = 18.601\ \text{A} \tag{39}$$

$$I_{b,\text{low}} = I_{a,\text{low}} + I_{c,\text{low}} = 18.439\ \text{A} \tag{40}$$

$$I_{b,\text{rms}} = \sqrt{\frac{0.48 \cdot \left(18.601^2 + 18.601 \cdot 18.439 + 18.439^2\right)}{3}} = 12.831\ \text{A}. \tag{41}$$

RMS value of the switch current $i_{S,\text{rms}}$

$$I_{S,\text{rms}} = \sqrt{{I_{a,\text{rms}}}^2 + {I_{b,\text{rms}}}^2 + {I_{c,\text{rms}}}^2} = 12.967\ \text{A}. \tag{42}$$

Conduction loss of the switch $P_{S(\text{cond})}$.

Due to the symmetrical topology and control, so $i_{S1,\text{rms}} = i_{S2,\text{rms}} = i_{S,\text{rms}}$. Then, the conduction loss can be estimated as

$$P_{s(\text{cond})} = P_{s1(\text{cond})} + P_{s2(\text{cond})} = 2 \cdot ({I_{s,\text{rms}}}^2 \cdot R_{ds(\text{on})}) = 3.262\ \text{W}. \tag{43}$$

b) Switching loss of the switch: Because $P_{\text{SW1}} = P_{\text{SW2}}$, the switching loss of the switch can be estimated as follows.

$$P_{\text{SW}} = P_{\text{SW1}} + P_{\text{SW2}} = 2 \cdot \left(\frac{1}{2} \cdot V_{ds} \cdot I_{S,\text{peak}} \cdot (t_{\text{on}} + t_{\text{off}}) \cdot f\right) = 9.989\ \text{W} \tag{44}$$

where t_{on} is the rising time of the switch during the switching and t_{off} is the falling time of the switch during the switching.

Because the rms calculation methods of the other components are all similar to the above descriptions, so their derivations are omitted here.

2) Conduction Loss of the Diode $\boldsymbol{P_{D(\text{cond})}}$*:* Because the average current in the capacitor is equal to zero, the average currents flowing through all diodes during their conduction state are equal to the output current. Also because the topology and control of the proposed circuit are symmetrical, $i_{d1,\text{rms}} = i_{d2,\text{rms}} = i_{d3,\text{rms}} = i_{d4,rms} = i_{d,\text{rms}}$. The conduction loss of the diode can then be judged as follows:

$$P_{D(\text{cond})} = P_{D1(\text{cond})} + P_{D2(\text{cond})} + P_{D3(\text{cond})} + P_{D4(\text{cond})} = 4 \cdot \left(V_f \cdot I_{d,\text{avg}} + {I_{d,\text{rms}}}^2 \cdot R_{d(\text{on})}\right) = 5.752\ \text{W} \tag{45}$$

where V_f is the conduction voltage drop of the diode and $R_{d(\text{on})}$ is the conduction resistance of the diode.

3) Capacitor Losses:

a) Loss of the voltage-double capacitor $\boldsymbol{P_C}$*:* Because $i_{C1,\text{rms}} = i_{C2,\text{rms}} = i_{C,\text{rms}}$, the loss of the voltage-double capacitor can be determined as follows:

$$P_C = P_{C1} + P_{C2} = 2 \cdot \left({I_{C,\text{rms}}}^2 \cdot R_C\right) = 2.592\ \text{W}. \tag{46}$$

b) Loss of the output capacitor $\boldsymbol{P_{CO}}$*:* Also because of the symmetry, $i_{CO1,\text{rms}} = i_{CO2,\text{rms}} = i_{CO,\text{rms}}$, then

$$P_{Co} = P_{\text{CO1}} + P_{\text{CO2}} = 2 \cdot \left({I_{\text{CO,rms}}}^2 \cdot R_{\text{CO}}\right) = 0.686\ \text{W}. \tag{47}$$

4) Inductor Losses:

a) Primary-side losses of the inductors $\boldsymbol{P_{LP}}$*:* Due to the symmetrical topology and control of the proposed circuit ($i_{Lp1,\text{rms}} = i_{Lp2,\text{rms}} = i_{Lp,\text{rms}}$), the following equation can

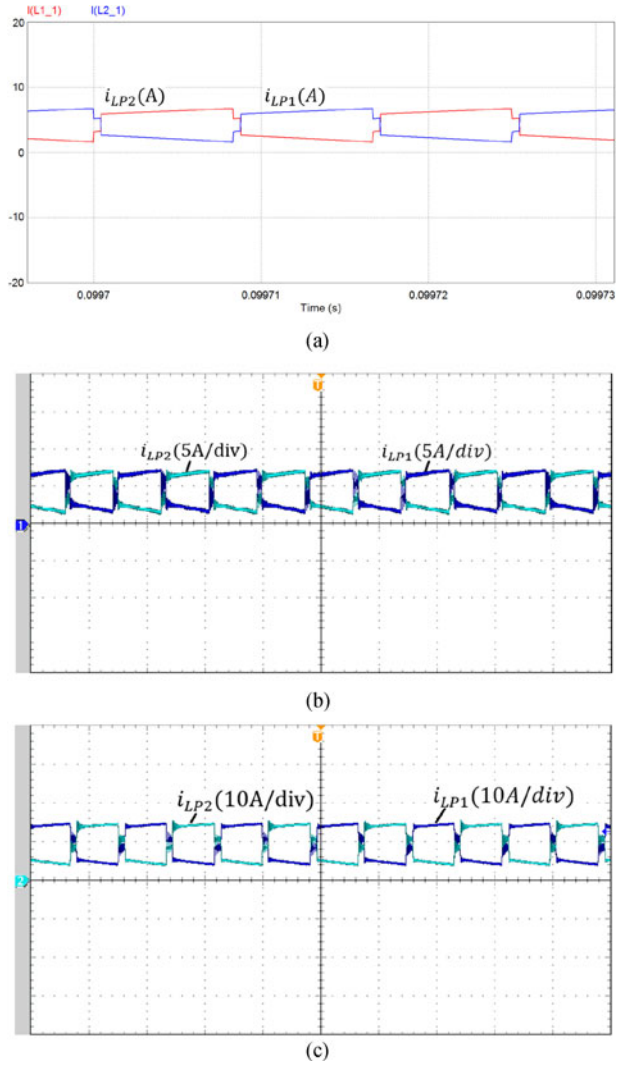

Fig. 10. Waveforms of the inductor current i_{LP1} and i_{LP2}. (a) Simulation. (b) Experiment-half load (10μs/div). (c) Experiment-full load (10 μs/div).

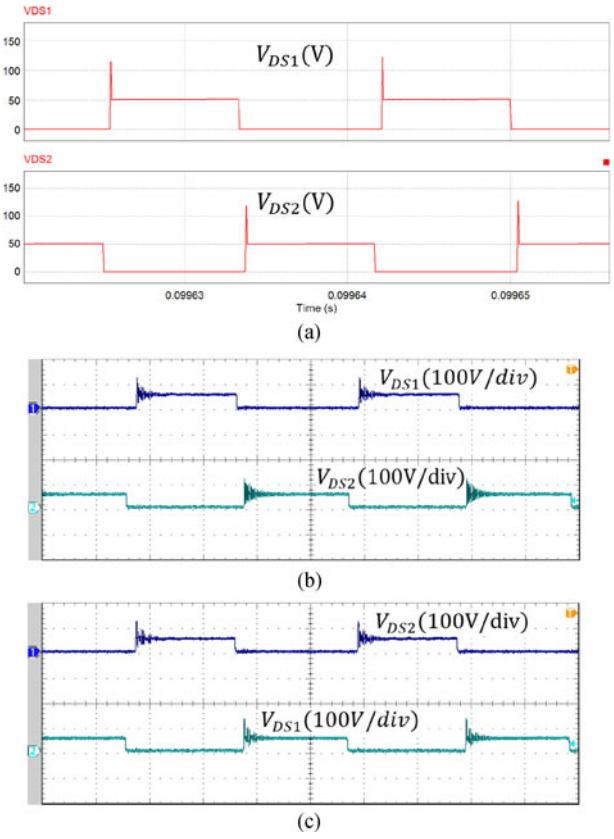

Fig. 11. Waveforms of the voltages across the switches S_1 and S_2. (a) Simulation. (b) Experiment-half load (4μs/div). (c) Experiment-full load (4μs/div).

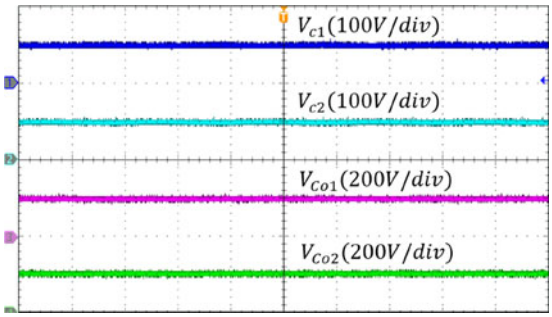

Fig. 12. Experimental waveforms of the capacitor voltages V_{C1}, V_{C2}, V_{Co1} and V_{Co2} (8 μs/div).

obtain the primary-side losses of the inductors:

$$\begin{aligned} P_{Lp} &= P_{Lp1} + P_{Lp2} \\ &= 2 \cdot \left({I_{Lp,\mathrm{rms}}}^2 \cdot R_{Lp} \right) \\ &= 1.782 \text{ W} \end{aligned} \tag{48}$$

where R_{LP} is the primary-side resistance of the inductor.

b) Secondary-side losses of the inductors P_{Ls}: Because the circuit topology and control are symmetrical, so $i_{Ls1,\mathrm{rms}} = i_{Ls2,\mathrm{rms}} = i_{Ls,rms}$. Then, the secondary-side losses of the

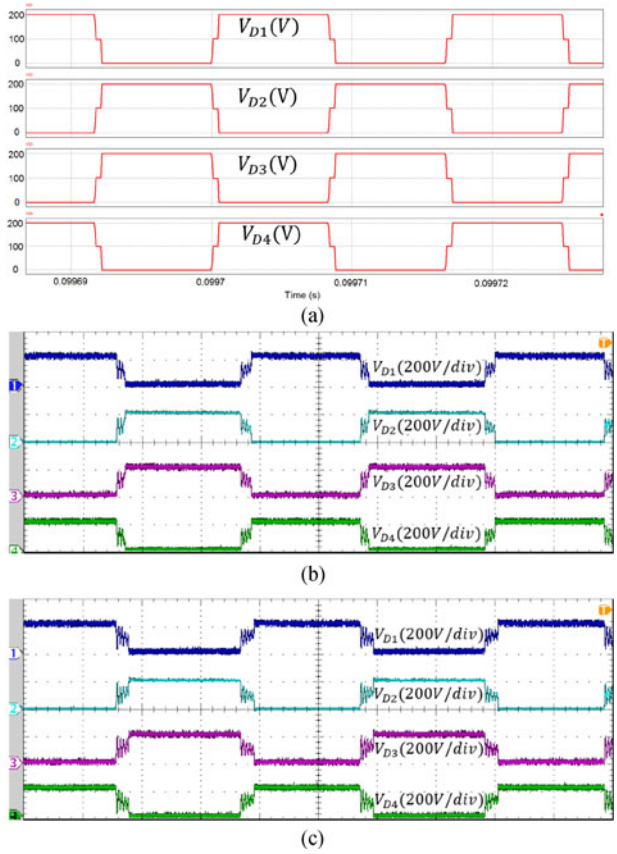

Fig. 13. Waveforms of the voltages across the diodes D_1, D_2, D_3, and D_4. (a) Simulation. (b) Experiment-half load (4 μs/div). (c) Experiment-full load (4 μs/div).

inductors are

$$\begin{aligned} P_{Ls} &= P_{Ls1} + P_{Ls2} \\ &= 2 \cdot \left({I_{Ls,\mathrm{rms}}}^2 \cdot R_{Ls} \right) \\ &= 0.347 \text{ W} \end{aligned} \tag{49}$$

where R_{LS} is the secondary-side resistance of the inductor.

5) Efficiency at Full Load: According to the above estimation of all losses, the efficiency of the proposed converter at full-load can be estimated as follows:

$$\begin{aligned} \eta &= \frac{P_o}{P_o + P_{Ls} + P_{Lp} + P_{Co} + P_C + P_{D(\mathrm{cond})} + P_{\mathrm{SW}} + P_{S(\mathrm{cond})}} \\ &= \frac{400}{400 + 0.347 + 1.782 + 0.686 + 2.592 + 5.752 + 9.989 + 3.262} \\ &= 0.942. \end{aligned} \tag{50}$$

V. Simulation and Experimental Results

A 400 W high step-up converter is presented. To verify the exactness of the theoretical analysis, the circuit simulation software PSIM will be used to simulate the circuit and the

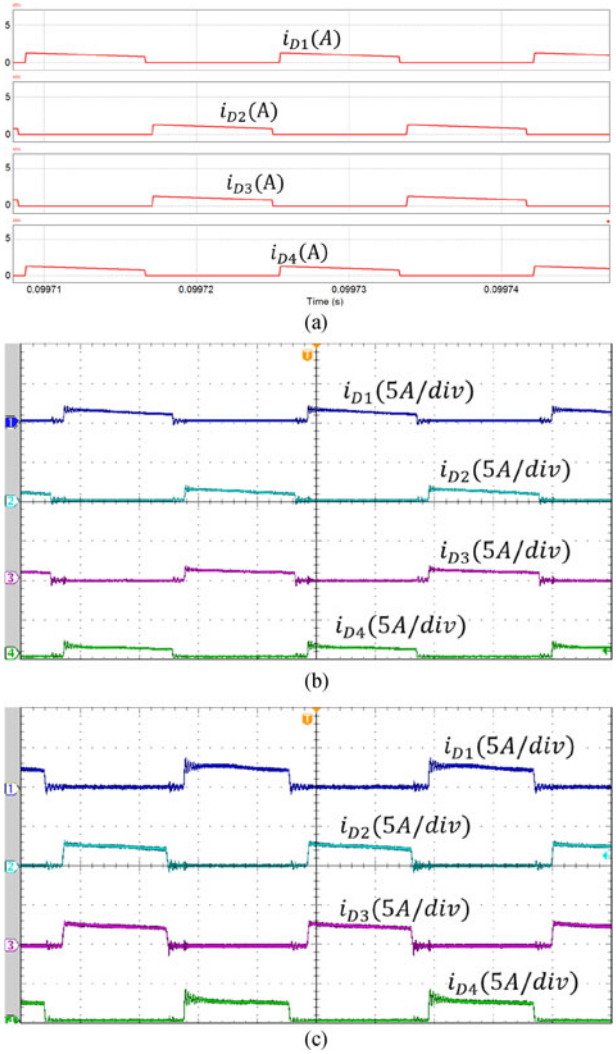

Fig. 14. Waveforms of the diode current i_{D1}, i_{D2}, i_{D3}, and i_{D4}. (a) Simulation. (b) Experiment-half load (4 μs/div). (c) Experiment-full load (4 μs/div).

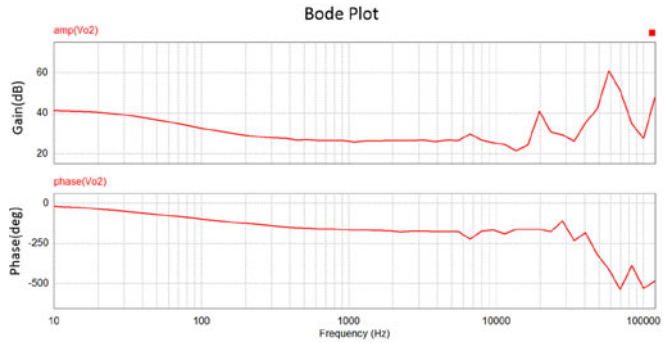

Fig. 15. Bod plot of the $\hat{v}_o/\hat{v}_c$.

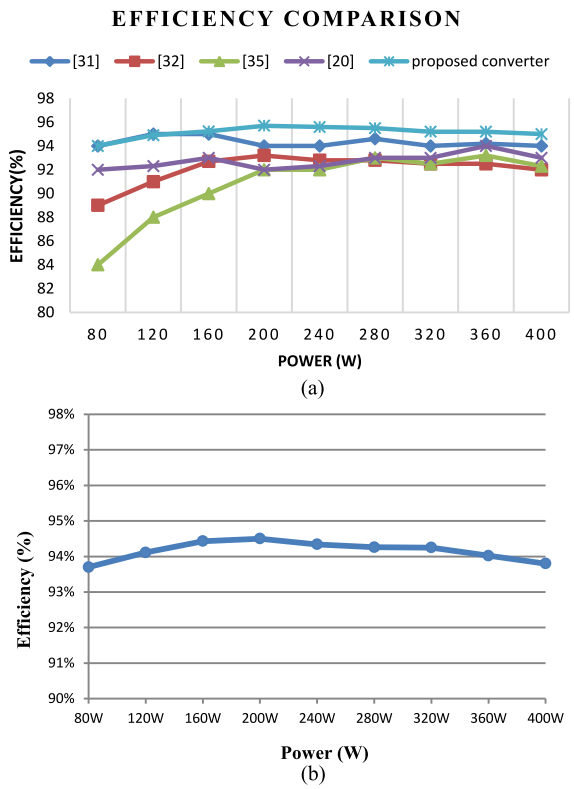

Fig. 16. Efficiency comparison and measurement of the proposed interleaved series-type high step-up converter under different power load. (a) Efficiency comparison. (b) Efficiency measurement.

experiments will also be conducted to finally confirm the functionality of the proposed circuit.

The circuit specifications are the same as Table II. The simulation is under the continuous conduction mode and the load is 200 W. Fig. 10 shows the waveforms of the primary-side currents i_{LP1} and i_{LP2} of the coupled inductors. From the results, one can know the peak current is about 7 A at the half-load and the experimental results match with the simulation ones. The full-load experimental result is also presented in Fig. 10.

Fig. 11 shows the waveforms of the voltages across the switches S_1 and S_2. From Fig. 11(b), the voltage stresses of the switches can be known to be about 50 V. This value corresponds with the one derived from the theoretical analysis. From (15), $V_S = \frac{V_{\rm in}}{1-D} = 50$ V. Therefore, the switch with the lower rating and conduction resistance can be applied to reduce the loss and increase the efficiency.

Fig. 12 shows the waveforms of the capacitor voltages. From Fig. 12, $V_{\rm C1}$ and $V_{\rm C2}$ can be known to be about 100 V. It can match with the one derived from the theoretical value. From (9), $V_{C1} = V_{C2} = \frac{V_{\rm in}\cdot(1+N\cdot k)}{1-D} = 99$ V. The values of $V_{\rm Co1}$ and $V_{\rm Co2}$ are about 200 V. As for the theoretical values, they are $V_{co1} = V_{co2} = \frac{2\cdot V_{\rm in}\cdot(1+N\cdot k)}{1-D} = 198$ V from (11).

Fig. 13 shows the waveforms of the voltages across the diodes. The voltage across each diode can be seen to be about one-half of the output voltage. The experimental results also match with the simulation ones. Fig. 14 shows the current waveform of each diode. The experimental results are also close to the simulation ones. Fig. 15 gives the simulation result of the control-to-output transfer function of the proposed converter. According to the result, the control loop of the proposed converter can be designed.

The efficiency comparison and measurement of the proposed interleaved series-type high step-up converter is shown in Fig. 16. Fig. 16(a) is the simulated results for the various topologies listed in Table I. The simulations are based on the same specification and switching components. From the results, the proposed converter has the better efficiency. Fig. 16(b) shows the experimental measurement result of the efficiency. The load range is from 80 to 400 W. From Fig. 16(b), the maximum efficiency can be seen to be about 94.5% occurring at 200 W. Due to the current sharing effect of the proposed topology, the current flowing through each component is smaller and the proposed converter can have the higher efficiency at the full load. The average efficiency is about 94%.

VI. Conclusion

This paper proposes a new interleaved series-type high step-up converter. The main concept is to use fewer components to step up as much voltage gain as possible to simplify the complexity of circuit design and analysis. The interleaved structure is applied to achieve the current sharing characteristic. In addition to reducing the current stress of the component, the current ripple of the circuit can also be decreased. With the series connection of voltage-double modules, the secondary sides of the coupled inductors are also in interleaved series connection. The two voltage-double modules commonly share the series secondary-side inductors. After the interleaved stored energy of the voltage-double modules, the two modules are in series connection with the input voltage and the primary-side and secondary-side of the coupled inductors to achieve the effect of high voltage gain. The turn ratio of the coupled inductor can also be adjusted to make the converter obtain the high voltage gain even the duty cycle is not high. Therefore, the ratings of the switches and diodes can be lower and the cost of the circuit can be decreased.

The proposed converter is operated in the situation that the input voltage is 24 V, the output voltage is 400 V, and the output power is 400 W. The maximum efficiency of this interleaved series-type high step-up converter is 94.5%. The voltage rating of the switch can be lower and the voltage ratings of all diodes are about one-half of the output voltage. The experiments confirm the advantages of high voltage gain, low rating of the component, less components, and high efficiency of the proposed converter.

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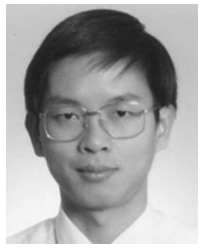

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